

August 1996

High Frequency NPN Transistor Array

Features

- Gain Bandwidth Product (f_T) >1GHz
- Power Gain 30dB (Typ) at 100MHz
- Noise Figure 3.5dB (Typ) at 100MHz
- Five Independent Transistors on a Common Substrate

Applications

- VHF Amplifiers
- Multifunction Combinations - RF/Mixer/Oscillator
- Sense Amplifiers
- Synchronous Detectors
- VHF Mixers
- IF Converter
- IF Amplifiers
- Synthesizers
- Cascade Amplifiers

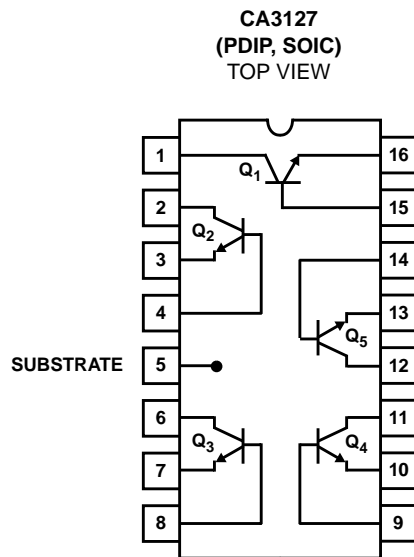
Description

The CA3127 consists of five general purpose silicon NPN transistors on a common monolithic substrate. Each of the completely isolated transistors exhibits low $1/f$ noise and a value of f_T in excess of 1GHz, making the CA3127 useful from DC to 500MHz. Access is provided to each of the terminals for the individual transistors and a separate substrate connection has been provided for maximum application flexibility. The monolithic construction of the CA3127 provides close electrical and thermal matching of the five transistors.

Ordering Information

| PART NUMBER (BRAND) | TEMP. RANGE (°C) | PACKAGE | PKG. NO. |
|---------------------|------------------|--------------------------|----------|
| CA3127E | -55 to 125 | 16 Ld PDIP | E16.3 |
| CA3127M (3127) | -55 to 125 | 16 Ld SOIC | M16.15 |
| CA3127M96 (3127) | -55 to 125 | 16 Ld SOIC Tape and Reel | M16.15 |

Pinout



CA3127

Absolute Maximum Ratings

The following ratings apply for each transistor in the device

| | |
|--|------|
| Collector-to-Emitter Voltage, V_{CEO} | 15V |
| Collector-to-Base Voltage, V_{CBO} | 20V |
| Collector-to-Substrate Voltage, V_{C1O} (Note 1) | 20V |
| Collector Current, I_C | 20mA |

Operating Conditions

Temperature Range

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. The collector of each transistor of the CA3127 is isolated from the substrate by an integral diode. The substrate (Terminal 5) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Thermal Information

| | |
|---|-------------------------------|
| Thermal Resistance (Typical, Note 2) | θ_{JA} (°C/W) |
| PDIP Package | 90 |
| SOIC Package | 175 |
| Maximum Power Dissipation, P_D (Any One Transistor) | 85mW |
| Maximum Junction Temperature (Die) | 175°C |
| Maximum Junction Temperature (Plastic Packages) | 150°C |
| Maximum Storage Temperature Range | -65°C to 150°C |
| Maximum Lead Temperature (Soldering 10s) | 300°C (SOIC - Lead Tips Only) |

Electrical Specifications $T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS | |
|---|---|----------------------|------------|------|---------------|---|
| DC CHARACTERISTICS (For Each Transistor) | | | | | | |
| Collector-to-Base Breakdown Voltage | $I_C = 10\mu\text{A}, I_E = 0$ | 20 | 32 | - | V | |
| Collector-to-Emitter Breakdown Voltage | $I_C = 1\text{mA}, I_B = 0$ | 15 | 24 | - | V | |
| Collector-to-Substrate Breakdown-Voltage | $I_{C1} = 10\mu\text{A}, I_B = 0, I_E = 0$ | 20 | 60 | - | V | |
| Emitter-to-Base Breakdown Voltage (Note 3) | $I_E = 10\mu\text{A}, I_C = 0$ | 4 | 5.7 | - | V | |
| Collector-Cutoff-Current | $V_{CE} = 10\text{V}, I_B = 0$ | - | - | 0.5 | μA | |
| Collector-Cutoff-Current | $V_{CB} = 10\text{V}, I_E = 0$ | - | - | 40 | nA | |
| DC Forward-Current Transfer Ratio | $V_{CE} = 6\text{V}$ | $I_C = 5\text{mA}$ | 35 | 88 | - | |
| | | $I_C = 1\text{mA}$ | 40 | 90 | - | |
| | | $I_C = 0.1\text{mA}$ | 35 | 85 | - | |
| Base-to-Emitter Voltage | $V_{CE} = 6\text{V}$ | $I_C = 5\text{mA}$ | 0.71 | 0.81 | 0.91 | V |
| | | $I_C = 1\text{mA}$ | 0.66 | 0.76 | 0.86 | V |
| | | $I_C = 0.1\text{mA}$ | 0.60 | 0.70 | 0.80 | V |
| Collector-to-Emitter Saturation Voltage | $I_C = 10\text{mA}, I_B = 1\text{mA}$ | - | 0.26 | 0.50 | V | |
| Magnitude of Difference in V_{BE} | Q_1 and Q_2 Matched | - | 0.5 | 5 | mV | |
| Magnitude of Difference in I_B | $V_{CE} = 6\text{V}, I_C = 1\text{mA}$ | - | 0.2 | 3 | μA | |
| DYNAMIC CHARACTERISTICS | | | | | | |
| Noise Figure | $f = 100\text{kHz}, R_S = 500\Omega, I_C = 1\text{mA}$ | - | 2.2 | - | dB | |
| Gain-Bandwidth Product | $V_{CE} = 6\text{V}, I_C = 5\text{mA}$ | - | 1.15 | - | GHz | |
| Collector-to-Base Capacitance | $V_{CB} = 6\text{V}, f = 1\text{MHz}$ | - | See Fig. 5 | - | pF | |
| Collector-to-Substrate Capacitance | $V_{C1} = 6\text{V}, f = 1\text{MHz}$ | - | | - | pF | |
| Emitter-to-Base Capacitance | $V_{BE} = 4\text{V}, f = 1\text{MHz}$ | - | | - | pF | |
| Voltage Gain | $V_{CE} = 6\text{V}, f = 10\text{MHz}, R_L = 1\text{k}\Omega, I_C = 1\text{mA}$ | - | 28 | - | dB | |
| Power Gain | Cascode Configuration | 27 | 30 | - | dB | |
| Noise Figure | $f = 100\text{MHz}, V_+ = 12\text{V}, I_C = 1\text{mA}$ | - | 3.5 | - | dB | |
| Input Resistance | Common-Emitter Configuration $V_{CE} = 6\text{V}, I_C = 1\text{mA}, f = 200\text{MHz}$ | - | 400 | - | Ω | |
| Output Resistance | | - | 4.6 | - | k Ω | |
| Input Capacitance | | - | 3.7 | - | pF | |
| Output Capacitance | | - | 2 | - | pF | |
| Magnitude of Forward Transadmittance | | - | 24 | - | mS | |

NOTE:

3. When used as a zener for reference voltage, the device must not be subjected to more than 0.1mJ of energy from any possible capacitance or electrostatic discharge in order to prevent degradation of the junction. Maximum operating zener current should be less than 10mA.

Test Circuits

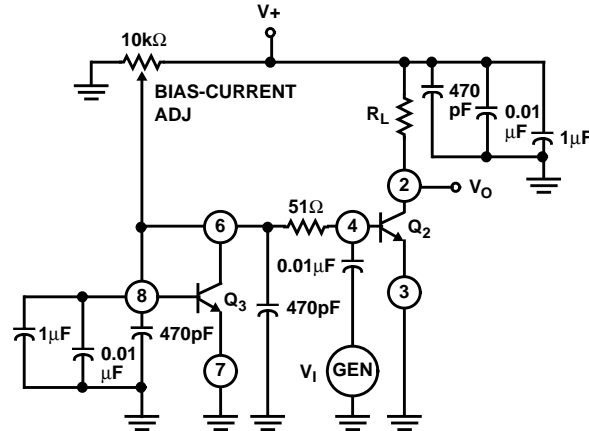
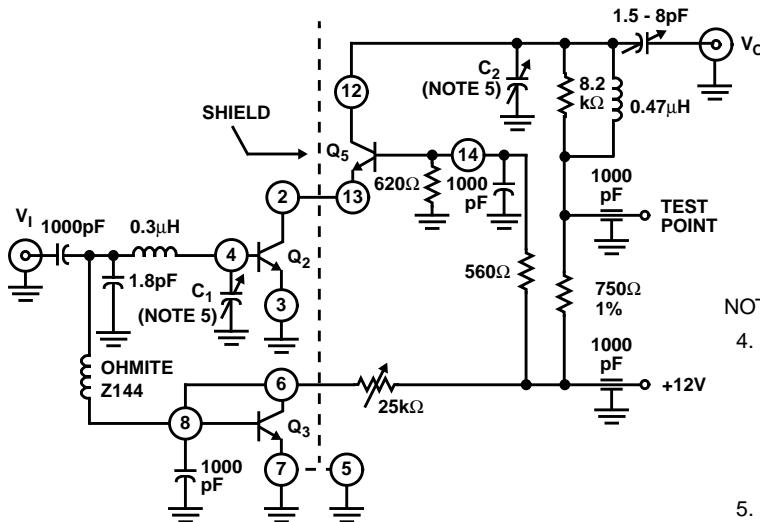


FIGURE 1. VOLTAGE-GAIN TEST CIRCUIT USING CURRENT-MIRROR BIASING FOR Q₂



NOTES:

4. This circuit was chosen because it conveniently represents a close approximation in performance to a properly unilateralized single transistor of this type. The use of Q₃ in a current-mirror configuration facilitates simplified biasing. The use of the cascode circuit in no way implies that the transistors cannot be used individually.
5. E.F. Johnson number 160-104-1 or equivalent.

FIGURE 2. 100MHz POWER-GAIN AND NOISE-FIGURE TEST CIRCUIT

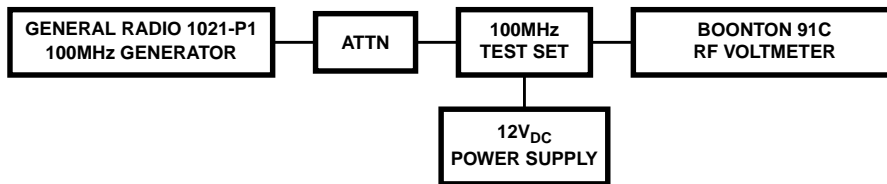


FIGURE 3A. POWER GAIN SET-UP

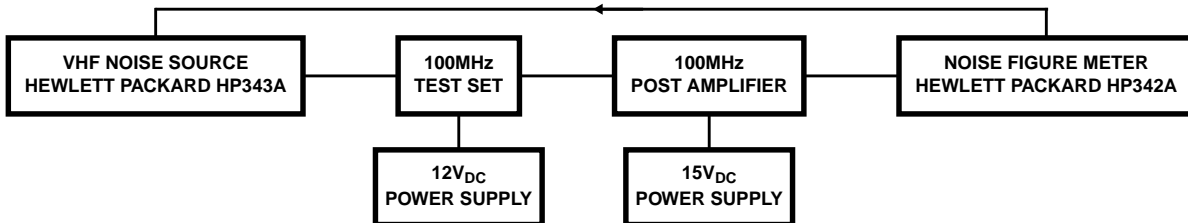


FIGURE 3B. NOISE FIGURE SET-UP
FIGURE 3. BLOCK DIAGRAMS OF POWER-GAIN AND NOISE-FIGURE TEST SET-UPS

Typical Performance Curves

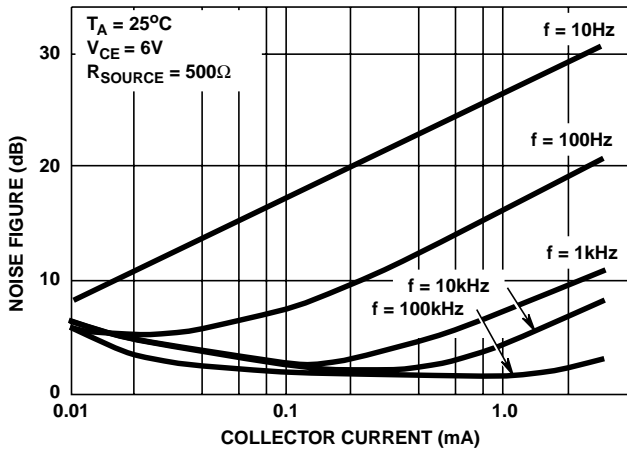


FIGURE 4. NOISE FIGURE vs COLLECTOR CURRENT

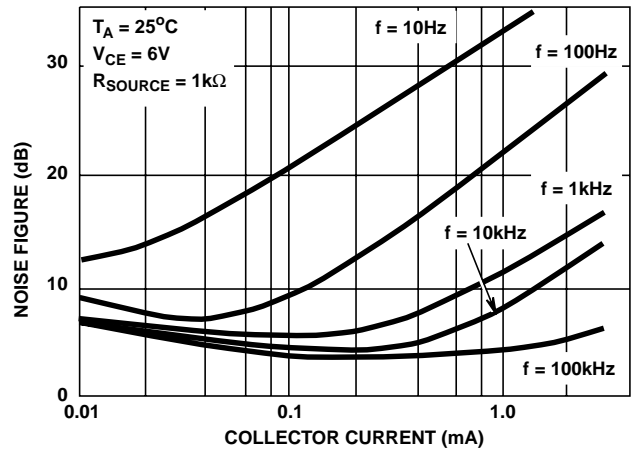


FIGURE 5. NOISE FIGURE vs COLLECTOR CURRENT

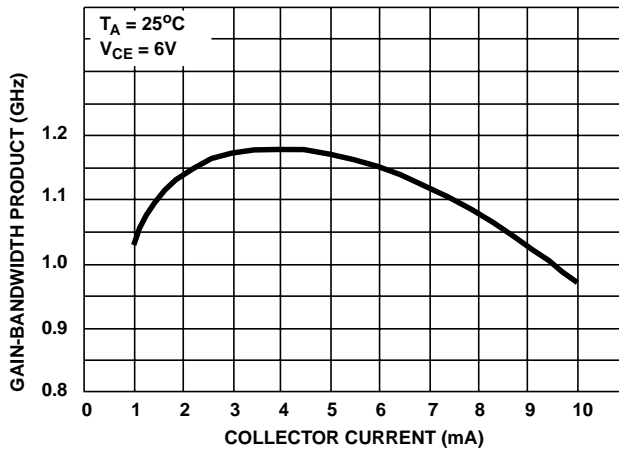


FIGURE 6. GAIN-BANDWIDTH PRODUCT vs COLLECTOR CURRENT

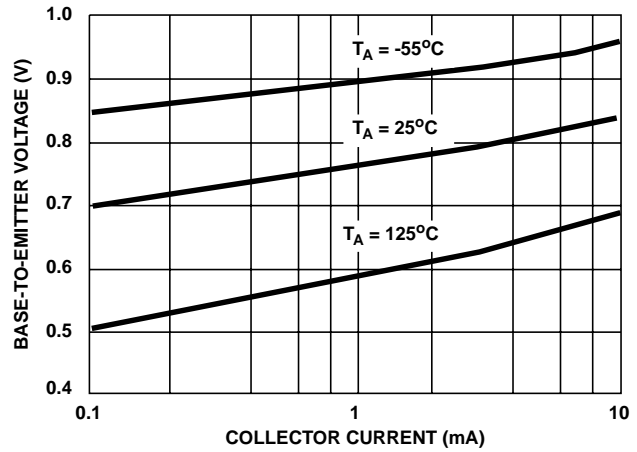


FIGURE 7. BASE-TO-EMITTER VOLTAGE vs COLLECTOR CURRENT

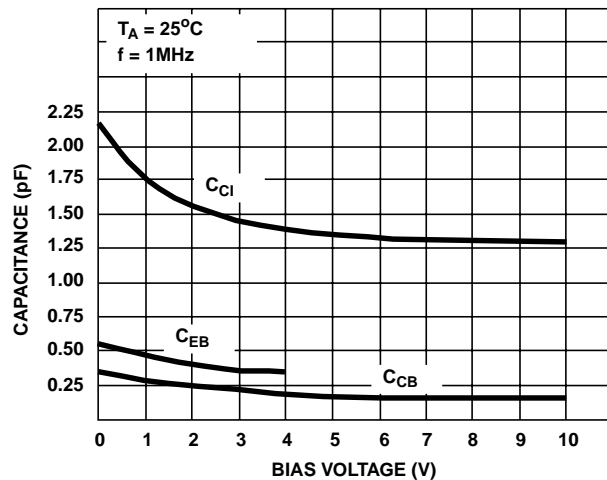


FIGURE 8A. CAPACITANCE vs BIAS VOLTAGE FOR Q₂

| TRAN-SISTOR | CAPACITANCE (pF) | | | | | | | |
|----------------|------------------|-------|------------------|-------|------------------|-------|------------------|-------|
| | C _{CB} | | C _{CCE} | | C _{CEB} | | C _{CCI} | |
| | PKG | TOTAL | PKG | TOTAL | PKG | TOTAL | PKG | TOTAL |
| BIAS (V) | - | 6V | - | 6V | - | 4V | - | 6V |
| Q ₁ | 0.025 | 0.190 | 0.090 | 0.125 | 0.365 | 0.610 | 0.475 | 1.65 |
| Q ₂ | 0.015 | 0.170 | 0.225 | 0.265 | 0.130 | 0.360 | 0.085 | 1.35 |
| Q ₃ | 0.040 | 0.200 | 0.215 | 0.240 | 0.360 | 0.625 | 0.210 | 1.40 |
| Q ₄ | 0.040 | 0.190 | 0.225 | 0.270 | 0.365 | 0.610 | 0.085 | 1.25 |
| Q ₅ | 0.010 | 0.165 | 0.095 | 0.115 | 0.140 | 0.365 | 0.090 | 1.35 |

FIGURE 8B. TYPICAL CAPACITANCE VALUES AT f = 1MHz. THREE TERMINAL MEASUREMENT. GUARD ALL TERMINALS EXCEPT THOSE UNDER TEST.

Typical Performance Curves (Continued)

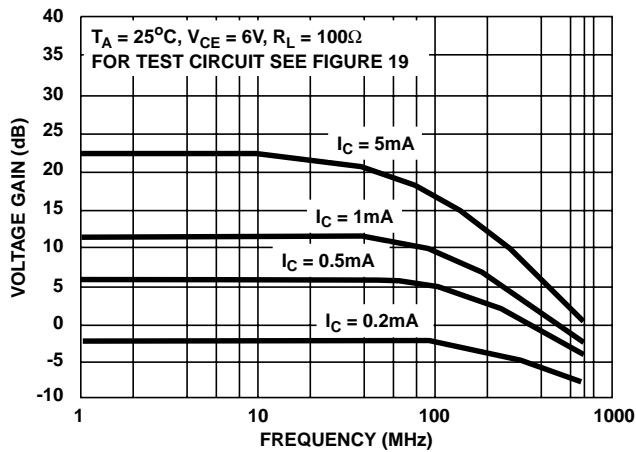


FIGURE 9. VOLTAGE GAIN vs FREQUENCY

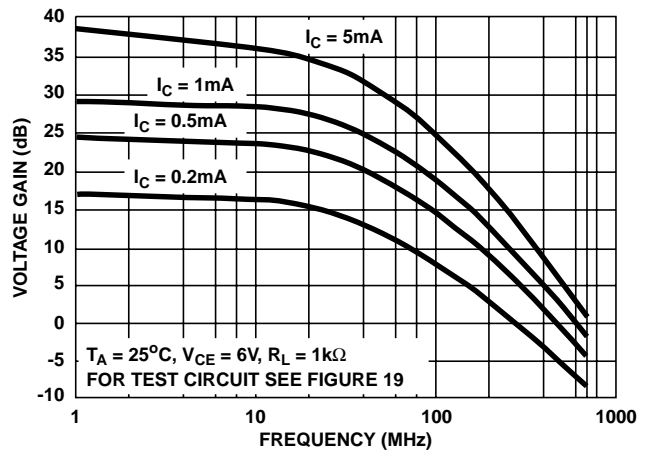


FIGURE 10. VOLTAGE GAIN vs FREQUENCY

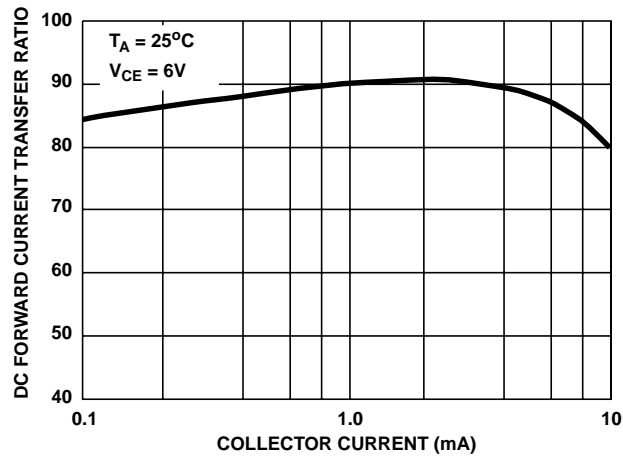


FIGURE 11. DC FORWARD-CURRENT TRANSFER RATIO (h_{FE}) vs COLLECTOR CURRENT

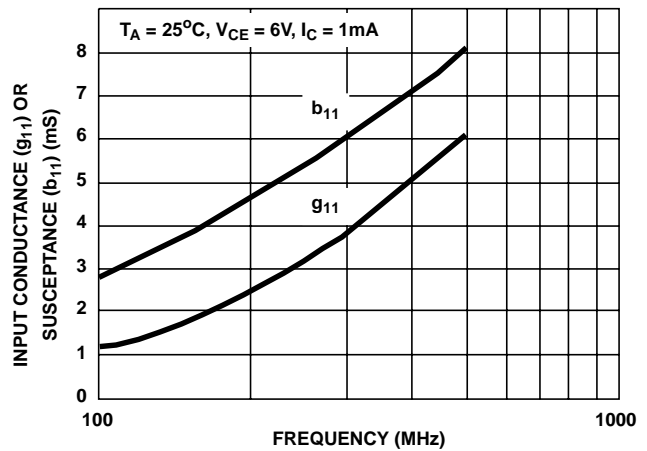


FIGURE 12. INPUT ADMITTANCE (Y_{11}) vs FREQUENCY

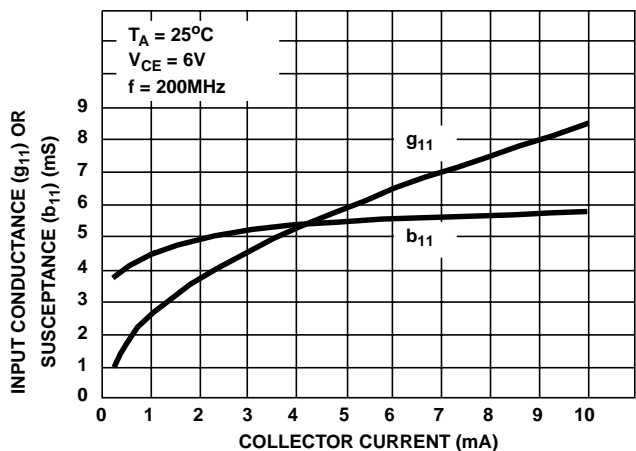


FIGURE 13. INPUT ADMITTANCE (Y_{11}) vs COLLECTOR CURRENT

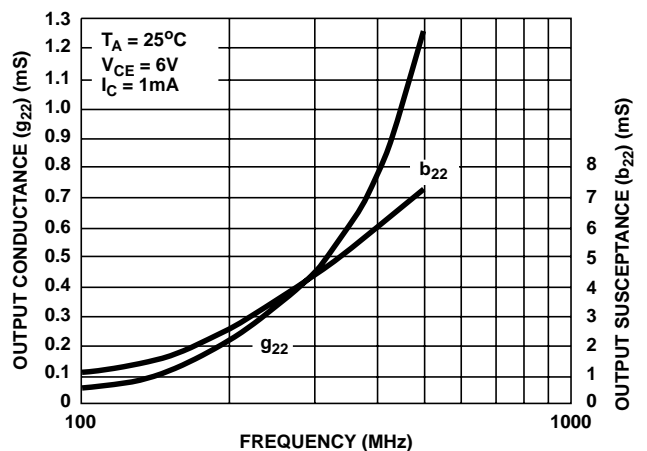


FIGURE 14. OUTPUT ADMITTANCE (Y_{22}) vs FREQUENCY

Typical Performance Curves (Continued)

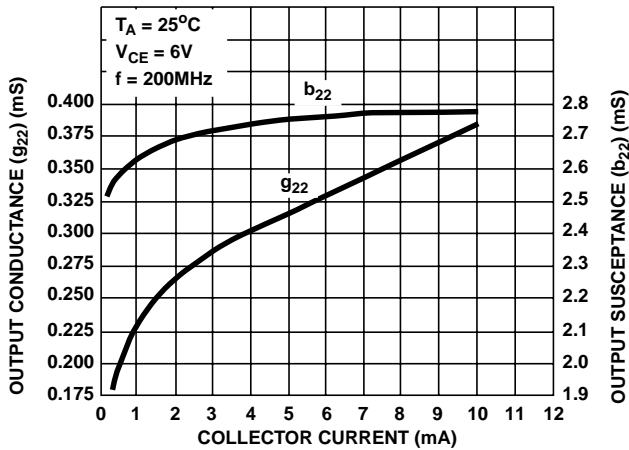


FIGURE 15. OUTPUT ADMITTANCE (Y_{22}) vs COLLECTOR CURRENT

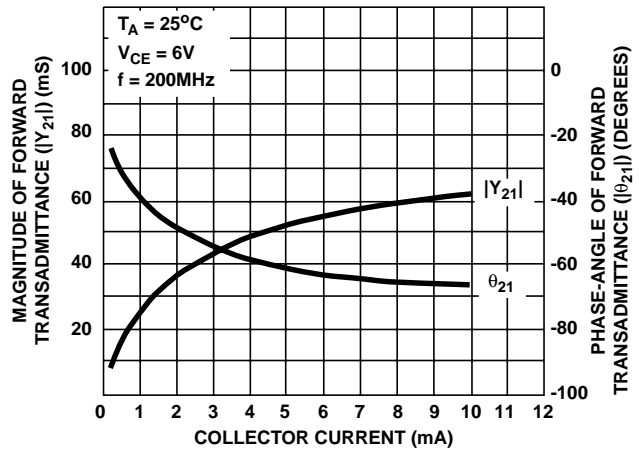


FIGURE 16. FORWARD TRANSMITTANCE (Y_{21}) vs COLLECTOR CURRENT

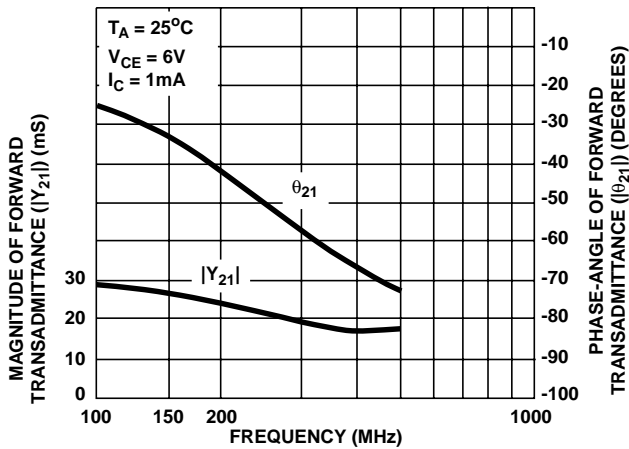


FIGURE 17. FORWARD TRANSMITTANCE (Y_{21}) vs FREQUENCY

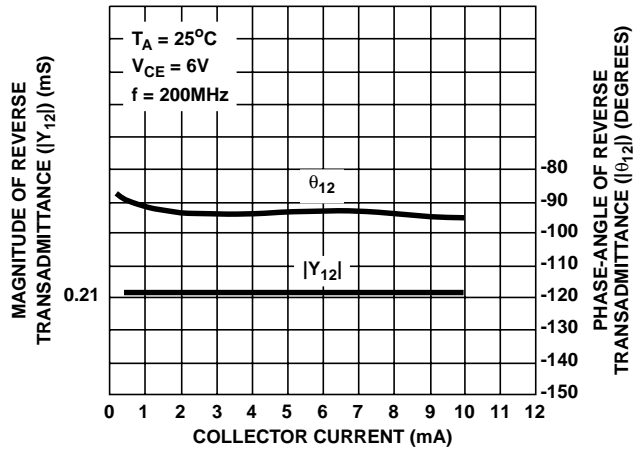


FIGURE 18. REVERSE TRANSMITTANCE (Y_{12}) vs COLLECTOR CURRENT

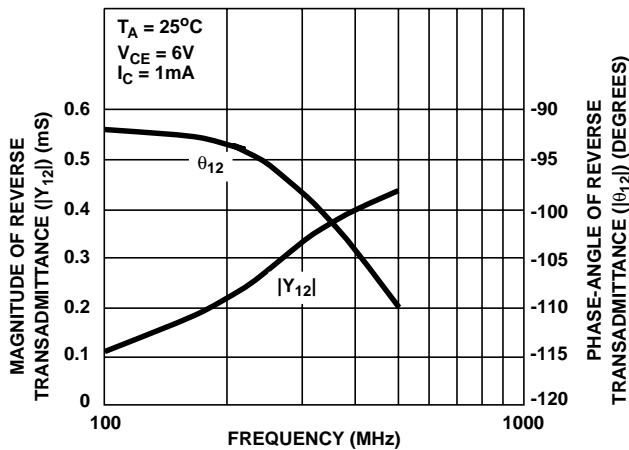


FIGURE 19. REVERSE TRANSMITTANCE (Y_{12}) vs FREQUENCY

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see web site <http://www.intersil.com>

Sales Office Headquarters

NORTH AMERICA

Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (321) 724-7000
FAX: (321) 724-7240

EUROPE

Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA

Intersil (Taiwan) Ltd.
Taiwan Limited
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029