

# LH5268A

CMOS 64K (8K × 8) Static RAM

## FEATURES

- 8,192 × 8 bit organization
- Access time: 100 ns (MAX.)
- Power consumption:
  - Operating:
    - 220 mW (MAX.)
    - 55 mW (MAX.) ( $t_{RC}$ ,  $t_{WC} = 1 \mu s$ )
  - Standby:
    - 220  $\mu W$  (MAX.)
  - Data retention:
    - 3.0  $\mu W$  ( $V_{CC} = 3 V$ ,  $T_A = 25^\circ C$ )
- Fully-static operation
- Three-state outputs
- Single +5 V power supply
- TTL compatible I/O
- Packages:
  - 28-pin, 600-mil DIP
  - 28-pin, 300-mil SK-DIP
  - 28-pin, 450-mil SOP

## DESCRIPTION

The LH5268A is a static RAM organized as 8,192 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

## PIN CONNECTIONS

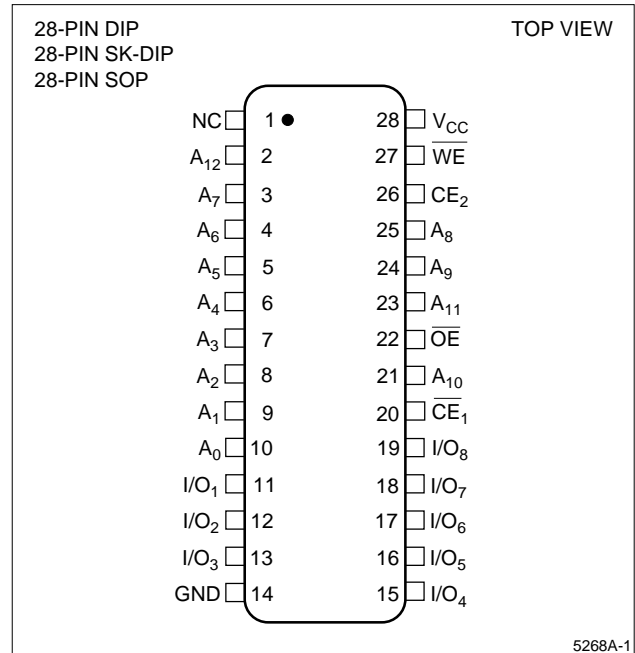


Figure 1. Pin Connections for DIP, SK-DIP, and SOP Packages



## TRUTH TABLE

$\overline{CE}_1$	$CE_2$	$\overline{WE}$	$\overline{OE}$	MODE	I/O <sub>1</sub> - I/O <sub>8</sub>	SUPPLY CURRENT	NOTE
H	X	X	X	Deselect	High-Z	Standby ( $I_{SB}$ )	1
X	L	X	X	Deselect	High-Z	Standby ( $I_{SB}$ )	1
L	H	L	X	Write	D <sub>IN</sub>	Operating ( $I_{CC}$ )	1
L	H	H	L	Read	D <sub>OUT</sub>	Operating ( $I_{CC}$ )	
L	H	H	H	Output disable	High-Z	Operating ( $I_{CC}$ )	

## NOTE:

- X = H or L

## ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	$V_{CC}$	-0.3 to +7.0	V	1
Input voltage	$V_{IN}$	-0.3 to $V_{CC} + 0.3$	V	1,2
Operating temperature	$T_{opr}$	0 to +70	°C	
Storage temperature	$T_{stg}$	-65 to +150	°C	

## NOTES:

- The maximum applicable voltage on any pin with respect to GND.
- $V_{IN}$  (MIN.) = -3.0 V for pulse width ≤ 50 ns.

RECOMMENDED OPERATING CONDITIONS ( $T_A = 0$  to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage	$V_{CC}$	4.5	5.0	5.5	V	
Input voltage	$V_{IH}$	2.2		$V_{CC} + 0.3$	V	
	$V_{IL}$	-0.3		0.8	V	1

## NOTE:

- $V_{IN}$  (MIN.) = -3.0 V for pulse width ≤ 50 ns.

DC CHARACTERISTICS ( $T_A = 0$  to +70°C,  $V_{CC} = 5 V \pm 10\%$ )

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Input leakage current	$I_{LI}$	$V_{IN} = 0$ to $V_{CC}$	-1	1	μA	
Output leakage current	$I_{LO}$	$\overline{CE}_1 = V_{IH}$ or $CE_2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ $V_{I/O} = 0$ V to $V_{CC}$	-1	1	μA	
Operating current	$I_{CC}$	$\overline{CE}_1 = V_{IL}$ , $V_{IN} = V_{IL}$ or $V_{IH}$ $CE_2 = V_{IH}$ , $I_{I/O} = 0$ mA		40	mA	
		$\overline{CE}_1 = 0.2$ V, $V_{IN} = 0.2$ V or $V_{CC} - 0.2$ V $CE_2 = V_{CC} - 0.2$ V, $I_{I/O} = 0$ mA		10		
Standby current	$I_{SB1}$	$\overline{CE}_1 = V_{IH}$ or $CE_2 = V_{IL}$		3	mA	
	$I_{SB}$	$CE_2 \leq 0.2$ V or $\overline{CE}_1 \geq V_{CC} - 0.2$ V		40	μA	1
Output voltage	$V_{OL}$	$I_{OL} = 2.1$ mA		0.4	V	
	$V_{OH}$	$I_{OH} = -1.0$ mA	2.4		V	

## NOTE:

- $CE_2$  should be  $\geq V_{CC} - 0.2$  V or  $\leq 0.2$  V when  $\overline{CE}_1 \geq V_{CC} - 0.2$  V.

## AC CHARACTERISTICS

### (1) READ CYCLE ( $T_A = 0$ to $+70^\circ\text{C}$ , $V_{CC} = 5\text{ V} \pm 10\%$ )

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE	
Read cycle time	$t_{RC}$	100		ns		
Address access time	$t_{AA}$		100	ns		
Chip enable access time	(CE <sub>1</sub> )	$t_{ACE1}$		100	ns	
	(CE <sub>2</sub> )	$t_{ACE2}$		100	ns	
Output enable access time	$t_{OE}$		40	ns		
Output hold time	$t_{OH}$	10		ns		
Chip enable to output in Low-Z	(CE <sub>1</sub> )	$t_{LZ1}$	10	ns	1	
	(CE <sub>2</sub> )	$t_{LZ2}$	10	ns	1	
Output enable to output in Low-Z	$t_{OLZ}$	5		ns	1	
Chip enable to output in High-Z	(CE <sub>1</sub> )	$t_{HZ1}$	0	30	ns	1
	(CE <sub>2</sub> )	$t_{HZ2}$	0	30	ns	1
Output disable to output in High-Z	$t_{OHZ}$	0	20	ns	1	

**NOTE:**

- Active output to high-impedance and high-impedance to output active tests specified for a  $\pm 200$  mV transition from steady state levels into the test load.

### (2) WRITE CYCLE ( $T_A = 0$ to $+70^\circ\text{C}$ , $V_{CC} = 5\text{ V} \pm 10\%$ )

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Write cycle time	$t_{WC}$	100		ns	
Chip enable to end of write	$t_{CW}$	80		ns	
Address valid to end of write	$t_{AW}$	80		ns	
Address setup time	$t_{AS}$	0		ns	
Write pulse width	$t_{WP}$	60		ns	
Write recovery time	$t_{WR}$	0		ns	
Data valid to end of write	$t_{DW}$	40		ns	
Data hold time	$t_{DH}$	0		ns	
Output active from end of write	$t_{OW}$	10		ns	1
$\overline{WE}$ to output in High-Z	$t_{WZ}$	0	30	ns	1
$\overline{OE}$ to output in High-Z	$t_{OHZ}$	0	20	ns	1

**NOTE:**

- Active output to high-impedance and high-impedance to output active tests specified for a  $\pm 200$  mV transition from steady state levels into the test load.

## AC TEST CONDITIONS

PARAMETER	MODE	NOTE
Input voltage amplitude	0.6 to 2.4 V	
Input rise/fall time	10 ns	
Timing reference level	1.5 V	
Output load conditions	1TTL + C <sub>L</sub> (100 pF)	1

**NOTE:**

- Includes scope and jig capacitance.

**CAPACITANCE <sup>1</sup> (T<sub>A</sub> = 25°C, f = 1 MHz)**

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0 V			7	pF
Input/output capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> = 0 V			10	pF

**NOTE:**

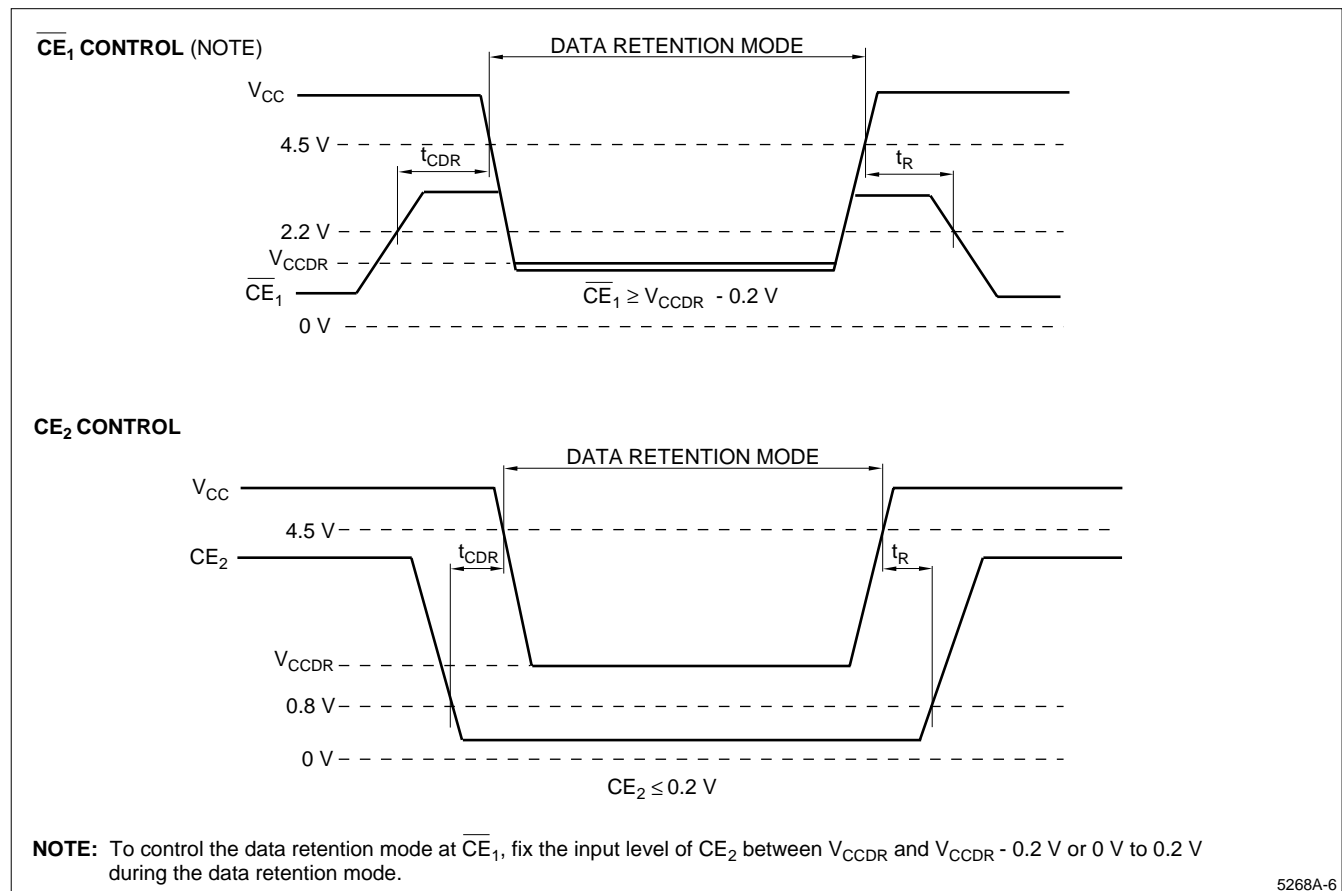
1. This parameter is sampled and not production tested.

**DATA RETENTION CHARACTERISTICS (T<sub>A</sub> = 0 to +70°C)**

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Data retention voltage	V <sub>CCDR</sub>	CE <sub>2</sub> ≤ 0.2 V or CE <sub>1</sub> ≥ V <sub>CCDR</sub> - 0.2 V	2.0	5.5	V	1
Data retention current	I <sub>CCDR</sub>	V <sub>CCDR</sub> = 3 V, CE <sub>2</sub> ≤ 0.2 V or CE <sub>1</sub> ≥ V <sub>CCDR</sub> - 0.2 V		1	μA	1
		T <sub>A</sub> = 25°C		20	μA	
Chip disable to data retention	t <sub>CDR</sub>		0		ns	
Recovery time	t <sub>R</sub>		t <sub>RC</sub>		ns	2

**NOTES:**

1. CE<sub>2</sub> should be ≥ V<sub>CCDR</sub> - 0.2 V or ≤ 0.2 V when CE<sub>1</sub> ≥ V<sub>CCDR</sub> - 0.2 V
2. t<sub>RC</sub> = Read cycle time



**Figure 3. Low Voltage Data Retention**

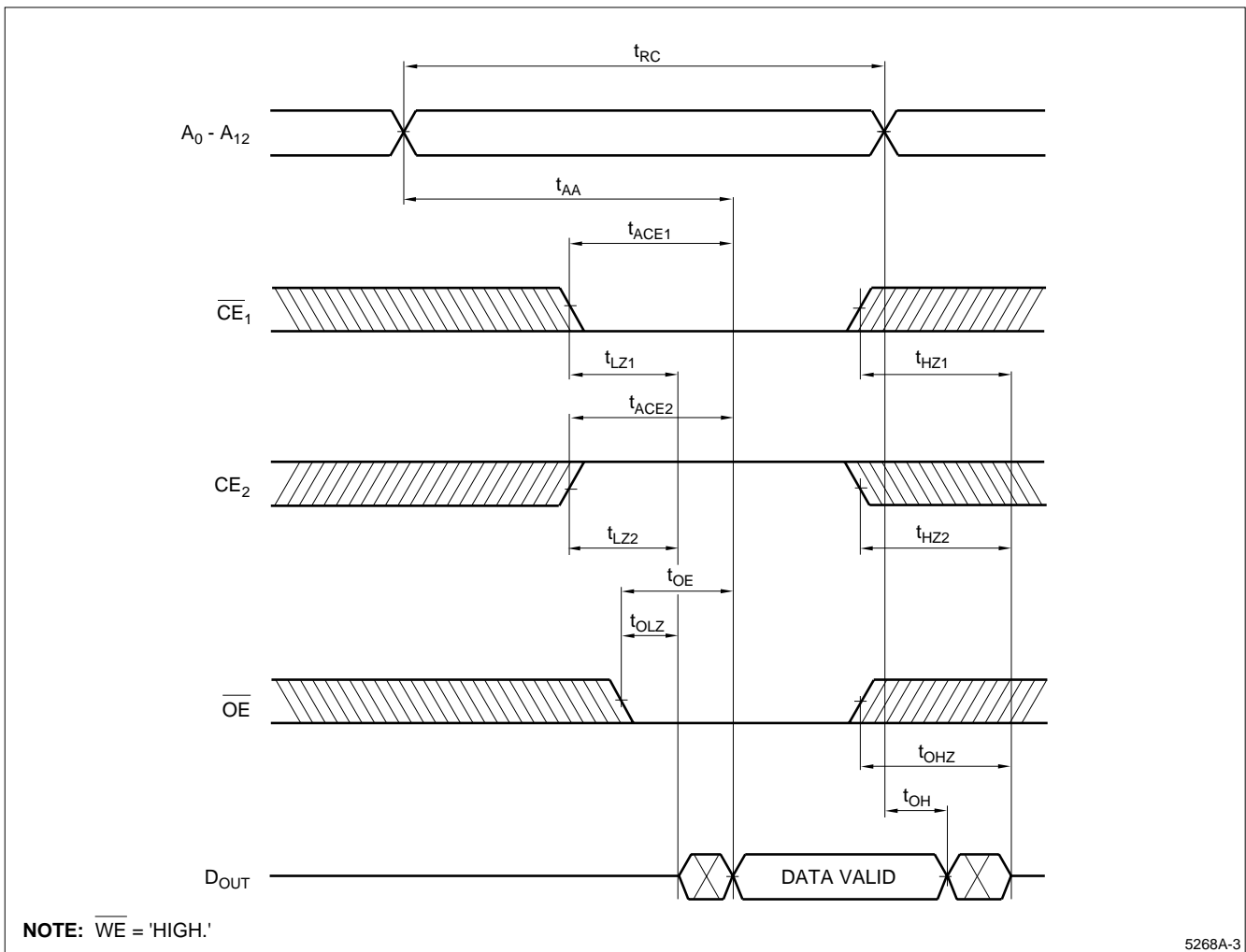
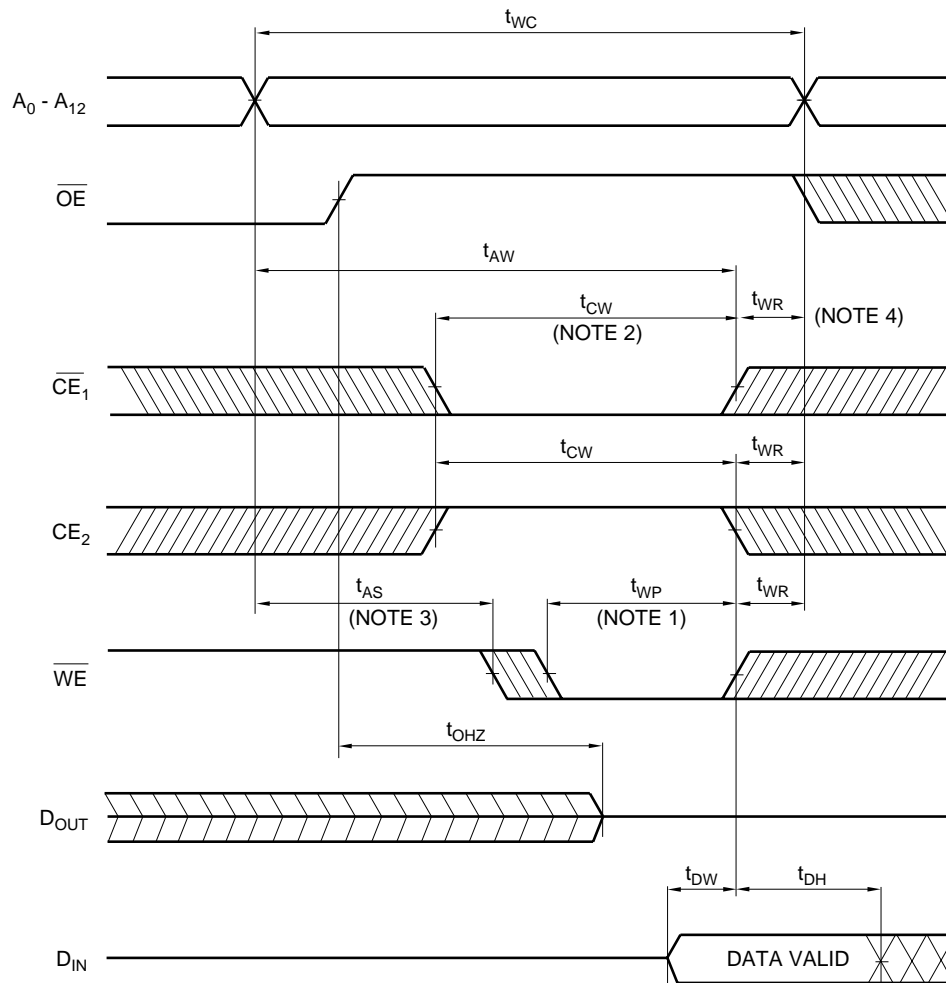


Figure 4. Read Cycle

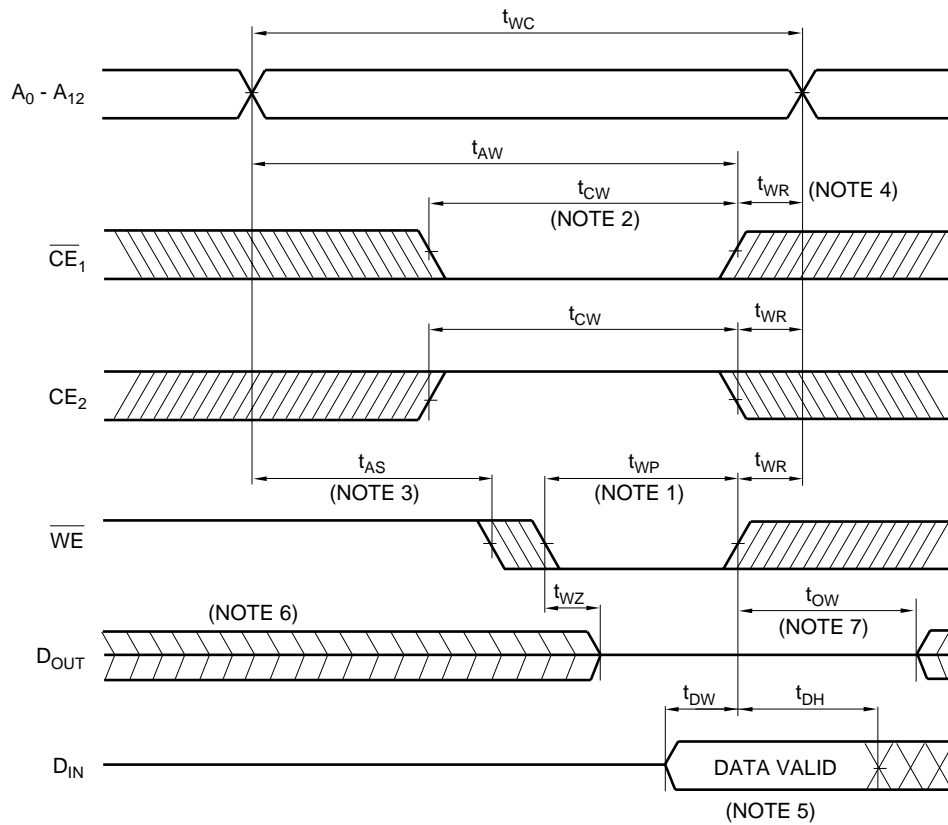


**NOTES:**

1. The writing occurs during an overlapping period of  $\overline{CE}_1 = \text{'LOW'}$ ,  $CE_2 = \text{'HIGH'}$ , and  $\overline{WE} = \text{'LOW'}$  ( $t_{WP}$ ).
2.  $t_{CW}$  is defined as the time from the last occurring transition, either  $\overline{CE}_1$  LOW transition or  $CE_2$  HIGH transition, to the time when the writing is finished.
3.  $t_{AS}$  is defined as the time from address change to writing start.
4.  $t_{WR}$  is defined as the time from writing finish to address change.

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**Figure 5. Write Cycle 1**

**NOTES:**

1. The writing occurs during an overlapping period of  $\overline{CE}_1 = \text{'LOW'}$ ,  $CE_2 = \text{'HIGH'}$ , and  $\overline{WE} = \text{'LOW'}$  ( $t_{WP}$ ).
2.  $t_{CW}$  is defined as the time from the last occurring transition, either  $\overline{CE}_1$  LOW transition or  $CE_2$  HIGH transition, to the time when the writing is finished.
3.  $t_{AS}$  is defined as the time from address change to writing start.
4.  $t_{WR}$  is defined as the time from writing finish to address change.
5. When I/O pins are in the output state, input signals with the opposite logic level must not be applied.
6. If  $\overline{CE}_1$  LOW transition or  $CE_2$  HIGH transition occurs at the same time or after  $\overline{WE}$  LOW transition, the outputs will remain high-impedance.
7. If  $\overline{CE}_1$  HIGH transition or  $CE_2$  LOW transition occurs at the same time or before  $\overline{WE}$  HIGH transition, the outputs will remain high-impedance.

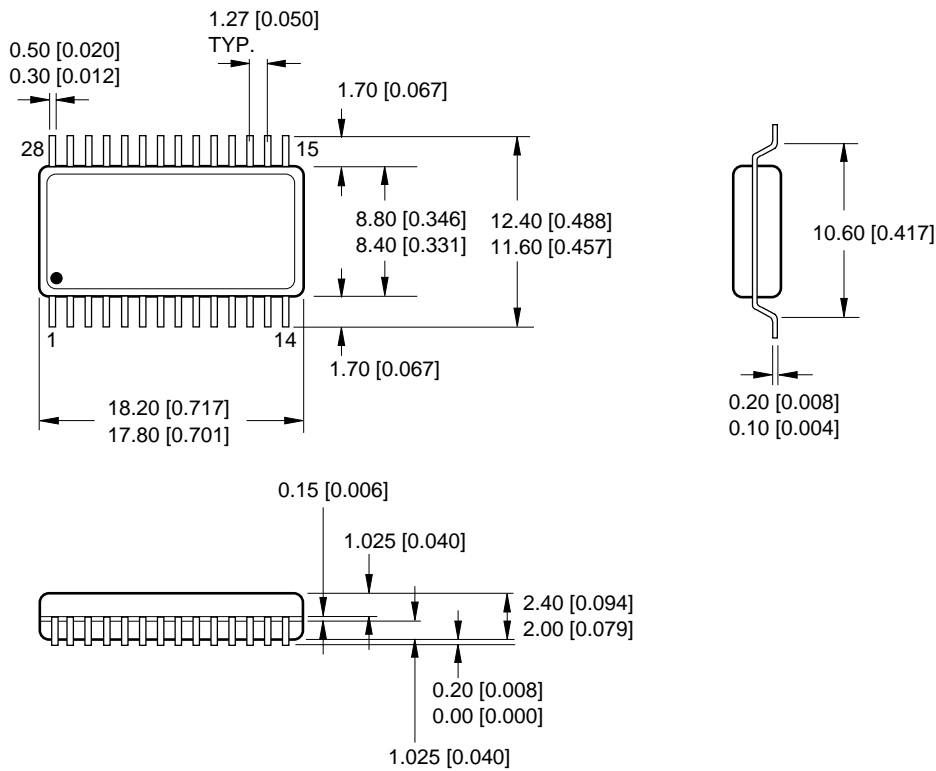
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**Figure 6. Write Cycle 2**





**28SOP (SOP028-P-0450)**

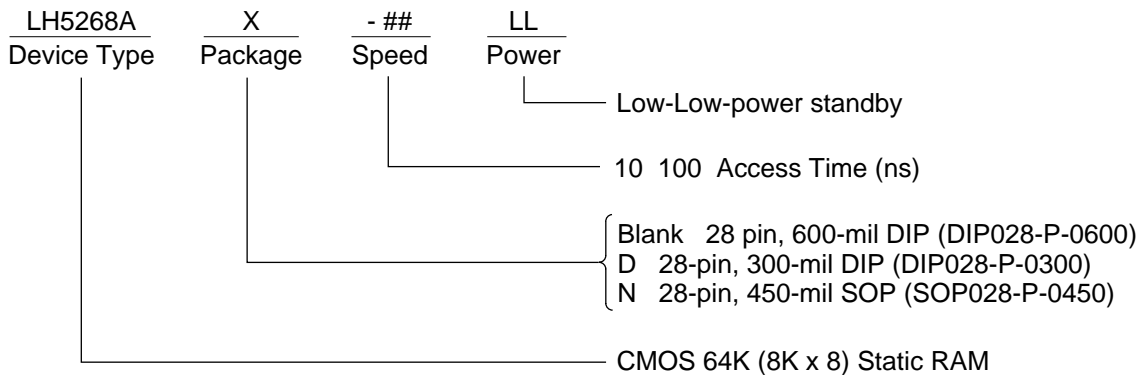


DIMENSIONS IN MM [INCHES]    MAXIMUM LIMIT  
MINIMUM LIMIT

28SOP

**28-pin, 450-mil SOP**

**ORDERING INFORMATION**



**Example:** LH5268AD-10LL (CMOS 64K (8K x 8) Static RAM, Low-Low-power standby, 100 ns, 28-pin, 300-mil DIP)

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