3.3V SINGLE SUPPLY 1:9 PECL-TO-TTL

FEATURES

- 3.3V power supply
- PECL-to-TTL version of popular ECLinPS E111
- Guaranteed low skew specification
- Latched input
- Differential ECL internal design
- V_{BB} output for single-ended operation
- Reset/enable
- Extra TTL and ECL power/ground pins
- Choice of ECL compatibility: MECL 10KH (10Hxxx) or 100K (100Hxxx)
- Available in 28-pin PLCC package

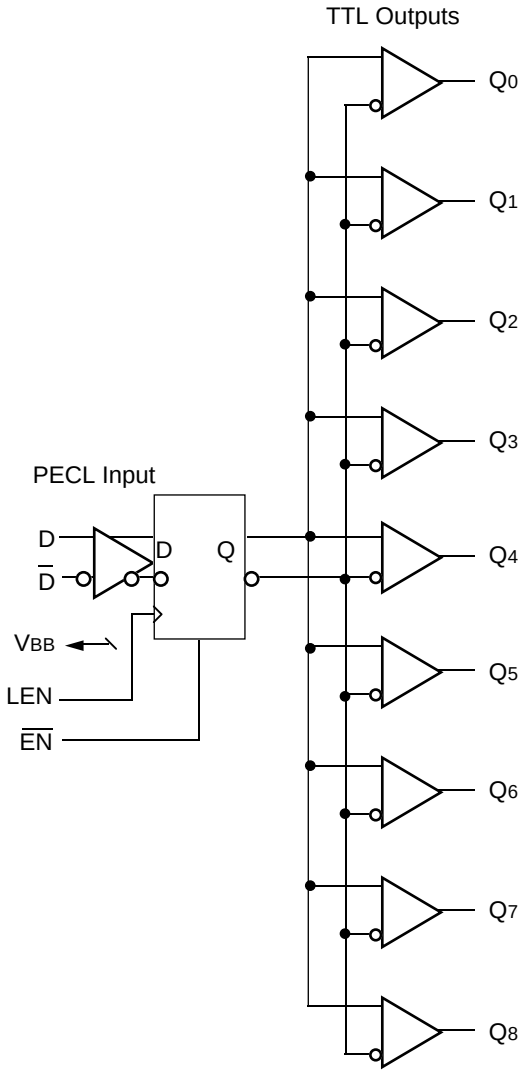
DESCRIPTION

The SY10/100H641L are single supply, low skew translating 1:9 clock drivers. Devices in the Micrel-Synergy H600 translator series utilize the 28-lead PLCC for optimal power pinning, signal flow-through and electrical performance.

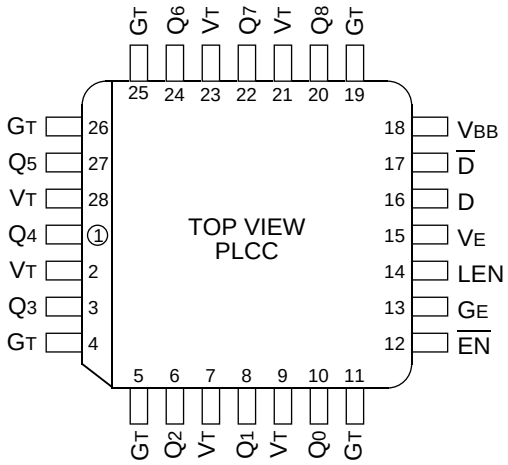
The devices feature a 24mA TTL output stage with AC performance specified into a 20pF load capacitance. A latch is provided on-chip. When LEN is LOW (or left open, in which case it is pulled LOW by the internal pull-downs), the latch is transparent. A HIGH on the enable pin (/EN) forces all outputs LOW.

The 10H version is compatible with MECL 10KH ECL logic levels. The 100H version is compatible with 100K levels.

BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

Pin	Function
G_T	TTL Ground (0V)
V_T	TTL V_{CC} (+3.0V)
V_E	ECL V_{CC} (+3.0V)
G_E	ECL Ground (0V)
D, /D	Signal Input (PECL)
V_{BB}	V_{BB} Reference Output (PECL)
$Q_0 – Q_8$	Signal Outputs (TTL)
/EN	Enable Input (PECL)
LEN	Latch Enable Input (PECL)

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Value	Unit
V_E (ECL) V_T (TTL)	Power Supply Voltage	–0.5 to +7.0 –0.5 to +7.0	V
V_I (ECL)	Input Voltage	0.0 to V_E	V
V_{OUT} (TTL)	Disabled 3-State Output	0.0 to V_T	V
I_{OUT} (ECL)	Output Current - Continuous - Surge	 50 100	mA
T_{store}	Storage Temperature	–65 to +150	°C
T_A	Operating Temperature	0 to +85	°C

NOTE:

1. Do not exceed.

TRUTH TABLE

D	LEN	/EN	Q
L	L	L	L
H	L	L	H
X	H	L	Q_0
X	X	H	L

DC ELECTRICAL CHARACTERISTICS

$V_T = V_E$ = +3.0V to +3.6V

Symbol	Parameter		T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
			Min.	Max.	Min.	Max.	Min.	Max.		
I_{EE}	Power Supply Current	ECL	—	30	—	30	—	30	mA	V_E Pin
I_{CCH}		TTL	—	30	—	30	—	30		Total all V_T pins
I_{CCL}			—	35	—	35	—	35		

TTL DC ELECTRICAL CHARACTERISTICS

$V_T = V_E$ = +3.0V to +3.6V

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
V_{OH}	Output HIGH Voltage	2.0	—	2.0	—	2.0	—	V	I_{OH} = –3.0mA
V_{OL}	Output LOW Voltage	—	0.5	—	0.5	—	0.5	V	I_{OL} = 24mA
I_{OS}	Output Short Circuit Current	–100	—	–100	—	–100	—	mA	V_{OUT} = 0V

10H ECL DC ELECTRICAL CHARACTERISTICS

$V_T = V_E$ = +3.0V to +3.6V

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
I_{IH}	Input HIGH Current	—	225	—	175	—	175	µA	—
I_{IL}	Input LOW Current	0.5	—	0.5	—	0.5	—	µA	—
V_{IH}	Input HIGH Voltage(1)	2.130	2.460	2.170	2.490	2.240	2.580	V	V_E = 3.3V
V_{IL}	Input LOW Voltage(1)	1.350	1.820	1.350	1.820	1.350	1.855	V	V_E = 3.3V
V_{BB}	Output Reference Voltage(1)	1.920	2.030	1.950	2.050	1.990	2.110	V	V_E = 3.3V

NOTE:

1. V_{IH}, V_{IL} and V_{BB} are referenced to V_E and will vary 1:1 with the power supply. The levels shown are for V_E = +3.3V.

100H ECL DC ELECTRICAL CHARACTERISTICS

$V_T = V_E$ = +3.0V to +3.6V

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
I_{IH}	Input HIGH Current	—	225	—	175	—	175	µA	—
I_{IL}	Input LOW Current	0.5	—	0.5	—	0.5	—	µA	—
V_{IH}	Input HIGH Voltage(1)	2.135	2.420	2.135	2.420	2.135	2.420	V	V_E = 3.3V
V_{IL}	Input LOW Voltage(1)	1.490	1.825	1.490	1.825	1.490	1.825	V	V_E = 3.3V
V_{BB}	Output Reference Voltage(1)	1.920	2.040	1.920	2.040	1.920	2.040	V	V_E = 3.3V

NOTE:

1. V_{IH}, V_{IL} and V_{BB} are referenced to V_E and will vary 1:1 with the power supply. The levels shown are for V_E = +3.3V.

AC ELECTRICAL CHARACTERISTICS

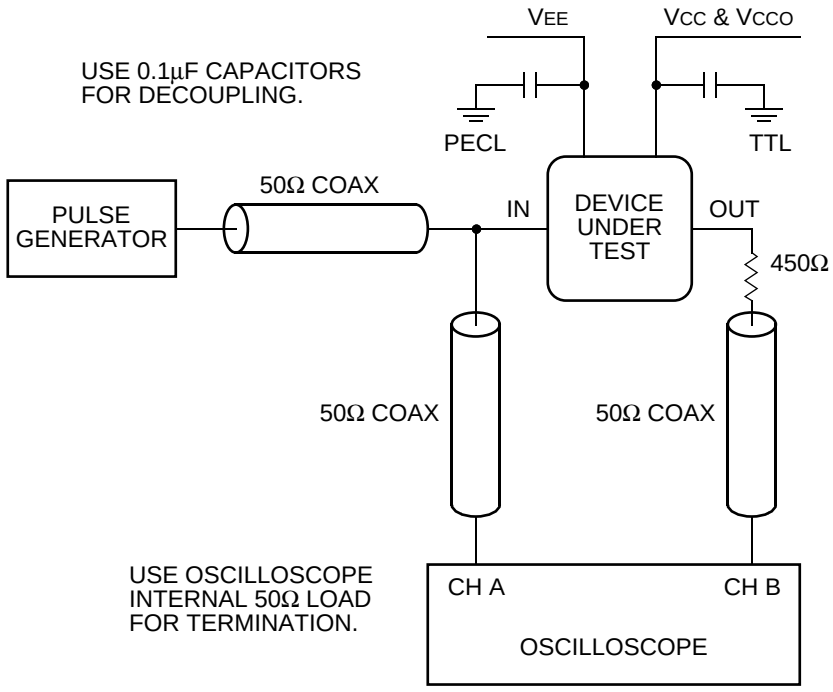
$V_T = V_E$ = +3.0V to +3.6V

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay D to Output	2.0 2.5	3.0 3.5	2.0 2.5	3.0 3.5	2.0 2.5	3.0 3.5	ns	C_L = 20pF
t_{skpp}	Part-to-Part Skew(1,4)	—	0.5	—	0.5	—	0.5	ns	C_L = 20pF
t_{skew++} t_{skew--}	Within-Device Skew(2,3,4)	— —	0.3(7) 0.35(8)	— —	0.3(7) 0.35(8)	— —	0.3(7) 0.35(8)	ns ns	C_L = 20pF C_L = 20pF
t_{PLH} t_{PHL}	Propagation Delay LEN to Output	2.0	3.5	2.0	3.5	2.0	3.5	ns	C_L = 20pF
t_{PLH} t_{PHL}	Propagation Delay /EN to Output	2.0	3.5	2.0	3.5	2.0	3.5	ns	C_L = 20pF
t_r t_f	Output Rise/Fall Time 1.0V to 2.0V	— —	1.7 1.6	— —	1.7 1.6	— —	1.7 1.6	ns	C_L = 20pF
f_{MAX}	Maximum Input Frequency(5,6)	135	—	135	—	135	—	MHz	
—	Pulse Width	1.5	—	1.5	—	1.5	—	ns	—
—	Recovery Time	1.25	—	1.25	—	1.25	—	ns	—
t_S	Set-up Time	0.5 (typ.)		0.5 (typ.)		0.5 (typ.)		ns	—
t_H	Hold Time	0.5 (typ.)		0.5 (typ.)		0.5 (typ.)		ns	—

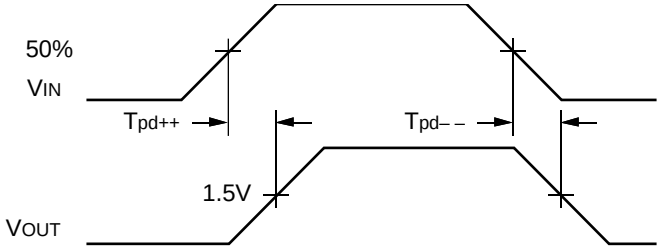
NOTES:

1. Device-to-Device Skew considering HIGH-to-HIGH transitions at common V_{CC} level.
2. Within-Device Skew considering HIGH-to-HIGH transitions at common V_{CC} level.
3. Within-Device Skew considering LOW-to-LOW transitions at common V_{CC} level.
4. All skew parameters are guaranteed but not tested.
5. Frequency at which output levels will meet a 0.8V to 2.0V minimum swing.
6. The f_{MAX} value is specified as the minimum guaranteed maximum frequency. Actual operational maximum frequency may be greater.
7. $V_T = V_E$ = +3.15V to +3.45V, (i.e. V_E +/– 5%).
8. $V_T = V_E$ = +3.0V to +3.6V, (i.e. V_E +/– 10%).

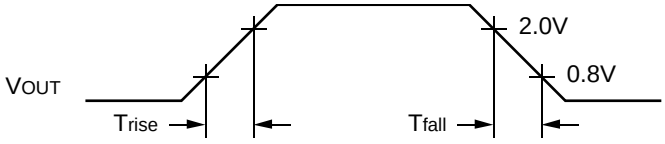
TTL SWITCHING CIRCUIT



ECL/TTL PROPAGATION DELAY — SINGLE ENDED



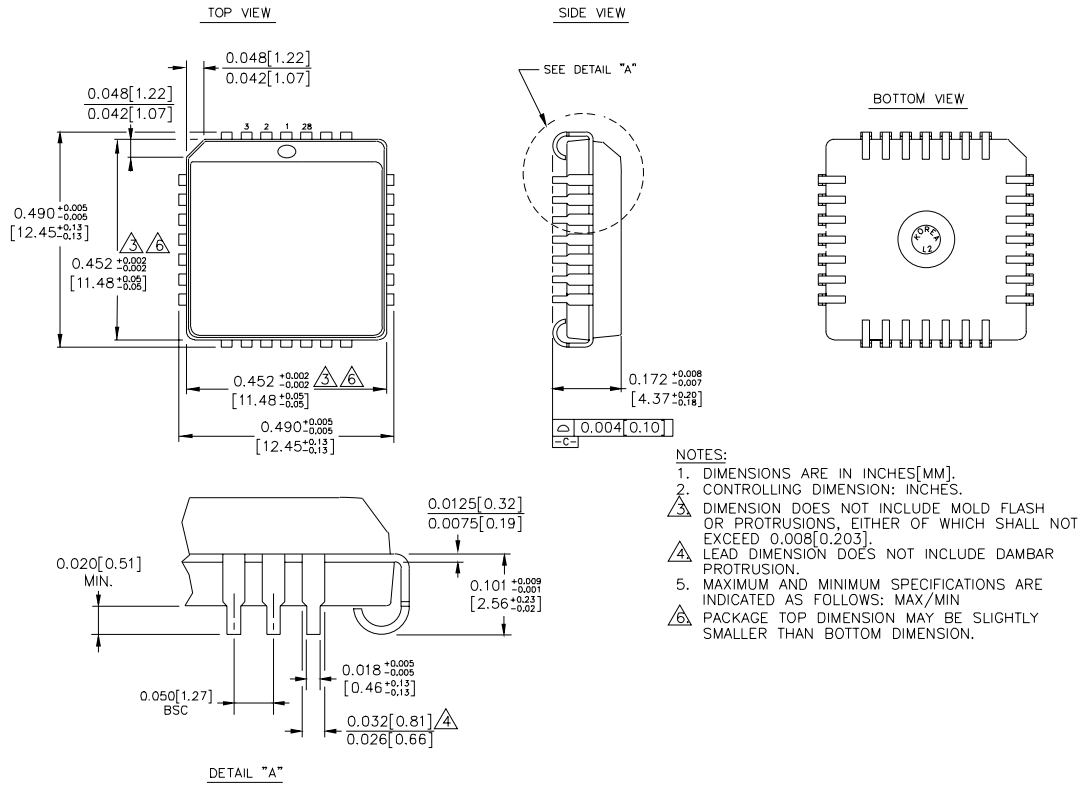
ECL/TTL WAVEFORMS: RISE AND FALL TIMES



PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10H641LC	J28-1	Commercial
SY10H641LJCTR	J28-1	Commercial
SY100H641LJC	J28-1	Commercial
SY100H641LJCTR	J28-1	Commercial

28 LEAD PLCC (J28-1)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

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