# DMC 60C52/32

CMOS SINGLE-COMPONENT 8-BIT MICROCOMPUTER

☐ FEATURES

- ○ 8 bit CPU optimized for control applications.

- ○ Pin-to-pin compatible with intel's 80C52/80C32.

- ○ 60C32 Low power CPU only.

- ○ 64K External Program Memory Space and Data Memory space.

- ○ 256 Bytes of On-Chip Data RAM.

- ○ 32 Programmable I/O Lines.

- ○ Three 16 Bit Timer/Counters.

- ○ Power control Modes.
    - – Idle Mode
    - – Power Down Mode

- ○ 6 interrupt sources.

- ○ TTL and CMOS Compatible Logic Levels.

- ○ MCS-51 Fully Compatible Instruction set.

- ○ ONCE™(ON-Circuit Emulation) Mode.

☐ MAXIMUM RATINGS

- ○ Ambient temperature under Bias ; $0°C \sim +70°C$
- ○ Storage temperature ; $-65°C \sim +150°C$
- ○ Voltage on any pin to Vss ; $-0.5°C \sim Vcc+0.5V$
- ○ Maximum I_{OL} per I/O pin ; 15mA
- ○ Power dissipation ; 1.5W

40DIP   Unit : mm

44PLCC   Unit : mm
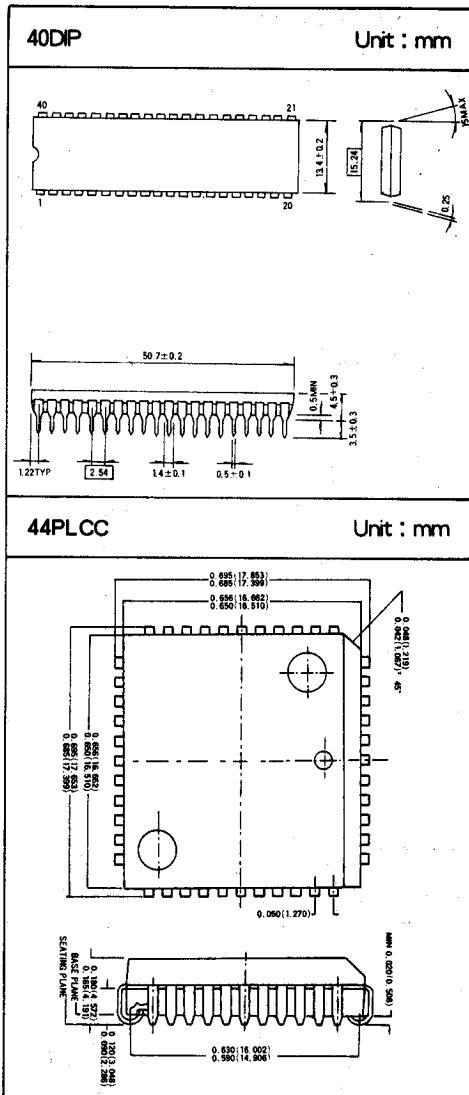
☐ **BLOCK DIAGRAM**
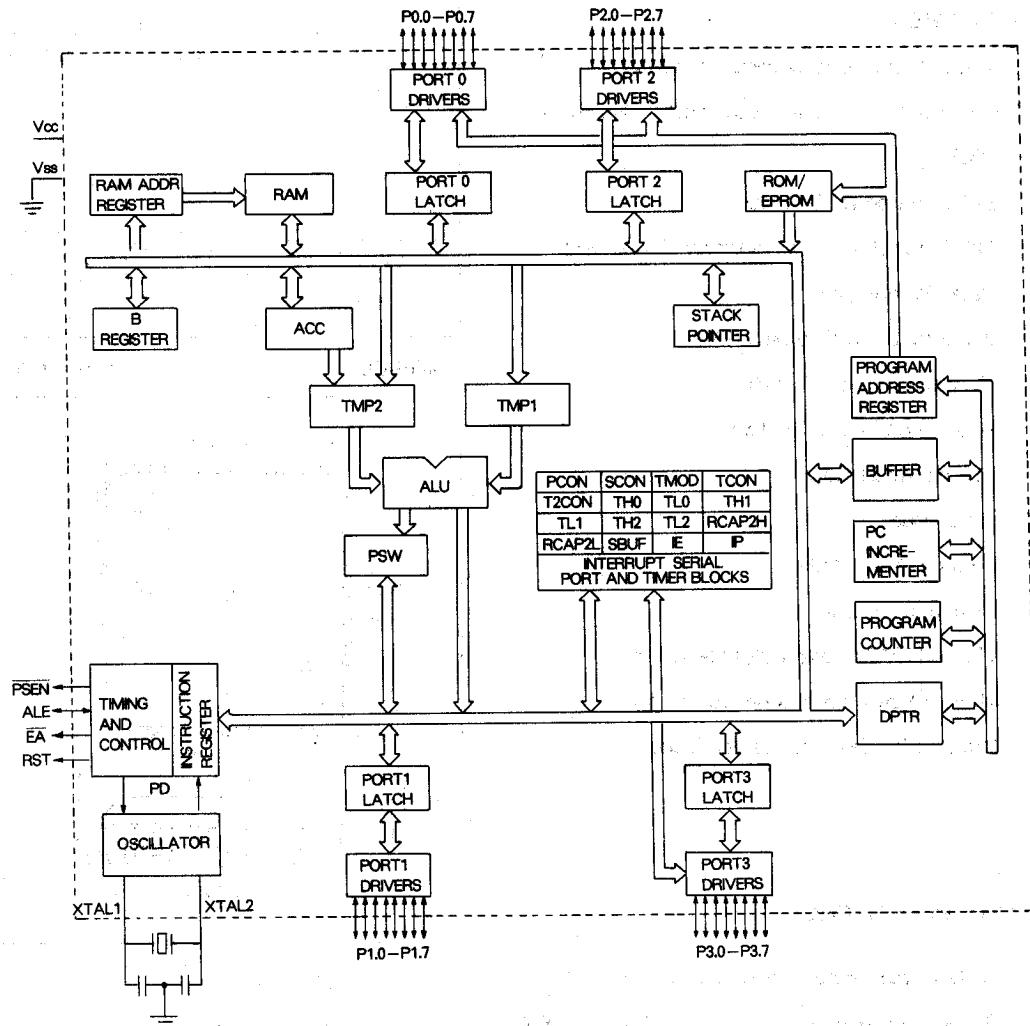
DMC 60C52/32

DESCRIPTION

The DAEWOO 60C32/60C52 is a high-performance micro controller fabricated with DAEWOO high-density CMOS technology. The DAEWOO CMOS technology combines the high speed and density characteristics of MOS with the low power attributes of CMOS.

The 60C52 contains a 8K×8ROM, a 256×8 RAM, 32 I/O lines, Three 16-bit counter/timers, a six source, two-priority level nested interrupt structure, a serial I/O port for either multi-processor communication, I/O expansion or full duplex UART, and on-chip oscillator and clock circuits.

In addition, the device has two software selectable modes of power reduction idle mode and power down mode. The idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning.

The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

PIN CONFIGURATION

40 DIP

T2/P1.0 [1]	[40] Vcc
T2EX/P1.1 [2]	[39] P0.0/AD0
P1.2 [3]	[38] P0.1/AD1
P1.3 [4]	[37] P0.2/AD2
P1.4 [5]	[36] P0.3/AD3
P1.5 [6]	[35] P0.4/AD4
P1.6 [7]	[34] P0.5/AD5
P1.7 [8]	[33] P0.6/AD6
RST [9]	[32] P0.7/AD7
RxD/P3.0 [10]	[31] EA/Vpp
TxD/P3.1 [11]	[30] ALE/PROG
INT0/P3.2 [12]	[29] PSEN
INT1/P3.3 [13]	[28] P2.7/A15
T0/P3.4 [14]	[27] P2.6/A14
T1/P3.5 [15]	[26] P2.5/A13
WR/P3.6 [16]	[25] P2.4/A12
RD/P3.7 [17]	[24] P2.3/A11
XTAL2 [18]	[23] P2.2/A10
XTAL1 [19]	[22] P2.1/A9
Vss [20]	[21] P2.0/A8
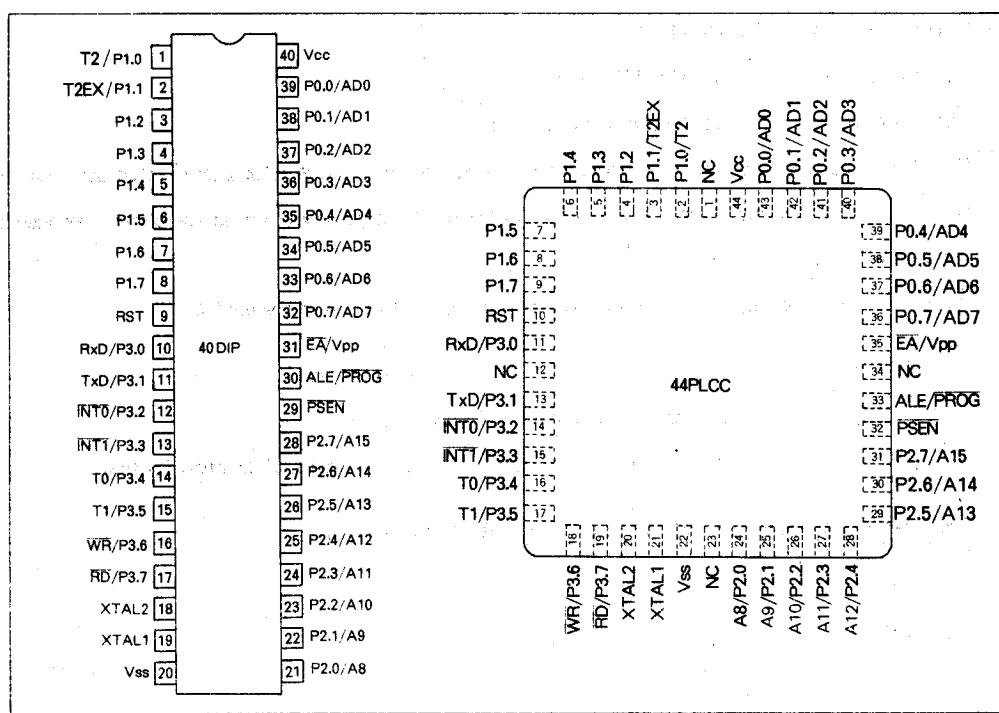
44PLCC

☐ PIN DESCRIPTION

Vcc : PIN40(40DIP), PIN44(44PLCC)

Supply voltage during normal, Idle and Power down operations.

Vss : PIN20(40DIP), PIN22(44PLCC)

Circuit ground.

Port0 : PIN32~39(40DIP), PIN36~43(44PLCC)

Port 0 is an 8-bit open drain bi-directional I/O port.

As an output port each pin can sink several LS TTL inputs.

Port 0 pins that have 1s written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data memory.

In this application it uses strong internal pullups when emitting 1's and can source and sink several LS TTL inputs.

Port 0 outputs the code bytes during program verification on the 60C52 external pullup resistors are required during program verification.

Por 1 : Pin 1~8(40DIP), PIN2~9(44PLCC)

Port 1 output buffers can drive LS TTL inputs.

Port 1 is an 8-bit bidirectional I/O port with internal pullups.

Port 1 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current because of the internal pullups.

In addition, Port 1 serves the functions of the following special features of the 60C52.

Port Pin	Alternate Function
P1.0	T2(External Count Input to Timer/Counter2)
P1.1	T2EX(Timer/Counter2 Capture/Reload Trigger and Direction Control)

Port 1 receives the low-order address bytes during ROM verification.

☐ PIN DESCRIPTION (Continued)

Port 2 : PIN21~28(40DIP), PIN24~31(44PLCC)

Port 2 is an 8-bit bidirectional I/O port with internal pullups. The port 2 output buffers can drive LS TTL inputs.

Port 2 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as input.

As inputs, Part 2 pins that are externally being pulled low will source current because of the internal pullups.

Port 2 emits the high order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16-bit addresses(MOVX @ DPTR). In this application it uses strong internal pullups when emitting 1s. During accesses to external Data Memory that use 8-bit addresses(MOVX @ Ri), Port 2 emits the contents of the P2 Special Function Register.

Port3 : PIN10~17(40DIP), PIN13~19(44PLCC)

Port 3 is an 8-bit bidirectional I/O port with internal pullups.

The port 3 output buffers can drive LS TTL input. Port 3 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current because of the pullups.

Port 3 also serves the function of various special feature of the MCS-51 Family, as listed below ;

Port PIN	PIN NO.	Alternate Function
P 3.0	10	R_xD(Serial input port)
P 3.1	11	T_xD(Serial output port)
P 3.2	12	$\overline{INT0}$ (external interrupt 0)
P 3.3	13	$\overline{INT1}$ (external interrupt 1)
P 3.4	14	T0(Timer 0 external input)
P 3.5	15	T1(Timer 1 external input)
P 3.6	16	$\overline{WR}$ (external data memory write strobe)
P 3.7	17	$\overline{RD}$ (external data memory read strobe)

RST : PIN 9(40DIP), PIN10(44PLCC)

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

An internal pulldown resistor permits a Power-On reset with only a Capacitor connected to Vcc.

☐ PIN DESCRIPTION (Continued)

ALE : PIN30(40DIP), PIN33(44PLCC)

Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes.

Note; however, that one ALE pulse is skipped during each access to external Data Memory.

This pin is also the program pulse input($\overline{PROG}$ during EPROM programming.

$\overline{PSEN}$: PIN29(40DIP), PIN32(44PLCC)

Program Store Enable is the read strobe to external Program memory. When the 60C52 is executing code from external Program Memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external Data Memory. $\overline{PSEN}$ is not activated during fetches from internal program memory.

$\overline{EA}$: PIN31(40DIP), PIN35(44PLCC)

External Access enable. $\overline{EA}$ must be strapped to Vss in order to enable the device to fetch code from external Program Memory locations starting at 0000H up to FFFFH. If $\overline{EA}$ is strapped to Vcc the device executes from internal Program memory unless the program counter contains an address greater than 0FFFH.

XTAL1 : PIN19(40DIP), PIN21(44PLCC)

Input to the inverting oscillator amplifier and input to the internal clock generator circuits.

XTAL2 : PIN18(40DIP), PIN20(44PLCC)

Output from the inverting oscillator amplifier

ⓒ Crystal Oscillator
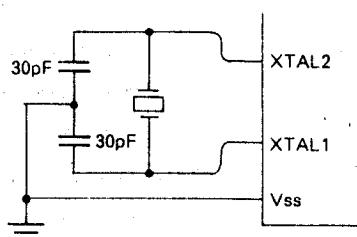
NC : PIN1, 12, 23, 34(44PLCC)

Non connection pins.

☐ IDLE MODE

In the Idle mode, the CPU puts itself to sleep while all the on chip peripherals stay active. The instruction that invokes the Idle mode is the last instruction executed in the normal operation mode before Idle mode is activated. The content of the on-chip RAM and all the Special Function Registers remain intact during this mode. The Idle mode can be terminated either by any enabled interrupt, at which time the process is picked up at the interrupt service routine and continued, or by a hardware reset which starts the processor the same as a power on reset.

☐ POWER DOWN MODE

In the Power Down mode the oscillator is stopped, and the instruction that invokes Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power Down mode is terminated.

The only exit from Power Down is a hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before Vcc is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

The control bits for the reduced power modes are in the Special Function Register PCON.

Table. Status of the external pins during Idle and Power Down modes.

Mode	Program Memory	ALE	PSEN	PORT 0	PORT 1	PORT 2	PORT 3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

☐ **ELECTRICAL CHARACTERISTICS(DC)**

(T_a =0°C~70°C or −40°C~85°C, Vcc=5V±20%, Vss=0V)

| SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
V_{IL}	Input low voltage, except $\overline{EA}$		−0.5		0.2Vcc−0.1	V
V_{IL1}	Input low voltage to $\overline{EA}$		0		0.2Vcc−0.3	V
V_{IH}	Input high voltage, except XTAL1, RST		0.2Vcc+0.9		Vcc+0.5	V
V_{IH1}	Input high voltage to XTAL1, RST		0.7Vcc		Vcc+0.5	V
V_{OL}	Output low voltage to ports 1, 2, 3	I_{OL} =1.6mA			0.45	V
V_{OL1}	Output low voltage to port 0, ALE, $\overline{PSEN}$	I_{OL} =3.2mA			0.45	V
V_{OH}	Output high voltage to ports 1, 2, 3, ALE, $\overline{PSEN}$	I_{OH} =−60μA	Vcc−0.3			V
		I_{OH} =−30μA	Vcc−0.7			V
		I_{OH} =−10μA	Vcc−1.5			V
V_{OH1}	Output high voltage (port 0 in external bus mode)	I_{OH} =−200μA	Vcc−0.3			V
		I_{OH} =−3.2mA	Vcc−0.7			V
		I_{OH} =−7.0mA	Vcc−1.5			V
I_{IL}	Logical 0 input current to ports 1, 2, 3	V_{IN} =0.45V		−10	−50	μA
I_{TL}	Logical 1-to-0 transition current to ports 1, 2, 3	V_{IN} =2V		−265	−650	μA
I_U	Input leakage current to port 0, $\overline{EA}$	0<$V_{IN}$$V_{CC}$		0.02	±10	μA
I_{CC}	Power supply current					
	Active mode @ 12MHz			15	30	mA
	Idle mode @ 12MHz			5	7.5	mA
	Power down mode			5	75	μA
R_{RST}	Internal reset pull-down resistor		40	100	225	kohm
C_{IO}	Pin capacitance			10		pF

DMC 60C52/32

☐ ELECTRICAL CHARACTERISTICS(AC)

$(T_a=0°C\sim70°C$ or $-40°C\sim85°C$, $V_{CC}=5V\pm20\%$, $V_{SS}=0V)$

SYMBOL	FIGURE	PARAMETER	12MHz CLOCK		VARIABLE CLOCK		UNIT
			MIN	MAX	MIN	MAX	
$1/t_{aa}$		Oscillator frequency : Speed Versions 60C52			3.5	16	MHz
t_{LHLL}	1	ALE pulse width	127		$2t_{aa}-40$		ns
t_{AVLL}	1	Address valid to ALE low	43		$t_{aa}-40$		ns
t_{LLAX}	1	Address hold after ALE low	53		$t_{aa}-30$		ns
t_{LLIV}	1	ALE low to valid instruction in		234		$4t_{aa}-100$	ns
t_{LLPL}	1	ALE low to $\overline{PSEN}$ low	53		$t_{aa}-30$		ns
t_{PLPH}	1	$\overline{PSEN}$ pulse width	205		$3t_{aa}-45$		ns
t_{PLIV}	1	$\overline{PSEN}$ low to valid instruction in		145		$3t_{aa}-105$	ns
t_{PXIX}	1	Input instruction hold after $\overline{PSEN}$	0		0		ns
t_{PXIZ}	1	Input instruction float after $\overline{PSEN}$		59		$t_{aa}-25$	ns
t_{AVIV}	1	Address to valid instruction in		312		$5t_{aa}-105$	ns
t_{PLAZ}	1	$\overline{PSEN}$ low to address float		10		10	ns
Data Memory							
t_{RLRH}	2, 3	$\overline{RD}$ pulse width	400		$6t_{aa}-100$		ns
t_{WLWH}	2, 3	$\overline{WR}$ pulse width	400		$6t_{aa}-100$		ns
t_{RLDV}	2, 3	$\overline{RD}$ low to valid data in		252		$5t_{aa}-165$	ns
t_{RHDX}	2, 3	Data hold after $\overline{RD}$	0		0		ns
t_{RHDZ}	2, 3	Data float after $\overline{RD}$		107		$2t_{aa}-60$	ns
t_{LLDV}	2, 3	ALE low to valid data in		517		$8t_{aa}-150$	ns
t_{AVDV}	2, 3	Address to valid data in		585		$9t_{aa}-165$	ns
t_{LLWL}	2, 3	ALE low to $\overline{RD}$ or $\overline{WR}$ low	200	300	$3t_{aa}-50$	$3t_{aa}+50$	ns
t_{AVWL}	2, 3	Address valid to $\overline{WR}$ low or $\overline{RD}$ low	203		$4t_{aa}-130$		ns
t_{QVWX}	2, 3	Data valid to $\overline{WR}$ transition	33		$t_{aa}-50$		ns
t_{WHQX}	2, 3	Data hold after $\overline{WR}$	33		$t_{aa}-50$		ns
t_{QVWH}	2, 3	Data valid to $\overline{WR}$ High	433		$7t_{aa}-150$		ns
t_{RLAZ}	2, 3	$\overline{RD}$ low to address float		0		0	ns
t_{WHLH}	2, 3	$\overline{RD}$ or $\overline{WR}$ high to ALE high	43	123	$t_{aa}-40$	$t_{aa}-40$	ns
External Clock							
t_{CHCX}	4	High time	20		20		ns
t_{CLCX}	4	Low time	20		20		ns
t_{CLCH}	4	Rise time		20		20	ns
t_{CHCL}	4	Fall time		20		20	ns

☐ ELECTRICAL CHARACTERISTICS(Continued)

($T_a=0°C \sim 70°C$ or $-40°C \sim 85°C$, $V_{cc}=5V \pm 20\%$, $V_{ss}=0V$)

SYMBOL	FIGURE	PARAMETER	16MHz CLOCK		VARIABLE CLOCK		UNIT
			MIN	MAX	MIN	MAX	
$1/t_{CLCL}$		Oscillator frequency : Speed Versions 60C52			3.5	16	MHz
t_{LHLL}	1	ALE pulse width	85		$2t_{CLCL}-40$		ns
t_{AVLL}	1	Address valid to ALE low	23		$t_{CLCL}-40$		ns
t_{LLAX}	1	Address hold after ALE low	33		$t_{CLCL}-30$		ns
t_{LLIV}	1	ALE low to valid instruction in		150		$4t_{CLCL}-100$	ns
t_{LLPL}	1	ALE low to PLEN low	23		$t_{CLCL}-40$		ns
t_{PLPH}	1	PSEN pulse width	143		$3t_{CLCL}-45$		ns
t_{PLIV}	1	SPEN low to valid instruction in		83		$3t_{CLCL}-105$	ns
t_{PXIX}	1	Input instruction hold after PSEN	0		0		ns
t_{PXIZ}	1	Input instruction float after PSEN		38		$t_{CLCL}-25$	ns
t_{AVIV}	1	Address to valid instruction in		208		$5t_{CLCL}-105$	ns
t_{PLAZ}	1	PSEN low to address float		10		10	ns
Data memory							
t_{RLRH}	2, 3	RD pulse width	275		$6t_{CLCL}-100$		ns
t_{WLWH}	2, 3	WR pulse width	275		$6t_{CLCL}-100$		ns
t_{RLDV}	2, 3	RD low to valid data in		148		$5t_{CLCL}-165$	ns
t_{RHDX}	2, 3	Data hold after RD	0		0		ns
t_{RHDZ}	2, 3	Data float after RD		55		$2t_{CLCL}-70$	ns
t_{LLDV}	2, 3	ALE low to valid data in		350		$8t_{CLCL}-150$	ns
t_{AVDV}	2, 3	Address to valid data in		398		$9t_{CLCL}-165$	ns
t_{LLWL}	2, 3	ALE low to RD or WR low	138	238	$3t_{CLCL}-50$	$3t_{CLCL}+50$	ns
t_{AVWL}	2, 3	Address valid to WR low or RD low	120		$4t_{CLCL}-130$		ns
t_{ZVWX}	2, 3	Data valid to WR transition	13		$t_{CLCL}-50$		ns
t_{WHQX}	2, 3	Data hold after WR	13		$t_{CLCL}-50$		ns
t_{QVWH}	2, 3	Data valid to WR High	288		$7t_{CLCL}-150$		ns
t_{RLAZ}	2, 3	RD low to address float		0		0	ns
t_{WHLH}	2, 3	RD or WR high to ALE high	23	103	$t_{CLCL}-40$	$t_{CLCL}+40$	ns
External Clock							
t_{CHCX}	4	High time	20		20		ns
t_{CLCX}	4	Low time	20		20		ns
t_{CLCH}	4	Rise time		20		20	ns
t_{CHCL}	4	Fall time		20		20	ns

☐ TIMING DIAGRAM
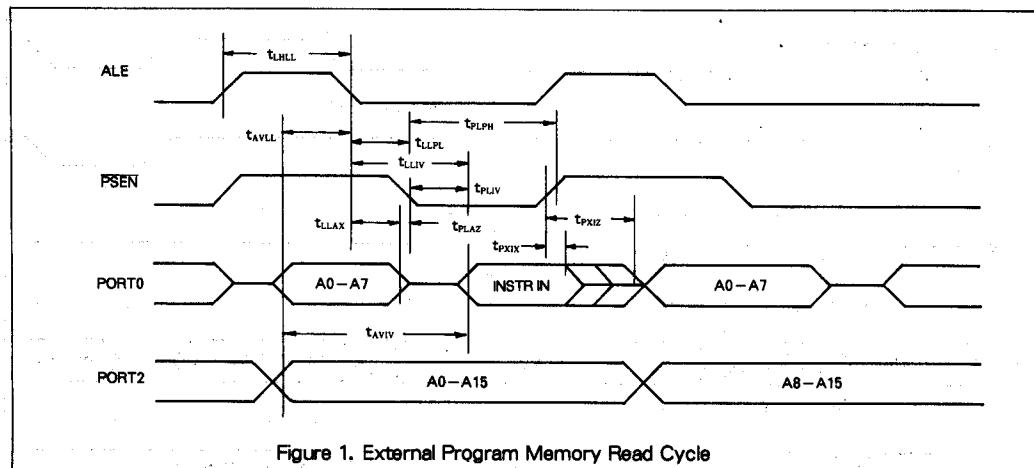
Figure 1. External Program Memory Read Cycle
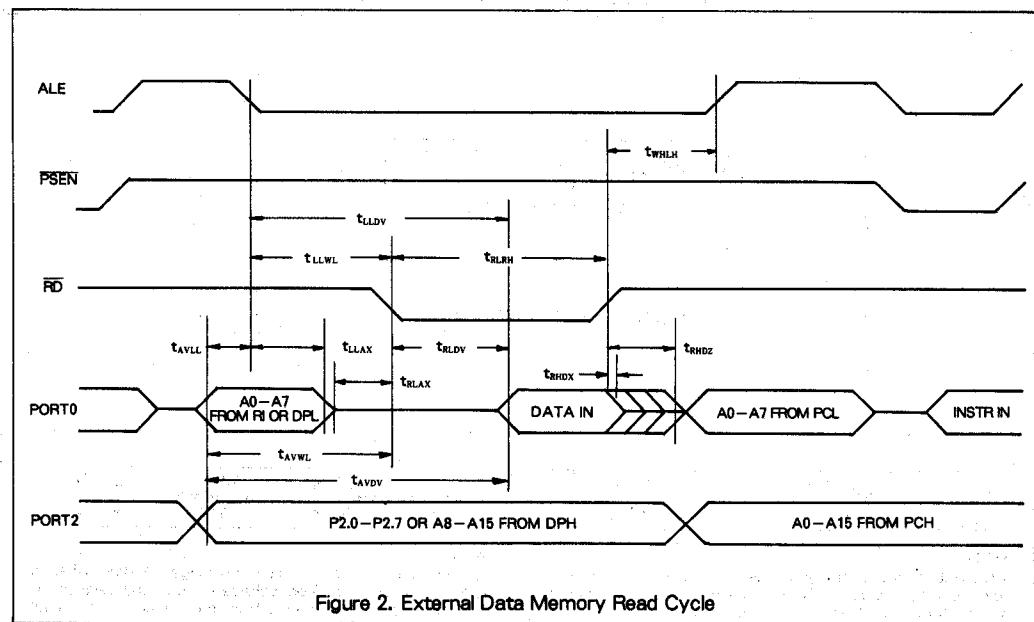
Figure 2. External Data Memory Read Cycle

☐ TIMING DIAGRAM (Continued)
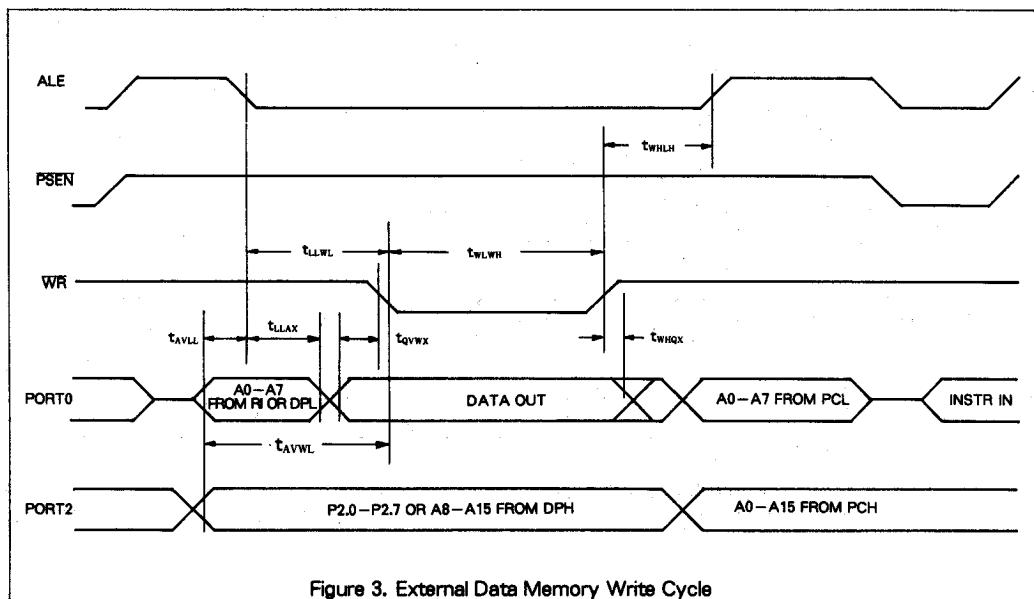
Figure 3. External Data Memory Write Cycle
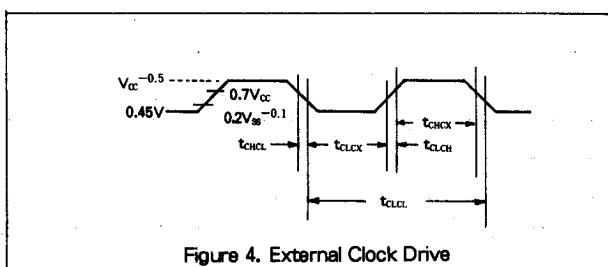
Figure 4. External Clock Drive

NOTE :
AC Inputs during testing are driven at Vcc -0.5 for a logic '1' and 0.45V for a logic '0'. Timing measurements are made at V_{IH} min for a logic '1' and V_{IL} for a logic '0'
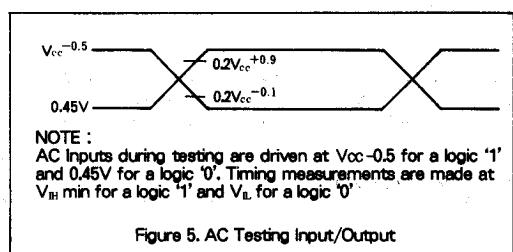
Figure 5. AC Testing Input/Output

NOTE :
For timing purposes, a port is no longer floating when a 100mV change from load voltage occurs, and begins to float when a 100mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OH}/I_{OL} \geq \pm 20mA$.
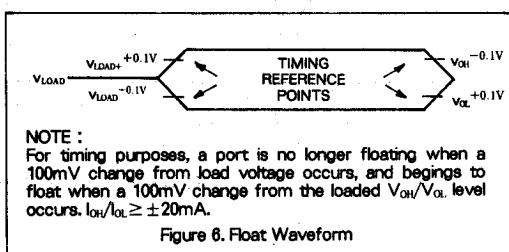
Figure 6. Float Waveform

☐ TIMING DIAGRAM (Continued)
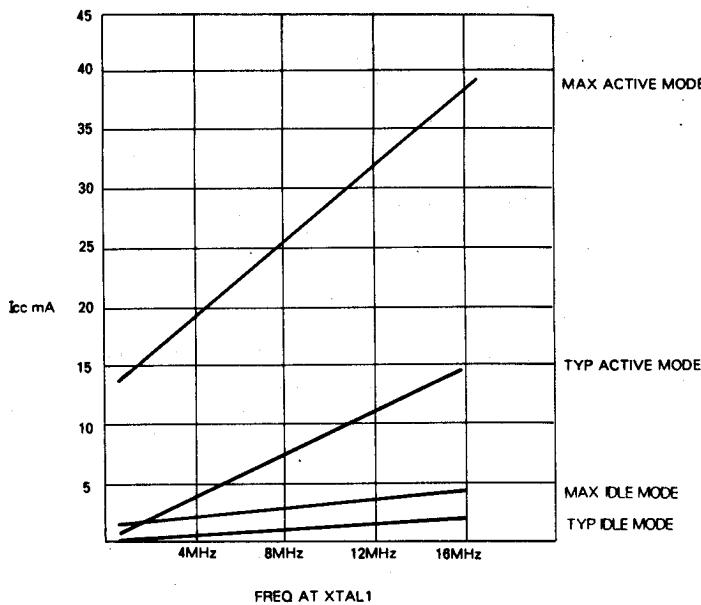
Figure 7. I_{cc} vs. FREQ
Valid only within frequency specifications
of the device under test
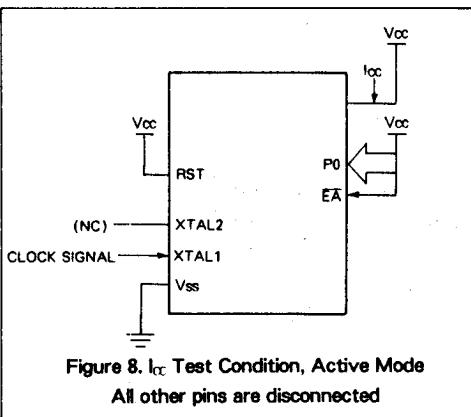
Figure 8. I_{cc} Test Condition, Active Mode
All other pins are disconnected
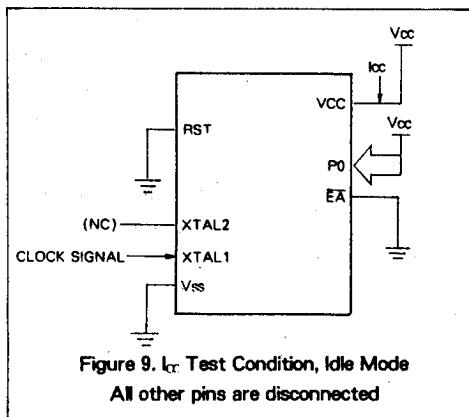
Figure 9. I_{cc} Test Condition, Idle Mode
All other pins are disconnected

TIMING DIAGRAM (Continued)
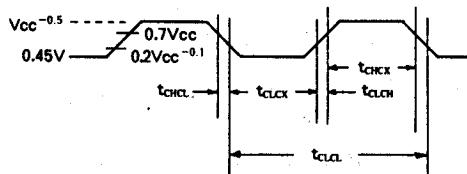
Figure 10. Clock Signal Waveform for I_{cc} Tests in Active and Idle Modes

$t_{CLCH} = t_{CHCL} = 5ns$
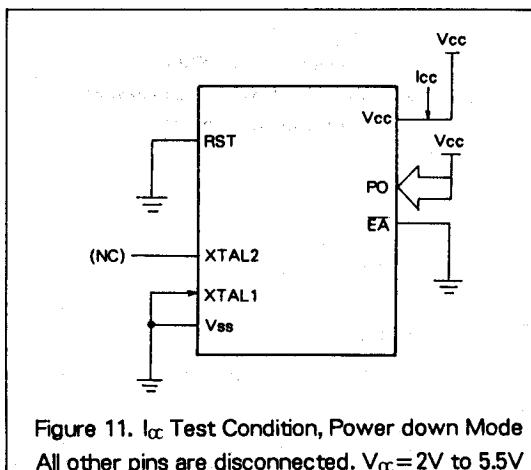
Figure 11. I_{cc} Test Condition, Power down Mode

All other pins are disconnected. $V_{cc} = 2V$ to 5.5V