DATA SHEET

TDA8764A
10-bit high-speed low-power ADC

Product specification
File under Integrated Circuits, IC11

2000 Jul 03

Philips
Semiconductors

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FEATURES

- 10-bit resolution (binary or gray code)
- Sampling rate up to 60 MHz
- DC sampling allowed
- One clock cycle conversion only
- High signal-to-noise ratio over a large analog input frequency range (9.3 effective bits at 5 MHz full-scale input at f_{clk} = 60 MHz)
- No missing codes guaranteed
- In Range (IR) CMOS output
- TTL and CMOS levels compatible digital inputs
- 2.7 to 3.6 V CMOS digital outputs
- Low-level AC clock input signal allowed
- Power dissipation only 312 mW
- Low analog input capacitance, no buffer amplifier required
- No sample-and-hold circuit required.

APPLICATIONS

High-speed analog-to-digital conversion for:

- Video data digitizing
- Radar pulse analysis
- High energy physics research
- Transient signal analysis
- ΣΔ modulators
- Medical imaging.

GENERAL DESCRIPTION

The TDA8764A is a 10-bit high-speed low-power Analog-to-Digital Converter (ADC) for professional video and other applications. It converts the analog input signal into 10-bit binary or gray coded digital words at a maximum sampling rate of 60 MHz. All digital inputs and outputs are TTL and CMOS compatible, although a low-level sine wave clock input signal is allowed.

The device requires an external source to drive its reference ladder.

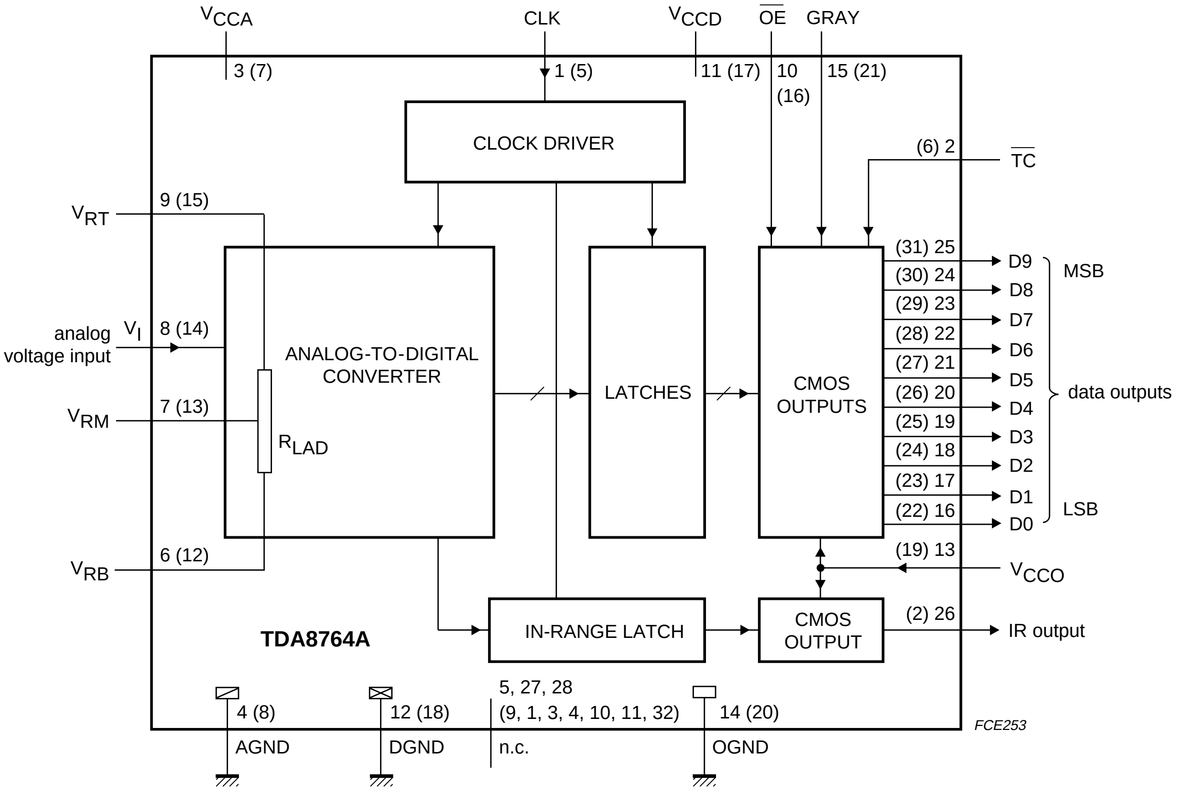
ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8764ATS/6	SSOP28	plastic shrink small outline package; 28 leads; body width 5.3 mm	SOT341-1
TDA8764AHL/6	LQFP32	plastic low profile quad flat package; 32 leads; body 5 × 5 × 1.4 mm	SOT401-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		2.7	3.3	3.6	V
I_{CCA}	analog supply current		–	29	37	mA
I_{CCD}	digital supply current		–	33	40	mA
I_{CCO}	output stages supply current	f_{clk} = 60 MHz; ramp input	–	0.5	2.0	mA
INL	integral non-linearity	f_{clk} = 60 MHz; ramp input	–	±0.8	±2	LSB
DNL	differential non-linearity	f_{clk} = 60 MHz; ramp input	–	±0.35	±0.9	LSB
$f_{clk(max)}$	maximum clock frequency	TDA8764ATS and TDA8764AHL	60	–	–	MHz
P_{tot}	total power dissipation	f_{clk} = 60 MHz; ramp input	–	312	411	mW

BLOCK DIAGRAM



The pin numbers given in parenthesis refer to the TDA8764AHL.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN		DESCRIPTION
	TDA8764ATS	TDA8764AHL	
CLK	1	5	clock input
$\overline{\text{TC}}$	2	6	twos complement input (active LOW)
V_{CCA}	3	7	analog supply voltage (5 V)
AGND	4	8	analog ground
n.c.	5	9	not connected
V_{RB}	6	12	reference voltage BOTTOM input
V_{RM}	7	13	reference voltage MIDDLE input
V_I	8	14	analog input voltage
V_{RT}	9	15	reference voltage TOP input
$\overline{\text{OE}}$	10	16	output enable input (active LOW)
V_{CCD}	11	17	digital supply voltage (5 V)
DGND	12	18	digital ground
V_{CCO}	13	19	supply voltage for output stages (2.7 to 3.6 V)
OGND	14	20	output ground
GRAY	15	21	gray code input (active HIGH)
D0	16	22	data output; bit 0 (LSB)
D1	17	23	data output; bit 1
D2	18	24	data output; bit 2
D3	19	25	data output; bit 3
D4	20	26	data output; bit 4
D5	21	27	data output; bit 5
D6	22	28	data output; bit 6
D7	23	29	data output; bit 7
D8	24	30	data output; bit 8
D9	25	31	data output; bit 9 (MSB)
IR	26	2	in range data output
n.c.	27	1	not connected
n.c.	28	3	not connected
n.c.	–	4	not connected
n.c.	–	10	not connected
n.c.	–	11	not connected
n.c.	–	32	not connected

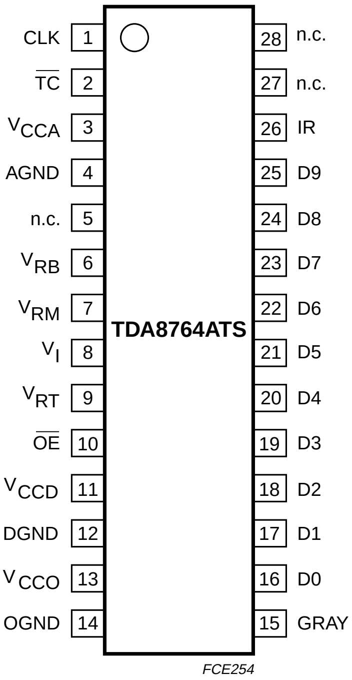


Fig.2 Pin configuration (SSOP28).

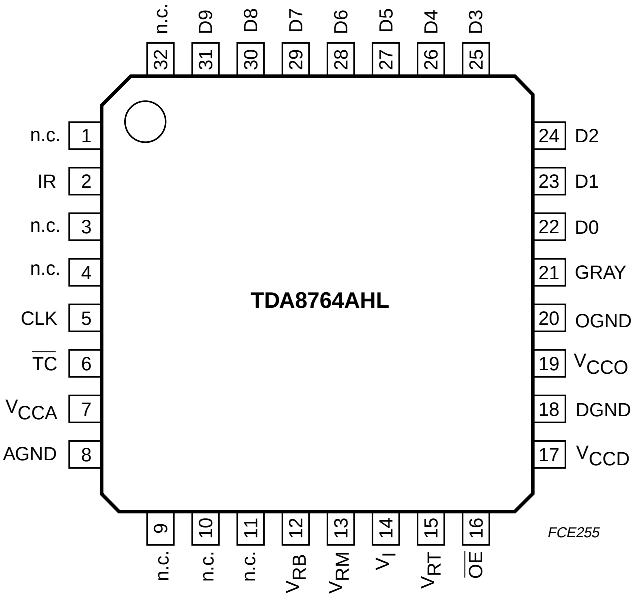


Fig.3 Pin configuration (LQFP32).

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage	note 1	–0.3	+7.0	V
V_{CCD}	digital supply voltage	note 1	–0.3	+7.0	V
V_{CCO}	output stages supply voltage	note 1	–0.3	+7.0	V
ΔV_{CC}	supply voltage difference between				
	$V_{CCA} - V_{CCD}$		–1.0	+1.0	V
	$V_{CCA} - V_{CCO}$		–1.0	+4.0	V
	$V_{CCD} - V_{CCO}$		–1.0	+4.0	V
V_I	input voltage	referenced to AGND	–0.3	+7.0	V
$V_{i(sw)(p-p)}$	AC input voltage for switching (peak-to-peak value)	referenced to DGND	–	V_{CCD}	V
I_O	output current		–	10	mA
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		–40	+85	°C
T_j	junction temperature		–	150	°C

Note

1. The supply voltages V_{CCA}, V_{CCD} and V_{CCO} may have any value between –0.3 and +7.0 V provided that the supply voltage differences ΔV_{CC} are respected.

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		
	SSOP28		110	K/W
	LQFP32		90	K/W

CHARACTERISTICS

V_{CCA} = 4.75 to 5.25 V; V_{CCD} = 4.75 to 5.25 V; V_{CCO} = 2.7 to 3.6 V; AGND and DGND shorted together; T_{amb} = 0 to 70 °C; typical values measured at $V_{CCA} = V_{CCD}$ = 5 V; V_{CCO} = 3.3 V; V_{RB} = 1.3 V; V_{RT} = 3.7 V; C_L = 10 pF and T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		2.7	3.3	3.6	V
ΔV_{CC}	supply voltage difference between					
	$V_{CCA} - V_{CCD}$		–0.20	–	+0.20	V
	$V_{CCA} - V_{CCO}$		–0.20	–	+2.55	V
	$V_{CCD} - V_{CCO}$		–0.20	–	+2.55	V
I_{CCA}	analog supply current		–	29	37	mA
I_{CCD}	digital supply current		–	33	40	mA
I_{CCO}	output stages supply current	f_{clk} = 60 MHz; ramp input	–	0.5	2.0	mA
Inputs						
PIN CLK (REFERENCED TO DGND); note 1						
V_{IL}	LOW-level input voltage		0	–	0.8	V
V_{IH}	HIGH-level input voltage		2	–	V_{CCD}	V
I_{IL}	LOW-level input current	V_{CLK} = 0.8 V	–1	0	+1	μA
I_{IH}	HIGH-level input current	V_{CLK} = 2 V	–	2	10	μA
C_i	input capacitance		–	2	–	pF
PINS $\overline{OE}$; TC AND GRAY (REFERENCED TO DGND); see Tables 3 and 4						
V_{IL}	LOW-level input voltage		0	–	0.8	V
V_{IH}	HIGH-level input voltage		2	–	V_{CCD}	V
I_{IL}	LOW-level input current	V_{IL} = 0.8 V	–1	–	–	μA
I_{IH}	HIGH-level input current	V_{IH} = 2 V	–	–	1	μA
PIN V_I (ANALOG INPUT VOLTAGE REFERENCED TO AGND)						
I_{IL}	LOW-level input current	$V_I = V_{RB}$ = 1.3 V	–	0	–	μA
I_{IH}	HIGH-level input current	$V_I = V_{RT}$ = 3.7 V	–	55	–	μA
Y_i	input admittance	f_i = 5 MHz; note 2				
	R_i input resistance		–	45	–	kΩ
	C_i input capacitance		3	5	7	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reference voltages for the resistor ladder; see Table 1						
V_{RB}	reference voltage BOTTOM		1.2	1.3	2.2	V
V_{RT}	reference voltage TOP		3.4	3.7	$V_{CCA} - 0.8$	V
$V_{diff(ref)}$	differential reference voltage $V_{RT} - V_{RB}$		2.2	2.4	3.2	V
I_{ref}	reference current	$V_{diff} = 2.4$ V	–	17.6	–	mA
R_{LAD}	resistor ladder		–	136	–	Ω
TC_{RLAD}	temperature coefficient of the resistor ladder		–	1860	–	ppm
			–	253	–	mΩ/K
$V_{offset(B)}$	offset voltage BOTTOM	$V_{diff} = 2.4$ V; note 3	–	200	–	mV
$V_{offset(T)}$	offset voltage TOP	$V_{diff} = 2.4$ V; note 3	–	190	–	mV
$V_{I(p-p)}$	analog input voltage (peak-to-peak value)	$V_{diff} = 2.4$ V; note 4	1.95	2.01	2.10	V
Outputs						
PINS D9 TO D0 AND IR (REFERENCED TO OGND)						
V_{OL}	LOW-level output voltage	$I_{OL} = 1$ mA	0	–	0.5	V
V_{OH}	HIGH-level output voltage	$I_{OH} = -1$ mA	$V_{CCO} - 0.5$	–	V_{CCO}	V
I_{OZ}	output current in 3-state mode	$0.5\ V < V_O < V_{CCO}$	–20	–	+20	µA
Switching characteristics						
PIN CLK; see Fig.5; note 1						
$f_{clk(max)}$	maximum clock frequency		60	–	–	MHz
t_{CPH}	clock pulse width HIGH	$T_{amb} = 25$ °C	7.0	–	–	ns
t_{CPL}	clock pulse width LOW	$T_{amb} = 25$ °C	3.5	–	–	ns
Analog signal processing						
LINEARITY						
INL	integral non-linearity	$f_{clk} = 60$ MHz; ramp input	–	±0.8	±2	LSB
DNL	differential non-linearity	$f_{clk} = 60$ MHz; ramp input; no missing code	–	±0.35	±0.9	LSB
E_{offset}	offset error	middle code	–	±1	–	LSB
E_G	gain error (from device to device)	note 5	–	±0.5	–	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
BANDWIDTH (f_{CLK} = 60 MHz)						
B	analog bandwidth	full-scale sine wave; note 6	–	30	–	MHz
		75% full-scale sine wave; note 6	–	45	–	MHz
		small signal at mid-scale; V_I = ±10 LSB at code 512; note 6	–	700	–	MHz
t_{stLH}	analog input settling time LOW-to-HIGH	full-scale square wave; see Fig.7; note 7	–	5	–	ns
t_{stHL}	analog input settling time HIGH-to-LOW	full-scale square wave; see Fig.7; note 7	–	5	–	ns
HARMONICS (f_{CLK} = 60 MHz)						
$H_{all(FS)}$	harmonics (full-scale); all components	f_i = 5 MHz				
	second harmonic		–	–68	–	dB
	third harmonic		–	–67	–	dB
SFDR	spurious free dynamic range	f_i = 5 MHz	–	72	–	dB
THD	total harmonic distortion	f_i = 5 MHz	–	–64	–	dB
		f_i = 15 MHz	–	–57	–	dB
SIGNAL-TO-NOISE RATIO; note 8						
SNR_{FS}	signal-to-noise ratio (full-scale)	without harmonics; f_{clk} = 60 MHz; f_i = 5 MHz	–	58	–	dB
		without harmonics; f_{clk} = 60 MHz; f_i = 15 MHz	53	57	–	dB
EFFECTIVE BITS; note 8						
EB	effective bits	f_{clk} = 60 MHz				
		f_i = 5 MHz	–	9.3	–	bits
		f_i = 10 MHz	–	8.9	–	bits
		f_i = 15 MHz	–	8.8	–	bits
		f_i = 20 MHz	–	8.6	–	bits
TWO-TONE; note 9						
TTID	two-tone intermodulation distortion	f_{clk} = 60 MHz	–	–67	–	dB
BIT ERROR RATE						
BER	bit error rate	f_{clk} = 60 MHz; f_i = 5 MHz; V_I = ±16 LSB at code 512	–	10^{-13}	–	times/ sample

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing (f_{clk} = 60 MHz; C_L = 10 pF); see Fig.5 and note 10						
t_{ds}	sampling delay time		–	0.7	2	ns
t_h	output hold time		4	–	–	ns
t_d	output delay time TDA8764ATS	V_{CCO} = 2.7 V	–	10	14	ns
		V_{CCO} = 3.3 V	–	9	13	ns
t_d	output delay time TDA8764AHL	V_{CCO} = 2.7 V	–	13	17	ns
		V_{CCO} = 3.3 V	–	12	16	ns
C_L	digital output load capacitance		–	–	10	pF
SR	slew rate	V_{CCO} = 2.7 V	0.2	0.3	–	V/ns
3-state output delay times (f_{clk} = 60 MHz); see Fig.6						
t_{dZH}	enable HIGH	V_{CCO} = 3.3 V	–	16	20	ns
t_{dZL}	enable LOW	V_{CCO} = 3.3 V	–	30	34	ns
t_{dHZ}	disable HIGH	V_{CCO} = 3.3 V	–	25	30	ns
t_{dLZ}	disable LOW	V_{CCO} = 3.3 V	–	23	27	ns

Notes

1. The rise and fall times of the clock signal must not be less than 0.5 ns.
2. The input admittance is $Y_i = \frac{1}{R_i} + j\omega Ci$
3. Analog input voltages producing code 0 up to and including code 1023:
   a) $V_{offset(B)}$ (offset voltage BOTTOM) is the difference between the analog input which produces data equal to 00 and the reference voltage BOTTOM (V_{RB}) at T_{amb} = 25 °C.

   b) $V_{offset(T)}$ (offset voltage TOP) is the difference between V_{RT} (reference voltage TOP) and the analog input which produces data outputs equal to code 1023 at T_{amb} = 25 °C.
4. In order to ensure the optimum linearity performance of such converter architecture the lower and upper extremities of the converter reference resistor ladder (corresponding to output codes 0 and 1023 respectively) are connected to pins V_{RB} and V_{RT} via offset resistors R_{OB} and R_{OT} as shown in Fig.4.

   a) The current flowing into the resistor ladder is $I_L = \frac{V_{RT} - V_{RB}}{R_{OB} + R_L + R_{OT}}$ and the full-scale input range at the converter, to cover code 0 to 1023, is $V_I = R_L \times I_L = \frac{R_L}{R_{OB} + R_L + R_{OT}} \times (V_{RT} - V_{RB}) = \dot{0}.8375 \times (V_{RT} - V_{RB})$

   b) Since R_L, R_{OB} and R_{OT} have similar behaviour with respect to process and temperature variation, the ratio $\frac{R_L}{R_{OB} + R_L + R_{OT}}$ will be kept reasonably constant from device to device. Consequently variation of the output codes at a given input voltage depends mainly on the difference $V_{RT} - V_{RB}$ and its variation with temperature and supply voltage. When several ADCs are connected in parallel and fed with the same reference source, the matching between each of them is then optimized.
5. $E_G = \frac{(V_{1023} - V_0) - V_{i(p-p)}}{V_{i(p-p)}} \times 100$
6. The analog bandwidth is defined as the maximum input sine wave frequency which can be applied to the device. No glitches greater than 2 LSBs, nor any significant attenuation are observed in the reconstructed signal.

7. The analog input settling time is the minimum time required for the input signal to be stabilized after a sharp full-scale input (square wave signal) in order to sample the signal and obtain correct output data.
8. Effective bits are obtained via a Fast Fourier Transform (FFT) treatment taking 8K acquisition points per equivalent fundamental period. The calculation takes into account all harmonics and noise up to half of the clock frequency (Nyquist frequency). Conversion to signal-to-noise ratio: $S/N = EB \times 6.02 + 1.76$ dB.
9. Intermodulation measured relative to either tone with analog input frequencies of 4.5 and 4.3 MHz. The two input signals have the same amplitude and the total amplitude of both signals provides full-scale to the converter.
10. Output data acquisition: the output data is available after the maximum delay time of t_d. It is recommended to have the lowest possible output load. These parameters are guaranteed by characterization and not by production test.

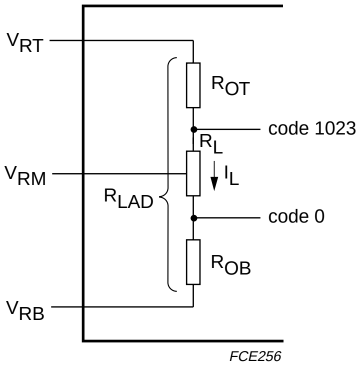


Fig.4 Explanation of note 4.

Table 1 Output coding and input voltage (typical values; referenced to AGND; V_{RB} = 1.3 V; V_{RT} = 3.7 V; binary/gray codes

STEP	V_I	IR	BINARY OUTPUT BITS										GRAY OUTPUT BITS									
			D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
U/F	<1.5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1.5	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	:	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
1022	:	1	1	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	1
1023	3.51	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
O/F	>3.51	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0

Table 2 Output coding and input voltage (typical values; referenced to AGND; binary/twos complement codes

STEP	V_I	IR	BINARY OUTPUT BITS										TWOS COMPLEMENT OUTPUT BITS									
			D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
U/F	<1.5	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	1.5	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
1	:	1	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
1022	:	1	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	1	1	0
1023	3.51	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
O/F	>3.51	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1

Table 3 $\overline{\text{TC}}$ mode selection

$\overline{\text{TC}}$	$\overline{\text{OE}}$	D9 to D0	IR
X	1	high-impedance	high-impedance
0	0	active; twos complement	active
1	0	active; binary	active

Table 4 Gray mode selection

GRAY	$\overline{\text{OE}}$	D9 to D0	IR
X	1	high-impedance	high-impedance
0	0	active; binary	active
1	0	active; gray	active

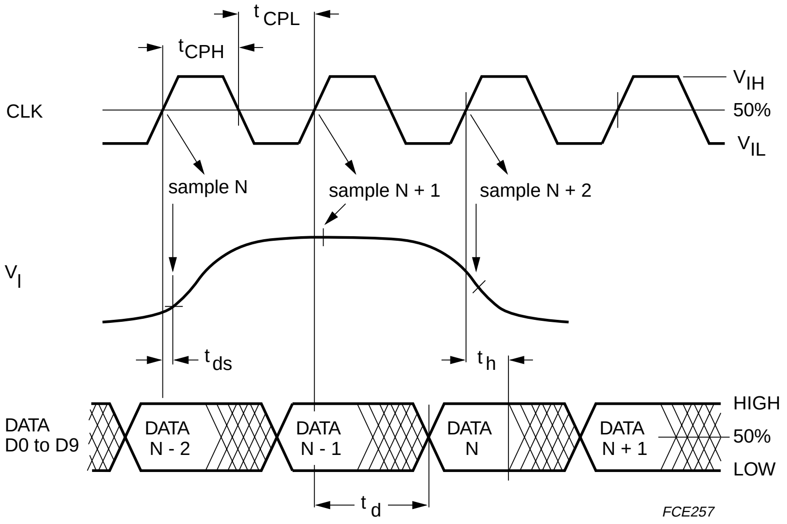
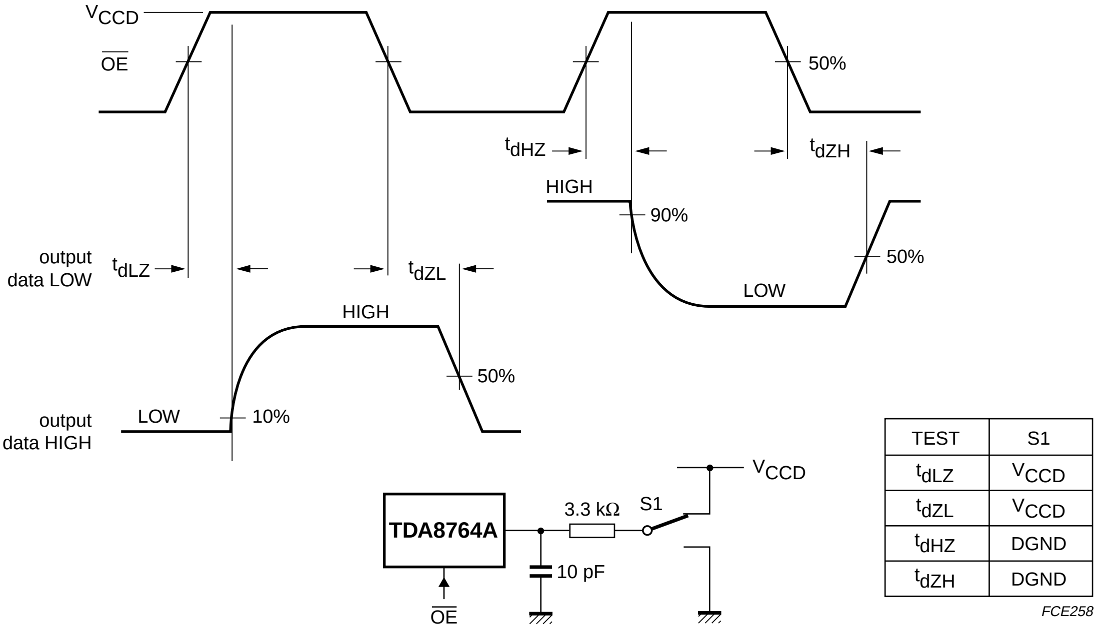


Fig.5 Timing diagram.



TEST	S1
t_{dLZ}	V_{CCD}
t_{dZL}	V_{CCD}
t_{dHZ}	DGND
t_{dZH}	DGND

f_{OE} = 100 kHz.

Fig.6 Timing diagram and test conditions of 3-state output delay time.

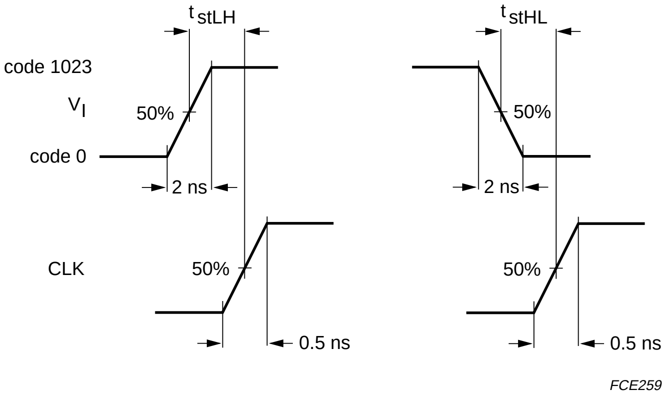


Fig.7 Analog input settling-time diagram.

INTERNAL PIN CONFIGURATIONS

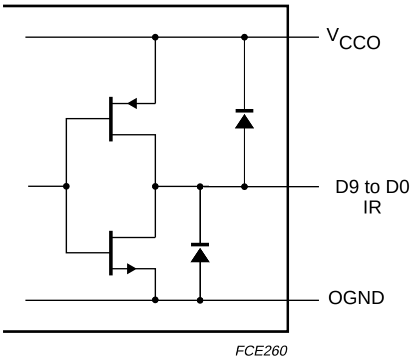


Fig.8 CMOS data and in range outputs.

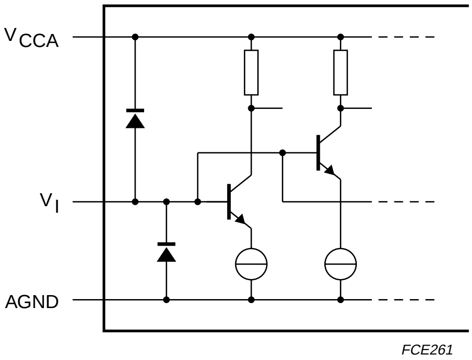


Fig.9 Analog input.

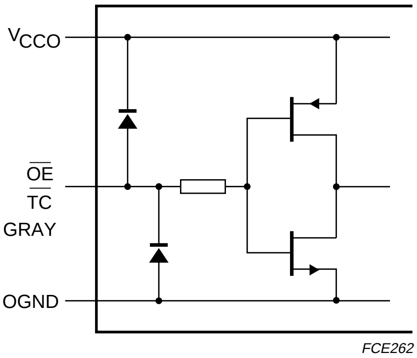


Fig.10 $\overline{OE}$, GRAY and $\overline{TC}$ inputs.

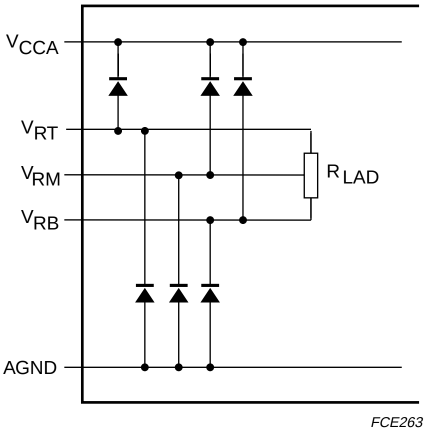


Fig.11 V_{RB}, V_{RM} and V_{RT} inputs.

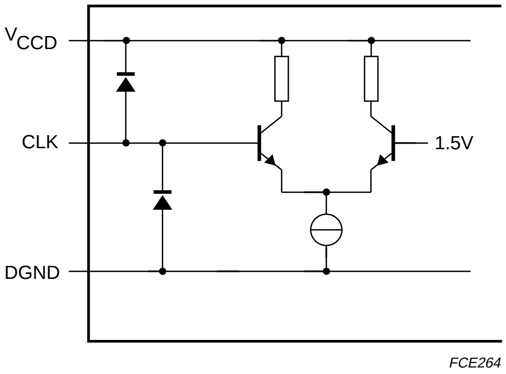
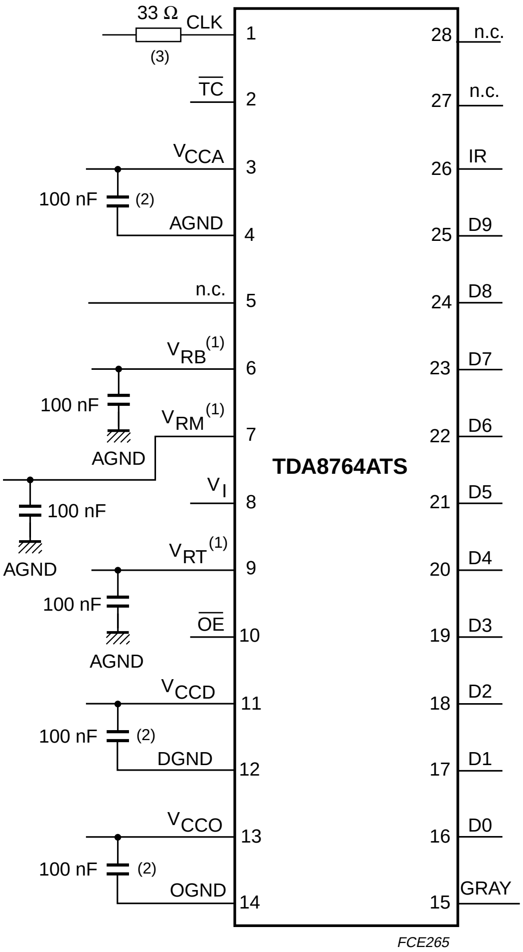


Fig.12 CLK input.

APPLICATION INFORMATION



The analog and digital supplies should be separated and well decoupled.

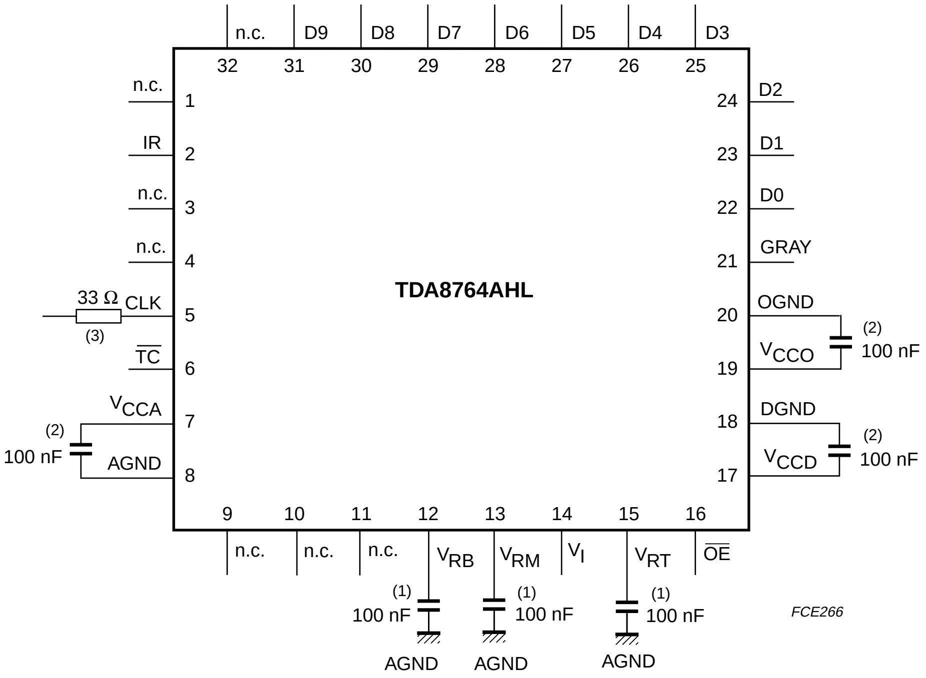
An application note is available and describes the design and the realization of a demoboard that uses TDA8764ATS with an application environment.

(1) V_{RB}, V_{RM} and V_{RT} are decoupled to AGND.

(2) Decoupling capacitor for supplies **must be placed close to the device.**

(3) This resistor is mandatory (33 Ω is its minimum value) and must be near the clock source.

Fig.13 Application diagram (SSOP28).



The analog and digital supplies should be separated and well decoupled.

An application note is available and describes the design and the realization of a demoboard that uses TDA8764AHL with an application environment.

(1) V_{RB}, V_{RM} and V_{RT} are decoupled to AGND.

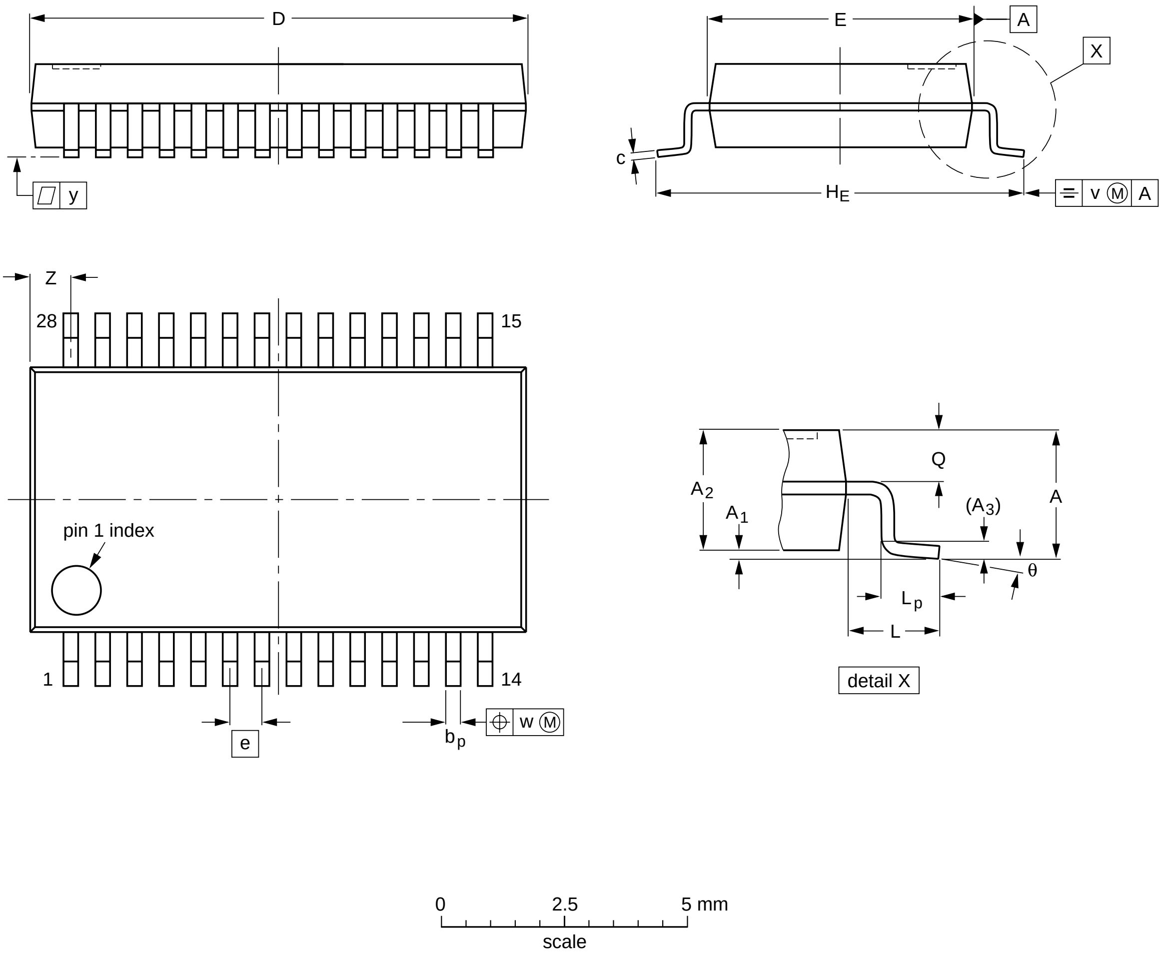
(2) Decoupling capacitor for supplies **must be placed close to the device.**

(3) This resistor is mandatory (33 Ω is its minimum value) and must be near the clock source.

Fig.14 Application diagram (LQFP32).

PACKAGE OUTLINES

SSOP28: plastic shrink small outline package; 28 leads; body width 5.3 mm SOT341-1



DIMENSIONS (mm are the original dimensions)

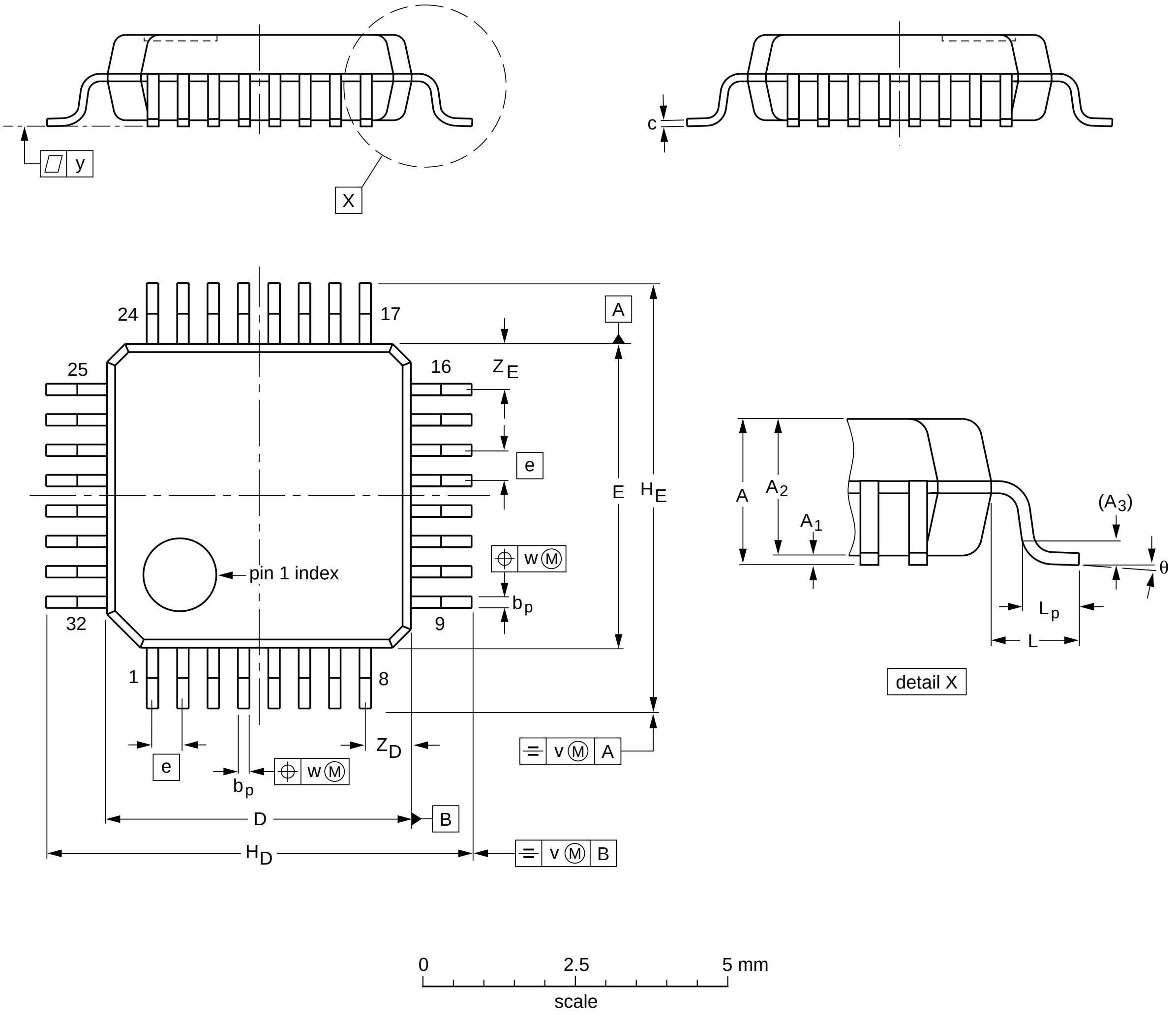
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	10.4 10.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.1 0.7	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT341-1		MO-150				~~95-02-04~~ 99-12-27

LQFP32: plastic low profile quad flat package; 32 leads; body 5 x 5 x 1.4 mm **SOT401-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.15 0.05	1.5 1.3	0.25	0.27 0.17	0.18 0.12	5.1 4.9	5.1 4.9	0.5	7.15 6.85	7.15 6.85	1.0	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT401-1	136E01	MS-026				~~99-12-27~~ 00-01-19

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *“Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS (1)
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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SCA70

Printed in The Netherlands 613502/01/pp24 Date of release: 2000 Jul 03 Document order number: 9397 750 06996

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