DATA SHEET

PCK2000

CK97 (66/100MHz) System Clock Generator

Product specification

1998 Sep 29

Philips
Semiconductors

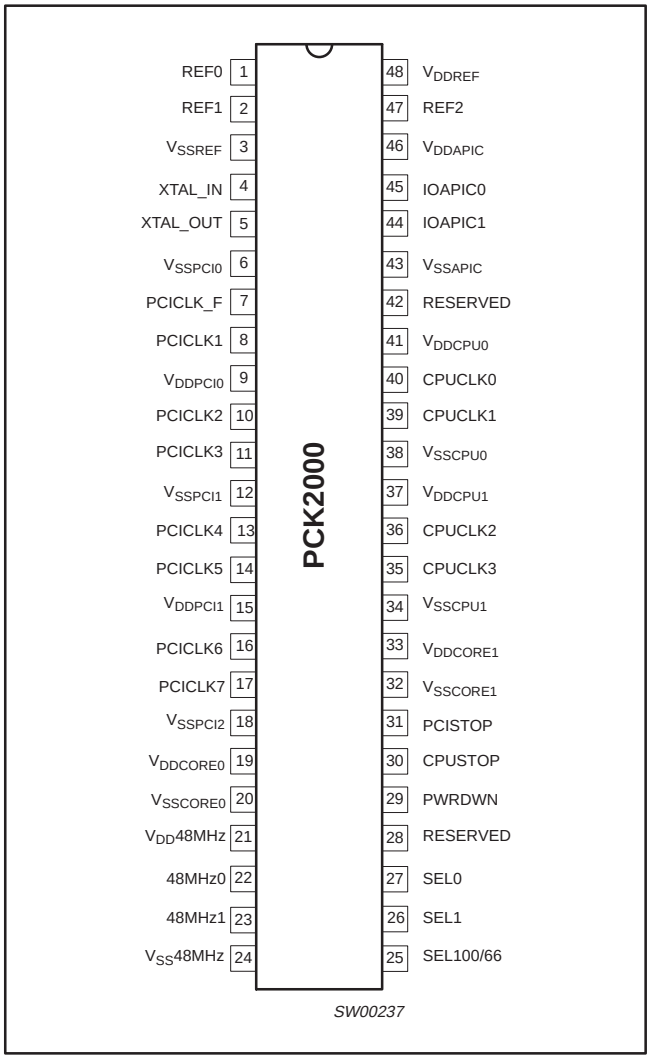
PHILIPS

CK97 (66/100MHz) System Clock Generator PCK2000

FEATURES

- Mixed 2.5V and 3.3V operation
- Four CPU clocks at 2.5V
- Eight synchronous PCI clocks at 3.3V, one free-running
- Two 2.5V IOAPIC clocks @ 14.318 MHz
- Two 3.3V 48MHz USB clock outputs
- Three 3.3V reference clocks @ 14.318 MHz
- Reference 14.31818 MHz Xtal oscillator input
- 100 MHz or 66 MHz operation
- Part provides frequencies for Pentium Pro and Pentium II™ motherboards
- Power management control input pins
- 175 ps CPU clock jitter
- 175 ps skew on outputs
- 1.5 – 4 ns CPU–PCI delay
- Power down if PWRDWN is held LOW
- Available in 48-pin SSOP package
- See PCK2000M for 28-pin mobile version

PIN CONFIGURATION



SW00237

DESCRIPTION

The PCK2000 is a clock synthesizer/driver chip for a Pentium Pro or other similar processors.

The PCK2000 has four CPU clock outputs at 2.5V. There are eight PCI clock outputs running at 33MHz. One of the PCI clock outputs is free-running. Additionally, the part has two 3.3V USB clock outputs at 48MHz, two 2.5V IOAPIC clock outputs at 14.318MHz, and three 3.3V reference clock outputs at 14.318MHz. All clock outputs meet Intel's drive strength, rise/fall time, jitter, accuracy, and skew requirements.

The part possesses dedicated powerdown, CPUSTOP, and PCISTOP input pins for power management control. These inputs are synchronized on-chip and ensure glitch-free output transitions. When the CPUSTOP input is asserted, the CPU clock outputs are driven LOW. When the PCISTOP input is asserted, the PCI clock outputs are driven LOW, except for free running PCICLK_F clock output..

Finally, when the PWRDWN input pin is asserted, the internal reference oscillator and PLLs are shut down, and all outputs are driven LOW.

The PCK2000 is available in a 48–pin SSOP package.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DRAWING NUMBER
48-Pin Plastic SSOP	0°C to +70°C	PCK2000 DL	PCK2000 DL	SOT370-1

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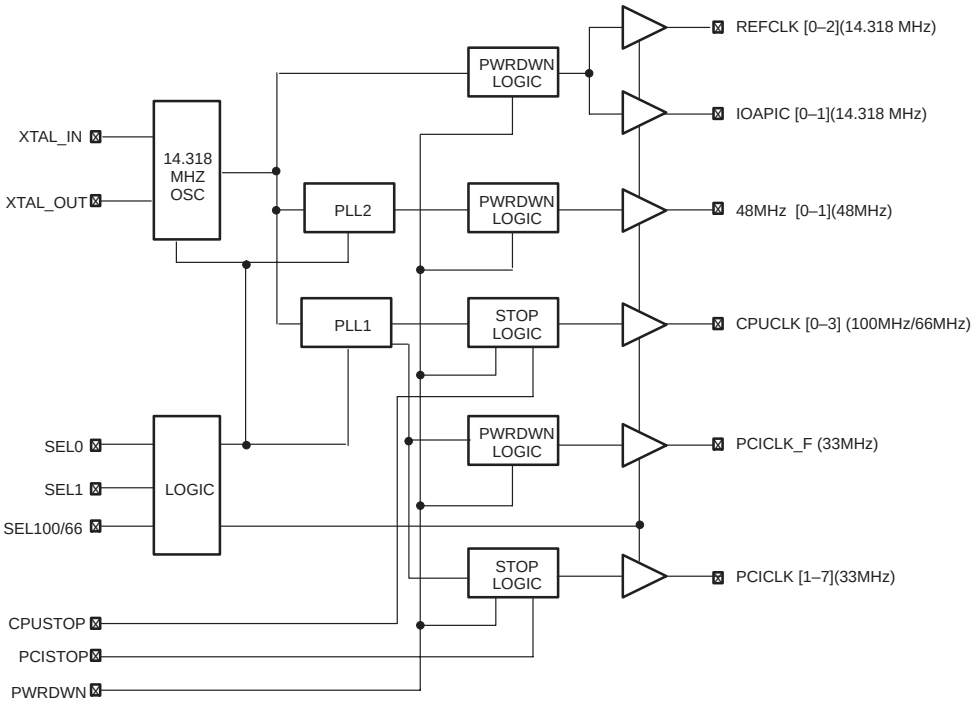
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 2, 47	REF [0–2]	14.318 MHz clock outputs
3	V_{SSREF}	GROUND for REF outputs
48	V_{DDREF}	POWER for REF outputs
4	XTAL_IN	14.318 MHz crystal input
5	XTAL_OUT	14.318 MHz crystal output
6, 12, 18	V_{SSPCI} [0–2]	GROUND for PCI outputs
7	PCICLK_F	Free-running PCI output
9, 15	V_{DDPCI} [0–1]	POWER for PCI outputs
8, 10, 11, 13, 14, 16, 17	PCICLK [1–7]	PCI clock outputs.
19, 33	V_{DDCORE} [0–1]	Isolated POWER for core
20, 32	V_{SSCORE} [0–1]	Isolated GROUND for core
21	V_{DD} 48MHz	POWER for 48MHz outputs
24	V_{SS} 48MHz	GROUND for 48MHz outputs
22, 23	48MHz [0–1]	48MHz outputs
26, 27	SEL0,1	Logic select pins.
25	SEL100/66	Select pin for enabling 66 MHz or 100MHz. L = 66 MHz H = 100MHz
29	PWRDWN	Control pin to put device in powerdown state, active low
30	CPUSTOP	Control pin to disable CPU clocks, active low
31	PCISTOP	Control pin to disable PCI clocks, active low
37, 41	V_{DDCPU} [0–1]	POWER for CPU outputs
34, 38	V_{SSCPU} [0–1]	GROUND for CPU outputs
35, 36, 39, 40	CPUCLK [0–3]	CPU clock outputs @2.5V
43	V_{SSAPIC}	GROUND for IOAPIC outputs
46	V_{DDAPIC}	POWER for IOAPIC outputs
44, 45	IOAPIC [0–1]	IOAPIC output @ 2.5V
28, 42	RESERVED	Reserved for future use

NOTES:

1. V_{DD} and V_{SS} names in the above tables reflects a likely internal POWER and GROUND partition to reduce the effects of internal noise on the performance of the device. In reality, the platform will be configured with the V_{DDAPIC} and V_{DDCPU} pins tied to a 2.5V supply, all remaining V_{DD} pins tied to a common 3.3V supply and all V_{SS} pins being common.

BLOCK DIAGRAM



SELECT FUNCTIONS

SEL100/66	SEL1	SEL0	FUNCTION	NOTES
0	0	0	TRI-State	1
0	0	1	Reserved	
0	1	0	Reserved	
0	1	1	Active 66MHz	
1	0	0	Test mode	1
1	0	1	Reserved	
1	1	0	Reserved	
1	1	1	Active 100MHz	

NOTE:
1. Internal decode logic for all three select inputs implemented.

FUNCTION DESCRIPTION	OUTPUTS					
	CPU	PCI, PCI_F	48MHz	REF	IOAPIC	NOTES
3-STATE	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	
TEST MODE	TCLK/2	TCLK/6	TCLK/2	TCLK	TCLK	

NOTE:
1. TCLK is a test clock driven in on the XTAL_IN input in Test Mode.

FUNCTION TABLE

SEL 100/66	CPU/PCI RATIO	CPUCLK (0–3) (MHz)	CPICLK (1–7) PCICLK_F (MHz)	REF (0–2) IOAPIC (0–1) (MHz)	48MHz (0–1)
0	2	66.66	33.33	14.318	48
1	3	100	33.33	14.318	48

CLOCK ENABLE CONFIGURATION

CPUSTOP	PCISTOP	PWRDWN	CPUCLK	PCICLK	PCICLK_F	OTHER CLOCKS	PLLs	OSCILLATOR
X	X	0	LOW	LOW	LOW	Stopped	OFF	OFF
0	0	1	LOW	LOW	33MHz	Running	Running	Running
0	1	1	LOW	33MHz	33MHz	Running	Running	Running
1	0	1	100/66MHz	LOW	33MHz	Running	Running	Running
1	1	1	100/66MHz	33MHz	33MHz	Running	Running	Running

POWER MANAGEMENT REQUIREMENTS

SIGNAL	SIGNAL STATE	LATENCY
		NO. OF RISING EDGES OF FREE RUNNING PCICLK
CPUSTOP	0 (DISABLED)	1
	1 (ENABLED)	1
PCISTOP	0 (DISABLED)	1
	1 (ENABLED)	1
PWRDWN	1 (NORMAL OPERATION)	3ms
	0 (POWER DOWN)	2 MAX

NOTES:
1. Clock ON/OFF latency is defined as the number of rising edges of free running PCICLKs between the clock disable goes HIGH/LOW to the first valid clock that comes out of the device.
2. Power up latency is when PWRDWN goes inactive (HIGH) to when the first valid clocks are driven from the device.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to V_{SS} (V_{SS} = 0V)

SYMBOL	PARAMETER	CONDITION	LIMITS		UNIT
			MIN	MAX	
V_{DD3}	DC 3.3V core supply voltage		–0.5	+4.6	V
V_{DDQ3}	DC 3.3V I/O supply voltage		–0.5	+4.6	V
V_{DDQ2}	DC 2.5V I/O supply voltage		–0.5	+3.6	V
I_{IK}	DC input diode current	V_I < 0		–50	mA
V_I	DC input voltage	Note 2	–0.5	5.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or V_O < 0		±50	mA
V_O	DC output voltage	Note 2	–0.5	V_{CC} + 0.5	V
I_O	DC output source or sink current	V_O >= 0 to V_{CC}		±50	mA
T_{STG}	Storage temperature range		–65	+150	°C
P_{TOT}	Power dissipation per package plastic medium-shrink (SSOP)	For temperature range: –40 to +125°C above +55°C derate linearly with 11.3mW/K		850	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{DD3}	DC 3.3V core supply voltage	Note 1	3.135	3.465	V
V_{DDQ3}	DC 3.3V I/O supply voltage	Note 2	3.135	3.465	V
V_{DDQ2}	DC 2.5V I/O supply voltage	Note 3	2.135	2.625	V
V_I	DC input voltage range		0	V_{DD3}	V
V_O	DC output voltage range		0	V_{DDQ2} V_{DDQ3}	V
T_{amb}	Operating ambient temperature range in free air		0	+70	°C

NOTES:
1. $V_{DD3} = V_{DDCORE1} = V_{DDCORE2}$ = 3.3V
2. $V_{DDQ3} = V_{DDREF} = V_{DDPCI0} = V_{DDPCI1} = V_{DD48MHz}$ = 3.3V
3. $V_{DDQ2} = V_{DDAPIC} = V_{DDCPU0} = V_{DDCPU1}$ = 2.5V

DC CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS			LIMITS T_{amb} = 0°C to +70°C			UNIT
		V_{DD} (V)	OTHER		MIN	TYP	MAX	
V_{IH}	HIGH level input voltage	3.135 to 3.465		V_{DDQ2} = 2.5V ±5%	2.0		V_{DD} + 0.3	V
V_{IL}	LOW level input voltage	3.135 to 3.465		V_{DDQ3} = 3.3V ±5%	V_{SS} – 0.3		0.8	V
V_{OH2}	2.5V output HIGH voltage CPUCLK, IOAPIC	2.375 to 2.625	I_{OH} = –1mA	V_{DDQ3} = 3.3V ±5%	2.0		–	V
V_{OL2}	2.5V output LOW voltage CPUCLK, IOAPIC	2.375 to 2.625	I_{OL} = 1mA		–		0.4	V
V_{OH3}	3.3V output HIGH voltage REF, 48MHz	3.135 to 3.465	I_{OH} = –1mA		2.0		–	V
V_{OL3}	3.3V output LOW voltage REF, 48MHz	3.135 to 3.465	I_{OL} = 1mA		–		0.4	V
V_{POH}	PCI output HIGH voltage	3.135 to 3.465	I_{OH} = –1mA		2.4		–	V
V_{POL}	PCI output LOW voltage	3.135 to 3.465	I_{OL}= 1mA		–		0.55	V
I_{OH}	CPUCLK output HIGH current	2.375	V_{OUT} = 1.0V		–27		–	mA
		2.625	V_{OUT} = 2.375V		–		–27	
I_{OH}	IOAPIC output HIGH current	2.375	V_{OUT} = 1.4V		–36		–	mA
		2.625	V_{OUT} = 2.5V		–		–21	
I_{OH}	48MHz, REF output HIGH current	3.135	V_{OUT} = 1.0V		–29		–	mA
		3.465	V_{OUT} = 3.135V		–		–23	
I_{OH}	PCI output HIGH current	3.135	V_{OUT} = 1.0V		–33		–	mA
		3.465	V_{OUT} = 3.135V		–		–33	
I_{OL}	CPUCLK output LOW current	2.375	V_{OUT} = 1.2V		27		–	mA
		2.625	V_{OUT} = 0.3V		–		30	
I_{OL}	IOAPIC output LOW current	2.375	V_{OUT} = 1.0V		36		–	mA
		2.625	V_{OUT} = 0.2V		–		31	
I_{OL}	48MHz, REF output LOW current	3.135	V_{OUT} = 1.95V		29		–	mA
		3.465	V_{OUT} = 0.4V		–		27	
I_{OL}	PCI output LOW current	3.135	V_{OUT} = 1.95V		30		–	mA
		3.465	V_{OUT} = 0.4V		–		38	
$\pm I_I$	Input leakage current	3.465			–		5	µA
$\pm I_{OZ}$	3-State output OFF-State current	3.465	V_{OUT} = V_{dd} or GND	I_O = 0	–		10	µA
Cin	Input pin capacitance						5	pF
Cxtal	Xtal pin capacitance, as seen by external crystal					18		pF
Cout	Output pin capacitance						6	pF
I_{dd3}	Operating supply current	3.465	66MHz mode	Outputs loaded[1]			170	mA
			100MHz mode	Outputs loaded[1]			170	mA
	Powerdown supply current		All static inputs to V_{DD} or GND				500	µA
I_{dd2}	Operating supply current	2.625	66MHz mode	Output loaded[1]			72	mA
			100MHz mode	Output loaded[1]			100	mA
	Powerdown supply current		All static inputs to V_{DD} or GND				100	µA

NOTE:
1. All clock outputs loaded with maximum lump capacitance test load specified in AC characteristics section.

AC CHARACTERISTICS

VDDREF = VDDPCI (0–1) = VDD48MHz = 3.3V ± 5%; VDDAPIC = VDDCPU (0–1) = 2.5V ± 5%; $f_{crystal}$ = 14.31818 MHz

CPU CLOCK OUTPUTS, CPU(0–3) (LUMP CAPACITANCE TEST LOAD = 20pF)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS T_{amb} = 0°C to +70°C		UNIT
			NOTES	MIN	MAX	
T_{HKP} (t_P)	CPUCLK period	66MHz	2	15.0	15.5	ns
T_{HKH} (t_H)	CPUCLK HIGH time		1, 5	5.2		
T_{HKL} (t_L)	CPUCLK LOW time		1, 5	5.0		
T_{HKP} (t_P)	CPUCLK period	100MHz	2	10.0	10.5	ns
T_{HKH} (t_H)	CPUCLK HIGH time		1, 5	3.0		
T_{HKL} (t_L)	CPUCLK LOW time		1, 5	2.8		
T_{HRISE} (t_R)	CPUCLK rise time		9	0.4	1.6	ns
T_{HFALL} (t_F)	CPUCLK fall time		9	0.4	1.6	ns
T_{JITTER} (t_{JC})	CPUCLK jitter				175	ps
DUTY CYCLE (t_D)	Output Duty Cycle		1	45	55	%
T_{HSKW} (t_{SK})	CPU Bus CLK skew		2		175	ps
T_{HSTB} (f_{ST})	CPUCLK stabilization from Power-up		7		3	ms

PCI CLOCK OUTPUTS, PCI(0–7) (LUMP CAPACITANCE TEST LOAD = 30pF)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS T_{amb} = 0°C to +70°C		UNIT
		NOTES	MIN	MAX	
T_{PKP} (t_P)	PCICLK period	3	30.0		ns
T_{PKPS}	PCICLK period stability	8		500	ps
T_{PKH} (t_H)	PCICLK HIGH time	1	12.0		ns
T_{PKL} (t_L)	PCICLK LOW time	1	12.0		ns
T_{HRISE} (t_R)	PCICLK rise time	10	0.5	2.0	ns
T_{HFALL} (t_F)	PCICLK fall time	10	0.5	2.0	ns
T_{PSKW} (t_{SK})	PCI Bus CLK skew	2		500	ps
$T_{HPOFFSET}$ (t_O)	CPUCLK to PCICLK Offset	2, 4	1.5	4.0	ns
T_{PSTB} (f_{ST})	PCICLK stabilization from Power-up	7		3	ms

APIC(0–1) CLOCK OUTPUT (LUMP CAPACITANCE TEST LOAD = 20pF)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS T_{amb} = 0°C to +70°C		UNIT
			NOTES	MIN	MAX	
f	Frequency, Actual	Frequency generated by Crystal		14.31818		MHz
T_{HRISE} (t_R)	Output rise edge rate			1	4	ns
T_{HFALL} (t_F)	Output fall edge rate			1	4	ns
DUTY CYCLE (t_D)	Duty Cycle			45	55	%
T_{HSTB} (f_{ST})	Frequency stabilization from Power-up (cold start)				3	ms

REF(0–2) CLOCK OUTPUT (LUMP CAPACITANCE TEST LOAD = 20pF)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS T_{amb} = 0°C to +70°C		UNIT
			NOTES	MIN	MAX	
f	Frequency, Actual	Frequency generated by Crystal		14.31818		MHz
T_{HRISE} (t_R)	Output rise edge rate			1	4	ns
T_{HFALL} (t_F)	Output fall edge rate			1	4	ns
DUTY CYCLE (t_D)	Duty Cycle			45	55	%
T_{HSTB} (f_{ST})	Frequency stabilization from Power-up (cold start)				3	ms

48MHZ(0–1) CLOCK OUTPUT (LUMP CAPACITANCE TEST LOAD = 20pF)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS T_{amb} = 0°C to +70°C		UNIT
			NOTES	MIN	MAX	
f	Frequency, Actual	Determined by PLL divider ratio		48.008		MHz
f_D	Devation from 48MHz	(48.008 – 48)/48		+167		ppm
T_{HRISE} (t_R)	Output rise edge rate			1	4	ns
T_{HFALL} (t_F)	Output fall edge rate			1	4	ns
DUTY CYCLE (t_D)	Duty Cycle			45	55	%
T_{HSTB} (f_{ST})	Frequency stabilization from Power-up (cold start)				3	ms

ALL CLOCK OUTPUTS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS T_{amb} = 0°C to +70°C		UNIT
			NOTES	MIN	MAX	
T_{PZL}, T_{PZH}	Output enable time			1.0	8.0	ns
T_{PLZ}, T_{PHZ}	Output disable time			1.0	8.0	ns

NOTES:
1. See Figure 3 for measure points.
2. Period, jitter, offset, and skew are measured on the rising edge @ 1.25V for 2.5V clocks and @ 1.5V for 3.3V clocks.
3. The PCICLK is the CPUCLK divided by two at CPUCLK = 66.6MHz. PCICLK is the CPUCLK divided by three at CPUCLK = 100MHz.
4. The CPUCLK must always lead the PCICLK as shown in Figure 2.
5. T_{HKH} is measured @ 2.0V as shown in Figure 4.
6. T_{HKL} is measured @ 0.4V as shown in Figure 4.
7. The time is specified from when V_{DDQ} achieves its nominal operating level (typical condition is V_{DDQ} = 3.3V) until the frequency output is stable and operating within specification.
8. Defined as once the clock is at its nominal operating frequency, the adjacent period changes cannot exceed the time specified.
9. T_{HRISE} and T_{HFALL} are measured as a transition through the threshold region V_{OL} = 0.4V and V_{OH} = 2.0V (1mA) JEDEC specification.
10. T_{HRISE} and T_{HFALL} (48MHz, REF, PC) are measured as a transition through the threshold region V_{OL} = 0.4V and V_{OH} = 2.4V

AC WAVEFORMS

V_M = 1.25V @ V_{DDQ2} and 1.5V @ V_{DDQ3}
$V_X = V_{OL} + 0.3V$
$V_Y = V_{OH} - 0.3V$
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

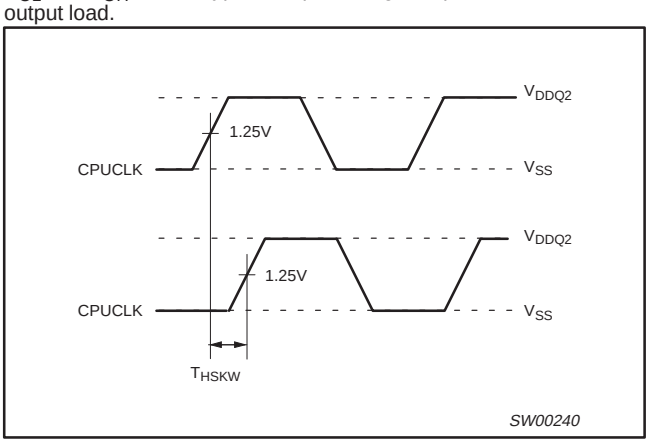


Figure 1. CPUCLK to CPUCLK skew

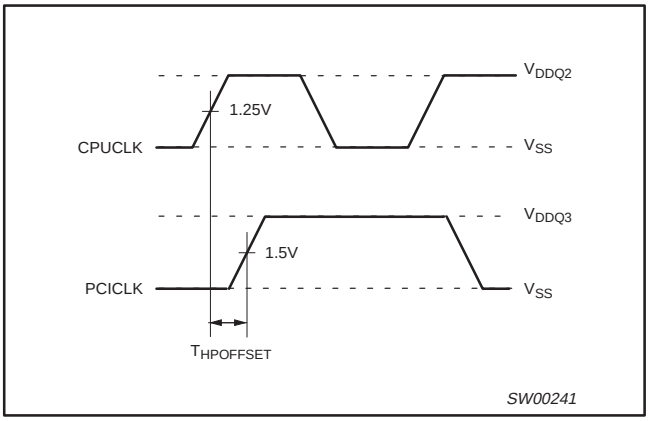


Figure 2. CPUCLK to PCICLK offset

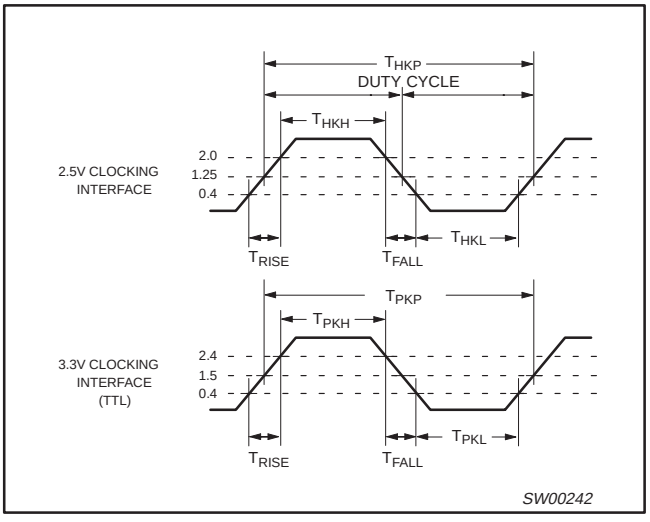


Figure 3. 2.5V/3.3V Clock waveforms

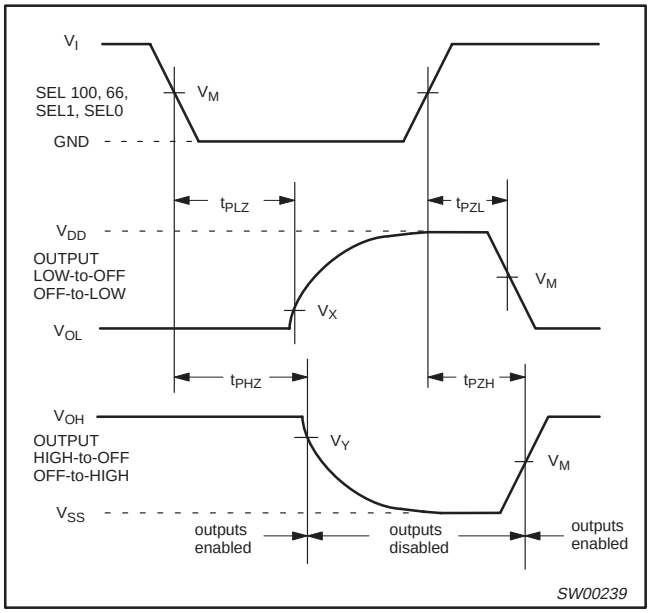


Figure 4. 3-State enable and disable times.

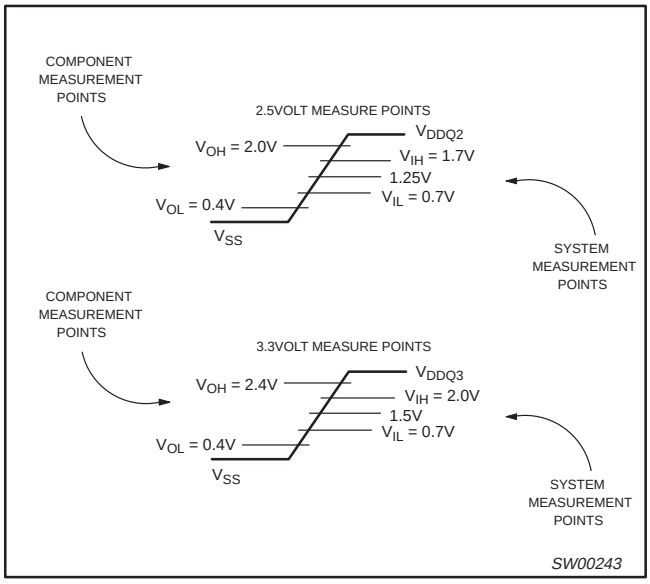


Figure 5. Component versus system measure points

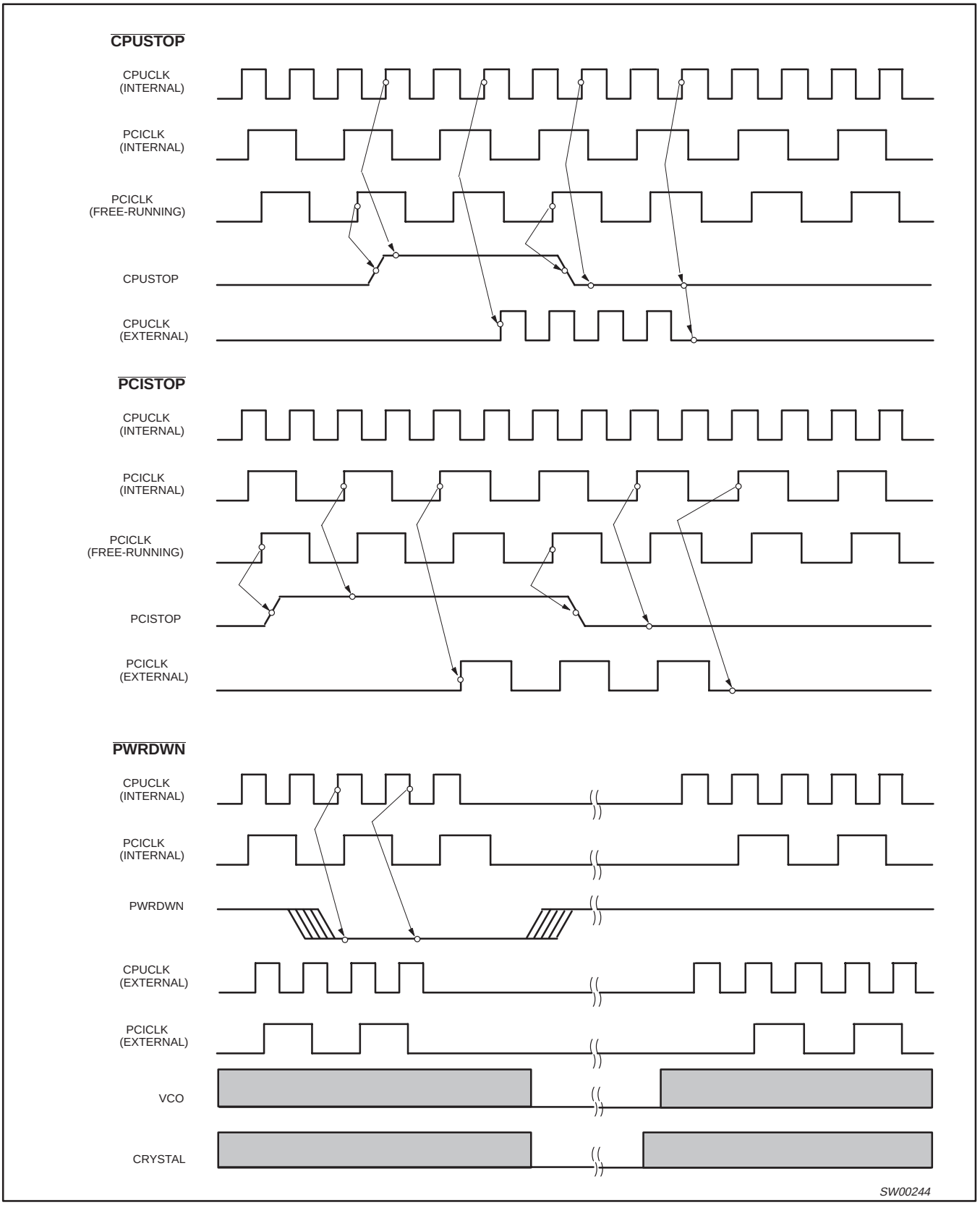
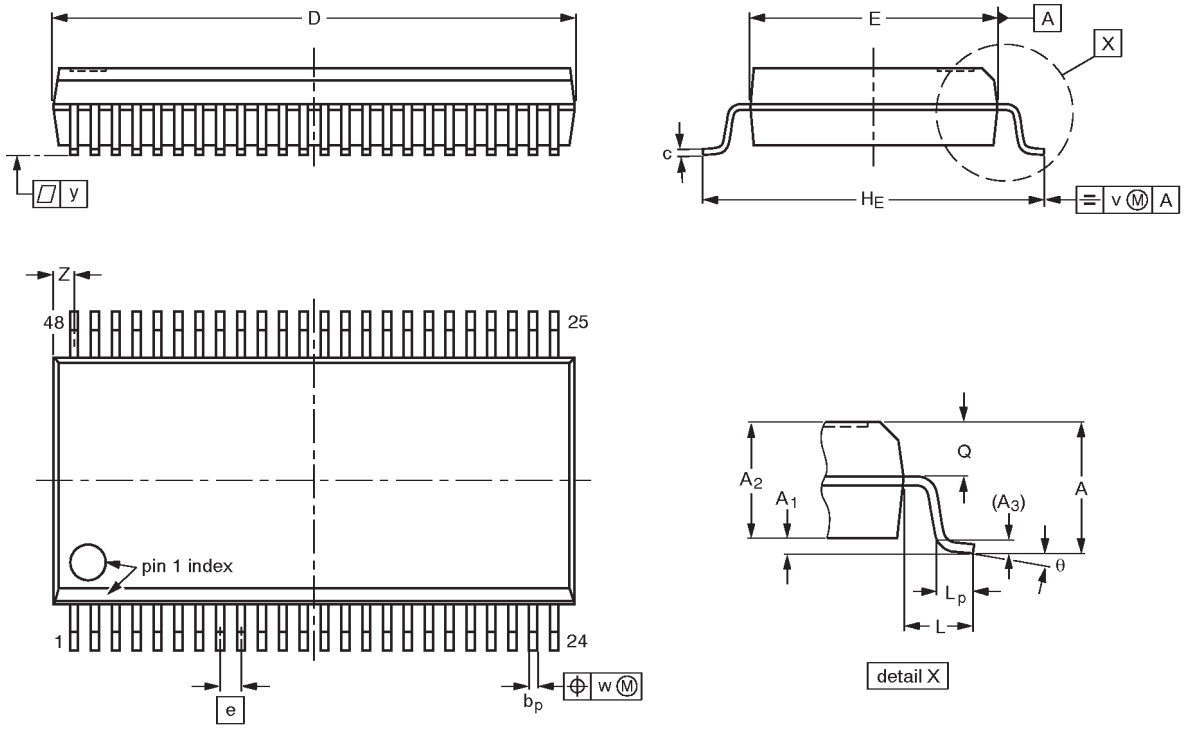
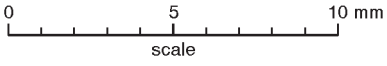


Figure 6. Power Management

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm **SOT370-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT370-1		MO-118AA				~~93-11-02~~ 95-02-04

NOTES

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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