DATA SHEET

NEC

TFT COLOR LCD MODULE
NL10276AC30-03

38 cm (15.0 inches), 1024 × 768 pixels, FULL-COLOR, MULTI-SCAN FUNCTION Wide viewing angle

DESCRIPTION

NL10276AC30-03 is a TFT(thin film transistor) active matrix color liquid crystal display (LCD) comprising amorphous silicon TFT attached to each signal electrode, a driving circuit and a backlight. NL10276AC30-03 has a built-in backlight with an inverter.

The 38cm (15.0 inches) diagonal display area contains 1024 × 768 pixels and can display full-color (more than 16 million colors simultaneously). Also, it has multi-scan function.

FEATURES

- High luminance
- Low reflection
- Wide viewing angle (with Retardation Film)
- Analog RGB signals
- Multi-scan function: e.g., XGA, SVGA, VGA, VGA-TEXT, PC-9801, MAC
- Incorporated edge type backlight (Two lamps, Inverter)
- Lamp holder replaceable (Part No. 150LHS03)

APPLICATIONS

- Desk-top type of PC
- Engineering work station

Regarding the use of OSD, please note that there is possibility of conflicts with a patent in Europe and the U.S. Thus, if such conflict might happen when you use OSD, we shall not be responsible for any trouble.

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STRUCTURE AND FUNCTIONS

A color TFT (thin film transistor) LCD module is comprised of a TFT liquid crystal panel structure, LSIs for driving the TFT array, and a backlight assembly. The TFT panel structure is created by sandwiching liquid crystal material in the narrow gap between a TFT array glass substrate and a color filter glass substrate. After the driver LSIs are connected to the panel, the backlight assembly is attached to the backside of the panel.

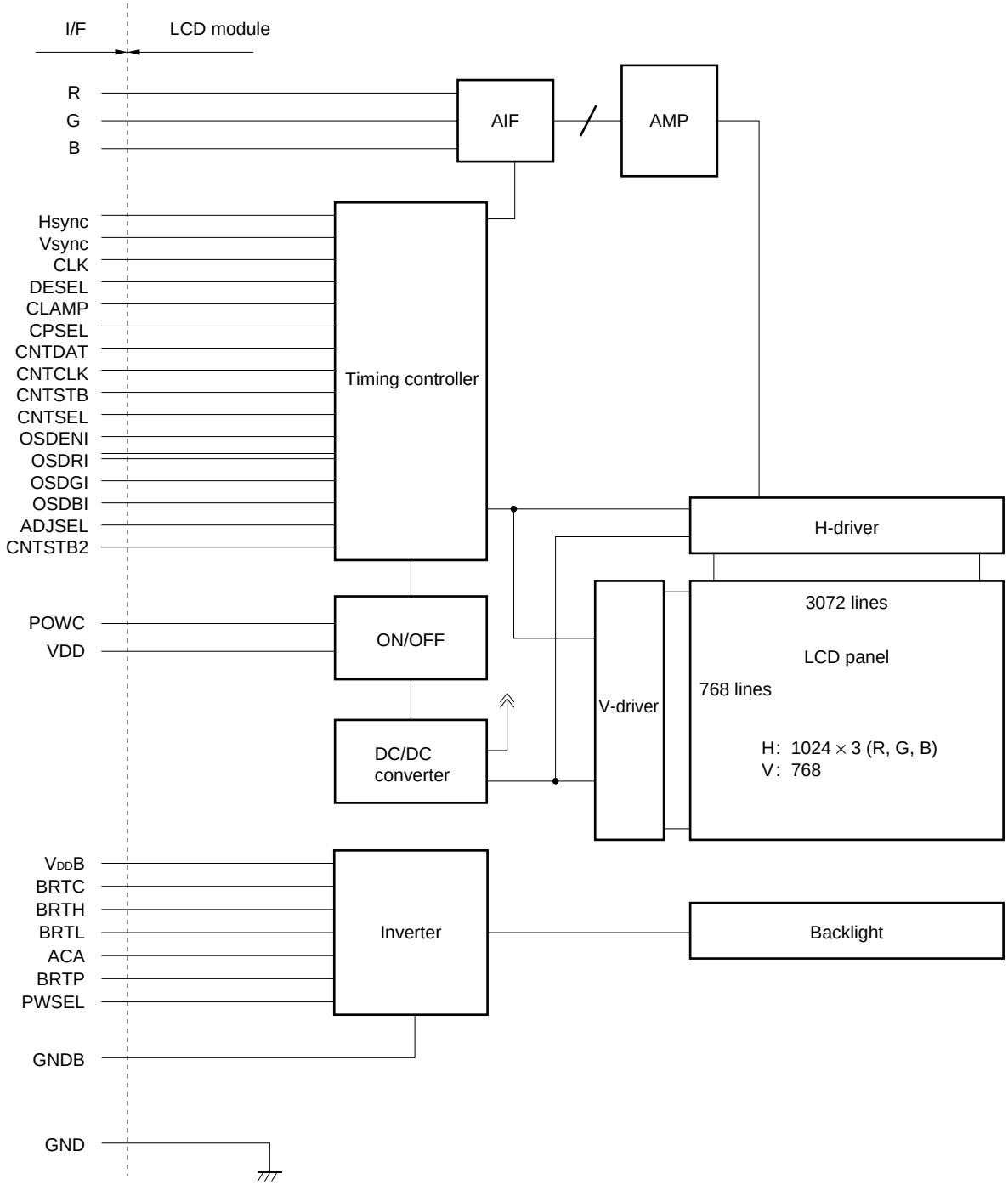
RGB (red, green, blue) data signals from a source system is modulated into a form suitable for active matrix addressing by the onboard signal processor and sent to the driver LSIs which in turn addresses the individual TFT cells.

Acting as an electro-optical switch, each TFT cell regulates light transmission from the backlight assembly when activated by the data source. By regulating the amount of light passing through the array of red, green, and blue dots, color images are created with clarity.

OUTLINE OF CHARACTERISTICS (at room temperature)

Display area	304.128 (H) × 228.096 (V) mm
Drive system	a-Si TFT active matrix.
Display colors	Full-color
Number of pixels	1024 × 768
Pixel arrangement	RGB vertical stripe
Pixel pitch	0.297 (H) × 0.297 (V) mm
Module size	350.0 (H) × 265.0 (V) × 20.0 (D) mm
Weight	1400 g (typ.)
Contrast ratio	200:1 (typ., perpendicular)
Viewing angle (more than the contrast ratio of 10:1)	
	• Horizontal : 55° (typ., left side, right side)
	• Vertical : 50° (typ., up side), 45° (typ, down side)
Designed viewing direction	
	• Wider viewing angle with contrast ratio : Down side (6 o'clock)
	• Wider viewing angle without image reversal : up side (12 o'clock)
	• Optimum grayscale (γ = 2.2) : perpendicular
Color gamut	42 % (typ., At center, To NTSC)
Response time	15 ms (typ.), "white" to "black"
Luminance	200 cd/m^2 (typ.)
Signal system	Analog RGB signals, Synchronous signals (Hsync and Vsync), CLK
Supply voltage	12 V, 12 V (Logic/LCD driving, Backlight)
Backlight	Edge light type: Two cold cathode fluorescent lamps with an inverter
	[Replaceable parts]
	• Lamp holder : 150LHS03
	• Inverter : 150PW031
Power consumption	15.6 W (typ.)

BLOCK DIAGRAM



Note Frame is not connected to GND and GNDB.

SPECIFICATIONS

GENERAL SPECIFICATIONS

Item	Contents	Unit
Module size	350.0 ± 0.6 (H) × 265.0 ± 0.6 (V) × 20.5 (max.) (D)	mm
Display area	304.128 (H) × 228.096 (V)	mm
Number of dots	1024 × 3 (H) × 768 (V)	dots
Pixel pitch	0.297 (H) × 0.297 (V)	mm
Dot pitch	0.099 (H) × 0.297 (V)	mm
Pixel arrangement	RGB (Red, Green, Blue) vertical stripe	–
Display colors	Full color	color
Weight	1500 (max.)	g

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Remarks
Supply voltage	V_{DD}	–0.3 to +14	V	Ta = 25°C
	V_{DD}B	–0.3 to +14	V	
Logic input voltage	Vin1	–0.3 to +5.5	V	Ta = 25°C V_{DD} = 12 V
R, G, B input voltage	Vin 2	–6.0 to +6.0	V	
CLK input voltage	Vin 3	–7.0 to +7.0	V	
BRTL input voltage	Vin 4	–0.3 to +1.5	V	
Storage temp.	Tst	–20 to + 60	°C	–
Operating temp.	Top	0 to +50	°C	Module surface **Note**
Humidity (no condensation)	≤ 95% relative humidity			Ta ≤ 40°C
	≤ 85% relative humidity			40 < Ta ≤ 50°C
	Absolute humidity shall not exceed Ta = 50°C, 85% relative humidity level.			Ta > 50°C

Note Measured at the display area

ELECTRICAL CHARACTERISTICS

(1) Logic, LCD driving, Backlight

(Ta = 25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage	V_{DD}	11.4	12.0	12.6	V	for Logic and LCD driving
	$V_{DD}B$	11.4	12.0	12.6	V	for backlight
Logic input “L” voltage 1	V_{IL1}	0	–	0.6	V	for BRTP
Logic input “H” voltage 1	V_{IH1}	4.5	–	5.25	V	
Logic input “L” voltage 2	V_{IL2}	0	–	0.8	V	Logic except BRTP
Logic input “H” voltage 2	V_{IH2}	2.2	–	5.25	V	
Input CLK voltage	V_{ICLK}	0.6	–	1.0	Vp-p	CLK
Input DC voltage level	V_{IDCCLK}	–4.5	–	+4.5	V	
Logic input “L” current 1	I_{IL1}	–10	–	–	μA	Hsync, Vsync
Logic input “H” current 1	I_{IH1}	–	–	160	μA	
Logic input “L” current 2	I_{IL2}	–1400	–	–	μA	CNTSEL, CPSEL, POWC, ADJSEL
Logic input “H” current 2	I_{IH2}	–	–	10	μA	
Logic input “L” current 3	I_{IL3}	–1.0	–	–	mA	BRTC, BRTL, ACA, PWSEL
Logic input “H” current 3	I_{IH3}	–	–	0.8	mA	
Logic input “L” current 4	I_{IL4}	–1.0	–	–	mA	BRTP
Logic input “H” current 4	I_{IH4}	–	–	10	mA	
Logic input “L” current 5	I_{IL5}	–10	–	–	μA	Logic except inputs above
Logic input “H” current 5	I_{IH5}	–	–	10	μA	
Supply current	I_{DD}	–	550	800	mA	V_{DD} = 12.0 V **Note**
	$I_{DD}B$	–	750	850	mA	$V_{DD}B$ = 12.0 V (Max. luminance)

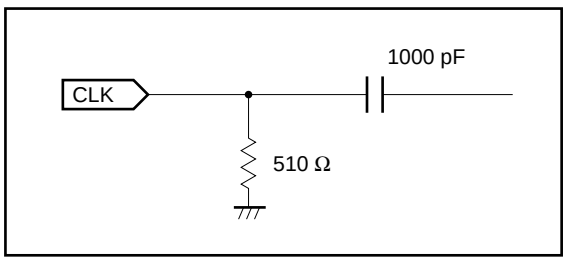
Note Pixel checkered pattern

(2) Video signal (R, G, B) input

(Ta = 25°C)

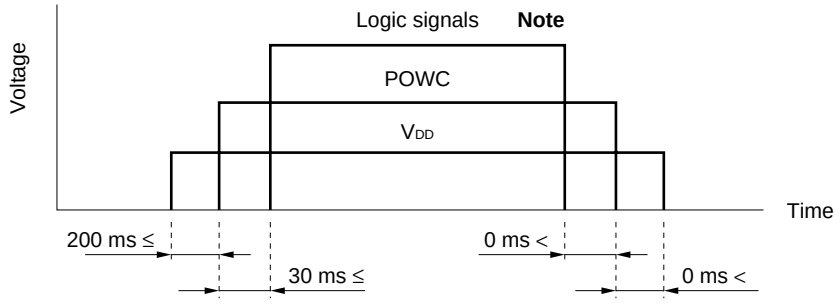
Item	Min.	Typ.	Max.	Unit	Remarks
Maximum amplitude (white - black)	0 (black)	0.7 (white)	0.9	Vp-p	Contrast adjustment is needed if the amplitude exceeds 0.7 Vp-p.
DC input level (black)	–3.5	–	+3.5	V	–

(3) CLK input equivalent circuit



SUPPLY VOLTAGE SEQUENCE

(1) Sequence of power supply



Note Synchronous signals, Control signals, CLK.

CAUTION
Wrong power sequence may cause damage to the module.

a) Logic signals (synchronous signals and control signals) should be “0” voltage (V), when V_{DD} is not input. If higher than 0.3 V is input to signal lines, the internal circuit will be damaged.

b) LCD module will shut down the power supply of driving voltage to LCD panel internally when one of CLK, Hsync, Vsync is not input more than 90 ms typically. As the display data are unstable in this period, the display is disordered. But the backlight works correctly even in this period. So the backlight ON/OFF should be controlled by BRTC signal.

c) The backlight ON/OFF (BRTC signal) should be controlled while logic signals are supplied. The backlight power supply (V_{DD}B) is not related to the power supply sequence. However, unstable data is displayed when the backlight power is turned ON without logic signals.

d) Keep POWC signal “L” more than 200 ms after the power supply (V_{DD}B) is input, if POWC signal is controlled.

e) Analog RGB input are independent of this power supply sequence.

f) 12 V for backlight should be started up within 80 ms, otherwise the protection circuit makes the backlight turn off.

(2) Ripple of supply voltage

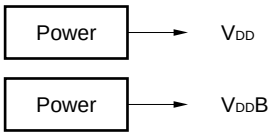
Please note that the ripple at the input connector of the module should be within the values shown in this table. If the ripple is beyond these values, the noise may appear on the screen.

	V_{DD} (for logic and LCD driver)	$V_{DD}B$ (for backlight)
Acceptable range	≤ 100 mVp-p	≤ 200 mVp-p

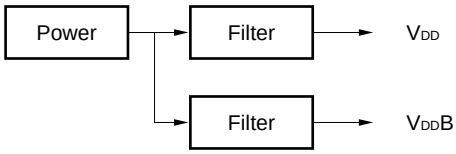
Note The acceptable range of ripple voltage includes spike noise.

Examples of the power supply connection

a) Separate the power supply

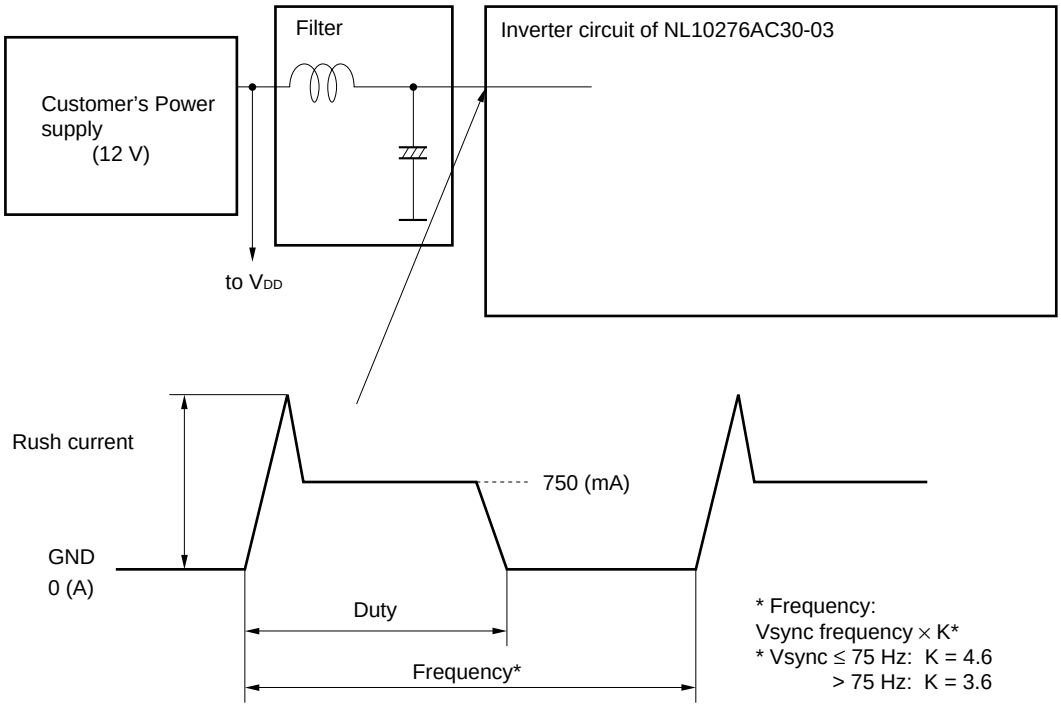


b) Put the filter



(3) Inverter current wave

In the luminance control mode, the rush current below flows into the inverter of the module. The duty cycle varies from 100% through 20% depending on the luminance control level. This might cause the noise on the screen. Please evaluate the appropriate value of the capacitor in the filter to eliminate the noise.



INTERFACE PIN CONNECTION

(1) CN1

Part No. : MRF03-6R-SMT

Adaptable socket: MRF03-6PR-SMT (board-to-board type)

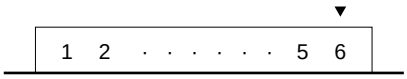
MRF-03-6P-0.8D (cable type)

MRF-03-6P-1.27 (cable type)

Supplier : HIROSE ELECTRIC CO., LTD.

Pin No.	Symbol	Pin No.	Symbol
1	B	4	Vsync
2	G	5	Hsync
3	R	6▼	CLK

Figure from socket view



(2) CN3

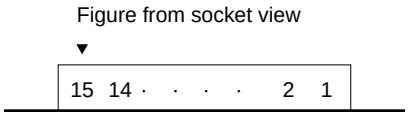
Part No. : IL-Z-15PL-SMTY

Adaptable socket: IL-Z-15S-S125C3

Supplier : Japan Aviation Electronics Industry Limited (JAE)

Pin No.	Symbol	Pin No.	Symbol
1	V_{DD}	9	GND
2	V_{DD}	10	CNTCLK
3	GND	11	CPSEL
4	GND	12	CLAMP
5	POWC	13	GND
6	CNTSEL	14	N.C.
7	CNTDAT	15▼	GND
8	CNTSTB		

Figure from socket view



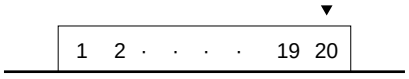
Note N.C. (No connection) should be open.

(3) CN3

Part No. : DF14A-20P-1.25H
Adaptable socket: DF14-20S-1.25C
Supplier : HIROSE ELECTRIC CO., LTD

Pin No.	Symbol	Pin No.	Symbol
1	GND	11	ADJSEL
2	OSDENI	12	N.C.
3	GND	13	CNTSTB2
4	OSDBI	14	GND
5	GND	15	N.C.
6	OSDGI	16	GND
7	GND	17	N.C.
8	OSDRI	18	N.C.
9	GND	19	N.C.
10	N.C.	20▼	N.C.

Figure from socket view



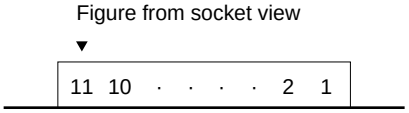
Note N.C. (No connection) should be open.

(4) CN201

Part No. : IL-Z-11PLI-SMTY
Adaptable socket: IL-Z-11S-S125C3
Supplier : Japan Aviation Electronics Industry Limited (JAE)

Pin No.	Symbol	Pin No.	Symbol
1	V_{DD}B	7	ACA
2	V_{DD}B	8	BRTC
3	V_{DD}B	9	BRTH
4	GNDB	10	BRTL
5	GNDB	11▼	N.C.
6	GNDB		

Figure from socket view

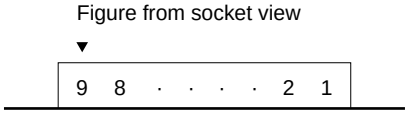


(5) CN202

Part No. : IL-Z-9PL1-SMTY
Adaptable socket: IL-Z-9S-S125C3
Supplier : Japan Aviation Electronics Industry Limited (JAE)

Pin No.	Symbol	Pin No.	Symbol
1	GNDB	6	BRTL
2	GNDB	7	BRTP
3	ACA	8	GNDB
4	BRTC	9▼	PWSEL
5	BRTH		

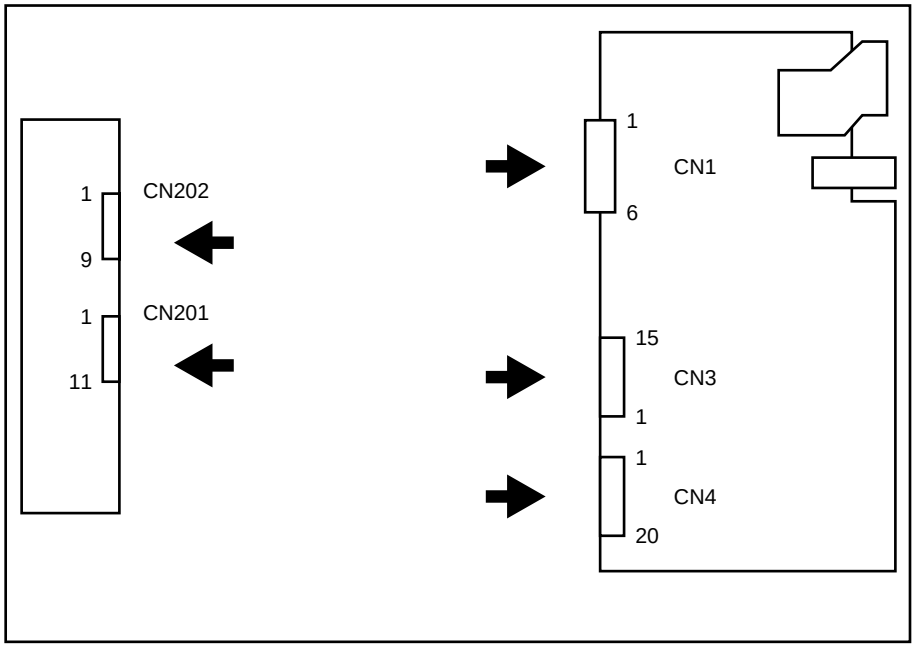
Figure from socket view



Note N.C. (No connection) should be open.

Caution For CN201 and CN202, pins with an identical symbol are connected inside the module. Do not use both of these pins at the same time.

<Rear view>



PIN FUNCTION

(1/2)

Symbol	I/O	Logic	Description
CLK	Input	Positive	Dot clock input. (ECL level) This timing-signal is for display data.
Hsync	Input	Negative	Horizontal synchronous signal input (TTL level)
Vsync	Input	Negative	Vertical synchronous signal input (TTL level)
R	Input	–	Red video signal input (0.7 Vp-p, 75 Ω)
G	Input	–	Green video signal input (0.7 Vp-p, 75 Ω)
B	Input	–	Blue video signal input (0.7 Vp-p, 75 Ω)
POWC	Input	Positive	Power control signal (TTL level) "H" or "Open": Logic and LCD power are on. "L" : Logic and LCD power are off. When POWC is "L", serial communication data is cleared. Please set again.
CNTSEL	Input	–	Display control signal in case of serial communications. (TTL level) "H" or "Open" : Default , "L" : External control External control is set up by serial communication.
CNTDAT	Input	Positive	Display control data (TTL level) Detail of CNTDAT is mentioned in **FUNCTIONS.**
CNTCLK	Input	Positive	CLK for display control data (TTL level) Detail of CNTCLK is mentioned in **FUNCTIONS.**
CNTSTB	Input	Positive	Latch pulse for display control data (TTL level) Detail of CNTSTB is mentioned in **FUNCTIONS.**
CPSEL	Input	–	CLAMP function select signal "H" or "Open": Default , "L" : External control
CLAMP	Input	Negative	Clamp timing signal of black level (TTL level) This mode works when CPSEL = "L".
ADJSEL	Input	Positive	Contrast, brightness select control signal (TTL level) "H" or "Open": Default , "L" : External control
CNTSTB2	Input	Positive	Latch pulse2 for display control data Detail of CNTSTB2 is mentioned in **FUNCTIONS**
OSDRI	Input	–	Input OSD-R data Detail is mentioned in **OSD FUNCTIONS**
OSDGI	Input	–	Input OSD-G data Detail is mentioned in **OSD FUNCTIONS**
OSDBI	Input	–	Input OSD-B data Detail is mentioned in **OSD FUNCTIONS**
OSDENI	Input	Positive	Enable signal for OSD Detail is mentioned in **OSD FUNCTIONS**

(2/2)

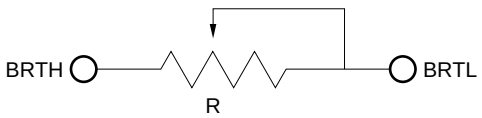
Symbol	I/O	Logic	Description
ACA	Input	Positive	Luminance control signal (TTL level) "H" or "Open": Normal luminance "L" : Low luminance (1/2 of normal luminance)
BRTC	Input	Positive	Backlight ON/OFF control signal (TTL level) "H" or "Open": Backlight ON, "L" : Backlight OFF
BRTH	Input	–	Variable resistor control of Voltage control See [Function select] for detail.
BRTL			
BRTP	Input	–	Luminance control signal
PWSEL	Input	Positive	Select the control of luminance (TTL level) See [Function select] for detail.
V_{DD}	–	–	Power supply for Logic and LCD driving +12 V (±5 %)
V_{DD}B	–	–	Power supply for backlight. +12 V (±5 %)
GND	–	–	Signal ground for Logic and LCD driving (Connect to system ground)
GNDB	–	–	Ground for backlight, GNDB is not connected to the frame ground of LCD module.

Note Frame ground, system ground (GND) and backlight ground (GNDB) are not connected in the module.

[Function select]

BRTP	PWSEL	How to adjust	
Valid	"L"	Luminance can be controlled by BRTP signal. See **OUTSIDE CONTROL FOR LUMINANCE** for more detail.	
Open	"H" or "Open"	Volume	Please connect BRTP and BRTL. **Note**
		Voltage	Fix BRTH to "0 V" and input proper voltage to BRTL. 1 V: maximum luminance (100%) 0 V: minimum luminance (20%)

Note The variable resistor for luminance control should be 10 kΩ type, and zero point of the resistor correspond to the minimum of luminance.



Mating variable resistor:
10 KΩ ± 5 %, B curve

Maximum luminance (100 %): R = 10 KΩ
Minimum luminance (20 %) : R = 0 Ω

FUNCTIONS

This LCD module has following functions controled by serial data input (table 1)

(1) Control Display position (VERTICAL) : See table 3
(2) Control Display position (HORIZONTAL) : See table 6
(3) Control CLK delay : See table 4
(4) Change CLK fall/rise synchronous : See table 5
(5) Contrast control :
(6) Sub-Contrast control :
(7) Sub-Brightness control :

} See table 9, 10 and **COLOR CONTROL FUNCTION AND GRAPH IMAGE**

Set up the following items to work the functions above

(A) Expansion mode : See table 2 and **EXPANSION FUNCTION**
(B) CLK counts of horizontal period : See table 7
(C) CLK frequency range : See table 8

HOW TO USE THE FUNCTIONS ABOVE

When CNTSEL is “L”, the functions ((1)-(4), (A)-(C)) above are valid. (When CNTSEL is “H” or open, default values are valid.) After serial data are transferred, they are latched by CNTSTB. Once the data is latched, the functions (1)-(4), (A)-(C) are effective.

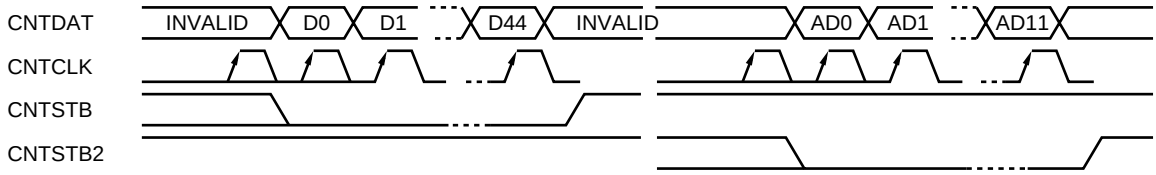
When ADJSEL is “L”, functions (5)-(7) are valid. (When ADJSEL is “H” or open, default values are valid.)

After serial data are transferred, they are latched by CNTSTB2. Once the data is latched, the functions (5)-(7) are effective.

Keep CNTSTB/CNTSTB2 “L” while transferring data.

Changing data is allowed when power is on. But display may be disturbed while changing. Turning off backlight using BRTC function is recommended in this period.

SERIAL COMMUNICATION TIMING AND WAVEFORM



Parameter	Symbol	Min.	Max.	Unit	Remark
CLK pulse-width	Twck	50	–	ns	CNTCLK
CLK frequency	Fclk	–	5	MHz	
DATA set-up-time	Tdst	50	–	ns	CNTDAT
DATA hold-time	Tdhl	50	–	ns	
Latch pulse-width	Twlp	50	–	ns	CNTSTB, CNTSTB2
Latch set-up-time	Tlst	50	–	ns	
Rise / fall time	Tr, Tf	–	50	ns	CNTXXX

SERIAL COMMUNICATION WAVEFORM

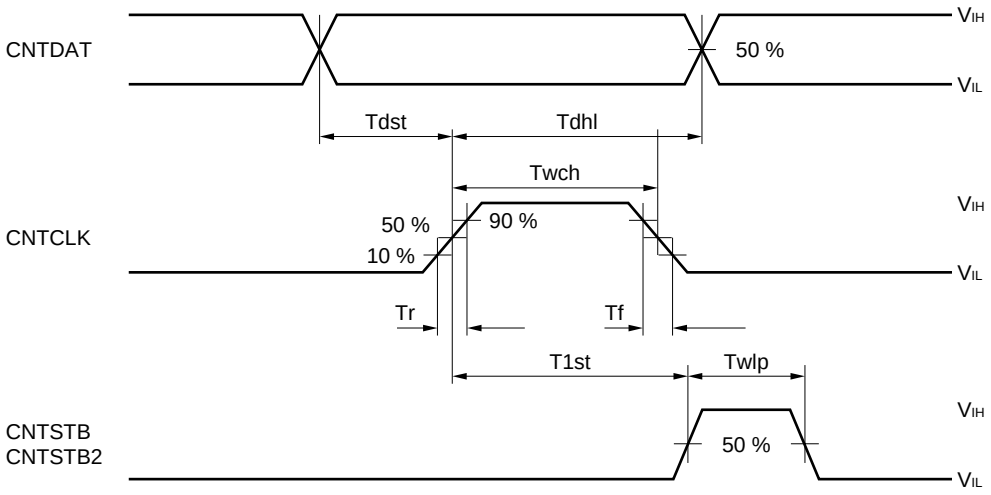


Table 1. CNTDAT Composition (1/2)

DATA	DATA name	Function	
D0	VEX3	Expansion mode	See table 2
D1	VEX2	Expansion mode	
D2	VEX1	Expansion mode	
D3	VEX0	Expansion mode	
D4	VD10	Vertical display position (MSB)	See table 3
D5	VD9	Vertical display position	
D6	VD8	Vertical display position	
D7	VD7	Vertical display position	
D8	VD6	Vertical display position	
D9	VD5	Vertical display position	
D10	VD4	Vertical display position	
D11	VD3	Vertical display position	
D12	VD2	Vertical display position	
D13	VD1	Vertical display position	
D14	VD0	Vertical display position (LSB)	
D15	DELAY6	CLK delay (MSB)	See table 4
D16	DELAY5	CLK delay	
D17	DELAY4	CLK delay	
D18	DELAY3	CLK delay	
D19	DELAY2	CLK delay	
D20	DELAY1	CLK delay	
D21	DELAY0	CLK delay (LSB)	
D22	CKS	CLK reverse signal	See table 5
D23	HD8	Horizontal display position (MSB)	See table 6
D24	HD7	Horizontal display position	
D25	HD6	Horizontal display position	
D26	HD5	Horizontal display position	
D27	HD4	Horizontal display position	
D28	HD3	Horizontal display position	
D29	HD2	Horizontal display position	
D30	HD1	Horizontal display position	
D31	HD0	Horizontal display position (LSB)	
D32	HSE10	CLK count of horizontal period (MSB)	See table 7
D33	HSE9	CLK count of horizontal period	
D34	HSE8	CLK count of horizontal period	
D35	HSE7	CLK count of horizontal period	
D36	HSE6	CLK count of horizontal period	
D37	HSE5	CLK count of horizontal period	
D38	HSE4	CLK count of horizontal period	
D39	HSE3	CLK count of horizontal period	

Table 1. CNTDAT Composition (continuation) (2/2)

DATA	DATA name	Function	
D40	HSE2	CLK count of horizontal period	See table 7
D41	HSE1	CLK count of horizontal period	
D42	HSE0	CLK count of horizontal period (LSB)	
D43	MOD1	CLK frequency select	See table 8
D44	MOD0	CLK frequency select	
AD11	DAA0	Color adjust select data (LSB)	See table 10
AD10	DAA1	Color adjust select data	
AD9	DAA2	Color adjust select data	
AD8	DAA3	Color adjust select data (MSB)	
AD7	DAD7	Color adjust data (MSB)	See table 9
AD6	DAD6	Color adjust data	
AD5	DAD5	Color adjust data	
AD4	DAD4	Color adjust data	
AD3	DAD3	Color adjust data	
AD2	DAD2	Color adjust data	
AD1	DAD1	Color adjust data	
AD0	DAD0	Color adjust data (LSB)	

Table 2. Display Mode (VEX3 to VEX0: 4 bit)

VEX3	VEX2	VEX1	VEX0	Vertical magnification	Display mode	Display image
0	0	0	0	1	XGA	Standard **Note**
0	0	0	1	1.25	SVGA	
0	0	1	0	1.6	PC98, VGA, TEXT	
0	0	1	1	–	Prohibit	
0	1	0	0	–	Prohibit	
0	1	0	1	–	Prohibit	
0	1	1	0	–	Prohibit	
0	1	1	1	–	Prohibit	
1	0	0	0	–	Prohibit	See **DISPLAY IMAGE**
1	0	0	1	1.2	832 × 624 (MAC)	
1	0	1	0	–	Prohibit	
1	0	1	1	–	Prohibit	
1	1	0	0	–	Prohibit	
1	1	0	1	–	Prohibit	
1	1	1	0	–	Prohibit	
1	1	1	1	–	Prohibit	

Note When CNTSEL is “H” or “Open”, display mode is fixed to XGA.

Table 3. Vertical Position (VD10 to VD0: 11 bit)

VD10	VD9	VD8	VD7	VD6	VD5	VD4	VD3	VD2	VD1	VD0	Vertical position [H] **Note 1**
0	0	0	0	0	0	0	0	0	0	0	Prohibit
0	0	0	0	0	0	0	0	0	0	1	Prohibit
0	0	0	0	0	0	0	0	0	1	0	Prohibit
0	0	0	0	0	0	0	0	0	1	1	Prohibit
0	0	0	0	0	0	0	0	1	0	0	4
0	0	0	0	0	0	0	0	1	0	1	5
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	1	1	0	1	2045
1	1	1	1	1	1	1	1	1	1	0	2046
1	1	1	1	1	1	1	1	1	1	1	2047 **Note 2**

Notes 1. Horizontal line number for effective VIDEO signal from Vsync-fall is shown in this column.

2. The maximum vertical position is Vsync total.

3. When CNTSEL is “H” or “Open”, vertical position is fixed to 35 [H].

Table 4. CLK Delay (DELAY6 to DELAY0: 7 bit)

DELAY [6..0]	Delay	Unit
00H	9.5	ns
01H	9.8	ns
02H	10.0	ns
03H	10.3	ns
04H	10.5	ns
05H	10.8	ns
06H	11.0	ns
07H	11.3	ns
08H	11.5	ns
09H	11.8	ns
0AH	12.1	ns
0BH	12.3	ns
0CH	12.5	ns
0DH	12.8	ns
0EH	13.1	ns
0FH	13.3	ns
10H	13.6	ns
11H	13.8	ns
12H	14.1	ns
13H	14.4	ns
14H	14.6	ns
15H	14.9	ns
16H	15.1	ns
17H	15.4	ns
18H	15.7	ns
19H	16.0	ns
1AH	16.2	ns
1BH	16.5	ns
1CH	16.7	ns
1DH	17.0	ns
1EH	17.2	ns
1FH	17.5	ns
20H	17.7	ns
21H	18.0	ns
22H	18.3	ns
23H	18.5	ns
24H	18.8	ns
25H	19.0	ns
26H	19.3	ns
27H	19.6	ns
28H	19.9	ns
29H	20.2	ns
2AH	20.4	ns

DELAY [6..0]	Delay	Unit
2BH	20.7	ns
2CH	20.9	ns
2DH	21.2	ns
2EH	21.4	ns
2FH	21.7	ns
30H	22.0	ns
31H	22.2	ns
32H	22.58	ns
33H	22.8	ns
34H	23.0	ns
35H	23.3	ns
36H	23.5	ns
37H	23.8	ns
38H	24.1	ns
39H	24.3	ns
3AH	24.6	ns
3BH	24.9	ns
3CH	25.1	ns
3DH	25.4	ns
3EH	25.6	ns
3FH	25.9	ns
40H	26.2	ns
41H	26.5	ns
42H	26.7	ns
43H	27.0	ns
44H	27.2	ns
45H	27.5	ns
46H	27.7	ns
47H	28.0	ns
48H	28.3	ns
49H	28.6	ns
4AH	28.9	ns
4BH	29.1	ns
4CH	29.4	ns
4DH	29.6	ns
4EH	29.9	ns
4FH	30.1	ns
50H	30.4	ns
51H	30.7	ns
52H	31.0	ns
53H	31.2	ns
54H	31.4	ns
55H	31.7	ns

DELAY [6..0]	Delay	Unit
56H	32.0	ns
57H	32.2	ns
58H	32.6	ns
59H	32.9	ns
5AH	33.1	ns
5BH	33.4	ns
5CH	33.6	ns
5DH	33.8	ns
5EH	34.1	ns
5FH	34.4	ns
60H	34.7	ns
61H	34.9	ns
62H	35.2	ns
63H	35.4	ns
64H	35.7	ns
65H	36.0	ns
66H	36.2	ns
67H	36.4	ns
68H	36.7	ns
69H	37.0	ns
6AH	37.3	ns
6BH	37.5	ns
6CH	37.7	ns
6DH	38.0	ns
6EH	38.2	ns
6FH	38.5	ns
70H	38.7	ns
71H	39.0	ns
72H	39.3	ns
73H	39.5	ns
74H	39.7	ns
75H	40.0	ns
76H	40.3	ns
77H	40.5	ns
78H	40.8	ns
79H	41.1	ns
7AH	41.4	ns
7BH	41.6	ns
7CH	41.9	ns
7DH	42.1	ns
7EH	42.4	ns
7FH	42.6	ns

Notes 1, When CNTSEL is “H” or “Open”, DELAY[6..0] is fixed to 00H.

2. These values are typical at Ta = 25°C. Changing ambient temperature or power supply change the delay.

Please set up a preferable display position. See the following references.

<1> Variation of CLK delay by temperature drift (for reference). The temperature constant of CLK delay is 0.2 %/°C.

Calculated example:

In case of delay time is 20 ns at Ta = 25°C;

(a) In case Ta rising to 50°C.

Increase of delay time → (50°C – 25°C) × 0.002 × 20 ns = +1 ns

So, the total delay time is 21 ns at Ta = 50°C.

(b) In case Ta falling to 0°C.

Decrease of delay time → (0°C – 25°C) × 0.002 × 20 ns = –1 ns

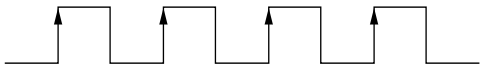
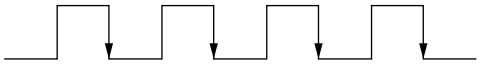
So, the total delay time is 19 ns at Ta = 0°C.

<2> Variation of CLK delay time between each LCD module (for reference).

–10.5 % to +14.4 %

	MOD setting			
	0,0	0,1	1,0	1,1
The upper limit of CLK delay: DELAY [6..0]	Prohibit	59H	6BH	7FH

Table 5. CLK Reverse Signal

CKS	Function
0	DATA are sampled on rising edge of CLK 
1	DATA are sampled on falling edge of CLK 

Note When CNTSEL is “H” or “Open”, CKS is assumed to be “0”.

Table 6. Display Horizontal Position (HD8 to HD0: 9 bits)

HD8	HD7	HD6	HD5	HD4	HD3	HD2	HD1	HD0	Horizontal position [CLK] **Note 1**
0	0	0	0	0	0	0	0	0	Prohibit
0	0	0	0	0	0	0	0	1	Prohibit
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
0	0	0	1	1	1	1	1	1	Prohibit
0	0	1	0	0	0	0	0	0	64
0	0	1	0	0	0	0	0	1	65
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	0	1	509
1	1	1	1	1	1	1	1	0	510
1	1	1	1	1	1	1	1	1	511

Notes 1. Number of CLKs from Hsync-fall to effective VIDEO signal is shown here.

2. When CNTSEL is “H” or “Open”, Horizontal position is set to 296 [CLK].

Table 7. CLK Count of Horizontal Period (HSE10 to HSE0: 11 bit)

HSE10	HSE 9	HSE 8	HSE 7	HSE 6	HSE 5	HSE 4	HSE 3	HSE 2	HSE 1	HSE 0	CLK count **Note 1**
0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	1	1
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	1	1	0	1	2045
1	1	1	1	1	1	1	1	1	1	0	2046
1	1	1	1	1	1	1	1	1	1	1	2047

Notes 1. Number of CLKs from Hsync to next Hsync.

2. When CNTSEL is “H” or “Open”, CLK count is set to 1344 [CLK].

3. Selected CLK count must be identical with that of input signal.

Table 8. CLK Frequency Select (MOD1 to MOD0: 2 bit)

MOD1	MOD0	CLK frequency [MHz]
0	0	Prohibit
0	1	65 to 80
1	0	50 to 65
1	1	20 to 50

Notes 1. Set up MOD1 and MOD0 complying with input CLK frequency.

2. When CNTSEL is “H” or “Open”, CLK frequency is set to 65 - 80 MHz.

Table 9. Color Control Data (DAD7 to DAD0: 8 bit)

DAD7	DAD6	DAD5	DAD4	DAD3	DAD2	DAD1	DAD0	D/A **Note 1**
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
0	1	1	1	1	1	1	1	127
1	0	0	0	0	0	0	0	128
1	0	0	0	0	0	0	1	129
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	0	1	253
1	1	1	1	1	1	1	0	254
1	1	1	1	1	1	1	1	255

Notes 1. Value for the function selected according to table 10.

2. Valid range of D/A depends on the selected function.

3. See **Color control function and graph image** for more detail.

Table 10. Color Adjust Select Data (DAA3 to DAA0: 4 bit)

DAA3	DAA2	DAA1	DAD0	Function
0	0	0	0	Prohibit
0	0	0	1	Main contrast
0	0	1	0	Prohibit
0	0	1	1	Prohibit
0	1	0	0	Sub-contrast R
0	1	0	1	Sub-contrast G
0	1	1	0	Sub-contrast B
0	1	1	1	Sub-brightness R
1	0	0	0	Sub-brightness G
1	0	0	1	Sub-brightness B
1	0	1	0	Prohibit
1	0	1	1	Prohibit
1	1	0	0	Prohibit
1	1	0	1	Prohibit
1	1	1	0	Prohibit
1	1	1	1	Prohibit

Note See more detail **Color control function and graph image**.

EXPANSION FUNCTION

HOW TO USE EXPANSION MODE

Expansion mode is a function to expand screen. For example, VGA signal has 640 × 480 pixels. But, if the display data can expanded to 1.6 times vertically and horizontally, VGA screen image can be displayed fully on the screen of XGA resolution.

This LCD module has the function of expanding vertical direction as shown in Table 1. And expanding horizontal direction is possible by setting input CLK frequency which is equivalent to the magnification. It is necessary to make this CLK outside of this LCD module.

The below image is display example, HD and VD is set to most suitable frequency.

Please adopt this mode after evaluating display quality, because the appearance of expansion mode is happened to become bad some cases.

The followings show display magnifications for each mode.

Input display	Number of pixels	Magnification		
		Vertical	Horizontal	**Note**
XGA	1024 × 768	1	1	
SVGA	800 × 600	1.25	1.25	
VGA	640 × 480	1.6	1.6	
VGA text	720 × 400	1.6	1.4	
PC9801	640 × 400	1.6	1.6	
MAC	832 × 624	1.2	1.2	

Note The horizontal magnification multiples the input clock (CLK).
Input CLK = system CLK × horizontal magnification

Example In case of XGA and VGA, CLK frequency can be decided as follows.
XGA: (system CLK (65 MHz)) × 1.0 = 65 MHz
VGA: (system CLK (25.175 MHz)) × 1.6 = 40.28 MHz

SETTING SERIAL DATA

Input signal								Module serial data setting		
Mode	System CLK [MHz]	Hsync [kHz]	Vsync [Hz]	Horizontal		Vertical		HSE	HD	VD
				Count Number [CLK]	DSP* **Note 1** [CLK]	Count Number [H]	DSP* **Note 1** [H]	Calculation formula		
				(A)	(B)	–	(C)	(A) × Ver.mag.	(B) × Hor.mag.	= (C)
XGA (1024 × 768)	65 75 78.75	48.363 56.476 60.023	60.004 70.069 75.029	1344 1328 1312	296 280 272	806 806 800	35 35 31	(A) × 1	(B) × 1	= (C)
MAC (832 × 624)	57.283	49.725	74.5	1152	288	667	42	(A) × 1.2	(B) × 1.2	
SVGA (800 × 600)	36* 40* 50* 49.5*	35.156 37.879 48.077 46.875	56.25 60.317 72.188 75	1024 1056 1040 1056	200 216 184 240	625 628 666 666	24 27 29 24	(A) × 1.25	(B) × 1.25	
VGA (640 × 480)	25.175* 31.5* 31.5* 30.24*	31.469 37.861 37.5 35.0	59.94 72.809 75 66.667	800 832 840 864	144 168 184 160	525 520 500 525	35 31 19 42	(A) × 1.6	(B) × 1.6	
VGA text (720 × 400)	28.322* 31.5*	31.469 37.927	70.087 85.039	900 936	153 180	449 446	37 45	(A) × 1.4	(B) × 1.4	
PC9801 (640 × 400)	21.053*	24.827	56.432	848	144	440	33	(A) × 1.6	(A) × 1.6	443

Notes 1. DSP = Display Start Period. DSP is total of “pulse-width” and “back-porch”.

2. HD and VD are approximate value. Set HD and VD in case of adjusting display to the screen center.

3. The pulse-width of Hsync, Vsync and back-porch are the same as XGA-mode. (Standard-mode).

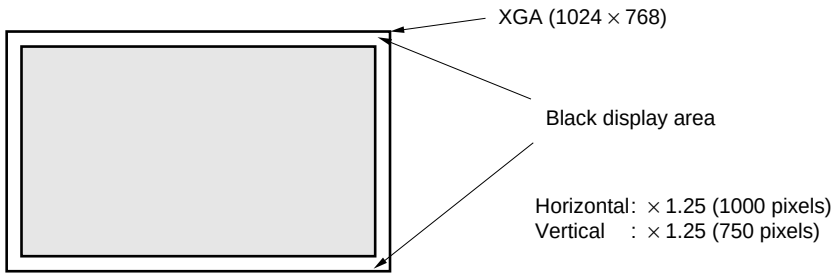
4. HSE see CLK number of table 7.

5. HD see horizontal position of table 6.

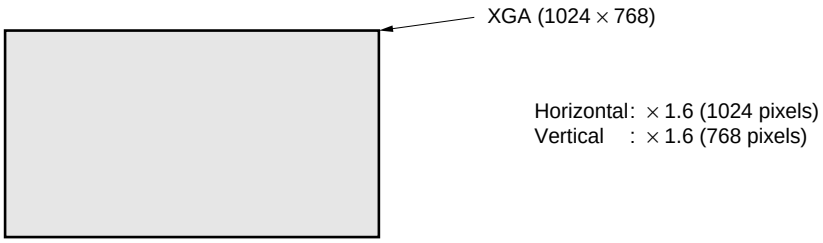
6. VD see vertical position of table 3.

DISPLAY IMAGE

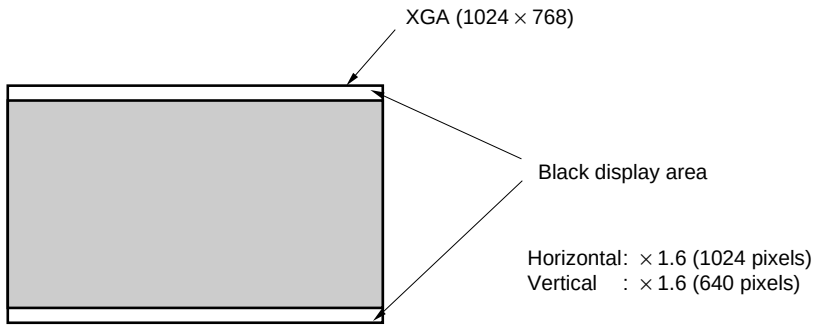
1) SVGA mode (800 × 600)



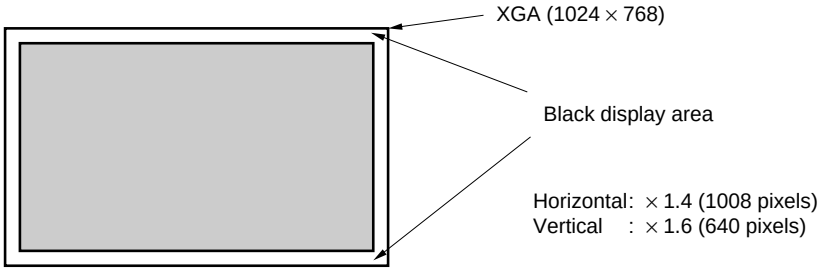
2) VGA mode (640 × 480)



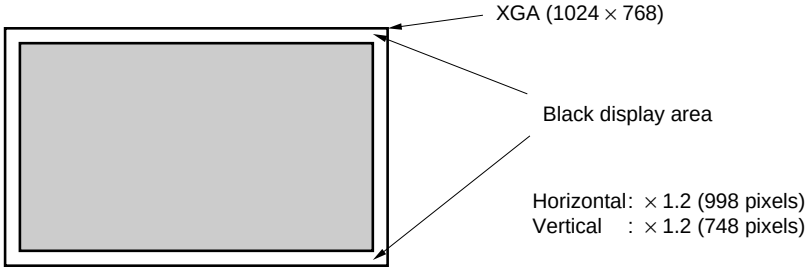
3) PC9801 mode (640 × 400)



4) VGA text mode (720 × 400)



5) 832 × 624 MAC mode (832 × 624)



COLOR CONTROL FUNCTION AND GRAPH IMAGE

This LCD module can adjust the following functions by serial data input (table.1)

(1) Main contrast:
(2) Sub-contrast R/G/B:
(3) Sub-brightness R/G/B:

} See table 9, 10 and **Color control function and graph image**

(1) Main contrast

This function adjusts R/G/B contrast at the same time. Contrast control the amplitude of input video signal.

Default value : 128
Valid range : 78 to 198
Contrast minimum : 198
Contrast maximum : 78
ADJSEL = “H” or “Open”: Maincontrast = 128

(2) Sub-contrast R, G, B

Sub-contrast can be adjusted for each R/G/B. Contrast control the amplitude of input video signal.

Default value : 128
Valid range : 78 to 198
Contrast minimum : 78
Contrast maximum : 198
ADJSEL = “H” or “Open”: Sub-contrast R.G.B = 128

(3) Sub-brightness R, G, B

Sub-brightness can be adjusted for each R/G/B. Brightness adjust the black level of input video signal.

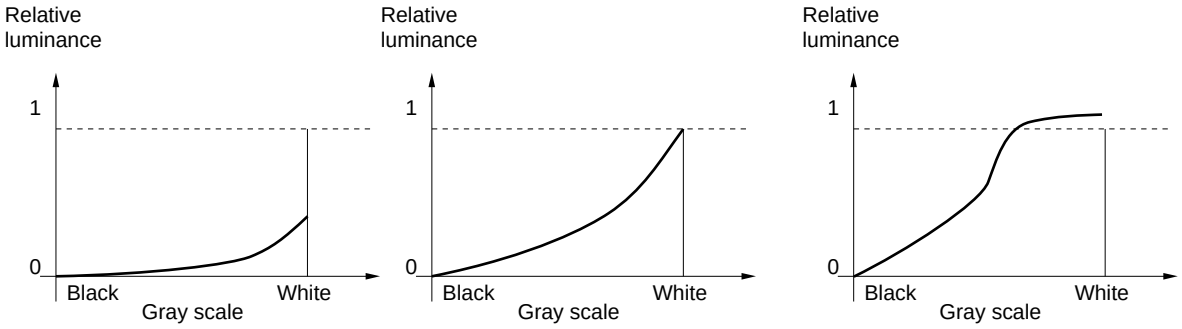
Default value : 128
Valid range : 55 to 163
Brightness minimum : 55
Brightness maximum : 163
ADJSEL = “H” or “Open”: Sub-brightness R.G.B = 128

Notes 1. Setting these values out of proper ranges may cause deterioration of LCD. Keep the values in valid ranges.

2. Difference between each LCD module may be seen even if the values for the functions are the identical. Moreover, optical characteristics are affected by this function. A sufficient evaluation to adopt this function is recommended.

<GRAPH IMAGE>

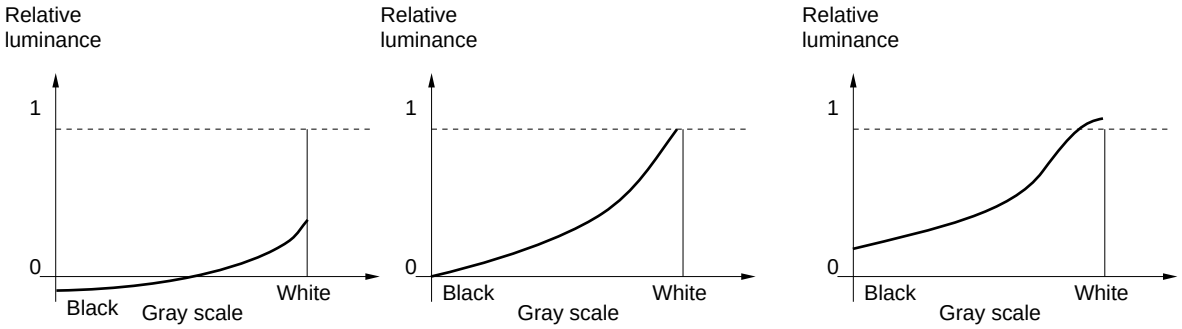
- Main contrast & Sub contrast



Main contrast
max. ← DEFAULT → min.

Sub contrast
max. ← DEFAULT → min.

- Sub brightness



Sub brightness
min. ← DEFAULT → max.

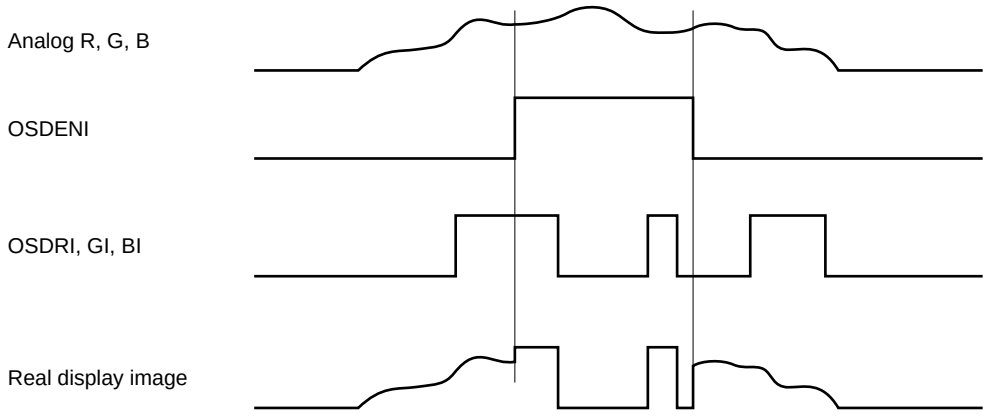
OSD FUNCTION

OSD (On Screen Display) is a function to display other digital data on analog data. Possible to display 1 bit data for each R/G/B color (8 colors). OSD is valid for the period of OSDENI.

OSDRI, OSDGI, OSDBI : digital data for OSD
OSDENI = “H” : OSD signal is valid
OSDENI = “L” : OSD signal is not valid

OSD is a sub-display for function-control and the display quality is not guaranteed. Please adopt the OSD image under sufficient evaluation of display quality.

<OSD image>



Note Regarding the use of OSD, please note that there is possibility of conflicts with a patent in Europe and the U.S.
Thus, if such conflict might happen when you use OSD, we shall not be responsible for any trouble.

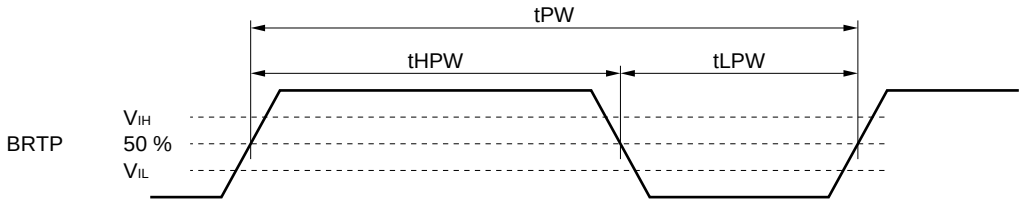
OUTSIDE CONTROL FOR LUMINANCE

Outside control is valid when PWSEL = “L” and BRTP signal is inputted. Luminance can be controlled by the duty value of input signal for BRTP.

Duty = 100%: Luminance is maximum.

Duty = 20% : Luminance is minimum.

Timing for BRTP



Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Frequency	1/tPW	185	–	340	Hz	–
Pulse-width	tHPW/tPW	20	–	100	%	at max. luminance (100%)
Input voltage	V_{IL}	–	–	0.6	V	–
	V_{IH}	4.5	–	–	V	–

Regarding set up for the frequency, please refer to following method.

Set up the frequency = Vsync frequency × (n + 0.25) or (n + 0.75)

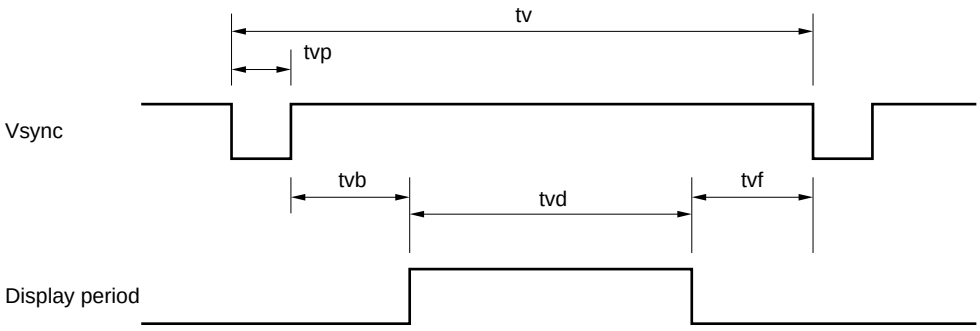
Please adopt the frequency under sufficient evaluation of display quality because the display may be disturbed depending on a frequency.

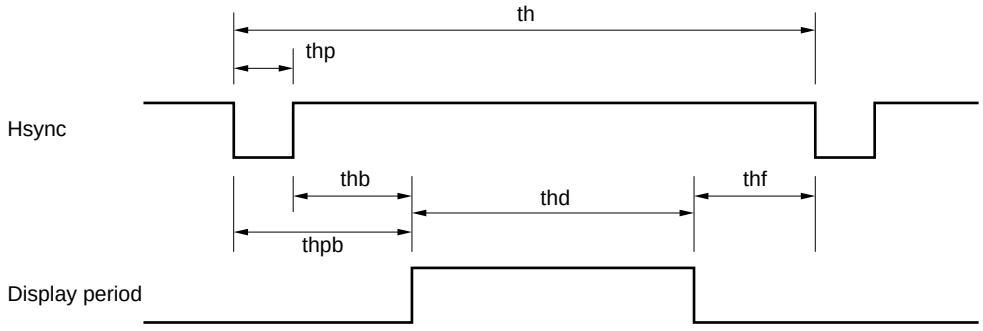
INPUT SIRIAL TIMING

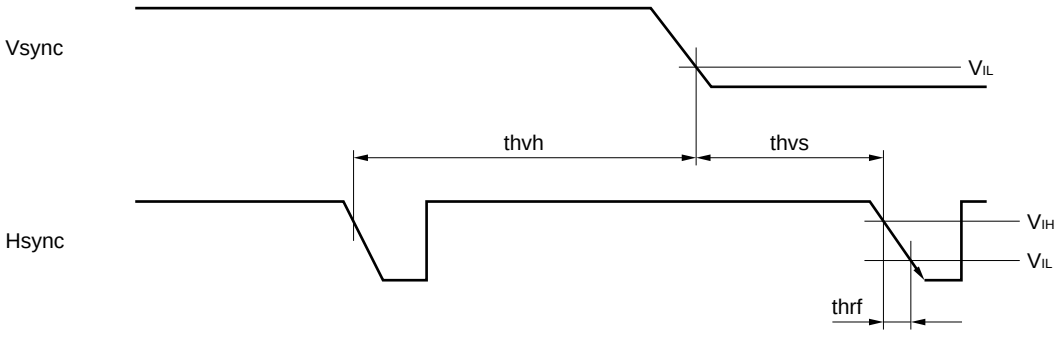
XGA MODE (STANDARD)

	Name	Symbol	Min.	Typ.	Max.	Unit	Remark
CLK	Frequency	1/tc	52.0 –	65.0 15.385	80.0 –	MHz ns	XGA standard
	Rise/Fall	tcrf	–	–	10	ns	–
	Pulse-width	tcl/tc	0.4	0.5	0.6	–	–
Hsync	Period	th	16.0 –	20.677 1344	22.7 –	μs CLK	48.363 kHz (typ.)
	Display	thd	– –	15.754 1024	– –	μs CLK	–
	Front-porch	thf	– 10	0.369 24	– –	μs CLK	–
	Pulse-width	thp	– 16	2.092 136	– –	μs CLK	–
	Back-porch	thb	1.0 44	2.462 160	– –	μs CLK	**Note**
	Pulse-width + Back-porch	thbp	1.8	–	–	μs	–
	Vsync - Hsync timing	thvh	3	–	–	CLK	–
		thvs	1	–	–	CLK	–
	Rise/Fall	thrf	–	–	10	ns	–
Vsync	Period	tv	13.3 –	16.665 806	18.5 –	ms H	60.004 Hz (typ.)
	Display	tvd	– –	15.880 768	– –	μs H	–
	Front-porch	tvf	– 1	62.031 3	– –	μs H	–
	Pulse-width	tvp	– 2	124.06 6	– –	μs H	–
	Back-porch	tvb	– 5	599.63 29	– –	μs H	–
Analog R, G, B	–	tda	4	–	–	ns	–

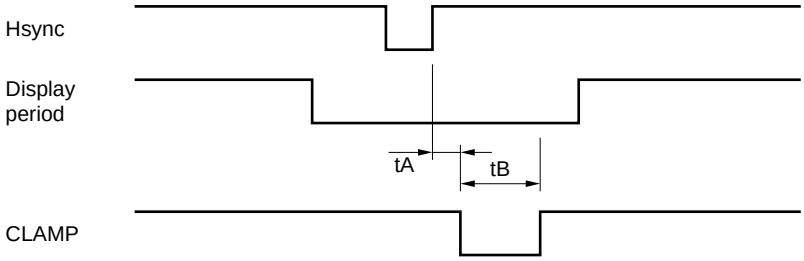
Note Back-porch (thb) must exceed both 1.0 μs and 44 CLK.


tv
tvp
Vsync
tvb
tvd
tvf
Display period


th
thp
Hsync
thb
thd
thf
thpb
Display period


Vsync
VIL
thvh
thvs
Hsync
VIH
VIL
thrf

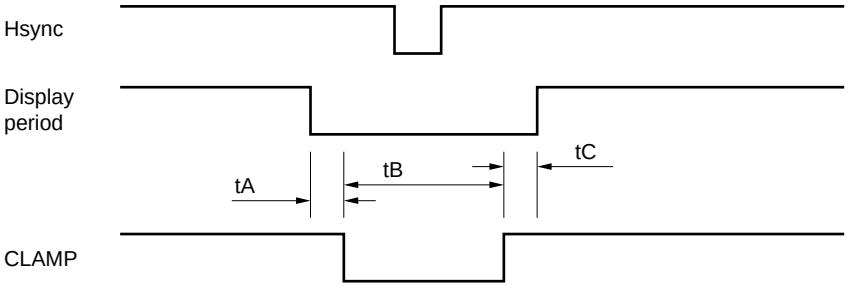
TIMING FOR GENERATING CLAMP SIGNAL INTERNALLY



MOD1	MOD2	tA [CLK]	tB [ns]
0	0	Prohibit	
0	1	2	27
1	0		20
1	1		15

Note Exclude noises on analog R, G, B signal. Analog R, G, B signals are the black level reference during CLAMP = "L". If noises are on the analog signals, luminance level of display is changed and the image quality of the display may be worse.

TIMING FOR INPUTING CLAMP SIGNAL EXTERNALLY



Item	Min.	Typ.	Max.	Unit	Remarks
tA	0.1	–	–	μs	–
tB	0.3	–	–	μs	–
tC	0.2	–	–	μs	–

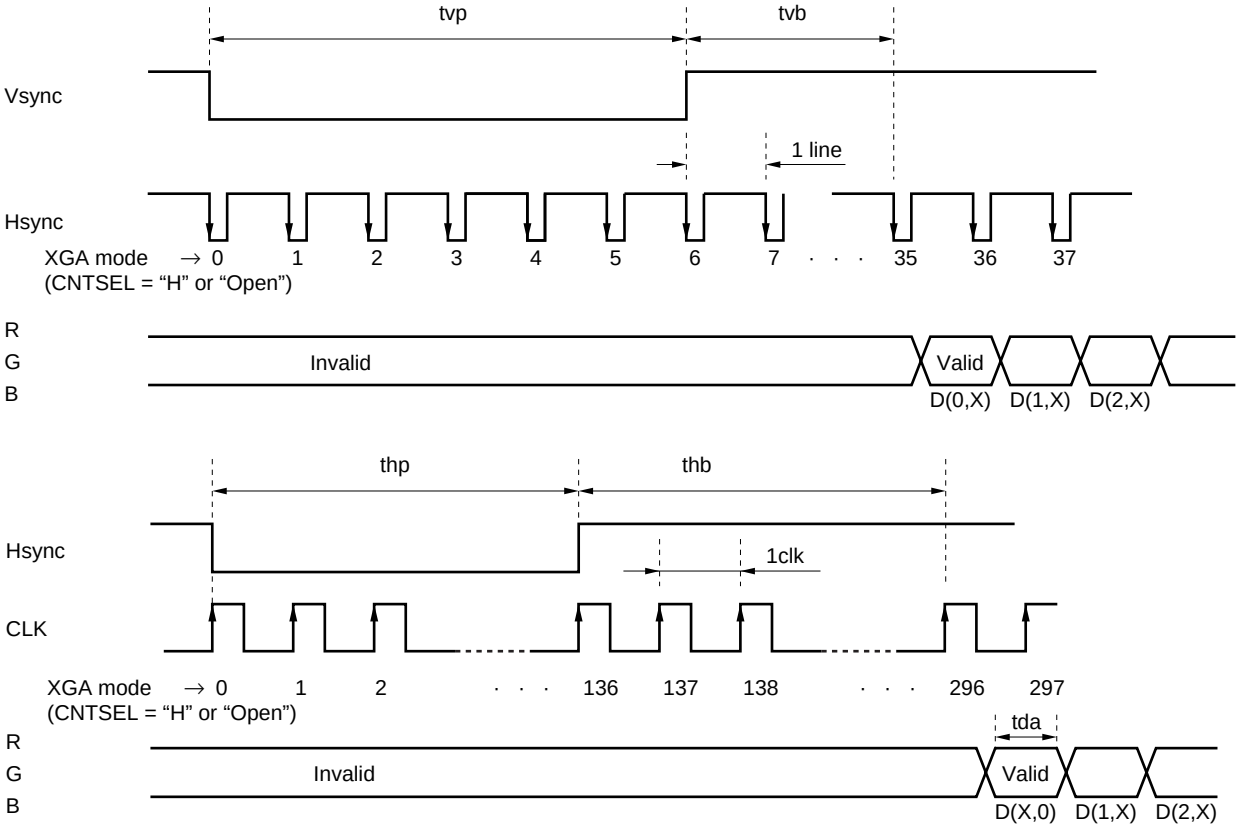
Note Exclude noises on analog R, G, B signal. Analog R, G, B signals are the black level reference during CLAMP = "L". If noises are on the analog signals, luminance level of display is changed and the image quality of the display may be worse.

INPUT SIGNAL AND DISPLAY POSITION

XGA standard timing

Pixels

D (0, 0)	D (0, 1)	D (0, 2)	• • •	• • •	D (0, 1023)
D (1, 0)	D (1, 1)	D (1, 2)	• • •	• • •	D (1, 1023)
D (2, 0)	D (2, 1)	D (2, 2)	• • •	• • •	D (2, 1023)
•	•	•	•		•
•	•	•	•		•
•	•	•	•		•
•	•	•	•		•
D (767, 0)	D (767, 1)	D (767, 2)	• • •	• • •	D (767, 1023)



Note tda should be minimum 4 ns.

OPTICAL CHARACTERISTICS

(Ta = 25°C, V_{DD} = 12 V, $V_{DD}B$ = 12 V) **Note 1**

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Contrast ratio	CR	Perpendicular	80	200	–	–	**Note 2**
Luminance	Lvmax	White	150	200	–	cd/m^2	–
Luminance uniformity	–	White	–	–	1.30	–	**Note 3**

Reference data

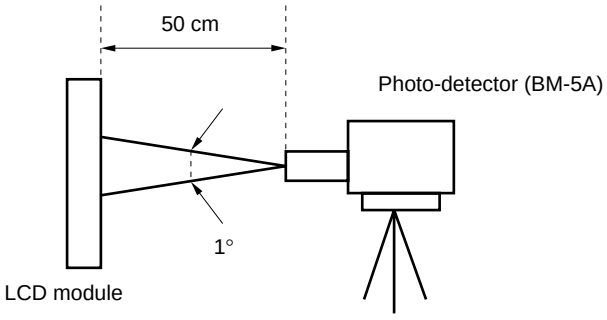
(Ta = 25°C, V_{DD} = 12 V, $V_{DD}B$ = 12 V) **Note 1**

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Contrast ratio	CR	Highest contrast ratio at θD = 10°	–	350	–	–	**Note 2**
Viewing angle range	θR	CR > 10, θU = 0°, θD = 0°	50	55	–	deg.	**Note 4**
	θL		50	55	–	deg.	
	θU	CR > 10, θR = 0°, θL = 0°	35	50	–	deg.	
	θD		30	45	–	deg.	
Color gamut	C	at center, to NTSC	35	42	–	%	–
Luminance control range	–	Maximum luminance: 100%	–	20 to 100	–	%	–
Response time	Ton	white to black	–	15	40	ms	**Note 5**
	Toff	black to white	–	40	50	ms	**Note 5**

Notes 1. The luminance is measured at 20 minutes after power on, with all pixels in “white”. The typical value is measured after luminance saturation.
Display mode : VESA XGA-75 Hz
RGB input voltage: 0.7 Vp-p
Contrast : Default value

2. The contrast ratio is calculated using the following formula.

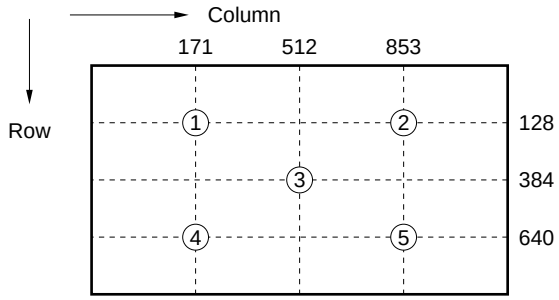
$$\text{Contrast ratio (CR)} = \frac{\text{Luminance with all pixels in “white”}}{\text{Luminance with all pixels in “black”}}$$



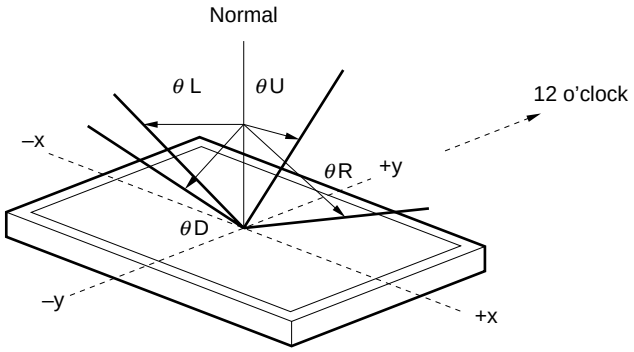
3. Luminance uniformity is calculated using the following formula.

$$\text{Luminance uniformity} = \frac{\text{Maximum luminance}}{\text{Minimum luminance}}$$

The luminance is measured near five points shown below.

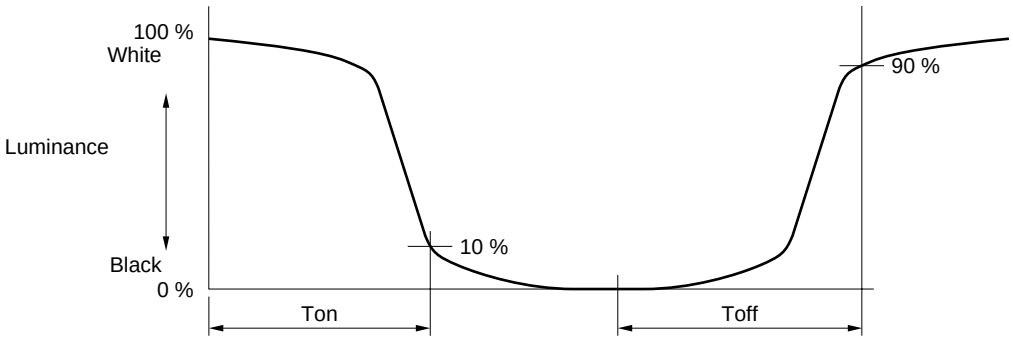


4. Definitions of viewing angle are as follows.



5. Definitions of response time is as follows.

Photo-detector output signal is measured when the luminance changes “white” to “black” and “black” to “white”. Response time are Ton and Toff of the photo-detector output amplitude. Ton is the time between 100% and 10%. Toff is the time between 0% and 90%.



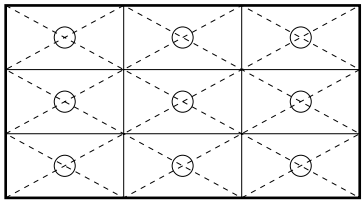
RELIABILITY TEST

Test item	Test condition	Judgment
High temperature/humidity operation	50 ±2°C, 85% relative humidity 240 hours, Display data is black.	**Note 1**
Heat cycle (operation)	<1> 0°C ±3°C ⋯ 1 hour 55°C ±3°C ⋯ 1 hour <2> 50 cycles, 4 hours/cycle <3> Display data is black.	**Note 1**
Thermal shock (non-operation)	<1> −20°C ±3°C ⋯ 30 minutes 60°C ±3°C ⋯ 30 minutes <2> 100 cycles <3> Temperature transition time is within 5 minutes.	**Note 1**
Vibration (non-operation)	<1> 5-100 Hz, 2 G 1 minute/cycle, X, Y, Z direction <2> 50 times each direction	**Notes 1, 2**
Mechanical shock (non-operation)	<1> 55 G, 11 ms X, Y, Z direction <2> 3 times each direction	**Notes 1, 2**
ESD (operation)	150 pF, 150 Ω, ±10 KV 9 places on a panel **Note 3** 10 times each place at one-second intervals	**Note 1**
Dust (operation)	15 kinds of dust (JIS Z 8901) Hourly 15 seconds stir, 8 times repeat	**Note 1**

Notes 1. Display function is checked by the same condition as LCD module out-going inspection.

2. Physical damage.

3. Discharge points are shown in the figure.



Next figures and sentences are very important. Please understand these, then read the text of a book.

CAUTION	This figure is a mark that you will get hurt and/or the module will have damages when you make a mistake to operate.

	This figure is a mark that you will get an electric shock when you make a mistake to operate.
	This figure is a mark that you will get hurt when you make a mistake to operate

CAUTION

Do not touch an inverter-on which is stuck a caution label-while LCD module is under operation, because of dangerous high voltage.

(1) Caution when taking out the module

<1> Pick the pouch only, in taking out module from a carrier box.

(2) Caution for handling the module

<1> As the electrostatic discharges may break LCD modules, handle LCD modules with care against electrostaic discharges.

<2> As LCD panels and backlight elements are made from fragile glass material, impulse and pressure to LCD modules should be avoided.

<3> As the surface of polarizer is very soft and easily scratched, use soft dry cloth without chemicals for cleaning.

<4> Do not pull the interface connectors in or out while LCD module is operating.

<5> Put modules display side down on a flat horizontal plane.

<6> Handle connectors and cables with care.

<7> The torque of mounting screw should be 0.392 N·m (4 kgf·cm) or less.

(3) Caution for the atmosphere

<1> Dew drop atmosphere should be avoided.

<2> Do not store and/or operate LCD modules in a high temperature and/or highly humid atmosphere. Storage in an electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.

<3> This module uses cold cathode fluorescent lamps. Therefore, the life time of lamps becomes short conspicuously at low temperature.

<4> Do not operate LCD modules in a high magnetic field.

(4) Caution for the module characteristics

<1> Do not apply fixed pattern data signal to the LCD module at product aging. Applying fixed pattern for a long time may cause image sticking.

(5) Other cautions

<1> Do not disassemble and/or reassemble LCD modules.

<2> Do not readjust variable resistor or switch etc.

<3> When returning modules for repair or etc., please pack the module not to be broken. We recommend the original shipping packages.

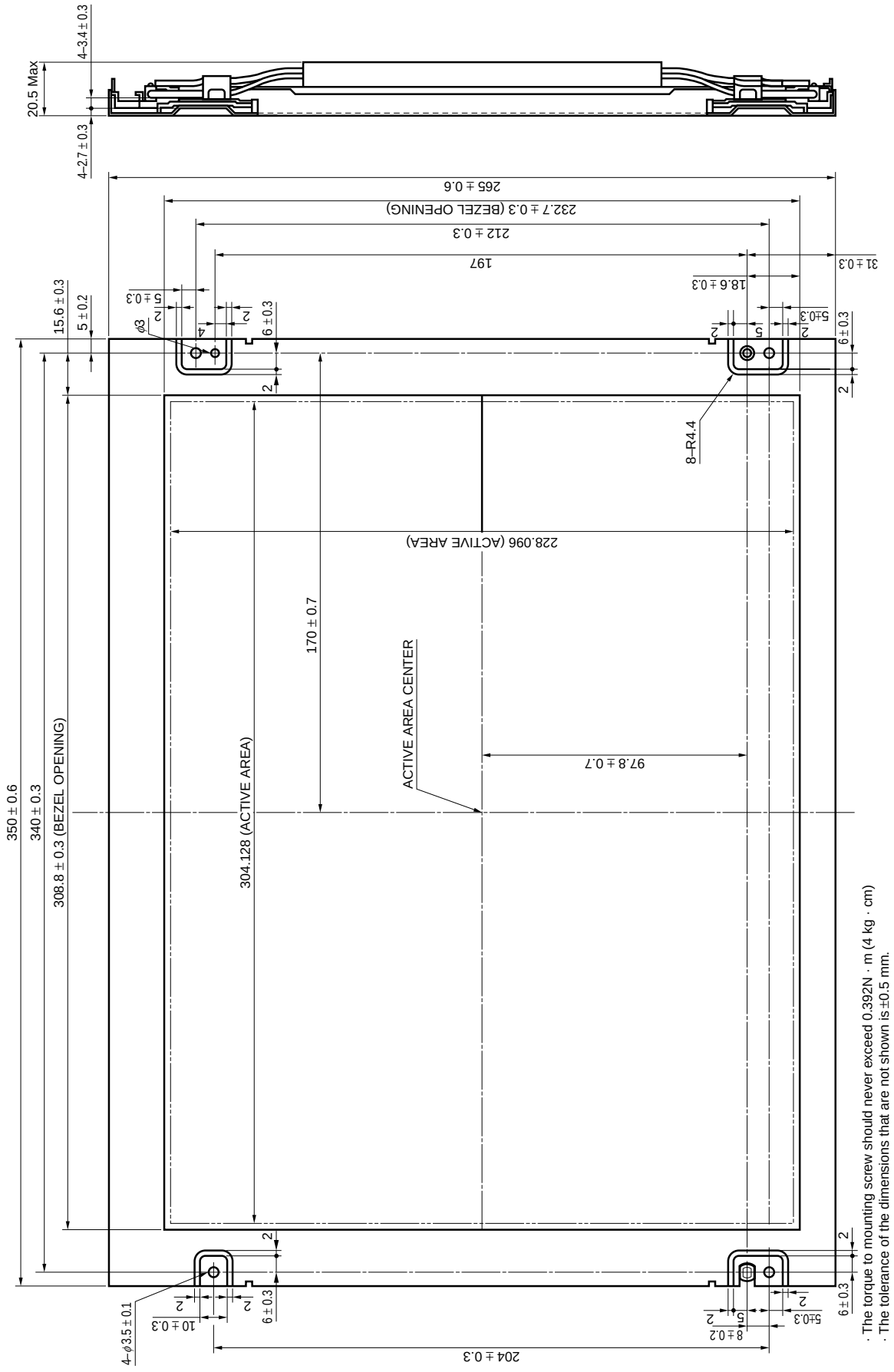
Liquid Crystal Display has the following specific characteristics. They are not defects or malfunctions.

The display conditions of LCD modules may be affected by the ambient temperature.
The LCD module uses cold cathode tubes for backlight. Optical characteristics, like luminance or uniformity, will change during time.

Uneven brightness and/or small spots may be noticed depending on different display patterns.

OUTLINE DRAWINGS

FRONT VIEW (Unit in mm)



OUTLINE DRAWING (Unit in mm)

REAR VIEW