International
IOR Rectifier

PD - 93997

IRF5806

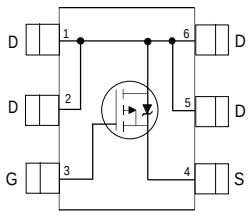
HEXFET® Power MOSFET

- Trench Technology
- Ultra Low On-Resistance
- P-Channel MOSFET
- Available in Tape & Reel

V_{DSS}	$R_{DS(on)}$ max	I_D
-20V	86mΩ@V_{GS} = -4.5V	-4.0A
	147mΩ@V_{GS} = -2.5V	-3.0A

Description

New trench HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in battery and load management applications.



Top View


Micro6™

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-Source Voltage	-20	V
I_D @ T_A = 25°C	Continuous Drain Current, V_{GS} @ -4.5V	-4.0	A
I_D @ T_A = 70°C	Continuous Drain Current, V_{GS} @ -4.5V	-3.3	
I_{DM}	Pulsed Drain Current①	-16.5	
P_D @T_A = 25°C	Maximum Power Dissipation③	2.0	W
P_D @T_A = 70°C	Maximum Power Dissipation③	1.3	W
	Linear Derating Factor	0.02	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
T_J , T_{STG}	Junction and Storage Temperature Range	-55 to + 150	°C

Thermal Resistance

	Parameter	Max.	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient③	62.5	°C/W

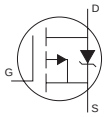
10/04/00

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-20	—	—	V	V_{GS} = 0V, I_D = -250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.011	—	V/°C	Reference to 25°C, I_D = -1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	47.1	86	mΩ	V_{GS} = -4.5V, I_D = -4.0A ②
		—	67.5	147		V_{GS} = -2.5V, I_D = -3.0A ②
$V_{GS(th)}$	Gate Threshold Voltage	-0.45	—	-1.2	V	V_{DS} = V_{GS}, I_D = -250µA
g_{fs}	Forward Transconductance	6.4	—	—	S	V_{DS} = -10V, I_D = -4.0A
I_{DSS}	Drain-to-Source Leakage Current	—	—	-15	µA	V_{DS} = -16V, V_{GS} = 0V
		—	—	-25		V_{DS} = -16V, V_{GS} = 0V, T_J = 70°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	-100	nA	V_{GS} = -12V
	Gate-to-Source Reverse Leakage	—	—	100		V_{GS} = 12V
Q_g	Total Gate Charge	—	8.3	11.4	nC	I_D = -4.0A
Q_{gs}	Gate-to-Source Charge	—	1.2	—		V_{DS} = -16V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	2.6	—		V_{GS} = -4.5V
$t_{d(on)}$	Turn-On Delay Time	—	6.2	9.3	ns	V_{DD} = -10V, V_{GS} = -4.5V
t_r	Rise Time	—	27	41		I_D = -1.0A
$t_{d(off)}$	Turn-Off Delay Time	—	94	140		R_G = 6.0Ω
t_f	Fall Time	—	126	190		R_D = 10Ω ②
C_{iss}	Input Capacitance	—	594	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	114	—		V_{DS} = -15V
C_{rss}	Reverse Transfer Capacitance	—	87	—		f = 1.0MHz

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-2.0	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	-16.5		
V_{SD}	Diode Forward Voltage	—	—	-1.2	V	T_J = 25°C, I_S = -2.0A, V_{GS} = 0V ②
t_{rr}	Reverse Recovery Time	—	116	174	ns	T_J = 25°C, I_F = -2.0A
Q_{rr}	Reverse Recovery Charge	—	90	135	nC	di/dt = -100A/µs ②



Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Pulse width ≤ 300µs; duty cycle ≤ 2%.

③ When mounted on 1 inch square Copper board, t ≤ 10sec.

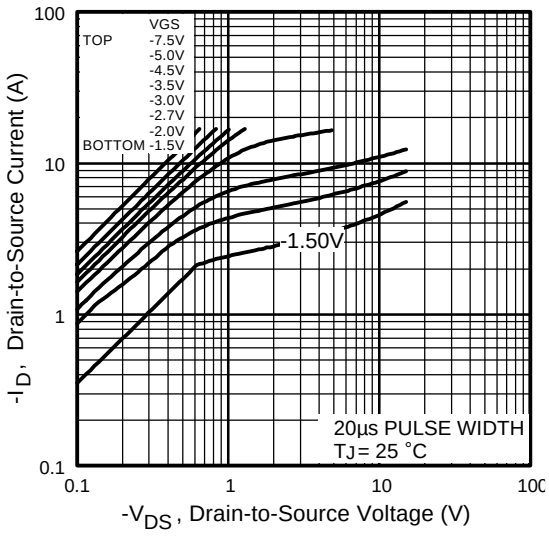


Fig 1. Typical Output Characteristics

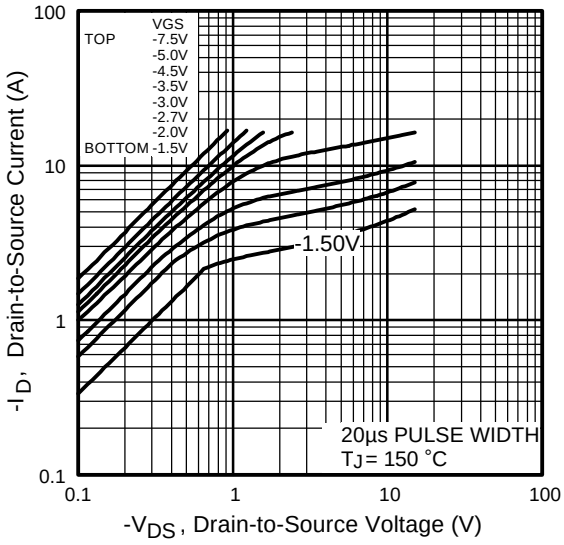


Fig 2. Typical Output Characteristics

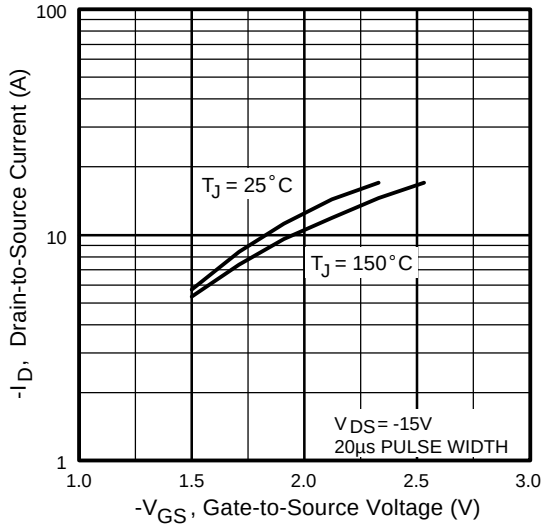


Fig 3. Typical Transfer Characteristics

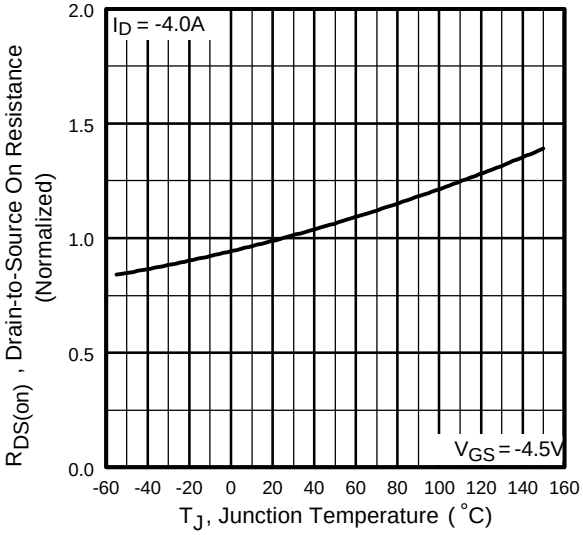


Fig 4. Normalized On-Resistance Vs. Temperature

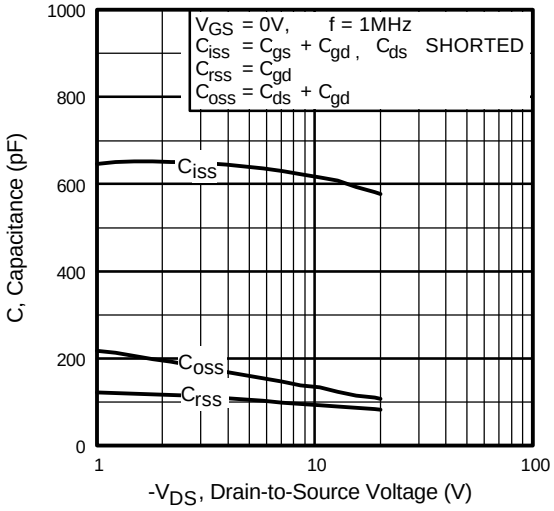


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

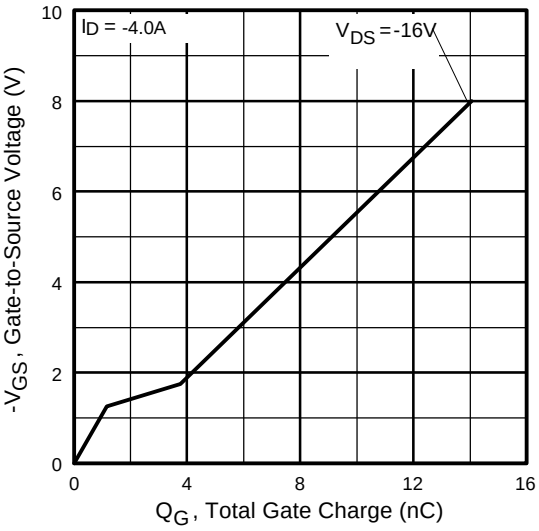


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

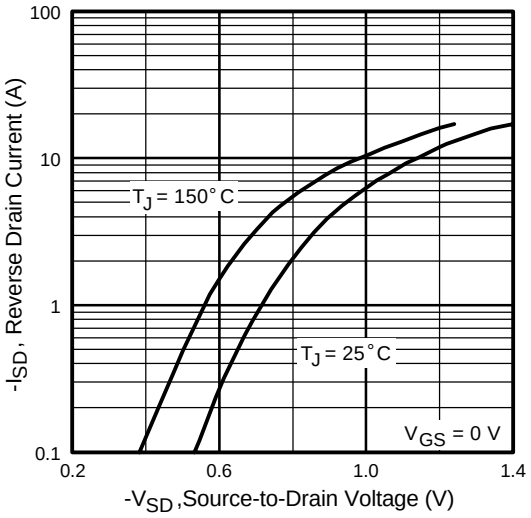


Fig 7. Typical Source-Drain Diode Forward Voltage

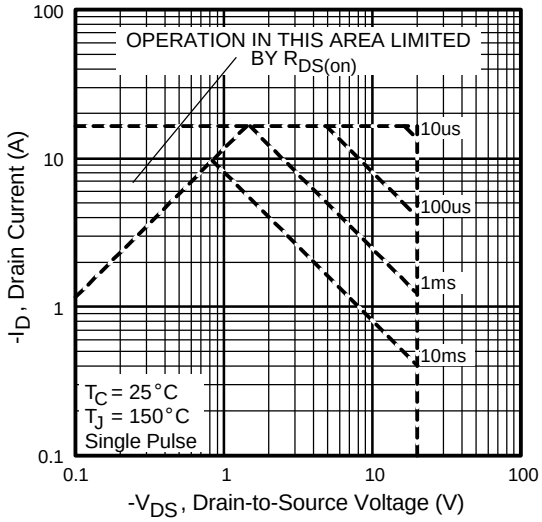


Fig 8. Maximum Safe Operating Area

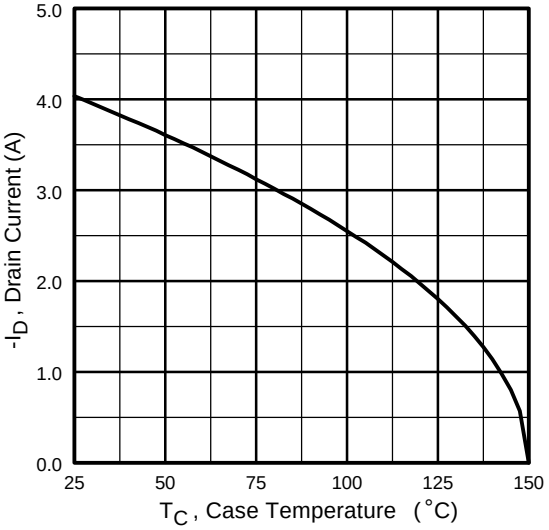


Fig 9. Maximum Drain Current Vs. Case Temperature

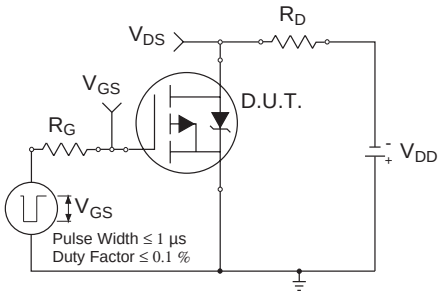


Fig 10a. Switching Time Test Circuit

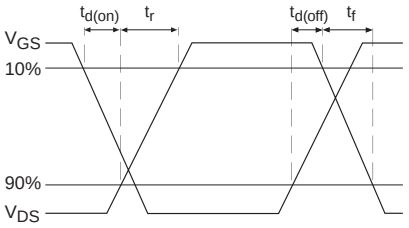


Fig 10b. Switching Time Waveforms

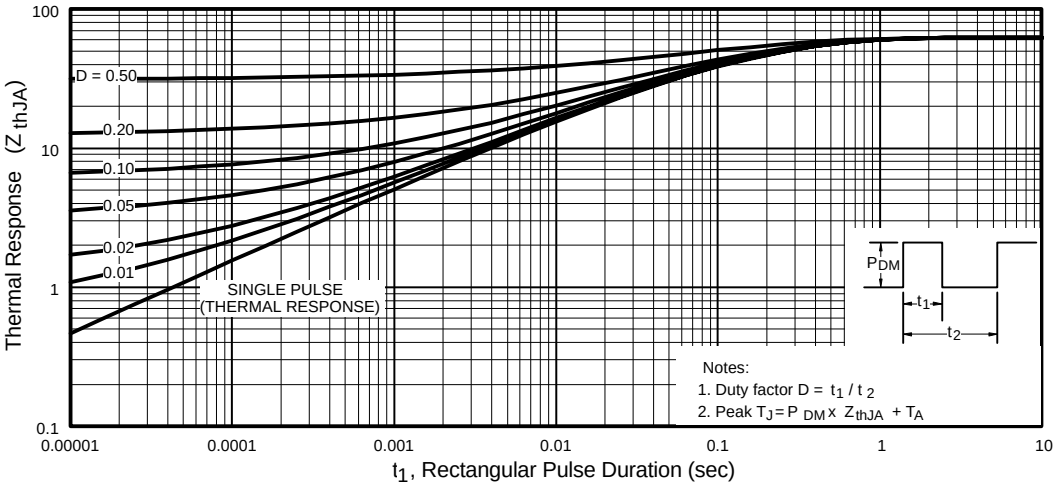


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

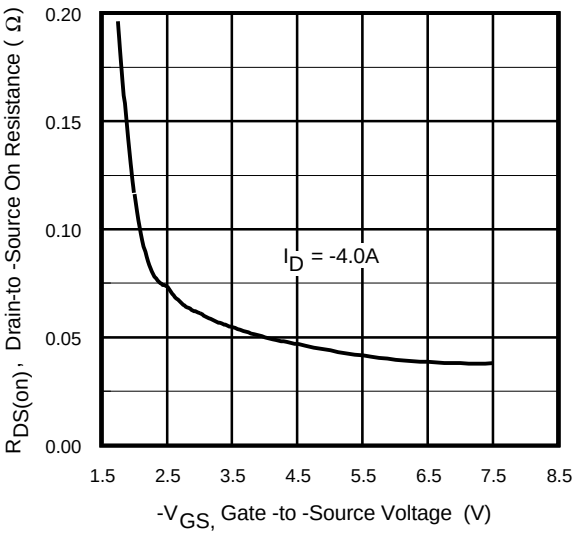


Fig 12. Typical On-Resistance Vs. Gate Voltage

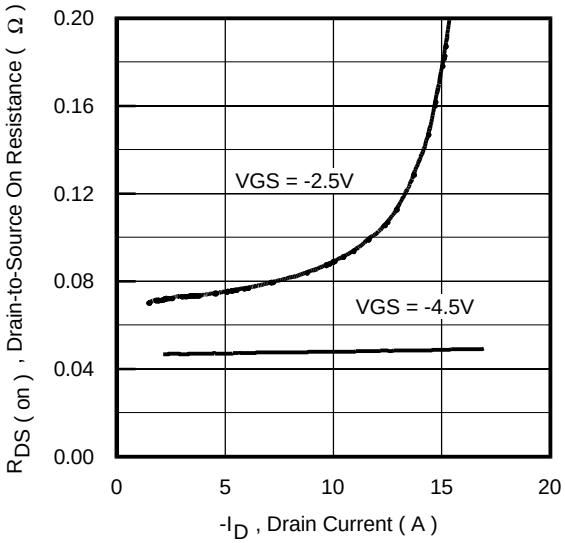


Fig 13. Typical On-Resistance Vs. Drain Current

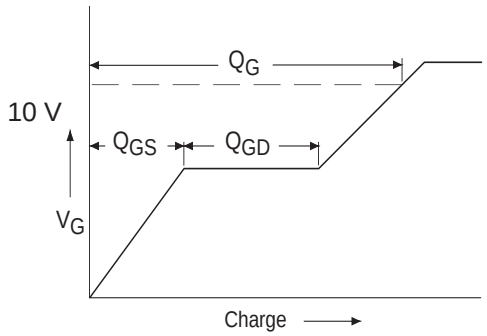


Fig 14a. Basic Gate Charge Waveform

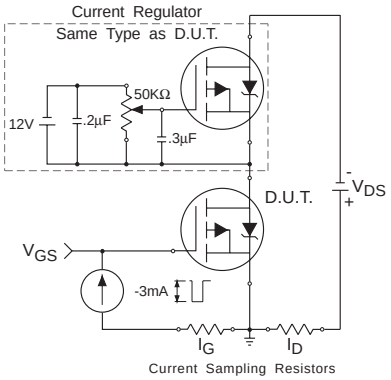


Fig 14b. Gate Charge Test Circuit

Package Outline

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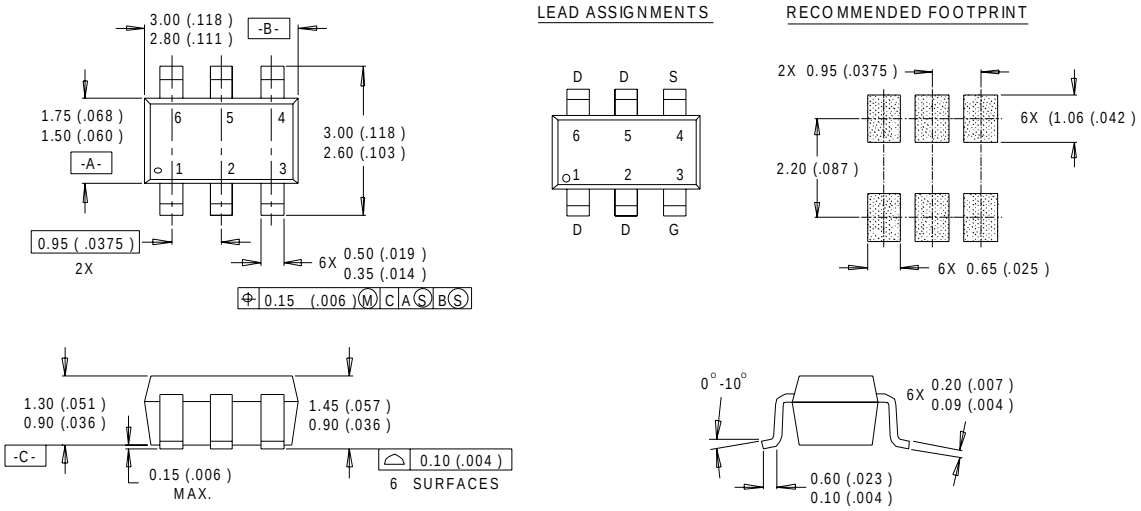

NOTES :
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION : MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).

Part Marking Information

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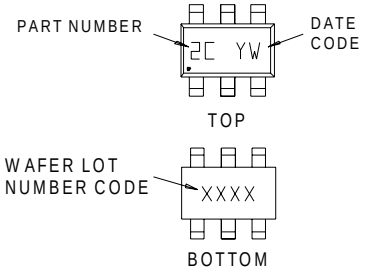
EXAMPLE : THIS IS AN IRLMS6702



PART NUMBER EXAMPLES:
2A = IRLMS1902
2B = IRLMS1503
2C = IRLMS6702
2D = IRLMS5703

DATE CODE EXAMPLES:
YWW = 9603 = 6C
YWW = 9632 = FF

YEAR	Y	WORK WEEK	W
2001	1	01	A
2002	2	02	B
2003	3	03	C
2004	4	04	D
2005	5	↓	↓
1996	6		
1997	7		
1998	8		
1999	9	↓	↓
2000	0	24	X
		25	Y
		26	Z

YEAR	Y	WORK WEEK	W
2001	A	27	A
2002	B	28	B
2003	C	29	C
2004	D	30	D
2005	E	↓	↓
1996	F		
1997	G		
1998	H		
1999	J	↓	↓
2000	K	50	X
		51	Y
		52	Z

WORK WEEK = (1-26) IF PRECEDED BY LAST DIGIT OF CALENDER YEAR
WORK WEEK = (27-52) IF PRECEDED BY A LETTER

Tape & Reel Information

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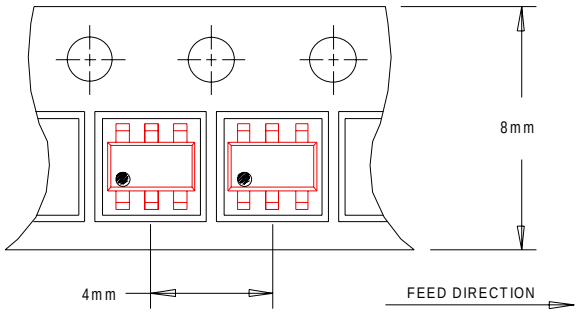
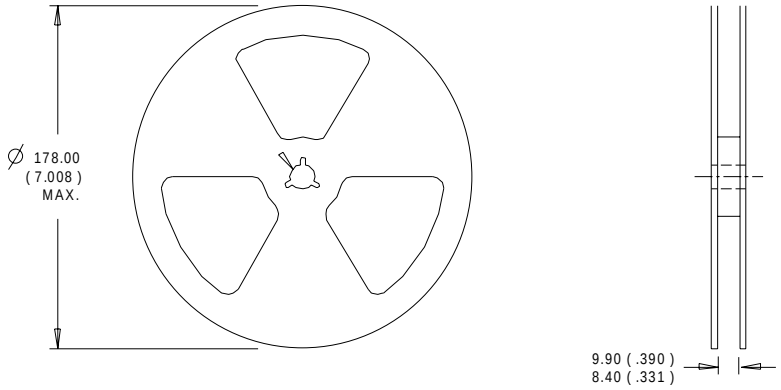


NOTES :
1. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTRE: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice.10/00