

## 2-band Electronic Volume

### Description

The CXA2547Q is a 2-channel electronic volume IC. A 34-bit serial data input controls the level and characteristics of the output signal. It may be used in car stereos and general audio systems.

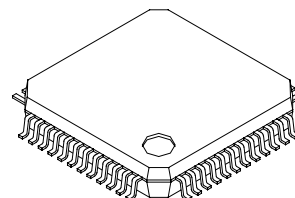
### Features

- Loudness
- Volume control  
(from 0 dB to  $-80$  dB,  $-\infty$  dB : Fine (1 dB-step)  
Coarse (8 dB-step)
- Balance
- Tone control  
(2-band, 2 dB-step from  $-15$  dB to  $+15$  dB)
- Fader  
2 dB-step to  $-20$  dB,  $-25$  dB,  $-35$  dB,  $-45$  dB,  $-60$  dB,  $-\infty$  dB)
- Input and gain selector (4 channels)
- Serial data control (DATA, CLK, CE)
- Single 8 V power supply
- Zero-cross detection circuit  
(L/R independent operation for the volume block)
- Timer
- Power-off mute
- Countermeasure to the noise of the portable telephone

### Structure

Bipolar silicon monolithic IC

48 pin QFP (Plastic)



### Absolute Maximum Ratings (Ta=25 °C)

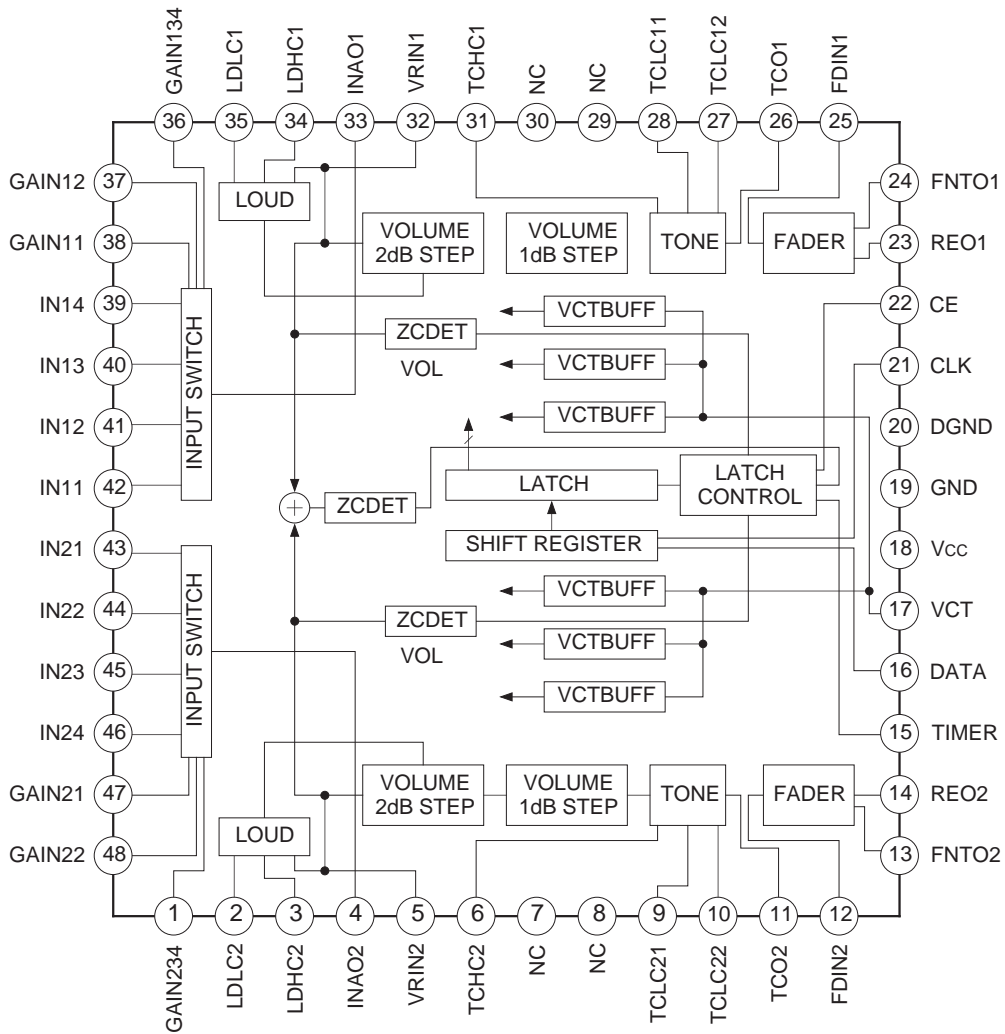
• Supply voltage	V <sub>CC</sub>	13	V
• Operating temperature	T <sub>opr</sub>	$-40$ to $+85$	°C
• Storage temperature	T <sub>stg</sub>	$-65$ to $+150$	°C
• Allowable power dissipation	P <sub>D</sub>	350	mW (Ta=85 °C)

### Recommended Operating Conditions

Supply voltage	V <sub>CC</sub>	7 to 12	V
----------------	-----------------	---------	---

Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.

Block Diagram and Pin Configuration



Pin Description

Pin No.	Symbol	I/O resistance Pin voltage	Equivalent circuit	Description
2 35	LDLC2 LDLC1	1.08 k VCT		Sets loudness low cut-off frequency.
3 34	LDHC2 LDHC1	24.05 k VCT		Set loudness high cut-off frequency
4 33	INAO2 INAO1	— VCT		Input selector output
5 32	VRIN2 VRIN1	10 k VCT		Volume input
6 31	TCHC2 TCHC1	5 k VCT		Set tone Treble frequency

Pin No.	Symbol	I/O resistance Pin voltage	Equivalent circuit	Description
7 30	NC	—		
8 29	NC	—		
9 28	TCLC21 TCLC11	8 k VCT		Sets tone Bass frequency
10 27	TCLC22 TCLC12	8 k VCT		Sets tone Bass frequency
11 26	TCO2 TCO1	— VCT		Tone control output

Pin No.	Symbol	I/O resistance Pin voltage	Equivalent circuit	Description
12 25	FDIN2 FDIN1	24 k VCT		Fader input
13 24	REO2 REO1	— VCT		Rear output
14 23	FNT02 FNT01	— VCT		Front output
15	TIMER	$\approx \infty$		Timer constant setting
16	DATA	$\approx \infty$		Serial data input

Pin No.	Symbol	I/O resistance Pin voltage	Equivalent circuit	Description
17	VCT	— VCT		1/2 V <sub>cc</sub>
18	V <sub>cc</sub>	— V <sub>cc</sub>		Power supply input
19	GND	— Gnd		Ground
20	DGND	— —		Digital ground
21	CLK	≈ ∞ —		Serial clock input
22	CE	≈ 20k —		Latch enable input Take care to set the low level as the input impedance is low.
1 36 37 38 47 48	GAIN234 GAIN134 GAIN12 GAIN11 GAIN21 GAIN22	≈ ∞ VCT		External gain setting for input amplifier
39 40 41 42 43 44 45 46	IN14 IN13 IN12 IN11 IN21 IN22 IN23 IN24	50 k VCT		Signal input

## Data Format

First Bit	D1	NOP
	D2	NOP
	D3	ISW
	D4	
	D5	LOUD
	D6	VRC1
	D7	
	D8	
	D9	
	D10	
	D11	
	D12	VRF1
	D13	VRC2
	D14	
	D15	
	D16	
	D17	
	D18	
	D19	VRF2
	D20	TONE BASS
	D21	
	D22	
	D23	
	D24	NOP
	D25	
	D26	
	D27	
	D28	TONE TREBLE
	D29	
	D30	
	D31	
	D32	FADER
	D33	
	D34	
	D35	
Last Bit	D36	FADER SELECT

ISW

Mode	D3	D4
IN14/IN24, GAIN134/GAIN234	1	1
IN13/IN23, GAIN134/GAIN234	1	0
IN12/IN22, GAIN12/GAIN22	0	1
IN11/IN21, GAIN11/GAIN21	0	0

LOUD

Mode	D5
ON	1
OFF	0

VRC1/VRC2

Output (dB)	D6/D13	D7/D14	D8/D15	D9/D16	D10/D17	D11/D18
0	1	1	1	1	1	1
-2	1	1	1	1	1	0
-4	1	1	1	1	0	1
-6	1	1	1	1	0	0
-8	1	1	1	0	1	1
-10	1	1	1	0	1	0
-12	1	1	1	0	0	1
-14	1	1	1	0	0	0
-16	1	1	0	1	1	1
-18	1	1	0	1	1	0
-20	1	1	0	1	0	1
-22	1	1	0	1	0	0
-24	1	1	0	0	1	1
-26	1	1	0	0	1	0
-28	1	1	0	0	0	1
-30	1	1	0	0	0	0
-32	1	0	1	1	1	1
-34	1	0	1	1	1	0
-36	1	0	1	1	0	1
-38	1	0	1	1	0	0
-40	1	0	1	0	1	1
-42	1	0	1	0	1	0
-44	1	0	1	0	0	1
-46	1	0	1	0	0	0
-48	1	0	0	1	1	1
-50	1	0	0	1	1	0
-52	1	0	0	1	0	1
-54	1	0	0	1	0	0
-56	1	0	0	0	1	1
-58	1	0	0	0	1	0
-60	1	0	0	0	0	1
-62	1	0	0	0	0	0
-64	0	1	1	1	1	—
-66	0	1	1	1	0	—
-68	0	1	1	0	1	—
-70	0	1	1	0	0	—
-72	0	1	0	1	1	—
-74	0	1	0	1	0	—
-76	0	1	0	0	1	—
-78	0	1	0	0	0	—
-80	0	0	1	—	—	—
-∞	0	0	0	—	—	—



VRF1/VRF2

Output (dB)	D12/D19
0	1
-1	0

BASS/TREBLE

Output (dB)	D20/D28	D21/D29	D22/D30
15	1	1	1
12	1	1	0
10	1	0	1
8	1	0	0
6	0	1	1
4	0	1	0
2	0	0	1
0	0	0	0

BOOST/CUT

Mode	D23/D31
BOOST	1
CUT	0

FADER

Output (dB)	D32	D33	D34	D35
-∞	1	1	1	1
-60	1	1	1	0
-45	1	1	0	1
-30	1	1	0	0
-25	1	0	1	1
-20	1	0	1	0
-18	1	0	0	1
-16	1	0	0	0
-14	0	1	1	1
-12	0	1	1	0
-10	0	1	0	1
-8	0	1	0	0
-6	0	0	1	1
-4	0	0	1	0
-2	0	0	0	1
0	0	0	0	0

## FADER SELECT

Mode	D36
FRONT	1
REAR	0

## RESET

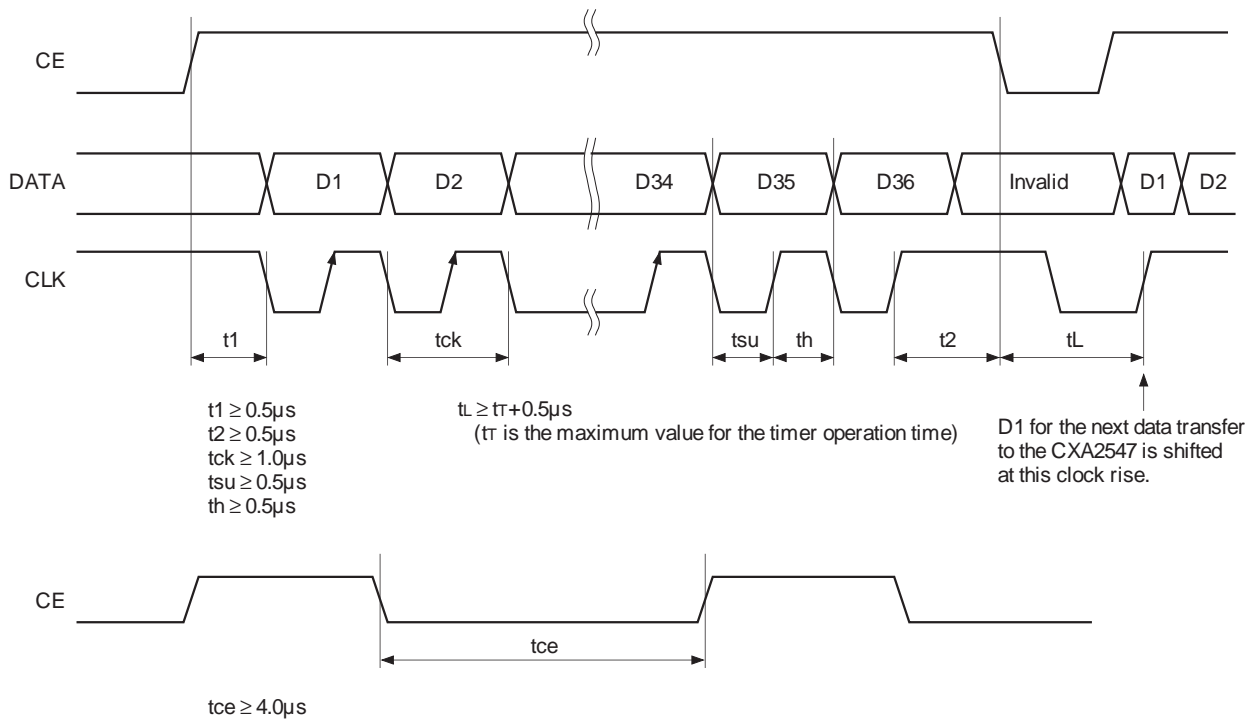
Reset is performed automatically when power is first supplied to the IC; there is no reset pin.

The following table shows the respective statuses of various settings after a reset has been performed.

Mode	Set value
INPUT	1
VRC1	-∞ dB
VRF1	-1 dB
VRC2	-∞ dB
VRF2	-1 dB
LOUD	OFF
TONE BASS	0 dB
TONE MID	0 dB
TONE TREBLE	0 dB
FADER	0 dB, REAR

\* Set all the transfer data to "0" for D24, D25, D26 and D27.

Timing Chart



Timer Waiting Period Setting Chart ( $V_{CC}=7$  to  $12$  V, operating temperature= $-40$  °C to  $85$  °C)

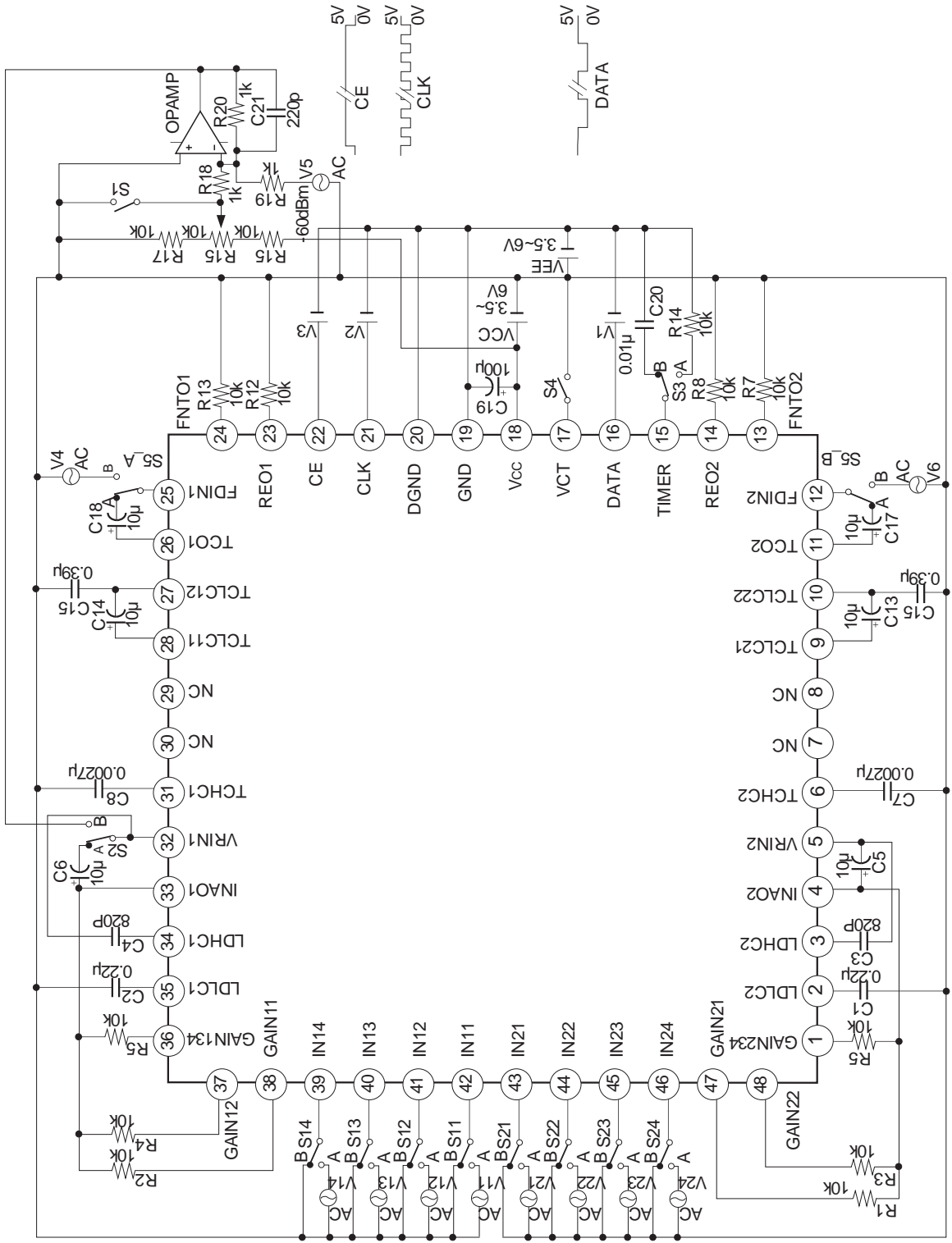
TIMER pin capacitance C	Waiting period		
	Min.	Typ.	Max.
C=100 pF	3 $\mu s$	5 $\mu s$	9 $\mu s$
C=0.001 $\mu F$	30 $\mu s$	50 $\mu s$	90 $\mu s$
C=0.01 $\mu F$	300 $\mu s$	500 $\mu s$	900 $\mu s$
C=0.1 $\mu F$	3 ms	5 ms	9 ms
C=1 $\mu F$	30 ms	50 ms	90 ms
C=10 $\mu F$	300 ms	500 ms	900 ms

## Electrical Characteristics

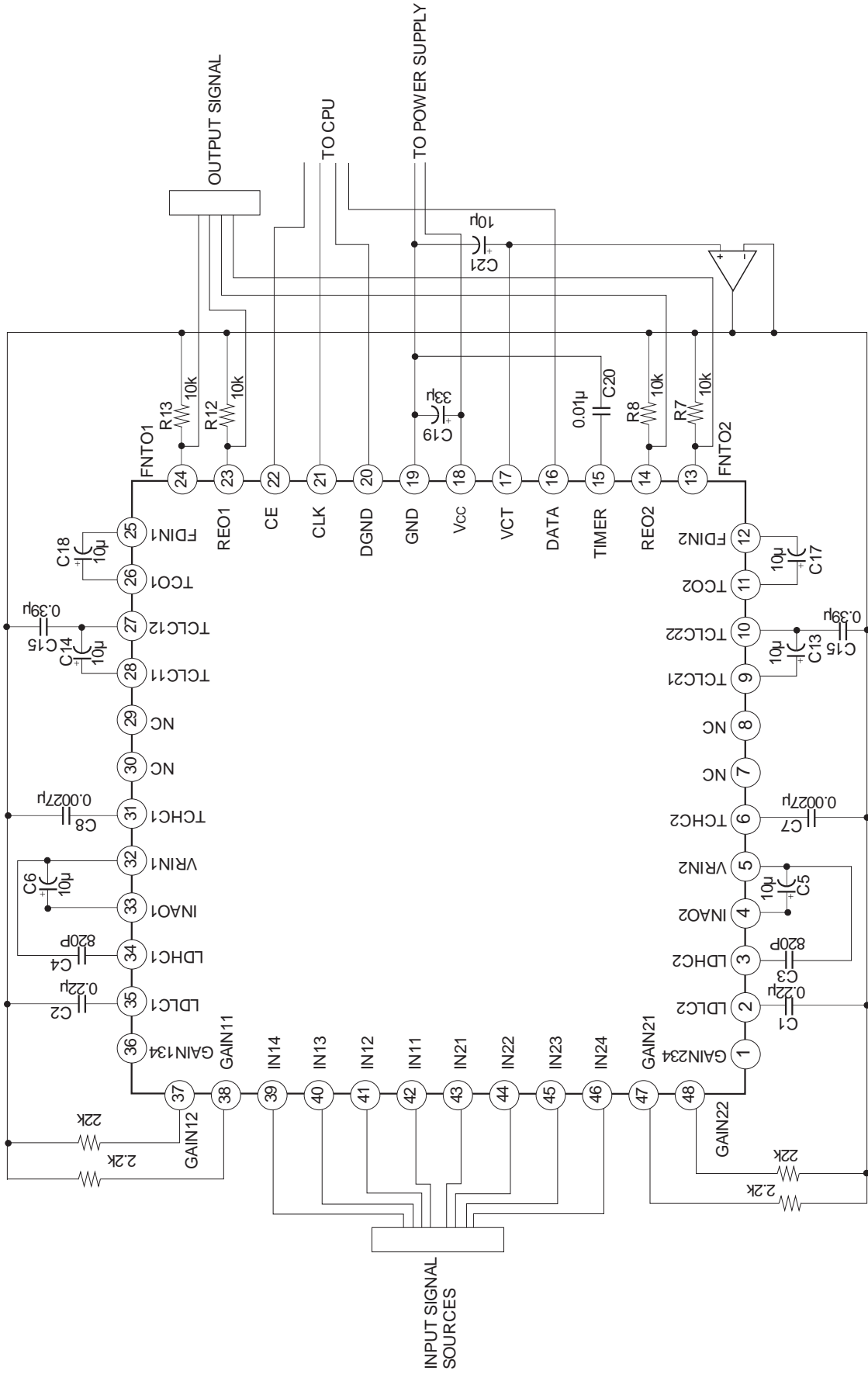
V<sub>CC</sub>=8 V, T<sub>a</sub>=25 °C, input=0 dB unless otherwise specified

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Current consumption	I <sub>CC</sub>	No signal	—	25	35	mA
Total harmonic distortion	THD	1 kHz, 5 dBm output	—	0.004	0.01	%
Output noise voltage	V <sub>n</sub>	Short-circuit at input, A weight	—	8	10	μV <sub>rms</sub>
Max. output voltage	V <sub>om</sub>	1 kHz	8	—	—	dBm
Separation	CS	1 kHz	72	90	—	dB
Max. attenuation factor	ATT <sub>m</sub>		85	90	—	
Loudness LOW boost	Gl <sub>b</sub>	100 Hz, VRC=−32 dB	13	15	17	
Loudness HIGH boost	Gl <sub>h</sub>	10 kHz, VRC=−32 dB	5	6	7	
Max. Bass boost gain	G <sub>bb</sub>		13	15	17	
Max. Bass cut gain	G <sub>bc</sub>		13	15	17	
Max. Treble boost gain	G <sub>tb</sub>		13	15	17	
Max. Treble cut gain	G <sub>tc</sub>		13	15	17	V
Input voltage HIGH	V <sub>sh</sub>	DATA, CLK, CE	3	—	6	
Input voltage LOW	V <sub>sl</sub>	DATA, CLK, CE	0	—	1.5	
Input voltage range	V <sub>in</sub>	IN11 to 14 IN21 to 24 VRIN1, 2 FDIN1, 2	The IC is not destroyed or does not operate abnormally.	1	—	V <sub>CC</sub> −1

Electrical Characteristics Measurement Circuit



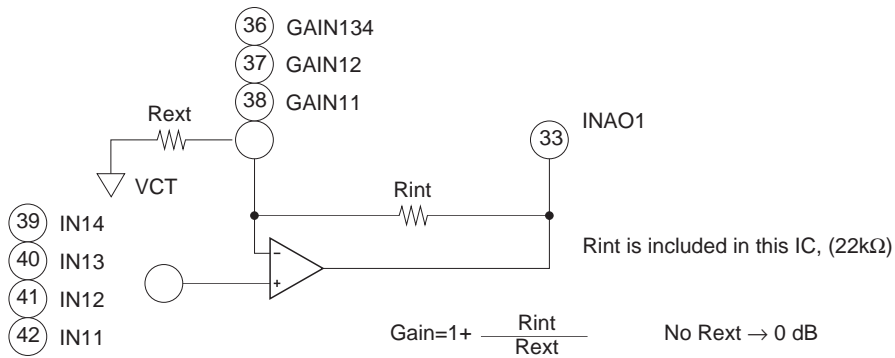
Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

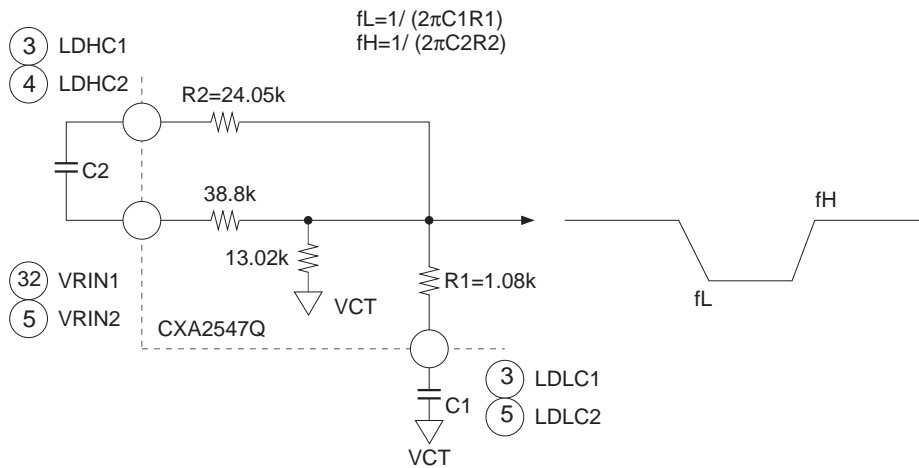
**Description of Operation**

(1) Input amplifier gain



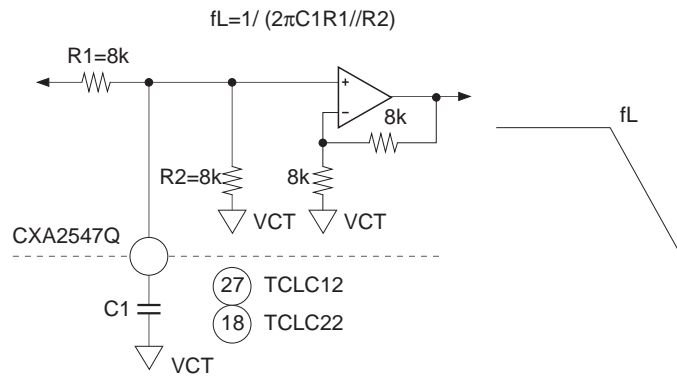
(2) LOUD

The loudness function achieves the necessary frequency response by using a filter as shown below. The resistors are built in this IC so that  $f_L$  and  $f_H$  can be set by selecting C1 and C2.

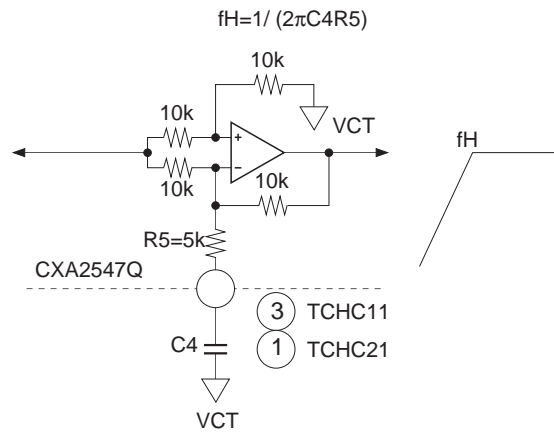


(3) Tone control

BASS : LPF



TREBLE : HPF

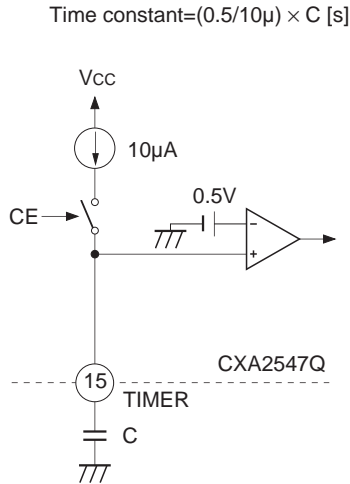




(4) Zero-cross detector and timer

A built-in zero-cross detection circuit is used to detect the zero-cross points of the input signal. When data arrived at the IC, they are executed at the next zero-cross point or when there is no input signal. This is to minimize 'click' noise during the transition of levels.

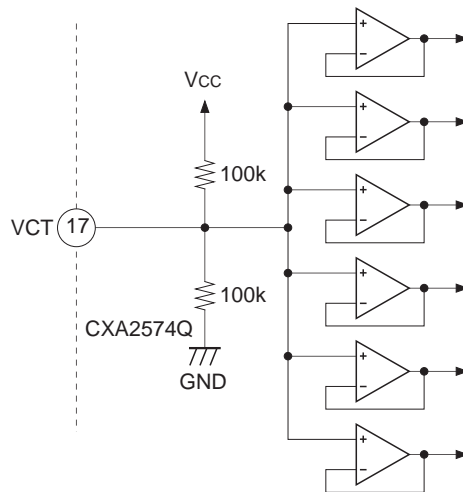
The timer circuit is added to ensure that the data is executed even when a zero-cross point is not detected after a certain period of time from the falling edge of the CE pulse.



(5) VCT pin

The internal circuit of VCT pin has the following structure.

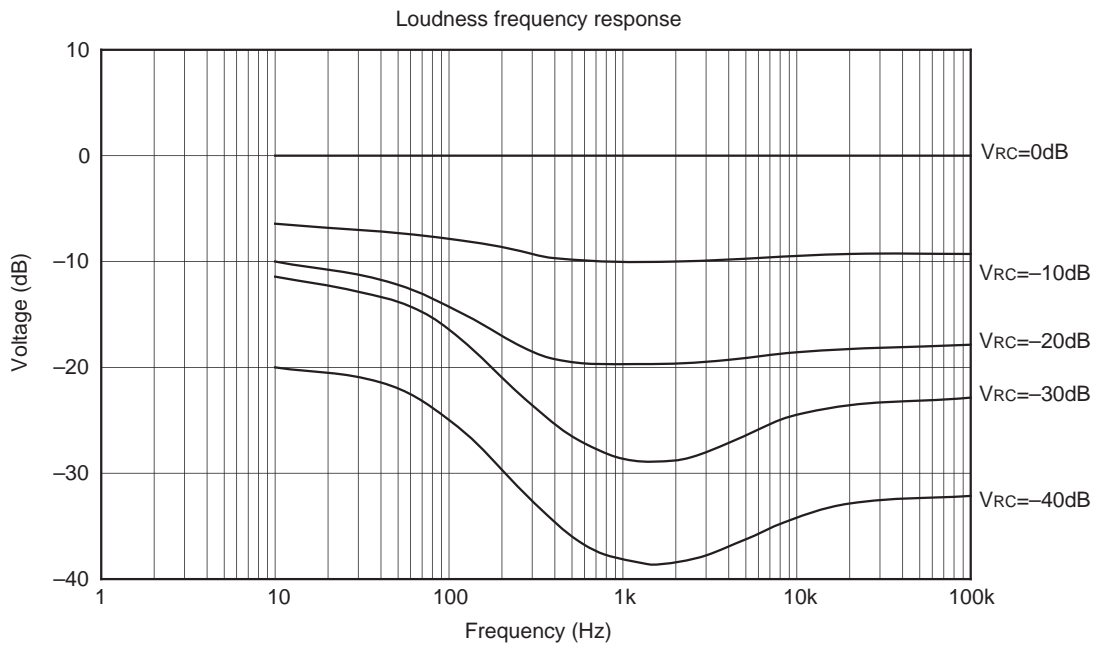
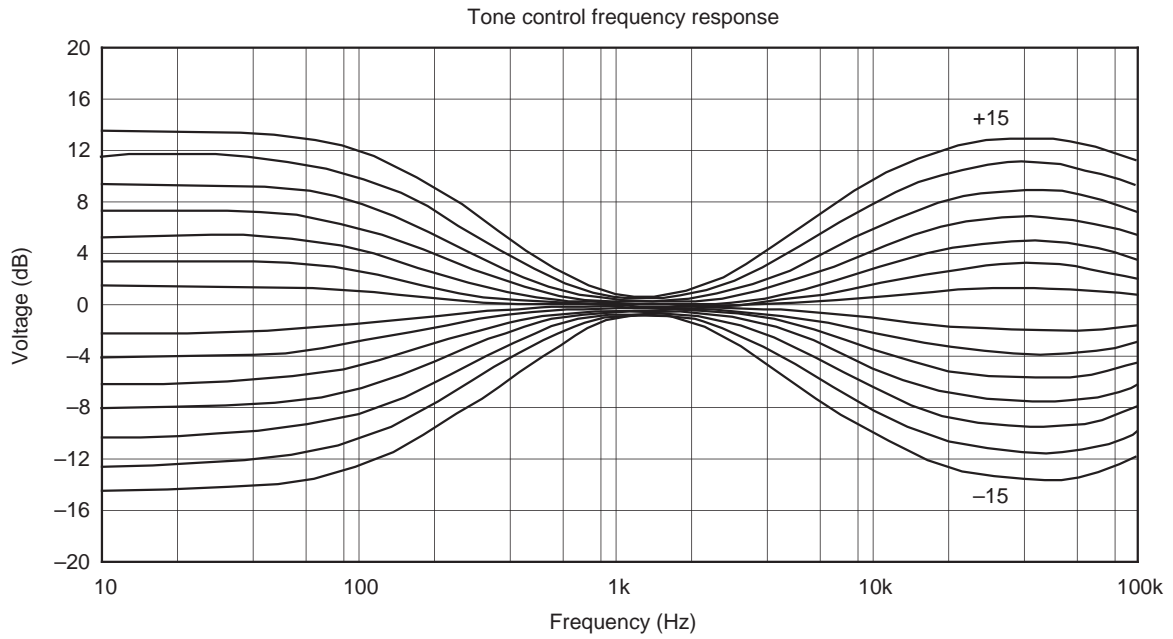
Insert a buffer when using the pin as a reference voltage for an external circuit.



(6) Power-off mute

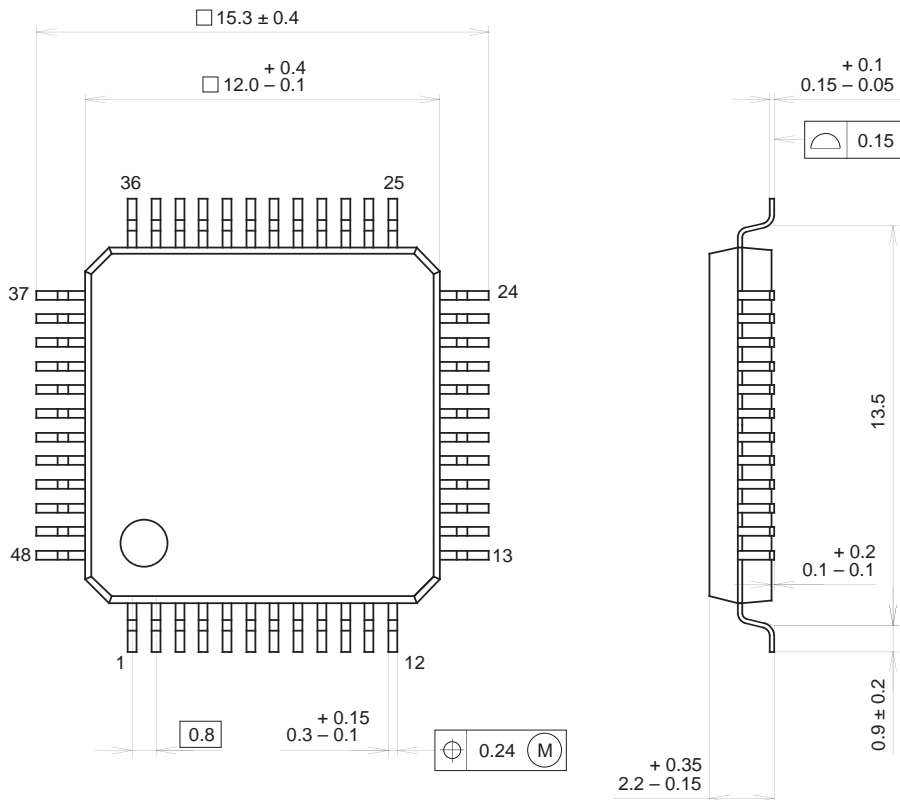
When  $V_{cc}$  goes below 5 V, the output stage bias of the fader output pins FNT01, FNT02, REO1, and REO2 is turned off and the pins go to high impedance. This operation prevents popping noises caused by the output pin potential deviating from  $V_{cc}/2$  when the power is turned off.

Example of Representative Characteristics



Package Outline Unit : mm

48PIN QFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP-48P-L04
EIAJ CODE	QFP048-P-1212
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.7g

NOTE : PALLADIUM PLATING  
 This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).