

Features

- High Voltage Type (20V Rating)
- Serial Data Input
- Active Parallel Output
- Storage Register Capability
- Master Clear
- Can Function as Demultiplexer
- 100% Tested for Quiescent Current at 20V
- 5V, 10V and 15V Parametric Ratings
- Standardized Symmetrical Output Characteristics
- Maximum Input Current of 1 μ A at 18V Over Full Package Temperature Range; 100nA at 18V and +25 $^{\circ}$ C
- Noise Margin (Over Full Package/Temperature Range)
 - 1V at VDD = 5V
 - 2V at VDD = 10V
 - 2.5V at VDD = 15V
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Multi-Line Decoders
- A/D Converters

Description

CD4099BMS 8-bit addressable latch is a serial input, parallel output storage register that can perform a variety of functions.

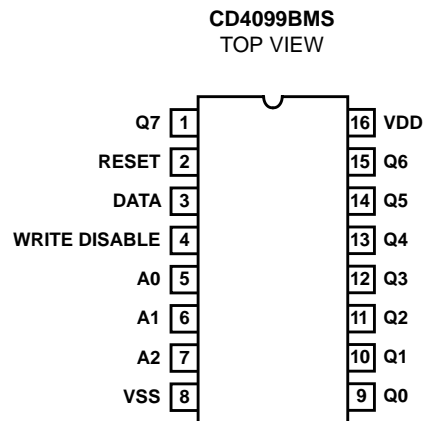
Data are inputted to a particular bit in the latch when that bit is addressed (by means of inputs A0, A1, A2) and when WRITE DISABLE is at a low level. When WRITE DISABLE is high, data entry is inhibited; however, all 8 outputs can be continuously read independent of WRITE DISABLE and address inputs.

A master RESET input is available, which resets all bits to a logic "0" level when RESET and WRITE DISABLE are at a high level. When RESET is at a high level, and WRITE DISABLE is at a low level, the latch acts as a 1 of 8 demultiplexer; the bit that is addressed has an active output which follows the data input, while all unaddressed bits are held to a logic "0" level.

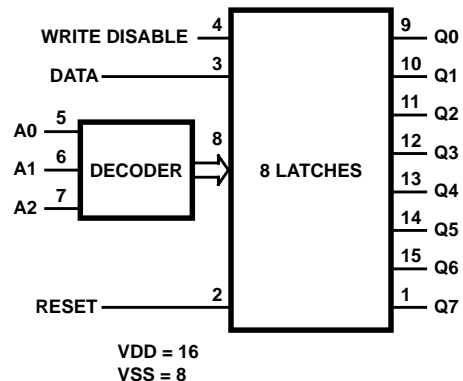
The CD4099BMS is supplied in these 16-lead outline packages:

| | |
|------------------|-----|
| Braze Seal DIP | H4X |
| Frit Seal DIP | H1F |
| Ceramic Flatpack | H6W |

Pinout



Functional Diagram



Specifications CD4099BMS

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) -0.5V to +20V
 (Voltage Referenced to VSS Terminals)
 Input Voltage Range, All Inputs -0.5V to VDD +0.5V
 DC Input Current, Any One Input ±10mA
 Operating Temperature Range -55°C to +125°C
 Package Types D, F, K, H
 Storage Temperature Range (TSTG) -65°C to +150°C
 Lead Temperature (During Soldering) +265°C
 At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for
 10s Maximum

Reliability Information

Thermal Resistance θ_{ja} θ_{jc}
 Ceramic DIP and FRIT Package 80°C/W 20°C/W
 Flatpack Package 70°C/W 20°C/W
 Maximum Package Power Dissipation (PD) at +125°C
 For TA = -55°C to +100°C (Package Type D, F, K) 500mW
 For TA = +100°C to +125°C (Package Type D, F, K) Derate
 Linearity at 12mW/°C to 200mW
 Device Dissipation per Output Transistor 100mW
 For TA = Full Package Temperature Range (All Package Types)
 Junction Temperature +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

| PARAMETER | SYMBOL | CONDITIONS (NOTE 1) | | GROUP A SUBGROUPS | TEMPERATURE | LIMITS | | UNITS |
|--------------------------------|--------|---------------------------------------|-----------|----------------------|----------------------|----------------|----------------|-------|
| | | | | | | MIN | MAX | |
| Supply Current | IDD | VDD = 20V, VIN = VDD or GND | | 1 | +25°C | - | 10 | μA |
| | | | | 2 | +125°C | - | 1000 | μA |
| | | VDD = 18V, VIN = VDD or GND | | 3 | -55°C | - | 10 | μA |
| Input Leakage Current | IIL | VIN = VDD or GND | VDD = 20 | 1 | +25°C | -100 | - | nA |
| | | | VDD = 18V | 2 | +125°C | -1000 | - | nA |
| | | | | 3 | -55°C | -100 | - | nA |
| Input Leakage Current | IIH | VIN = VDD or GND | VDD = 20 | 1 | +25°C | - | 100 | nA |
| | | | VDD = 18V | 2 | +125°C | - | 1000 | nA |
| | | | | 3 | -55°C | - | 100 | nA |
| Output Voltage | VOL15 | VDD = 15V, No Load | | 1, 2, 3 | +25°C, +125°C, -55°C | - | 50 | mV |
| Output Voltage | VOH15 | VDD = 15V, No Load (Note 3) | | 1, 2, 3 | +25°C, +125°C, -55°C | 14.95 | - | V |
| Output Current (Sink) | IOL5 | VDD = 5V, VOUT = 0.4V | | 1 | +25°C | 0.53 | - | mA |
| Output Current (Sink) | IOL10 | VDD = 10V, VOUT = 0.5V | | 1 | +25°C | 1.4 | - | mA |
| Output Current (Sink) | IOL15 | VDD = 15V, VOUT = 1.5V | | 1 | +25°C | 3.5 | - | mA |
| Output Current (Source) | IOH5A | VDD = 5V, VOUT = 4.6V | | 1 | +25°C | - | -0.53 | mA |
| Output Current (Source) | IOH5B | VDD = 5V, VOUT = 2.5V | | 1 | +25°C | - | -1.8 | mA |
| Output Current (Source) | IOH10 | VDD = 10V, VOUT = 9.5V | | 1 | +25°C | - | -1.4 | mA |
| Output Current (Source) | IOH15 | VDD = 15V, VOUT = 13.5V | | 1 | +25°C | - | -3.5 | mA |
| N Threshold Voltage | VNTH | VDD = 10V, ISS = -10μA | | 1 | +25°C | -2.8 | -0.7 | V |
| P Threshold Voltage | VPTH | VSS = 0V, IDD = 10μA | | 1 | +25°C | 0.7 | 2.8 | V |
| Functional | F | VDD = 2.8V, VIN = VDD or GND | | 7 | +25°C | VOH > VDD/2 | VOL < VDD/2 | V |
| | | VDD = 20V, VIN = VDD or GND | | 7 | +25°C | | | |
| | | VDD = 18V, VIN = VDD or GND | | 8A | +125°C | | | |
| | | VDD = 3V, VIN = VDD or GND | | 8B | -55°C | | | |
| Input Voltage Low (Note 2) | VIL | VDD = 5V, VOH > 4.5V, VOL < 0.5V | | 1, 2, 3 | +25°C, +125°C, -55°C | - | 1.5 | V |
| Input Voltage High (Note 2) | VIH | VDD = 5V, VOH > 4.5V, VOL < 0.5V | | 1, 2, 3 | +25°C, +125°C, -55°C | 3.5 | - | V |
| Input Voltage Low (Note 2) | VIL | VDD = 15V, VOH > 13.5V, VOL < 1.5V | | 1, 2, 3 | +25°C, +125°C, -55°C | - | 4 | V |
| Input Voltage High (Note 2) | VIH | VDD = 15V, VOH > 13.5V, VOL < 1.5V | | 1, 2, 3 | +25°C, +125°C, -55°C | 11 | - | V |

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
 2. Go/No Go test with limits applied to inputs.
 3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

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TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

| PARAMETER | SYMBOL | CONDITIONS (NOTE 1, 2) | GROUP A SUBGROUPS | TEMPERATURE | LIMITS | | UNITS |
|--|----------------|----------------------------|----------------------|---------------|--------|-----|-------|
| | | | | | MIN | MAX | |
| Propagation Delay Data to Output | TPHL1 TPLH1 | VDD = 5V, VIN = VDD or GND | 9 | +25°C | - | 400 | ns |
| | | | 10, 11 | +125°C, -55°C | - | 540 | ns |
| Propagation Delay Write Disable to Output | TPHL2 TPLH2 | VDD = 5V, VIN = VDD or GND | 9 | +25°C | - | 400 | ns |
| | | | 10, 11 | +125°C, -55°C | - | 540 | ns |
| Propagation Delay Reset to Output | TPHL3 | VDD = 5V, VIN = VDD or GND | 9 | +25°C | - | 350 | ns |
| | | | 10, 11 | +125°C, -55°C | - | 473 | ns |
| Propagation Delay Address to Output | TPHL4 TPLH4 | VDD = 5V, VIN = VDD or GND | 9 | +25°C | - | 450 | ns |
| | | | 10, 11 | +125°C, -55°C | - | 608 | ns |
| Transition Time | TTHL TTLH | VDD = 5V, VIN = VDD or GND | 9 | +25°C | - | 200 | ns |
| | | | 10, 11 | +125°C, -55°C | - | 270 | ns |

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

| PARAMETER | SYMBOL | CONDITIONS | NOTES | TEMPERATURE | LIMITS | | UNITS |
|-------------------------|--------|-----------------------------|-------|-------------------------|--------|-------|-------|
| | | | | | MIN | MAX | |
| Supply Current | IDD | VDD = 5V, VIN = VDD or GND | 1, 2 | -55°C, +25°C | - | 5 | µA |
| | | | | +125°C | - | 150 | µA |
| | | VDD = 10V, VIN = VDD or GND | 1, 2 | -55°C, +25°C | - | 10 | µA |
| | | | | +125°C | - | 300 | µA |
| | | VDD = 15V, VIN = VDD or GND | 1, 2 | -55°C, +25°C | - | 10 | µA |
| | | | | +125°C | - | 600 | µA |
| Output Voltage | VOL | VDD = 5V, No Load | 1, 2 | +25°C, +125°C, -55°C | - | 50 | mV |
| Output Voltage | VOL | VDD = 10V, No Load | 1, 2 | +25°C, +125°C, -55°C | - | 50 | mV |
| Output Voltage | VOH | VDD = 5V, No Load | 1, 2 | +25°C, +125°C, -55°C | 4.95 | - | V |
| Output Voltage | VOH | VDD = 10V, No Load | 1, 2 | +25°C, +125°C, -55°C | 9.95 | - | V |
| Output Current (Sink) | IOL5 | VDD = 5V, VOUT = 0.4V | 1, 2 | +125°C | 0.36 | - | mA |
| | | | | -55°C | 0.64 | - | mA |
| Output Current (Sink) | IOL10 | VDD = 10V, VOUT = 0.5V | 1, 2 | +125°C | 0.9 | - | mA |
| | | | | -55°C | 1.6 | - | mA |
| Output Current (Sink) | IOL15 | VDD = 15V, VOUT = 1.5V | 1, 2 | +125°C | 2.4 | - | mA |
| | | | | -55°C | 4.2 | - | mA |
| Output Current (Source) | IOH5A | VDD = 5V, VOUT = 4.6V | 1, 2 | +125°C | - | -0.36 | mA |
| | | | | -55°C | - | -0.64 | mA |
| Output Current (Source) | IOH5B | VDD = 5V, VOUT = 2.5V | 1, 2 | +125°C | - | -1.15 | mA |
| | | | | -55°C | - | -2.0 | mA |
| Output Current (Source) | IOH10 | VDD = 10V, VOUT = 9.5V | 1, 2 | +125°C | - | -0.9 | mA |
| | | | | -55°C | - | -1.6 | mA |

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TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

| PARAMETER | SYMBOL | CONDITIONS | NOTES | TEMPERATURE | LIMITS | | UNITS |
|---|----------------|-------------------------------|---------|----------------------|--------|------|-------|
| | | | | | MIN | MAX | |
| Output Current (Source) | IOH15 | VDD = 15V, VOUT = 13.5V | 1, 2 | +125°C | - | -2.4 | mA |
| | | | | -55°C | - | -4.2 | mA |
| Input Voltage Low | VIL | VDD = 10V, VOH > 9V, VOL < 1V | 1, 2 | +25°C, +125°C, -55°C | - | 3 | V |
| Input Voltage High | VIH | VDD = 10V, VOH > 9V, VOL < 1V | 1, 2 | +25°C, +125°C, -55°C | +7 | - | V |
| Propagation Delay Data to Output | TPHL1 TPLH1 | VDD = 10V | 1, 2, 3 | +25°C | - | 150 | ns |
| | | VDD = 15V | 1, 2, 3 | +25°C | - | 100 | ns |
| Propagation Delay Write Disable to Output | TPHL2 TPLH2 | VDD = 10V | 1, 2, 3 | +25°C | - | 160 | ns |
| | | VDD = 15V | 1, 2, 3 | +25°C | - | 120 | ns |
| Propagation Delay Reset to Output | TPHL3 | VDD = 10V | 1, 2, 3 | +25°C | - | 160 | ns |
| | | VDD = 15V | 1, 2, 3 | +25°C | - | 130 | ns |
| Propagation Delay Address to Output | TPHL4 TPLH4 | VDD = 10V | 1, 2, 3 | +25°C | - | 200 | ns |
| | | VDD = 15V | 1, 2, 3 | +25°C | - | 150 | ns |
| Transition Time | TTHL TTLH | VDD = 10V | 1, 2, 3 | +25°C | - | 100 | ns |
| | | VDD = 15V | 1, 2, 3 | +25°C | - | 80 | ns |
| Minimum Hold time Data to Write Disable | TH | VDD = 5V | 1, 2, 3 | +25°C | - | 150 | MHz |
| | | VDD = 10V | 1, 2, 3 | +25°C | - | 75 | MHz |
| | | VDD = 15V | 1, 2, 3 | +25°C | - | 50 | MHz |
| Minimum Data Setup Time Data to Write Disable | TS | VDD = 5V | 1, 2, 3 | +25°C | - | 100 | ns |
| | | VDD = 10V | 1, 2, 3 | +25°C | - | 50 | ns |
| | | VDD = 15V | 1, 2, 3 | +25°C | - | 35 | ns |
| Minimum Pulse Width Data | TW | VDD = 5V | 1, 2, 3 | +25°C | - | 200 | ns |
| | | VDD = 10V | 1, 2, 3 | +25°C | - | 100 | ns |
| | | VDD = 15V | 1, 2, 3 | +25°C | - | 80 | ns |
| Minimum Pulse Width Address | TW | VDD = 5V | 1, 2, 3 | +25°C | - | 400 | ns |
| | | VDD = 10V | 1, 2, 3 | +25°C | - | 200 | ns |
| | | VDD = 15V | 1, 2, 3 | +25°C | - | 125 | ns |
| Minimum Pulse Width Reset | TW | VDD = 5V | 1, 2, 3 | +25°C | - | 150 | ns |
| | | VDD = 10V | 1, 2, 3 | +25°C | - | 75 | ns |
| | | VDD = 15V | 1, 2, 3 | +25°C | - | 50 | ns |
| Input Capacitance | CIN | Any inputs | 1, 2 | +25°C | - | 7.5 | pF |

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

| PARAMETER | SYMBOL | CONDITIONS | NOTES | TEMPERATURE | LIMITS | | UNITS |
|---------------------|--------|-----------------------------|-------|-------------|--------|------|-------|
| | | | | | MIN | MAX | |
| Supply Current | IDD | VDD = 20V, VIN = VDD or GND | 1, 4 | +25°C | - | 25 | μA |
| N Threshold Voltage | VNTH | VDD = 10V, ISS = -10μA | 1, 4 | +25°C | -2.8 | -0.2 | V |

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TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

| PARAMETER | SYMBOL | CONDITIONS | NOTES | TEMPERATURE | LIMITS | | UNITS |
|---------------------------|-----------------|------------------------------|------------|-------------|-------------|--------------------|-------|
| | | | | | MIN | MAX | |
| N Threshold Voltage Delta | ΔV_{TN} | VDD = 10V, ISS = -10 μ A | 1, 4 | +25°C | - | ± 1 | V |
| P Threshold Voltage | VTP | VSS = 0V, IDD = 10 μ A | 1, 4 | +25°C | 0.2 | 2.8 | V |
| P Threshold Voltage Delta | ΔV_{TP} | VSS = 0V, IDD = 10 μ A | 1, 4 | +25°C | - | ± 1 | V |
| Functional | F | VDD = 18V, VIN = VDD or GND | 1 | +25°C | VOH > VDD/2 | VOL < VDD/2 | V |
| | | VDD = 3V, VIN = VDD or GND | | | | | |
| Propagation Delay Time | TPHL TPLH | VDD = 5V | 1, 2, 3, 4 | +25°C | - | 1.35 x +25°C Limit | ns |

NOTES: 1. All voltages referenced to device GND. 2. CL = 50pF, RL = 200K, Input TR, TF < 20ns. 3. See Table 2 for +25°C limit. 4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

| PARAMETER | SYMBOL | DELTA LIMIT |
|-------------------------|--------|-------------------------------|
| Supply Current - MSI-2 | IDD | $\pm 1.0\mu$ A |
| Output Current (Sink) | IOL5 | $\pm 20\%$ x Pre-Test Reading |
| Output Current (Source) | IOH5A | $\pm 20\%$ x Pre-Test Reading |

TABLE 6. APPLICABLE SUBGROUPS

| CONFORMANCE GROUP | MIL-STD-883 METHOD | GROUP A SUBGROUPS | READ AND RECORD |
|-------------------------------|--------------------|---------------------------------------|------------------------------|
| Initial Test (Pre Burn-In) | 100% 5004 | 1, 7, 9 | IDD, IOL5, IOH5A |
| Interim Test 1 (Post Burn-In) | 100% 5004 | 1, 7, 9 | IDD, IOL5, IOH5A |
| Interim Test 2 (Post Burn-In) | 100% 5004 | 1, 7, 9 | IDD, IOL5, IOH5A |
| PDA (Note 1) | 100% 5004 | 1, 7, 9, Deltas | |
| Interim Test 3 (Post Burn-In) | 100% 5004 | 1, 7, 9 | IDD, IOL5, IOH5A |
| PDA (Note 1) | 100% 5004 | 1, 7, 9, Deltas | |
| Final Test | 100% 5004 | 2, 3, 8A, 8B, 10, 11 | |
| Group A | Sample 5005 | 1, 2, 3, 7, 8A, 8B, 9, 10, 11 | |
| Group B | Subgroup B-5 | 1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas | Subgroups 1, 2, 3, 9, 10, 11 |
| | Subgroup B-6 | 1, 7, 9 | |
| Group D | Sample 5005 | 1, 2, 3, 8A, 8B, 9 | Subgroups 1, 2 3 |

NOTE: 1. 5% Parametric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

| CONFORMANCE GROUPS | MIL-STD-883 METHOD | TEST | | READ AND RECORD | |
|--------------------|--------------------|-----------|------------|-----------------|------------|
| | | PRE-IRRAD | POST-IRRAD | PRE-IRRAD | POST-IRRAD |
| Group E Subgroup 2 | 5005 | 1, 7, 9 | Table 4 | 1, 9 | Table 4 |

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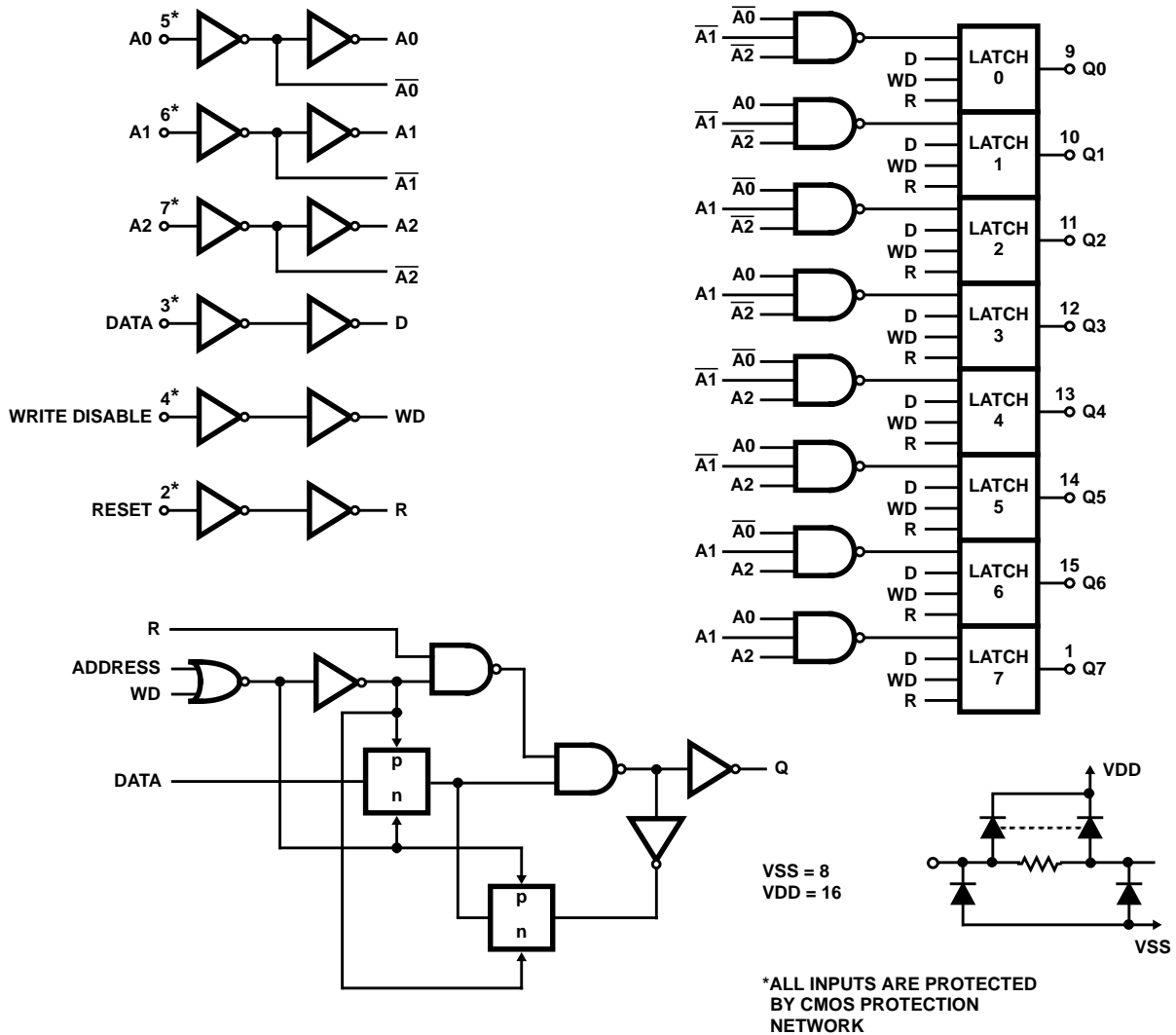
TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

| FUNCTION | OPEN | GROUND | VDD | 9V ± 0.5V | OSCILLATOR | |
|----------------------------|---------|--------|---------|-----------|------------|-------|
| | | | | | 50kHz | 25kHz |
| Static Burn-In 1 Note 1 | 1, 9-15 | 2-8 | 16 | | | |
| Static Burn-In 2 Note 1 | 1, 9-15 | 8 | 2-7, 16 | | | |
| Dynamic Burn-In Note 1 | - | 5-8 | 16 | 1, 9-15 | 2, 4 | 3 |
| Irradiation Note 2 | 1, 9-15 | 8 | 2-7, 16 | | | |

NOTES:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagram



CD4099BMS

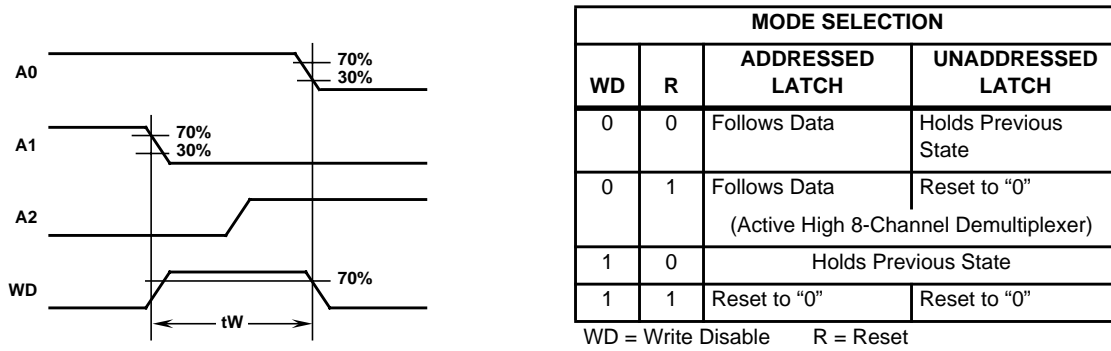


FIGURE 2. DEFINITION OF WRITE DISABLE ON TIME

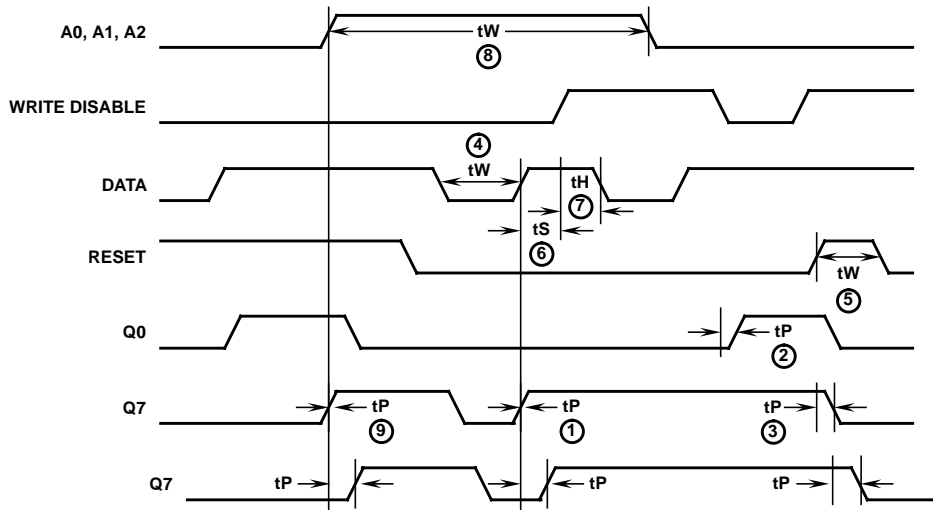


FIGURE 3. MASTER TIMING DIAGRAM

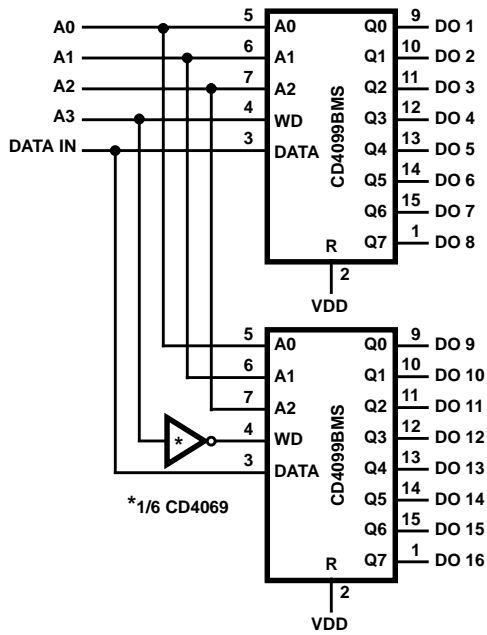


FIGURE 4. 1 OF 16 DECODER/DEMULPLEXER

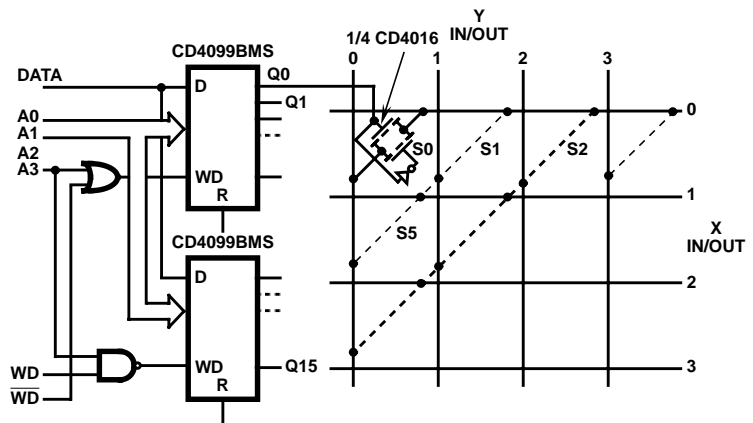


FIGURE 5. MULTIPLE SELECTION DECODING - 4 x 4 CROSSPOINT SWITCH

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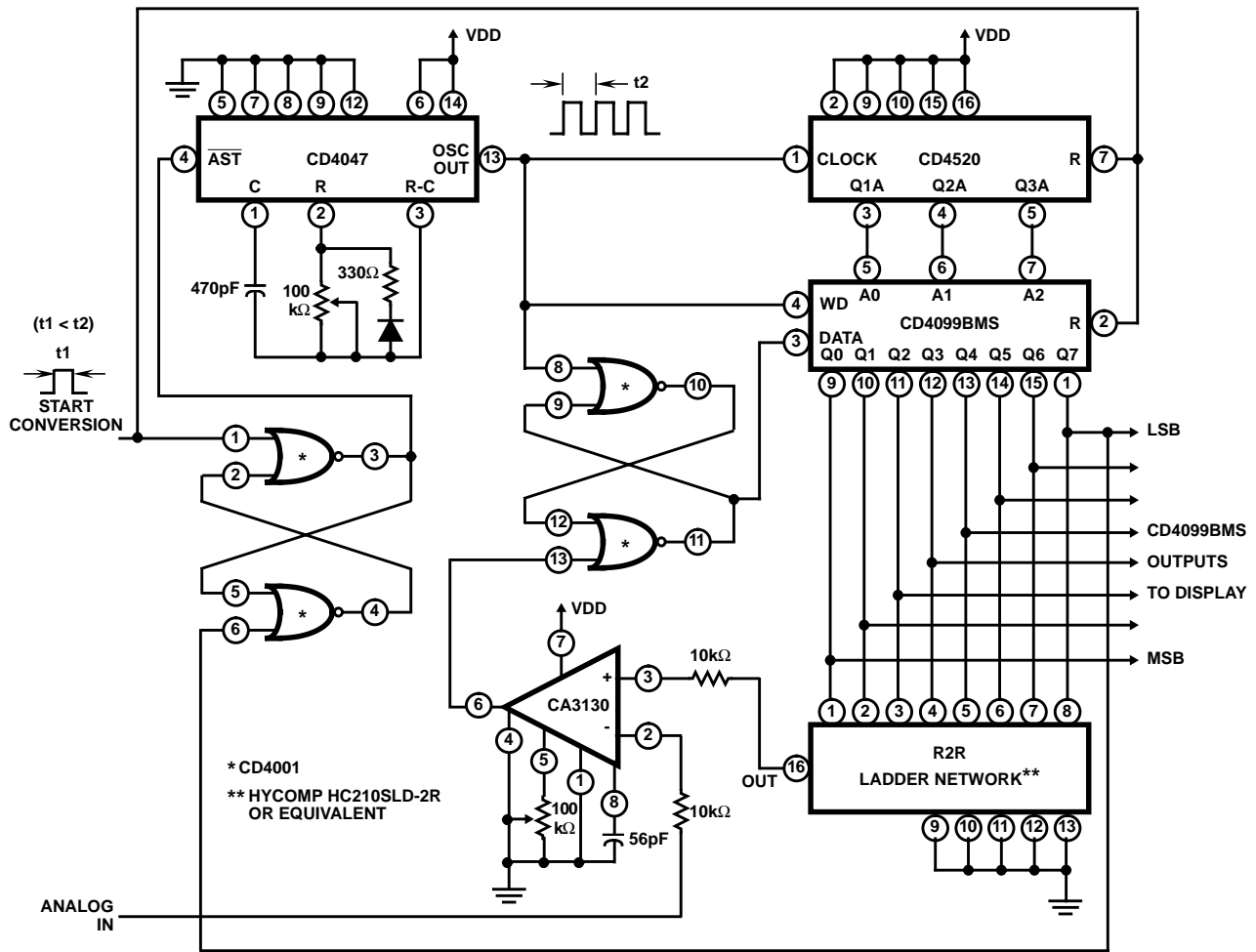


FIGURE 6. A/D CONVERTER

Typical Performance Characteristics

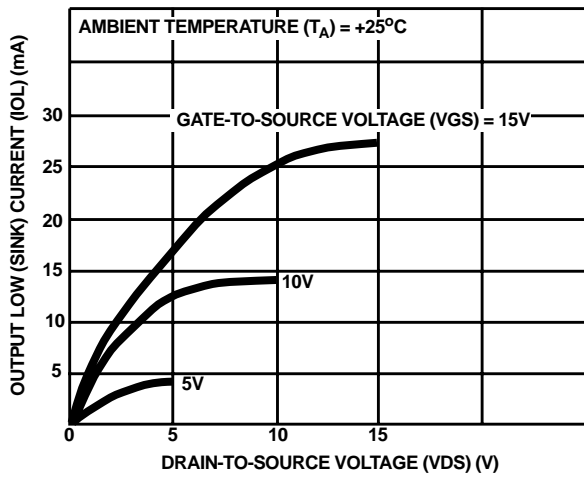


FIGURE 7. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

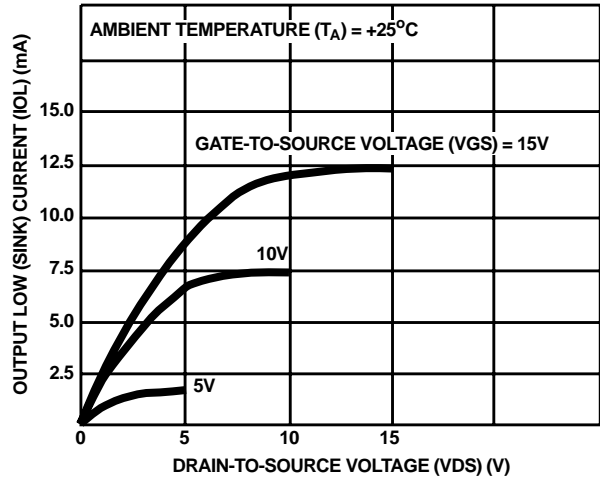


FIGURE 8. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

Typical Performance Characteristics (Continued)

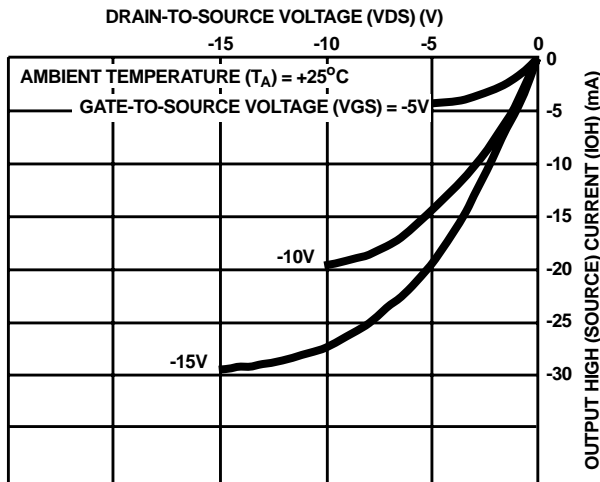


FIGURE 9. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

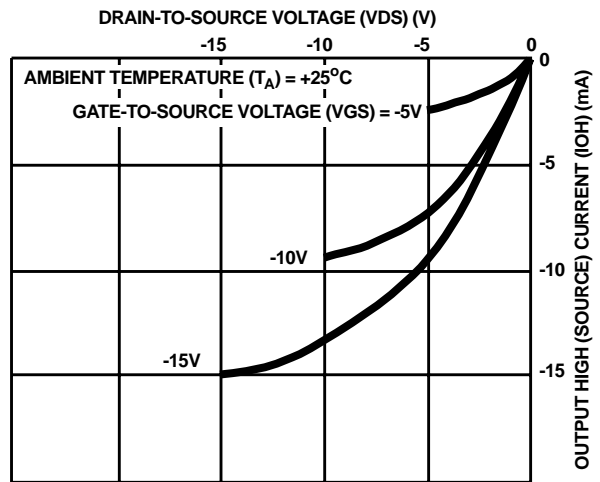


FIGURE 10. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

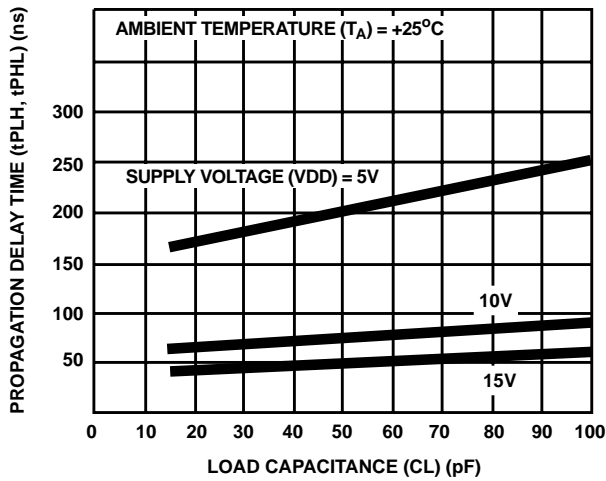


FIGURE 11. TYPICAL PROPAGATION DELAY TIME (DATA TO Qn) vs LOAD CAPACITANCE

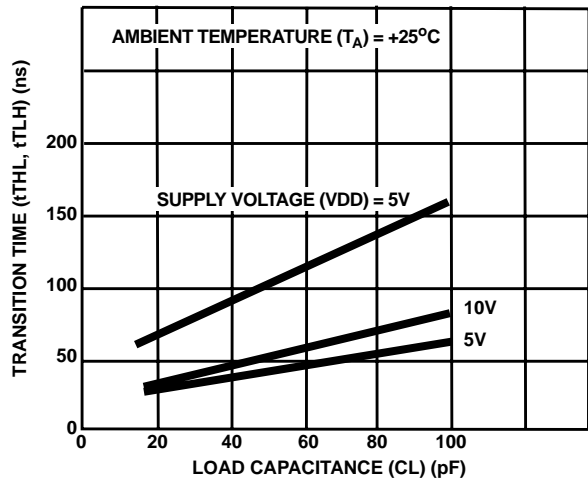


FIGURE 12. TYPICAL TRANSITION TIME vs LOAD CAPACITANCE

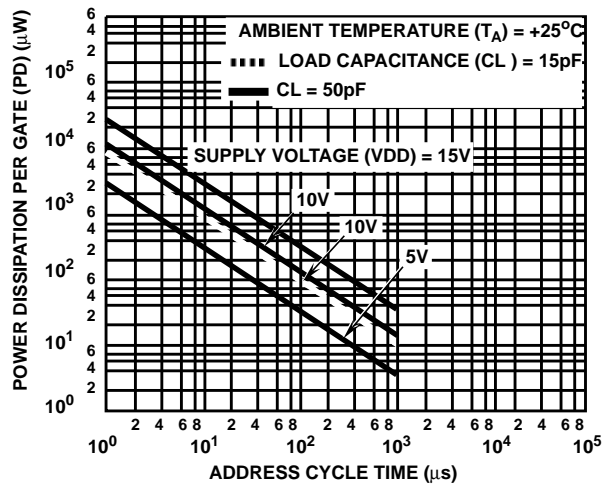
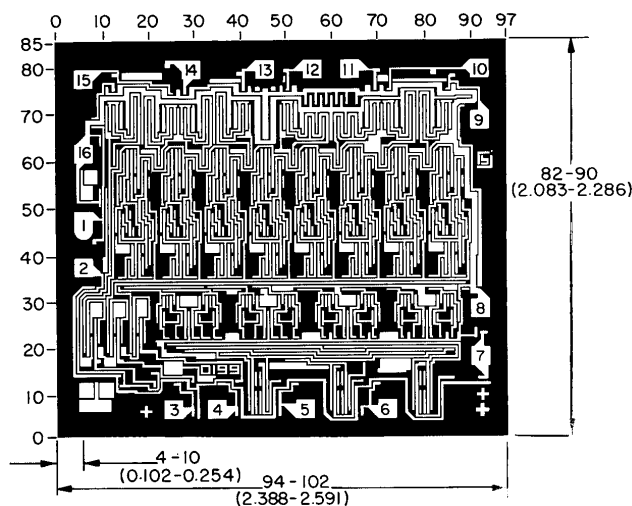


FIGURE 13. TYPICAL DYNAMIC POWER DISSIPATION vs ADDRESS CYCLE TIME

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Chip Dimensions and Pad Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: $11\text{k}\text{\AA} - 14\text{k}\text{\AA}$, AL.

PASSIVATION: $10.4\text{k}\text{\AA} - 15.6\text{k}\text{\AA}$, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

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