NEC

MOS FIELD EFFECT TRANSISTOR

μPA1727

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

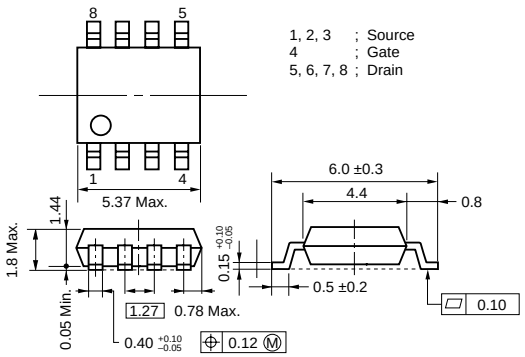
DESCRIPTION

The μPA1727 is N-Channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

- Single chip type
- Low On-state Resistance
- ★ $R_{DS(on)1}$ = 14 mΩ (TYP.) (V_{GS} = 10 V, I_D = 5.0 A)
- ★ $R_{DS(on)2}$ = 17 mΩ (TYP.) (V_{GS} = 4.5 V, I_D = 5.0 A)
- ★ $R_{DS(on)3}$ = 19 mΩ (TYP.) (V_{GS} = 4.0 V, I_D = 5.0 A)
- ★ Low C_{iss} : C_{iss} = 2400 pF (TYP.)
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

PACKAGE DRAWING (Unit : mm)



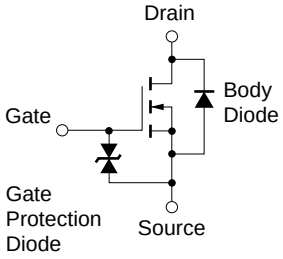
ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA1727	Power SOP8

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, All terminals are connected.)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	60	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC)	$I_{D(DC)}$	±10	A
Drain Current (Pulse) Note1	$I_{D(pulse)}$	±40	A
Total Power Dissipation (T_A = 25 °C) Note2	P_T	2.0	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to + 150	°C
Single Avalanche Current Note3	I_{AS}	10	A
★ Single Avalanche Energy Note3	E_{AS}	200	mJ

EQUIVALENT CIRCUIT



Notes 1. PW ≤ 10 μs, Duty cycle ≤ 1 %

★ **2.** Mounted on ceramic substrate of 1200 mm^2 x 2.2 mm

3. Starting T_{ch} = 25 °C, R_G = 25 Ω, V_{GS} = 20 V → 0 V

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage Exceeding the rated voltage may be applied to this device.

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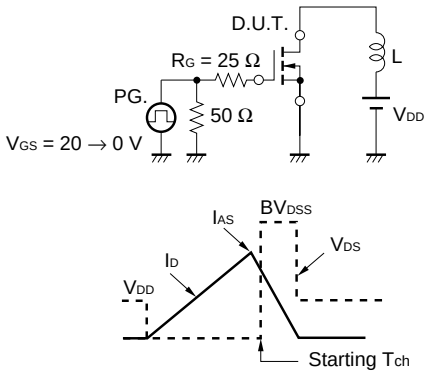
The mark ★ shows major revised points.

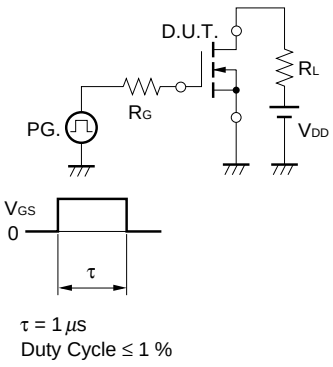
★ ELECTRICAL CHARACTERISTICS (T_A = 25 °C, All terminals are connected.)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 5.0 A		14	19	mΩ
	$R_{DS(on)2}$	V_{GS} = 4.5 V, I_D = 5.0 A		17	22	mΩ
	$R_{DS(on)3}$	V_{GS} = 4.0 V, I_D = 5.0 A		19	25	mΩ
Gate to Source Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = 10 V, I_D = 5.0 A	8.0	14		S
Drain Leakage Current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V			10	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±10	μA
Input Capacitance	C_{iss}	V_{DS} = 10 V		2400		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		400		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		200		pF
Turn-on Delay Time	$t_{d(on)}$	I_D = 5.0 A		24		ns
Rise Time	t_r	$V_{GS(on)}$ = 10 V		120		ns
Turn-off Delay Time	$t_{d(off)}$	V_{DD} = 30 V		120		ns
Fall Time	t_f	R_G = 10 Ω		71		ns
Total Gate Charge	Q_G	I_D = 10 A		45		nC
Gate to Source Charge	Q_{GS}	V_{DD} = 48 V		5.9		nC
Gate to Drain Charge	Q_{GD}	V_{GS} = 10 V		13		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	I_F = 10 A, V_{GS} = 0 V		0.8		V
Reverse Recovery Time	t_{rr}	I_F = 10 A, V_{GS} = 0 V		45		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100A/μs		84		nC

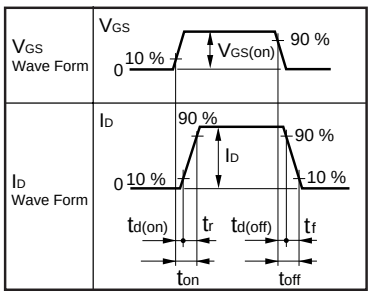
TEST CIRCUIT 1 AVALANCHE CAPABILITY



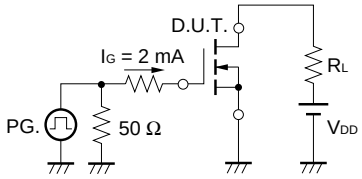
TEST CIRCUIT 2 SWITCHING TIME



τ = 1 μs
Duty Cycle ≤ 1 %



TEST CIRCUIT 3 GATE CHARGE



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