Microcomputer Components

8-bit CMOS Microcontroller

C505L

Data Sheet 06.99

C505L Data Sheet **Revision History:**		**Original Version: 06.99**
Previous Releases:		
Page (new version)	Page (prev. version)	Subjects (changes since last revision)
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8-Bit CMOS Microcontroller C505L

Advance Information

Features

- Fully compatible with the standard 8051 microcontroller
- Superset of the 8051 architecture with 8 datapointers
- Up to 20 MHz operating frequency
  - 375 ns instruction cycle time @ 16 MHz
  - 300 ns instruction cycle time @ 20 MHz (50% duty cycle)
- Program Memory
  - 32K bytes of on-chip OTP memory
  - Externally expandable up to 64 Kbytes
- 256-byte on-chip RAM
- 256-byte on-chip XRAM
- Five 8-bit and one 6-bit digital I/O ports (Port 5 with 6 bits only)
  - Port 1 with mixed analog/digital I/O capability
  - Port 3 with 2 LCD output lines as secondary functions
  - Port 4 and 5 with 8 and 6 LCD output lines respectively as secondary functions

(more features are on next page)

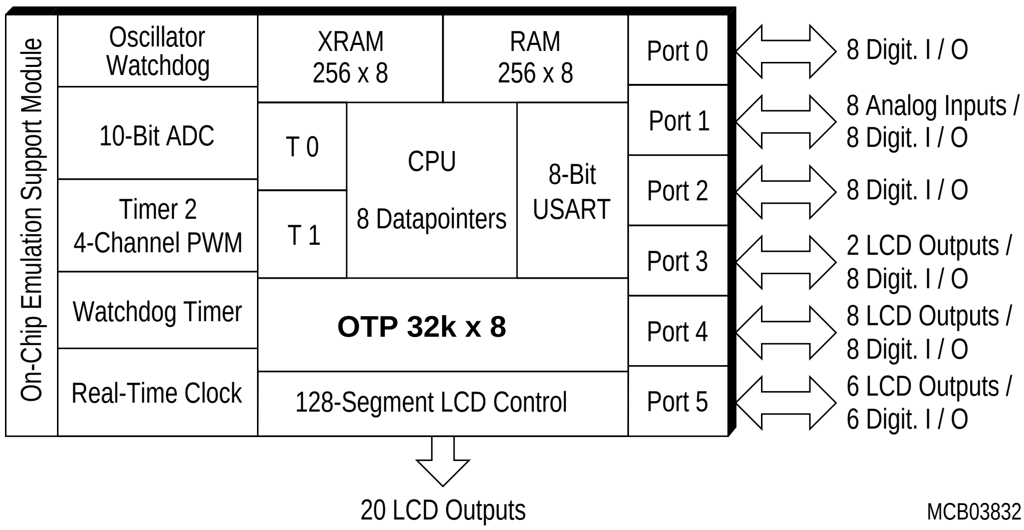


Figure 1
C505L Functional Units

Features (cont'd):

- Three 16-bit timers/counters
  – Timer 0 / 1 (C501 compatible)
  – Timer 2 with 4 channels for 16-bit capture/compare operation
- 128-segment LCD Controller
  – 1/4 duty cycle drive
  – 4 row and 32 column outputs
  – On-chip programmable reference voltage generation
  – 20 dedicated LCD output lines (4 rows + 16 columns)
- Real-Time Clock
  – 47-bit digital clock counter
  – Input frequency of 32.768 KHz required
  – Operates in a special power down mode
- Full duplex serial interface with programmable baudrate generator (USART)
- 10-bit A/D Converter with 8 multiplexed inputs
- Twelve interrupt sources with four priority levels
- On-chip emulation support logic (Enhanced Hooks™ [1)])
- Programmable 15-bit Watchdog Timer
- Oscillator Watchdog
- Fast power-on reset
- Power-saving modes
  – Slow-down mode
  – Idle mode (can be combined with slow-down mode)
  – 3 special power down modes
  – Software power-down mode with wake up capability through $\overline{\text{INT0}}$ pin or Real-Time Clock
- P-MQFP-80 package
- Temperature ranges: SAB-C505L T_A = 0 to 70 °C
  SAF-C505L T_A = – 40 to 85 °C
  SAK-C505L T_A = – 40 to 125 °C (max. operating frequency: 12 MHz)

Ordering Information

The ordering code for Infineon Technologies' microcontrollers provides an exact reference to the required product. This ordering code identifies:

- the derivative itself, i.e. its function set
- the specified temperature rage
- the package and the type of delivery

For the available ordering codes for the C505L please refer to the "**Product Information Microcontrollers**", which summarizes all available microcontroller variants.

1 "Enhanced Hooks Technology" is a trademark and patent of Metalink Corporation licensed to Infineon Technologies.

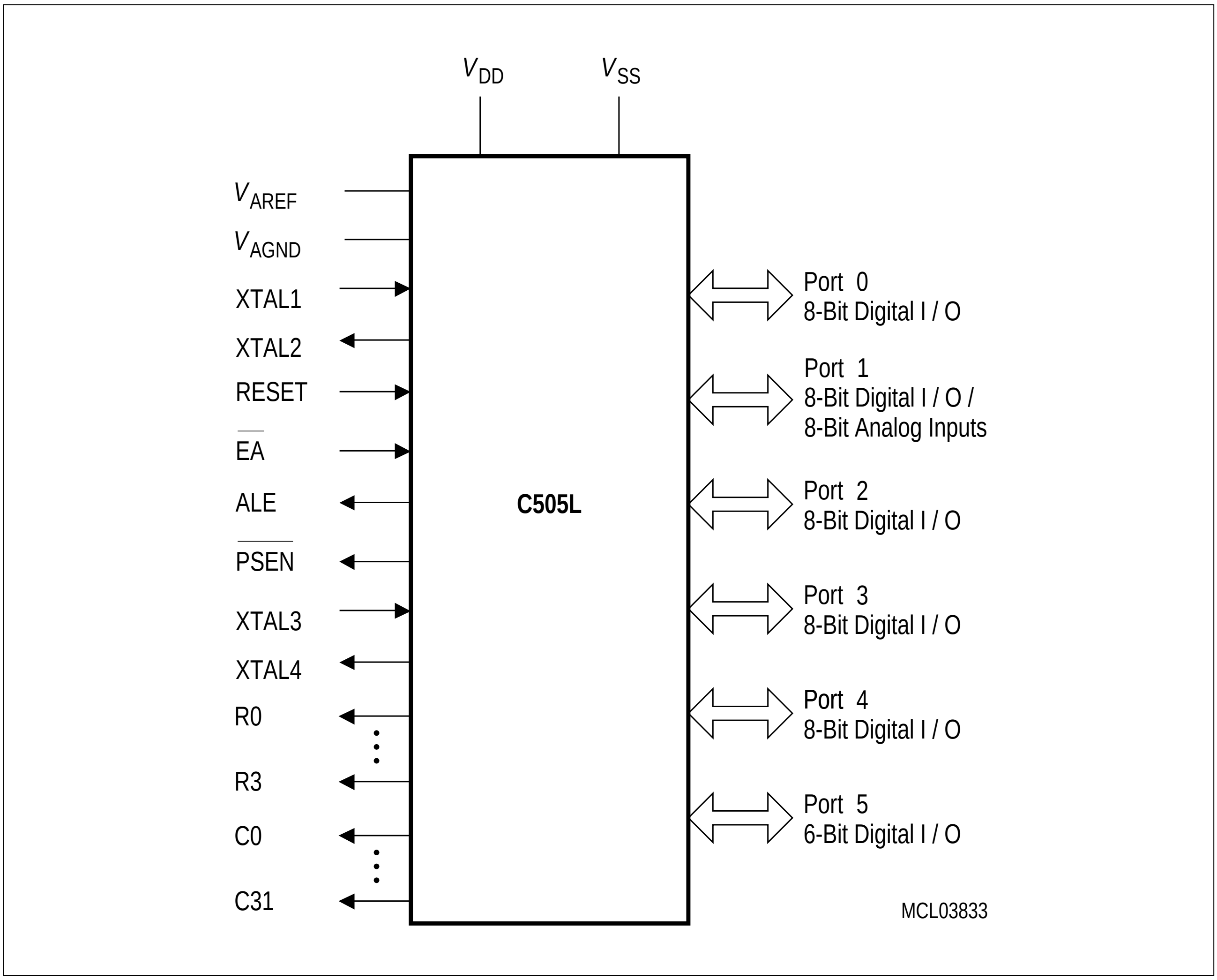


Figure 2
Logic Symbol

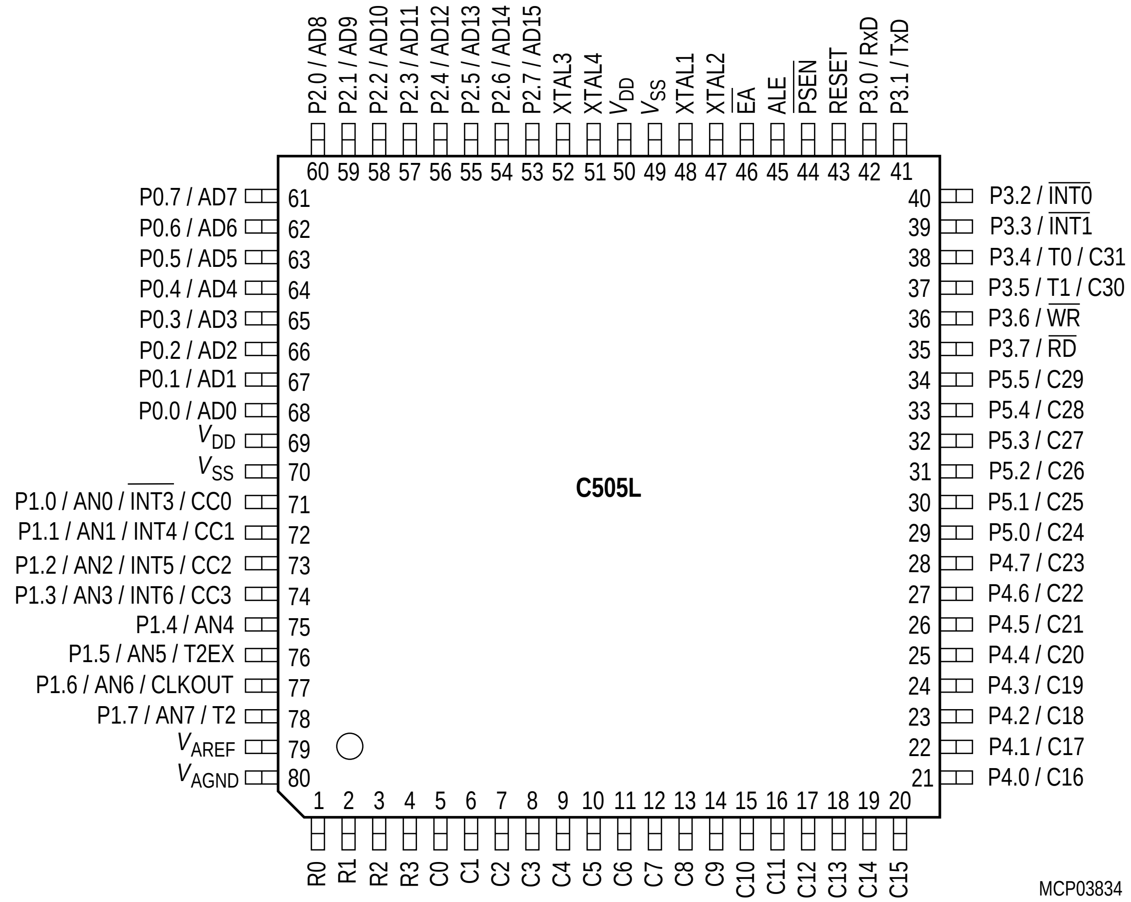


Figure 3
Pin Configuration P-MQFP-80 Package (top view)

Table 1
Pin Definitions and Functions

Symbol	Pin Number	I/O*)	Function
R0-R3	1-4	O	**LCD Row Outputs** Output of LCD controller row lines. These pins are driven by the LCD controller and drive the row input lines of the external LCD display. Enabling the LCD Controller makes these pins available for LCD output levels.
	1		R0 LCD row output 0
	2		R1 LCD row output 1
	3		R2 LCD row output 2
	4		R3 LCD row output 3 These pins should not be used for input.
C0-C15	5-20	O	**LCD Column Outputs** Output of LCD controller column lines 0 to 15. These pins are driven by the LCD controller and drive the column input lines of the external LCD display. Enabling the LCD controller makes these pins available for LCD output levels.
	5		C0 LCD column output 0
	6		C1 LCD column output 1
	7		C2 LCD column output 2
	8		C3 VCCLCD column output 3
	9		C4 LCD column output 4
	10		C5 LCD column output 5
	11		C6 LCD column output 6
	12		C7 LCD column output 7
	13		C8 LCD column output 8
	14		C9 LCD column output 9
	15		C10 LCD column output 10
	16		C11 LCD column output 11
	17		C12 LCD column output 12
	18		C13 LCD column output 13
	19		C14 LCD column output 14
	20		C15 LCD column output 15 These pins should not be used for input.

*) I = Input
O = Output

Table 1
Pin Definitions and Functions (cont'd)

Symbol	Pin Number	I/O*)	Function
P4.0-P4.7	21-28	I/O	**Port 4** is a 8-bit quasi-bidirectional port with internal pull-up arrangement. Port 4 pins that have a 1 written to them are pulled high by the internal pull-up transistors and in that state can be used as inputs. As inputs, port 4 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup transistors. Port 4 pins can also be configured as LCD column outputs. The secondary functions are assigned to the pins of port 4 as follows:
	21		P4.0 / C16 LCD column output 16
	22		P4.1 / C17 LCD column output 17
	23		P4.2 / C18 LCD column output 18
	24		P4.3 / C19 LCD column output 19
	25		P4.4 / C20 LCD column output 20
	26		P4.5 / C21 LCD column output 21
	27		P4.6 / C22 LCD column output 22
	28		P4.7 / C23 LCD column output 23 These pins should not be used for input when configured as LCD output pins.
P5.0-P5.5	29-34	I/O	**Port 5** is a 6-bit quasi-bidirectional port with internal pull-up arrangement. Port 5 pins that have a 1 written to them are pulled high by internal pull-up transistors and in that state can be used as inputs. As inputs, port 5 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup transistors. Port 5 pins can also be configured as LCD column outputs. The secondary functions are assigned to the pins of port 5 as follows:
	29		P5.0 / C24 LCD column output 24
	30		P5.1 / C25 LCD column output 25
	31		P5.2 / C26 LCD column output 26
	32		P5.3 / C27 LCD column output 27
	33		P5.4 / C28 LCD column output 28
	34		P5.5 / C29 LCD column output 29 These pins should not be used for input when configured as LCD output pins.

*) I = Input
O = Output

Table 1
Pin Definitions and Functions (cont'd)

Symbol	Pin Number	I/O*)	Function
P3.7-P3.0	35-42	I/O	**Port 3** is an 8-bit quasi-bidirectional port with internal pull-up arrangement. Port 3 pins that have a 1 written to them are pulled high by the internal pull-up transistors and in that state can be used as inputs. As inputs, port 3 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup transistors. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate (except for TxD and $\overline{WR}$). P3.4 and P3.5 can also be configured as LCD column outputs C31 and C30 respectively. These pins should not be used for input when configured as LCD output pins. The secondary functions are assigned to the pins of port 3 as follows:
	42		P3.0 / RxD — Receiver data input (asynch.) or data input/output (synch.) of serial interface
	41		P3.1 / TxD — Transmitter data output (asynch.) or clock output (synch.) of serial interface
	40		P3.2 / $\overline{INT0}$ — External interrupt 0 input / timer 0 gate control input
	39		P3.3 / $\overline{INT1}$ — External interrupt 1 input / timer 1 gate control input
	38		P3.4 / T0 / C31 — Timer 0 counter input / LCD column 31 output
	37		P3.5 / T1 / C30 — Timer 1 counter input / LCD column 30 output
	36		P3.6 / $\overline{WR}$ — $\overline{WR}$ control output; latches the data byte from port 0 into the external data memory
	35		P3.7 / $\overline{RD}$ — $\overline{RD}$ control output; enables the external data memory

*) I = Input
O = Output

Table 1
Pin Definitions and Functions (cont'd)

Symbol	Pin Number	I/O*)	Function
RESET	43	I	**RESET** A high level on this pin for two machine cycles while the oscillator is running resets the device. An internal diffused resistor to V_{SS} permits power-on reset using only an external capacitor to V_{DD}.
$\overline{\text{PSEN}}$	44	O	The **Program Store Enable** output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every three oscillator periods except during external data memory accesses. Remains high during internal program execution. This pin should not be driven during reset operation.
ALE	45	O	The **Address Latch Enable** output is used for latching the low-byte of the address into external memory during normal operation. It is activated every three oscillator periods except during an external data memory access. When instructions are executed from internal program memory ($\overline{\text{EA}}$ = 1), the ALE generation can be disabled by bit EALE in SFR SYSCON. This pin should not be driven during reset operation.
$\overline{\text{EA}}$	46	I	**External Access Enable** This pin must be held at high level. Instructions are fetched from the internal OTP memory when the PC is less than 8000_H. Instructions are fetched from external program memory, when the PC is greater than $7FFF_H$. This pin must not be held at low level.

*) I = Input
O = Output

Table 1
Pin Definitions and Functions (cont'd)

Symbol	Pin Number	I/O*)	Function
XTAL2	47	O	**XTAL2** Output of the inverting oscillator amplifier.
XTAL1	48	I	**XTAL1** Input to the inverting oscillator amplifier and input to the internal clock generator circuits. To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 is left unconnected. To operate above a frequency of 16 MHz, a duty cycle of 50% should be maintained. Minimum and maximum high and low times as well as rise/fall times specified in the AC characteristics (refer to data Sheet) must be observed.
XTAL4	51	O	**XTAL4** Output of the inverting real-time clock oscillator amplifier.
XTAL3	52	I	**XTAL3** Input to the inverting real-time clock oscillator amplifier. To drive the real-time clock from an external clock source, XTAL3 should be driven, while XTAL4 is left unconnected. Minimum and maximum high and low times as well as rise/fall times specified in the AC characteristics (refer to Data sheet) must be observed.

*) I = Input
O = Output

Table 1
Pin Definitions and Functions (cont'd)

Symbol	Pin Number	I/O*)	Function
P2.7-P2.0	53-60	I/O	**Port 2** is a an 8-bit quasi-bidirectional I/O port with internal pullup resistors. Port 2 pins that have a 1 written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 2 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullup transistors when issuing 1s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 issues the contents of the P2 special function register and uses only the internal pullup resistors.
P0.7-P0.0	61-68	I/O	**Port 0** is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have a 1 written to them float, and in that state can be used as high-impendance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program or data memory. In this application it uses strong internal pullup transistors when issuing 1s.

*) I = Input
O = Output

Table 1
Pin Definitions and Functions (cont'd)

Symbol	Pin Number	I/O*)	Function
P1.0-P1.7	71-78	I/O	**Port 1** is an 8-bit quasi-bidirectional port with internal pull-up arrangement. Port 1 pins can be used for digital input/output or as analog inputs to the A/D converter. Port 1 pins that have a 1 written to them are pulled high by internal pull-up transistors and in that state can be used as inputs. As inputs, port 1 pins being pulled low externally will source current (I_{IL}, in the DC characteristics) because of the internal pullup transistors. Port 1 pins are assigned to be used as analog inputs via the register P1ANA. As secondary digital functions, port 1 contains the interrupt, timer, clock, capture and compare pins. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate (except for compare functions). The secondary functions are assigned to the pins of port 1 as follows:
	71		P1.0 / AN0 / $\overline{\text{INT3}}$ / CC0 Analog input channel 0 interrupt 3 input / capture/compare channel 0 I/O
	72		P1.1 / AN1 / INT4 / CC1 Analog input channel 1/ interrupt 4 input / capture/compare channel 1 I/O
	73		P1.2 / AN2 / INT5 / CC2 Analog input channel 2 / interrupt 5 input / capture/compare channel 2 I/O
	74		P1.3 / AN3 / INT6 / CC3 Analog input channel 3 interrupt 6 input / capture/compare channel 3 I/O
	75		P1.4 / AN4 Analog input channel 4
	76		P1.5 / AN5 / T2EX Analog input channel 5 / timer 2 external reload / trigger input
	77		P1.6 / AN6 / CLKOUT Analog input channel 6 / system clock output
	78		P1.7 / AN7 / T2 Analog input channel 7 / timer/counter 2 input

*) I = Input
O = Output

Table 1
Pin Definitions and Functions (cont'd)

Symbol	Pin Number	I/O*)	Function
V_{AREF}	79	–	**Reference voltage** for the A/D converter.
V_{AGND}	80	–	**Reference ground** for the A/D converter.
V_{SS}	49, 70	–	**Ground** (0 V)
V_{DD}	50, 69	–	**Power Supply** (+ 5 V)

*) I = Input
O = Output

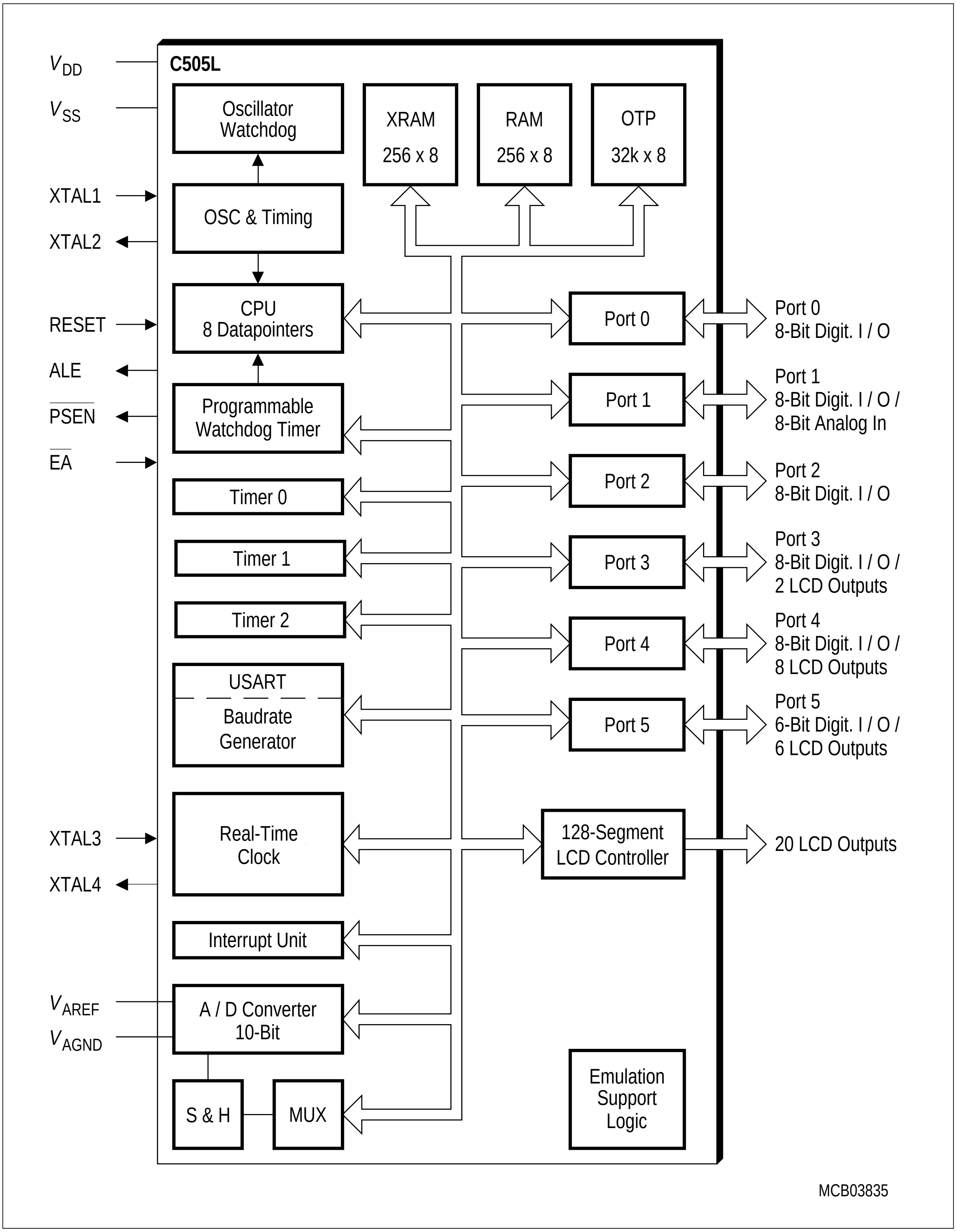


Figure 4
Block Diagram of the C505L

CPU

The C505L is efficient both as a controller and as an arithmetic processor. It has extensive facilities for binary and BCD arithmetic and excels in its bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44% one-byte, 41% two-byte, and 15% three-byte instructions. With a 16-MHz external clock, 58% of the instructions execute in 375 ns (20 MHz: 300 ns).

Special Function Register PSW (Address $D0_H$) **Reset Value: 00_H**

Bit No.	MSB						LSB	
	$D7_H$	$D6_H$	$D5_H$	$D4_H$	$D3_H$	$D2_H$	$D1_H$	$D0_H$	
$D0_H$	CY	AC	F0	RS1	RS0	OV	F1	P	PSW

Bit	Function
CY	Carry Flag Used by arithmetic instruction.
AC	Auxiliary Carry Flag Used by instructions which execute BCD operations.
F0	General Purpose Flag
RS1 RS0	Register Bank select control bits These bits are used to select one of the four register banks.
OV	Overflow Flag Used by arithmetic instruction.
F1	General Purpose Flag
P	Parity Flag Set/cleared by hardware after each instruction to indicate an odd/even number of “one” bits in the accumulator, i.e. even parity.

RS1	RS0	Function
0	0	Bank 0 selected, data address 00_H-07_H
0	1	Bank 1 selected, data address 08_H-$0F_H$
1	0	Bank 2 selected, data address 10_H-17_H
1	1	Bank 3 selected, data address 18_H-$1F_H$

Memory Organization

The C505L CPU manipulates operands in the following five address spaces:

- up to 64 Kbytes of program memory (32K on-chip OTP memory)
- up to 64 Kbytes of external data memory
- 256 bytes of internal data memory
- 256 bytes of internal XRAM data memory
- 20 bytes of LCD Controller registers
- 16 bytes of Real-Time Clock (RTC) registers
- A 128-byte Special Function Register (SFR) area

Figure 5 illustrates the memory address spaces of the C505L.

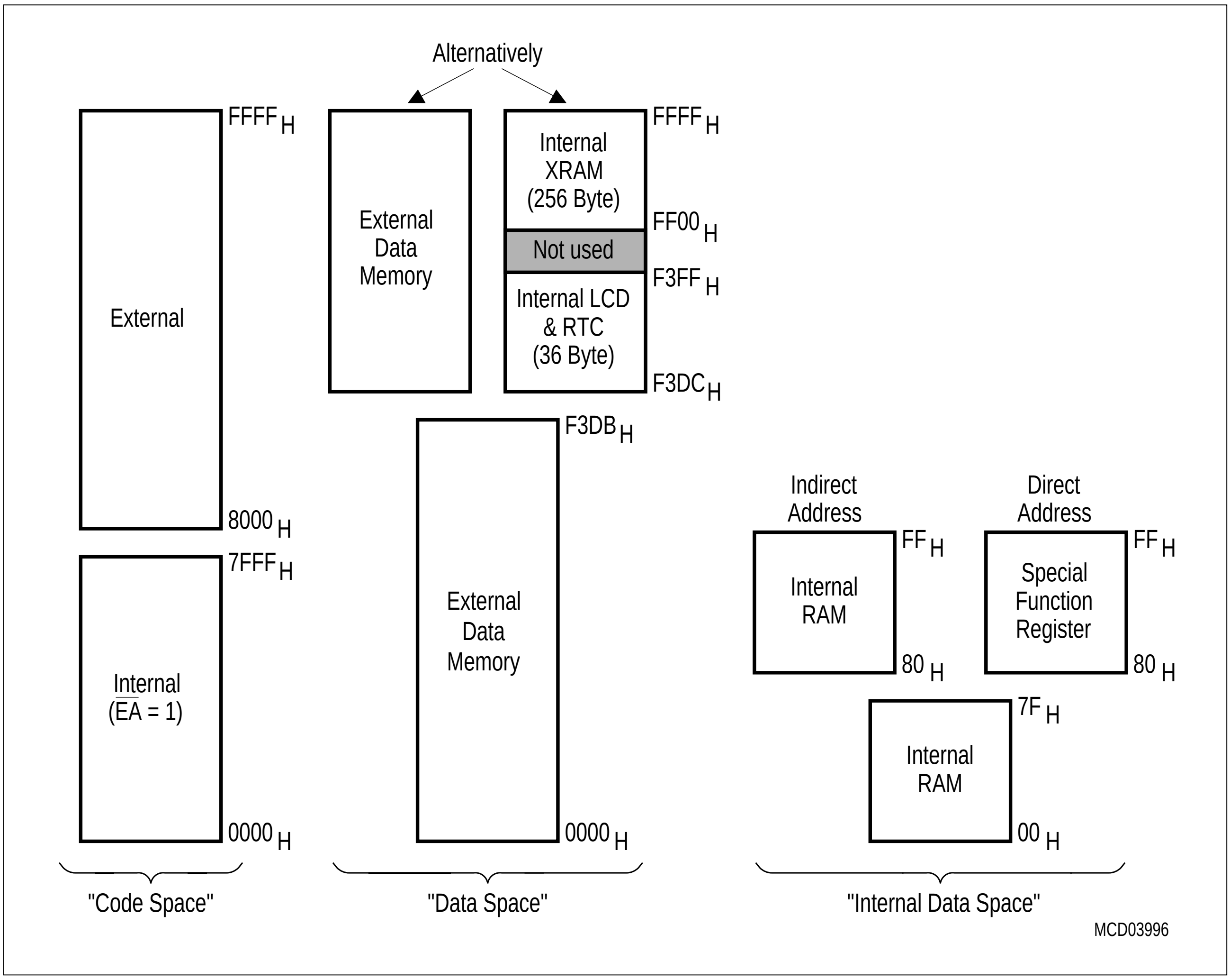


Figure 5
C505L Memory Map

Reset and System Clock

The reset input is an active high input at pin RESET. Since the reset is synchronized internally, the RESET pin must be held low for at least two machine cycles (12 oscillator periods) while the oscillator is running. A pull-down resistor is internally connected to V_{SS} to allow a power-up reset with an external capacitor only. An automatic reset can be obtained when V_{DD} is applied by connecting the RESET pin to V_{DD} via a capacitor. **Figure 6** shows the possible reset circuitries.

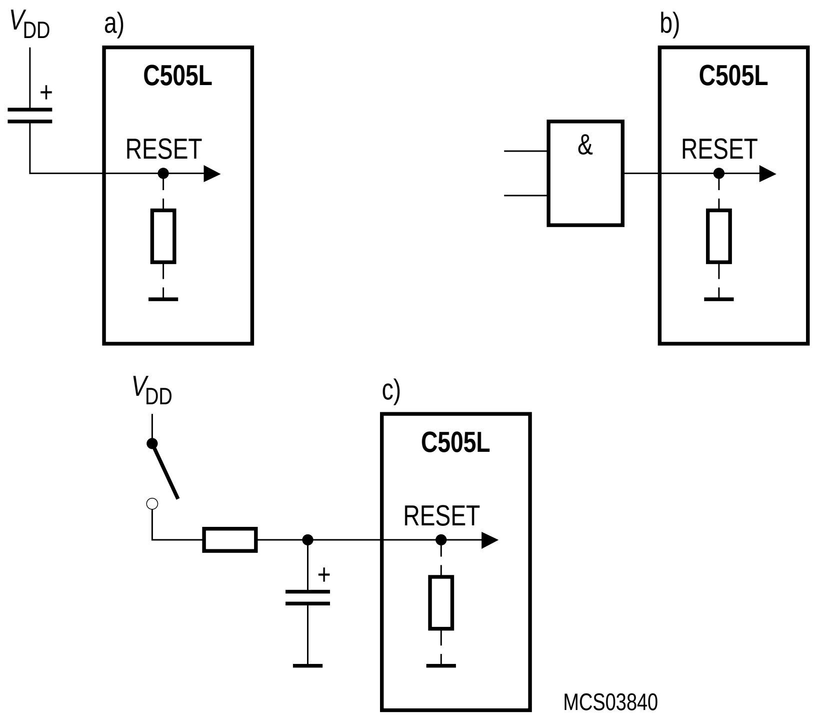


Figure 6
Reset Circuitries

Figure 7 and **Figure 8** show the recommended oscillator circiutries for crystal and external clock operations, respectively, for the system or main clock.

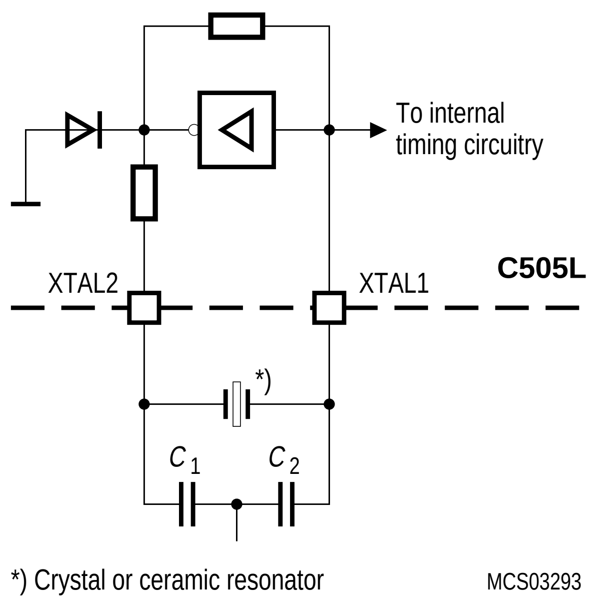


Figure 7
Recommended Oscillator Circuitries (for XTAL1-XTAL2)

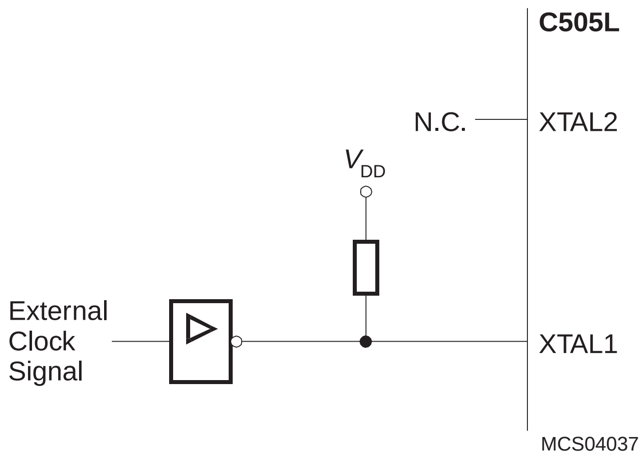


Figure 8
Recommended Oscillator Circuitries for Real-Time Clock (XTAL3-XTAL4)

Multiple Datapointers

As a functional enhancement to the standard 8051 architecture, the C505L contains eight 16-bit datapointers instead of only one datapointer. The instruction set uses just one of these datapointers at a time. The selection of the actual datapointer is done in the special function register DPSEL. **Figure 9** illustrates the datapointer addressing mechanism.

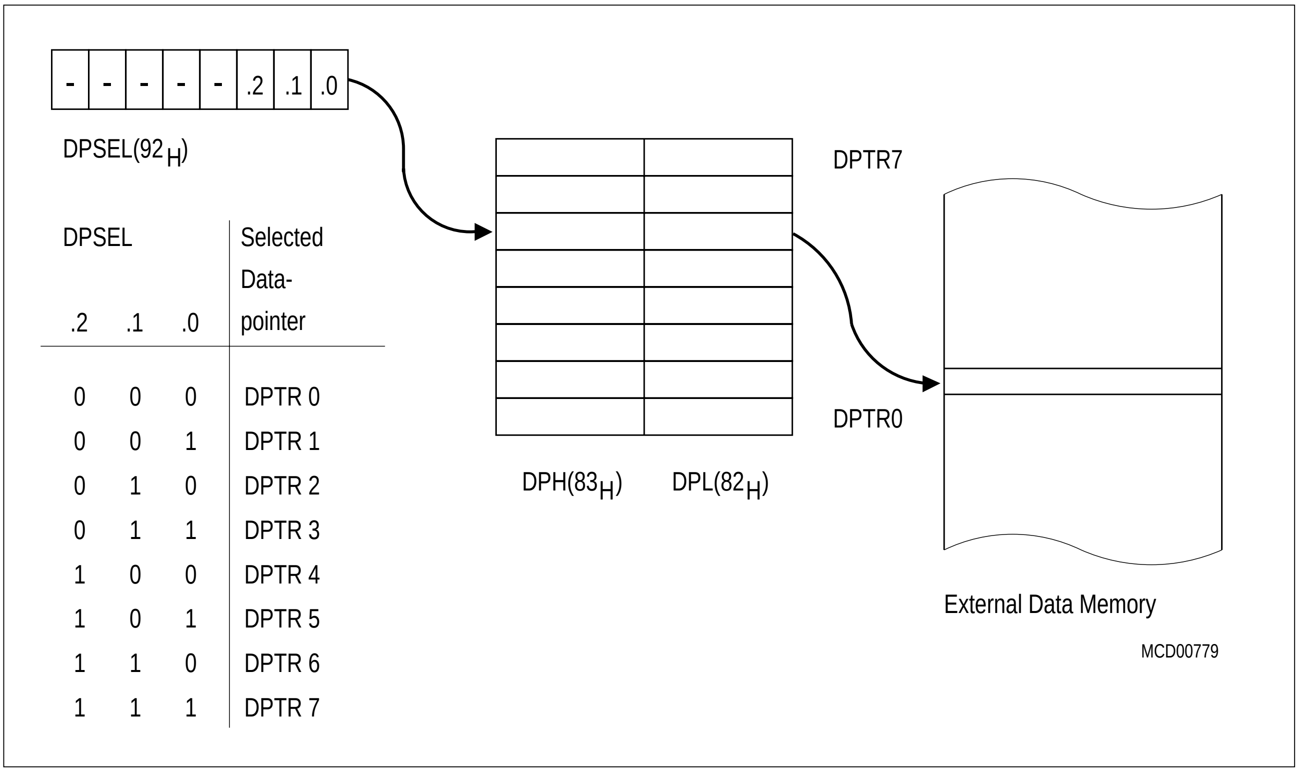


Figure 9
External Data Memory Addressing using Multiple Datapointers

Enhanced Hooks Emulation Concept

The Enhanced Hooks Emulation Concept of the C500 microcontroller family is a new, innovative way to control the execution of C500 MCUs and to gain extensive information on the internal operation of the controllers. Emulation of on-chip memory based programs is possible, too.

Each production chip has built-in logic for the support of the Enhanced Hooks Emulation Concept. Therefore, no costly bond-out chips are necessary for emulation. This also ensure that emulation and production chips are identical.

The Enhanced Hooks Technology™ [1)], which requires embedded logic in the C500 allows the C500 together with an EH-IC to function similar to a bond-out chip. This simplifies the design and reduces costs of an ICE-system. ICE-systems using an EH-IC and a compatible C500 are able to emulate all operating modes of the different versions of the C500 microcontrollers. This includes emulation of ROM, ROM with code rollover and ROMless modes of operation. It is also able to operate in single step mode and to read the SFRs after a break.

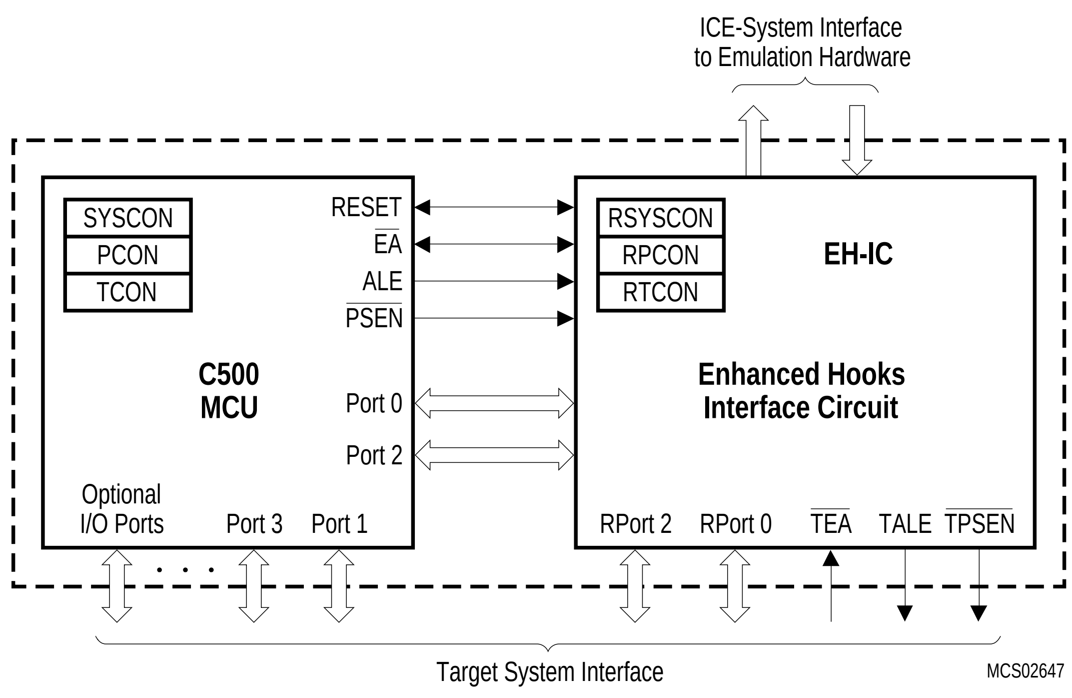


Figure 10
Basic C500 MCU Enhanced Hooks Concept Configuration

Port 0, port 2 and some of the control lines of the C500 based MCU are used by Enhanced Hooks Emulation Concept to control the operation of the device during emulation and to transfer informations about the program execution and data transfer between the external emulation hardware (ICE-system) and the C500 MCU.

1 “Enhanced Hooks Technology” is a trademark and patent of Metalink Corporation licensed to Infineon Technologies.

Special Function Registers

The registers, except the program counter and the four general purpose register banks, reside in the special function register area which consists of two portions: the standard special function register area and the mapped special function register area. Some of the C505L's SFRs (PCON1, VR0, VR1 and VR2) are located in the mapped SFR area. For accessing the mapped SFR area, bit RMAP in SFR SYSCON must be set. All other SFRs are located in the standard SFR area which is accessed when RMAP is cleared ("0").

The registers and data locations of the LCD Controller (LCD-SFRs) and the RTC (RTC-SFRs) are located in the external data memory area at addresses $F3DD_H$ to $F3EF_H$ and $F3F0_H$ to $F3FF_H$ respectively.

Special Function Register SYSCON (Address $B1_H$) **Reset Value: $XX100X01_B$**

Bit No.	MSB 7	6	5	4	3	2	1	LSB 0	
$B1_H$	–	–	EALE	RMAP	–	–	XMAP1	XMAP0	SYSCON

The shaded bits are not described in this section.

Bit	Function
RMAP	SFR map bit RMAP = 0: Access to the non-mapped (standard) SFR area is enabled. RMAP = 1: Access to the mapped SFR area is enabled.
–	Reserved bits for future use. Read by CPU returns undefined values.

As long as bit RMAP is set, mapped SFR area can be accessed. This bit is not cleared automatically by hardware. Thus, when non-mapped/mapped registers are to be accessed, the bit RMAP must be cleared/set respectively by software.

All SFRs with addresses where address bits 0-2 are 0 (e.g. 80_H, 88_H, 90_H, 98_H, …, $F8_H$, FF_H) are bit-addressable.

The 51 SFRs in the standard and mapped SFR area include pointers and registers that provide an interface between the CPU and the other on-chip peripherals. The SFRs of the C505L are listed in **Table 2** and **Table 3**. In **Table 2** they are organized in groups which refer to the functional blocks of the C505L. The LCD and RTC-SFRs are also included in **Table 2**. **Table 3** illustrates the contents of the SFRs in numeric order of their addresses. **Table 4** lists the LCD and the RTC-SFRs in numeric order of their addresses.

Table 2
Special Function Registers - Functional Blocks

Block	Symbol	Name	Address	Contents after Reset
CPU	ACC	Accumulator	**E0$_H$**[1)]	00$_H$
	B	B-Register	**F0$_H$**[1)]	00$_H$
	DPH	Data Pointer, High Byte	83$_H$	00$_H$
	DPL	Data Pointer, Low Byte	82$_H$	00$_H$
	DPSEL	Data Pointer Select Register	92$_H$	XXXXX000$_B$[3)]
	PSW	Program Status Word Register	**D0$_H$**[1)]	00$_H$
	SP	Stack Pointer	81$_H$	07$_H$
	SYSCON[2)]	System Control Register	B1$_H$	XX10XX01$_B$[3)]
	VR0[4)]	Version Register 0	FC$_H$	C5$_H$
	VR1[4)]	Version Register 1	FD$_H$	85$_H$
	VR2[4)]	Version Register 2	FE$_H$	[5)]
A/D-Converter	ADCON0[2)]	A/D Converter Control Register 0	**D8$_H$**[1)]	00X00000$_B$[3)]
	ADCON1	A/D Converter Control Register 1	DC$_H$	01XXX000$_B$[3)]
	ADDATH	A/D Converter Data Register High Byte	D9$_H$	00$_H$
	ADDATL	A/D Converter Data Register Low Byte	DA$_H$	00XXXXXX$_B$[3)]
	P1ANA[2)]	Port 1 Analog Input Selection Register	90$_H$[4)]	FF$_H$
Interrupt System	IEN0[2)]	Interrupt Enable Register 0	**A8$_H$**[1)]	00$_H$
	IEN1[2)]	Interrupt Enable Register 1	**B8$_H$**[1)]	00$_H$
	IP0[2)]	Interrupt Priority Register 0	A9$_H$	00$_H$
	IP1	Interrupt Priority Register 1	B9$_H$	XX000000$_B$[3)]
	TCON[2)]	Timer Control Register	**88$_H$**[1)]	00$_H$
	T2CON[2)]	Timer 2 Control Register	**C8$_H$**[1)]	00X00000$_B$
	SCON[2)]	Serial Channel Control Register	**98$_H$**[1)]	00$_H$
	IRCON	Interrupt Request Control Register	**C0$_H$**[1)]	00$_H$
XRAM	XPAGE	Page Address Register for Extended on-chip XRAM, LCD Controller and RTC	91$_H$	00$_H$
	SYSCON[2)]	System Control Register	B1$_H$	XX10XX01$_B$[3)]
Ports	P0	Port 0	**80$_H$**[1)]	FF$_H$
	P1	Port 1	**90$_H$**[1)]	FF$_H$
	P1ANA[2)]	Port 1 Analog Input Selection Register	**90$_H$**[1) 4)]	FF$_H$
	P2	Port 2	**A0$_H$**[1)]	FF$_H$
	P3	Port 3	**B0$_H$**[1)]	FF$_H$
	P4	Port 4	**E8$_H$**[1)]	00$_B$
	P5	Port 5	**F8$_H$**[1)]	XX111111$_B$

1) Bit-addressable SFRs
2) This SFR is listed repeatedly since some bits of it also belong to other functional blocks.
3) “X” means that the value is undefined and the location is reserved
4) This SFR is a mapped SFR. For accessing this SFR, bit RMAP in SFR SYSCON must be set.
5) The content of this SFR varies with the actual step of the C505L (e.g. 01$_H$ for the first step)

Table 2
Special Function Registers - Functional Blocks (cont'd)

Block	Symbol	Name	Address	Contents after Reset
Serial Channel	ADCON0 [2]	A/D Converter Control Register 0	**$D8_H$** [1]	$00X00000_B$ [3]
	PCON [2]	Power Control Register	87_H	00_H
	SBUF	Serial Channel Buffer Register	99_H	XX_H [3]
	SCON	Serial Channel Control Register	**98_H** [1]	00_H
	SRELL	Serial Channel Reload Register, low byte	AA_H	$D9_H$
	SRELH	Serial Channel Reload Register, high byte	BA_H	$XXXXXX11_B$ [3]
Timer 0/ Timer 1	TCON	Timer 0/1 Control Register	**88_H** [1]	00_H
	TH0	Timer 0, High Byte	$8C_H$	00_H
	TH1	Timer 1, High Byte	$8D_H$	00_H
	TL0	Timer 0, Low Byte	$8A_H$	00_H
	TL1	Timer 1, Low Byte	$8B_H$	00_H
	TMOD	Timer Mode Register	89_H	00_H
Compare/ Capture Unit / Timer 2	CCEN	Comp./Capture Enable Reg.	$C1_H$	00_H [3]
	CCH1	Comp./Capture Reg. 1, High Byte	$C3_H$	00_H
	CCH2	Comp./Capture Reg. 2, High Byte	$C5_H$	00_H
	CCH3	Comp./Capture Reg. 3, High Byte	$C7_H$	00_H
	CCL1	Comp./Capture Reg. 1, Low Byte	$C2_H$	00_H
	CCL2	Comp./Capture Reg. 2, Low Byte	$C4_H$	00_H
	CCL3	Comp./Capture Reg. 3, Low Byte	$C6_H$	00_H
	CRCH	Reload Register High Byte	CB_H	00_H
	CRCL	Reload Register Low Byte	CA_H	00_H
	TH2	Timer 2, High Byte	CD_H	00_H
	TL2	Timer 2, Low Byte	CC_H	00_H
	T2CON	Timer 2 Control Register	**$C8_H$** [1]	$00X00000_B$ [3]
	IEN0 [2]	Interrupt Enable Register 0	**$A8_H$** [1]	00_H
	IEN1 [2]	Interrupt Enable Register 1	**$B8_H$** [1]	00_H
Watchdog	WDTREL	Watchdog Timer Reload Register	86_H	00_H
	IEN0 [2]	Interrupt Enable Register 0	**$A8_H$** [1]	00_H
	IEN1 [2]	Interrupt Enable Register 1	**$B8_H$** [1]	00_H
	IP0 [2]	Interrupt Priority Register 0	$A9_H$	00_H
Power Save Modes	PCON [2]	Power Control Register	87_H	00_H
	PCON1 [4]	Power Control Register 1	**88_H** [1]	$0XX0XXXX_B$ [3]

1) Bit-addressable SFRs
2) This SFR is listed repeatedly since some bits of it also belong to other functional blocks.
3) "X" means that the value is undefined and the location is reserved
4) SFR is located in the mapped SFR area. For accessing this SFR, bit RMAP in SFR SYSCON must be set.

Table 2
Special Function Registers - Functional Blocks (cont'd)

Block	Symbol	Name	Address	Contents after Reset
LCD Controller	DAC0	D/A Conversion Register	$F3DC_H$	00_H [6)]
	LCON	LCD Control Register	$F3DD_H$	00_H [6)]
	LCRL	LCD Timer Reload Low Register	$F3DE_H$	00_H [6)]
	LCRH	LCD Timer Reload High Register	$F3DF_H$	00_H [6)]
	DIGn [5)]	LCD Digit Register 'n' [5)]	$F3En_H$	00_H [5) 6)]
Real-Time Clock	RTCON	Real-Time Clock Control Register	$F3F0_H$	00_H [6)]
	RTCR0	Real-Time Clock Initialization Register 0	$F3F1_H$	00_H [6)]
	RTCR1	Real-Time Clock Initialization Register 1	$F3F2_H$	00_H [6)]
	RTCR2	Real-Time Clock Initialization Register 2	$F3F3_H$	00_H [6)]
	RTCR3	Real-Time Clock Initialization Register 3	$F3F4_H$	00_H [6)]
	RTCR4	Real-Time Clock Initialization Register 4	$F3F5_H$	00_H [6)]
	CLREG0	Clock Count Register 0	$F3F6_H$	00_H [6)]
	CLREG1	Clock Count Register 1	$F3F7_H$	00_H [6)]
	CLREG2	Clock Count Register 2	$F3F8_H$	00_H [6)]
	CLREG3	Clock Count Register 3	$F3F9_H$	00_H [6)]
	CLREG4	Clock Count Register 4	$F3FA_H$	00_H [6)]
	RTINT0	Real-Time Clock Interrupt Register 0	$F3FB_H$	00_H [6)]
	RTINT1	Real-Time Clock Interrupt Register 1	$F3FC_H$	00_H [6)]
	RTINT2	Real-Time Clock Interrupt Register 2	$F3FD_H$	00_H [6)]
	RTINT3	Real-Time Clock Interrupt Register 3	$F3FE_H$	00_H [6)]
	RTINT4	Real-Time Clock Interrupt Register 4	$F3FF_H$	00_H [6)]

1) Bit-addressable SFRs
2) This SFR is listed repeatedly since some bits of it also belong to other functional blocks.
3) "X" means that the value is undefined and the location is reserved.
4) SFR is located in the mapped SFR area. For accessing this SFR, bit RMAP in SFR SYSCON must be set.
5) The notation "n" (n = 0 to F) in the LCD Digit Register address definition defines the number of the related LCD digit.
6) This register is located in the on-chip external data memory area.

Table 3
Contents of the SFRs, SFRs in Numeric Order of Their Addresses

Addr	Register	Content after Reset[1)]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
80_H [2)]	P0	FF_H	.7	.6	.5	.4	.3	.2	.1	.0
81_H	SP	07_H	.7	.6	.5	.4	.3	.2	.1	.0
82_H	DPL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
83_H	DPH	00_H	.7	.6	.5	.4	.3	.2	.1	.0
86_H	WDTREL	00_H	WDT PSEL	.6	.5	.4	.3	.2	.1	.0
87_H	PCON	00_H	SMOD	PDS	IDLS	SD	GF1	GF0	PDE	IDLE
88_H [2)]	TCON	00_H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
88_H [3)]	PCON1	$0XX0\text{-}XXXX_B$	EWPD	–	–	WS	–	–	–	–
89_H	TMOD	00_H	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
$8A_H$	TL0	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$8B_H$	TL1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$8C_H$	TH0	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$8D_H$	TH1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
90_H [2)]	P1	FF_H	T2	CLK-OUT	T2EX	.4	INT6	INT5	INT4	$\overline{INT3}$
90_H [3)]	P1ANA	FF_H	EAN7	EAN6	EAN5	EAN4	EAN3	EAN2	EAN1	EAN0
91_H	XPAGE	00_H	.7	.6	.5	.4	.3	.2	.1	.0
92_H	DPSEL	$XXXX\text{-}X000_B$	–	–	–	–	–	.2	.1	.0
98_H [2)]	SCON	00_H	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
99_H	SBUF	XX_H	.7	.6	.5	.4	.3	.2	.1	.0
$A0_H$ [2)]	P2	FF_H	.7	.6	.5	.4	.3	.2	.1	.0
$A8_H$ [2)]	IEN0	00_H	EA	WDT	ET2	ES	ET1	EX1	ET0	EX0
$A9_H$	IP0	00_H	OWDS	WDTS	.5	.4	.3	.2	.1	.0
AA_H	SRELL	$D9_H$	.7	.6	.5	.4	.3	.2	.1	.0

1) X means that the value is undefined and the location is reserved
2) Bit-addressable SFRs
3) SFR is located in the mapped SFR area. For accessing this SFR, bit RMAP in SFR SYSCON must be set.

Table 3
Contents of the SFRs, SFRs in Numeric Order of Their Addresses (cont'd)

Addr	Register	Content after Reset[1]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B0$_H$[2]	P3	FF$_H$	$\overline{\text{RD}}$	$\overline{\text{WR}}$	T1	T0	$\overline{\text{INT1}}$	$\overline{\text{INT0}}$	TxD	RxD
B1$_H$	SYSCON	XX10-XX01$_B$	–	–	EALE	RMAP	–	–	XMAP1	XMAP0
B8$_H$[2]	IEN1	00$_H$	EXEN2	SWDT	EX6	EX5	EX4	EX3	ESWI	EADC
B9$_H$	IP1	XX00-0000$_B$	–	–	.5	.4	.3	.2	.1	.0
BA$_H$	SRELH	XXXX-XX11$_B$	–	–	–	–	–	–	.1	.0
C0$_H$[2]	IRCON	00$_H$	EXF2	TF2	IEX6	IEX5	IEX4	IEX3	SWI	IADC
C1$_H$	CCEN	00$_H$	COCAH3	COCAL3	COCAH2	COCAL2	COCAH1	COCAL1	COCAH0	COCAL0
C2$_H$	CCL1	00$_H$	.7	.6	.5	.4	.3	.2	.1	.0
C3$_H$	CCH1	00$_H$	.7	.6	.5	.4	.3	.2	.1	.0
C4$_H$	CCL2	00$_H$	.7	.6	.5	.4	.3	.2	.1	.0
C5$_H$	CCH2	00$_H$	.7	.6	.5	.4	.3	.2	.1	.0
C6$_H$	CCL3	00$_H$	.7	.6	.5	.4	.3	.2	.1	.0
C7$_H$	CCH3	00$_H$	.7	.6	.5	.4	.3	.2	.1	.0
C8$_H$[2]	T2CON	00X0-0000$_B$	T2PS	I3FR	–	T2R1	T2R0	T2CM	T2I1	T2I0
CA$_H$	CRCL	00$_H$	.7	.6	.5	.4	.3	.2	.1	.0
CB$_H$	CRCH	00$_H$	.7	.6	.5	.4	.3	.2	.1	.0
CC$_H$	TL2	00$_H$	.7	.6	.5	.4	.3	.2	.1	.0
CD$_H$	TH2	00$_H$	.7	.6	.5	.4	.3	.2	.1	.0
D0$_H$[2]	PSW	00$_H$	CY	AC	F0	RS1	RS0	OV	F1	P
D8$_H$[2]	ADCON0	00X0-0000$_B$	BD	CLK	–	BSY	ADM	MX2	MX1	MX0
D9$_H$	ADDATH	00$_H$	.9	.8	.7	.6	.5	.4	.3	.2
DA$_H$	ADDATL	00XX-XXXX$_B$	.1	.0	–	–	–	–	–	–

1) X means that the value is undefined and the location is reserved
2) Bit-addressable SFRs

Table 3
Contents of the SFRs, SFRs in Numeric Order of Their Addresses (cont'd)

Addr	**Register**	**Content after Reset**[1)]	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
DC_H	ADCON1	01XX-X000$_B$	ADCL1	ADCL0	–	–	–	MX2	MX1	MX0
$E0_H$[2)]	ACC	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$E8_H$[2)]	P4	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$F0_H$[2)]	B	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$F8_H$[2)]	P5	XX00-0000$_H$	–	–	.5	.4	.3	.2	.1	.0
FC_H[3)4)]	VR0	$C5_H$	1	1	0	0	0	1	0	1
FD_H[3)4)]	VR1	85_H	0	0	0	0	0	1	0	1
FE_H[3)4)]	VR2	[5)]	.7	.6	.5	.4	.3	.2	.1	.0

1) X means that the value is undefined and the location is reserved.
2) Bit-addressable SFRs.
3) SFR is located in the mapped SFR area. For accessing this SFR, bit RMAP in SFR SYSCON must be set.
4) These are read-only registers.
5) The content of this SFR varies with the actual of the step C505L (e.g. 01_H for the first step).

Table 4
Contents of the LCD and the RTC Registers in Numeric Order of Their Addresses

Addr.	Register	Content after Reset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$F3DC_H$	DAC0	00_H	S7	S6	S5	S4	S3	S2	S1	S0
$F3DD_H$	LCON	00_H	DSB1	DSB0	0	0	0	0	CSEL	LCEN
$F3DE_H$	LCRL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$F3DF_H$	LCRH	00_H	SLT	.14	.13	.12	.11	.10	.9	.8
$F3En_H$	DIGn [1)]	00_H	SEGF	SEGA	SEGG	SEGB	SEGE	SEGC	SEGH	SEGD
$F3F0_H$	RTCON	00_H	0	0	0	0	RTPD	IRTC	ERTC	RTCS
$F3F1_H$	RTCR0	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$F3F2_H$	RTCR1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$F3F3_H$	RTCR2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$F3F4_H$	RTCR3	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$F3F5_H$	RTCR4	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$F3F6_H$	CLREG0	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$F3F7_H$	CLREG1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$F3F8_H$	CLREG2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$F3F9_H$	CLREG3	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$F3FA_H$	CLREG4	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$F3FB_H$	RTINT0	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$F3FC_H$	RTINT1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$F3FD_H$	RTINT2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$F3FE_H$	RTINT3	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$F3FF_H$	RTINT4	00_H	.7	.6	.5	.4	.3	.2	.1	.0

1) The notation “n” (n = 0 to F) in the LCD Digit Register address definition defines the number of the related LCD digit.

Digital I/O Ports

The C505L has five 8-bit and one 6-bit (port 5) digital I/O ports. Port 0 is an open-drain bidirectional I/O port, while ports 1 through 5 are quasi-bidirectional I/O ports with internal pull-up resistors. When configured as inputs, ports 1-5 will be pulled high, and will source current when externally pulled low. Port 0 will float when configured as input.

The output drivers of port 0 and 2 and the input buffers of port 0 are also used for accessing external memory. In this application, port 0 outputs the low byte of the external memory address, time-multiplexed with the byte being written or read. Port 2 outputs the high byte of the external memory address when the address is 16 bits wide. Otherwise, the port 2 pins continue emitting the P2 Special Function register (SFR) contents. In this function, port 0 is not an open-drain port, but uses a strong internal pull-up.

Therefore, the parallel I/O ports of the C505L can be grouped into six different types which are listed in **Table 5**.

Table 5
C505L Port Structure Types

Type	Description
A	Standard digital I/O ports which can also be used for external address/data bus.
B	Standard multifunctional digital I/O port lines
C	Mixed digital/analog I/O port lines with programmable analog input function
D	LCD Output Lines
E	Standard digital I/O or LCD output lines
F	Standard multifunctional digital I/O or LCD output lines

Type A and B port pins are standard C501-compatible I/O port lines, which can be used for digital I/O. The type A ports (port 0 and port 2) are also designed for accessing external data or program memory. Type B port lines are located at port 3 (except P3.4 and P3.5), and are used for digital I/O or for other alternate functions as described in the pin description. Type D port lines provide the LCD controller outputs R0-R3 and C0-C15 as primary functions. Type E port lines are located at port 4 and port 5 and provide the LCD controller output lines as alternate functions. Type F port lines are at P3.4/T0 and P3.5/T1 and have a digital alternate input each, apart from LCD output functions.

The C505L provides eight analog input lines that are implemented as mixed digital/analog inputs (type C). The 8 analog inputs, AN0-AN7, are located at the port 1 pins P1.0 to P1.7. After reset, all analog inputs are disabled and the related pins of port 1 are configured as digital inputs. The analog function of the specific port 1 pins are enabled by bits in the SFRs P1ANA. Writing a 0 to a bit position of P1ANA assigns the corresponding pin to operate as analog input.

Note: P1ANA is a mapped SFR and can only be accessed if bit RMAP in SFR SYSCON is set.

If a digital value is to be read by port 1, the voltage levels are to be held within the input voltage specifications (V_{IL}/V_{IH}).

Timer / Counter 0 and 1

Timer/Counter 0 and 1 can be used in four operating modes as listed in **Table 6**:

Table 6
Timer/Counter 0 and 1 Operating Modes

Mode	Description	TMOD		Input Clock	
		M1	M0	internal	external (max)
0	8-bit timer/counter with a divide-by-32 prescaler	0	0	$f_{OSC}/(6 \times 32)$	$f_{OSC}/(12 \times 32)$
1	16-bit timer/counter	0	1	$f_{OSC}/6$	$f_{OSC}/12$
2	8-bit timer/counter with 8-bit autoreload	1	0		
3	Timer/counter 0 used as one 8-bit timer/counter and one 8-bit timer Timer 1 stops	1	1		

In the "timer" function (C/$\overline{T}$ = '0') the register is incremented every machine cycle. Therefore the count rate is $f_{OSC}/6$.

In the "counter" function the register is incremented in response to a 1-to-0 transition at its corresponding external input pin (P3.4/T0, P3.5/T1). Since it takes two machine cycles to detect a falling edge the max. count rate is $f_{OSC}/12$. External inputs $\overline{INT0}$ and $\overline{INT1}$ (P3.2, P3.3) can be programmed to function as a gate to facilitate pulse width measurements. **Figure 11** illustrates the input clock logic.

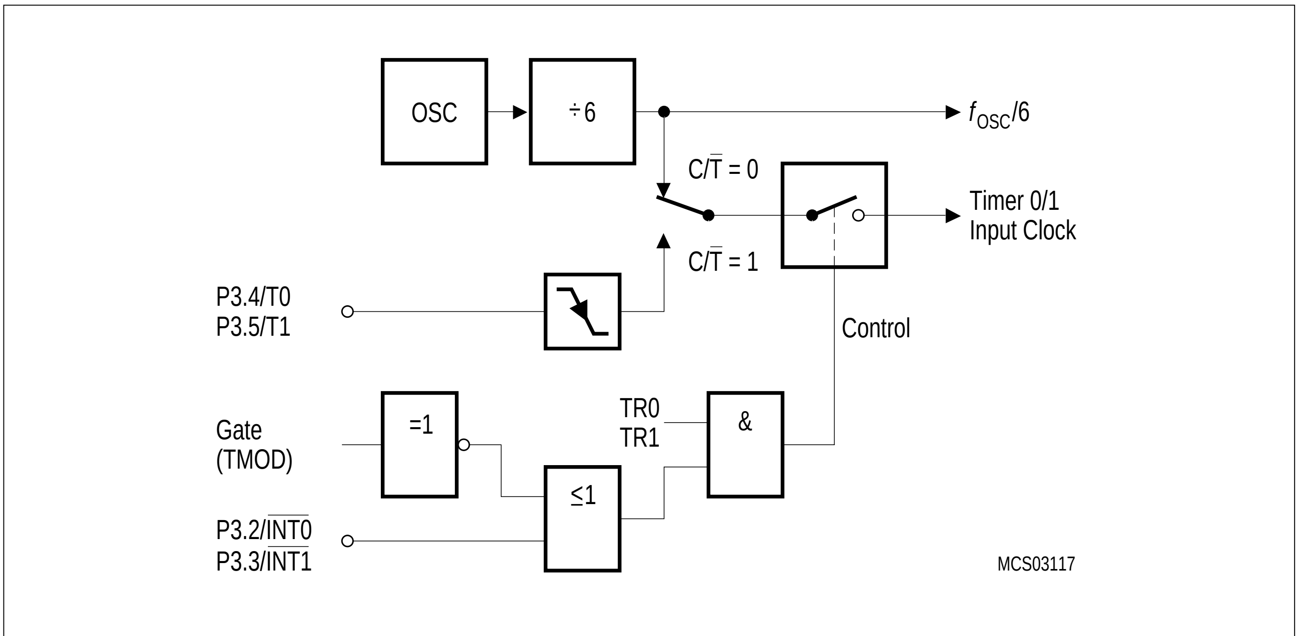


Figure 11
Timer/Counter 0 and 1 Input Clock Logic

Timer/Counter 2 with Compare/Capture/Reload

The timer 2 of the C505L provides additional compare/capture/reload features, which allow the selection of the following operating modes:

- Compare : up to 4 PWM signals with 16-bit/300 ns resolution (@ 20 MHz clock)
- Capture : up to 4 high speed capture inputs with 300 ns resolution
- Reload : modulation of timer 2 cycle time

The block diagram in **Figure 12** shows the general configuration of timer 2 with the additional compare/capture/reload registers. The I/O pins which can used for timer 2 control are located as multifunctional port functions at port 1.

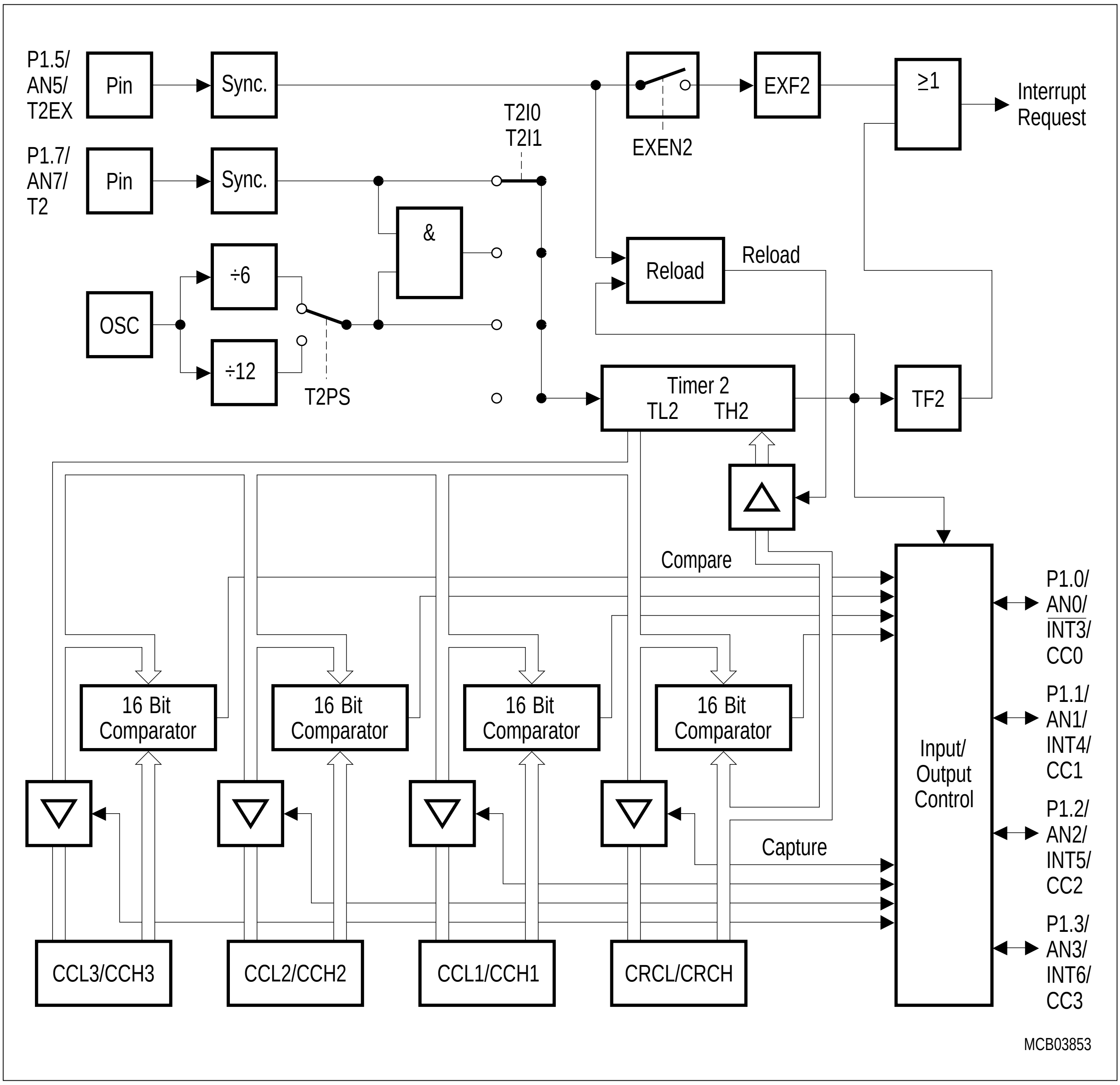


Figure 12
Timer 2 Block Diagram

Timer 2 Operating Modes

The timer 2, which is a 16-bit-wide register, can operate as timer, event counter, or gated timer. A roll-over of the count value in TL2/TH2 from all 1's to all 0's sets the timer overflow flag TF2 in SFR IRCON, which can generate an interrupt. The bits in register T2CON are used to control the timer 2 operation.

Timer Mode: In timer function, the count rate is derived from the oscillator frequency. A prescaler offers the possibility of selecting a count rate of 1/6 or 1/12 of the oscillator frequency.

Gated Timer Mode: In gated timer function, the external input pin T2 (P1.7) functions as a gate to the input of timer 2. If T2 is high, the internal clock input is gated to the timer. T2 = 0 stops the counting procedure. This facilitates pulse width measurements. The external gate signal is sampled once every machine cycle.

Event Counter Mode: In the event counter function. the timer 2 is incremented in response to a 1-to-0 transition at its corresponding external input pin T2 (P1.7). In this function, the external input is sampled every machine cycle. Since it takes two machine cycles (12 oscillator periods) to recognize a 1-to-0 transition, the maximum count rate is 1/6 of the oscillator frequency. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it must be held for at least one full machine cycle.

Reload of Timer 2: Two reload modes are selectable:
In mode 0, when timer 2 rolls over from all 1's to all 0's, it not only sets TF2 but also causes the timer 2 registers to be loaded with the 16-bit value in the CRC register, which is preset by software.
In mode 1, a 16-bit reload from the CRC register is caused by a negative transition at the correspon-ding input pin P1.5/T2EX. This transition will also set flag EXF2 if bit EXEN2 in SFR IEN1 has been set.

Timer 2 Compare Modes

The compare function of a timer/register combination operates as follows: the 16-bit value stored in a compare or compare/capture register is compared with the contents of the timer register; if the count value in the timer register matches the stored value, an appropriate output signal is generated at a corresponding port pin and an interrupt can be generated.

Compare Mode 0

In compare mode 0, upon matching the timer and compare register contents, the output signal changes from low to high. It goes back to a low level on timer overflow. As long as compare mode 0 is enabled, the appropriate output pin is controlled by the timer circuit only and writing to the port will have no effect. **Figure 13** shows a functional diagram of a port circuit when used in compare mode 0. The port latch is directly controlled by the timer overflow and compare match signals. The input line from the internal bus and the write-to-latch line of the port latch are disconnected when compare mode 0 is enabled.

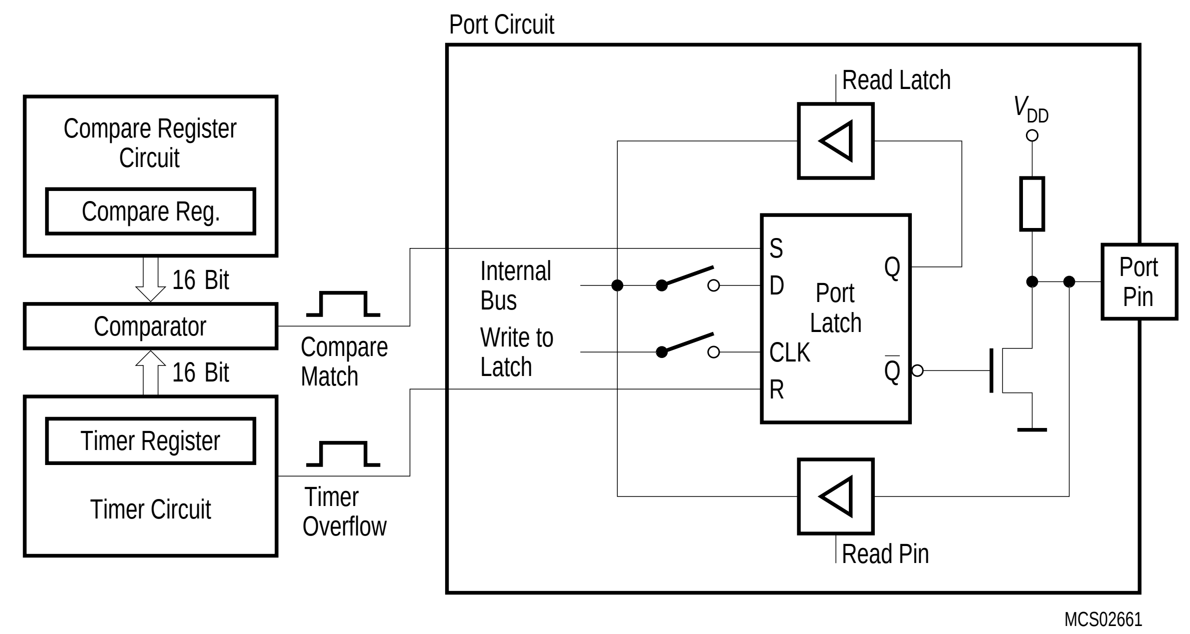


Figure 13
Port Latch in Compare Mode 0

Compare Mode 1

If compare mode 1 is enabled and the software writes to the appropriate output latch at the port, the new value will not appear at the output pin until the next compare match occurs. Thus, it can be choosen whether the output signal has to make a new transition (1-to-0 or 0-to-1, depending on the actual pin-level) or should keep its old value at the time when the timer value matches the stored compare value.

In compare mode 1 (see **Figure 14**) the port circuit consists of two separate latches. One latch (which acts as a "shadow latch") can be written under software control, but its value will only be transferred to the port latch (and thus to the port pin) when a compare match occurs.

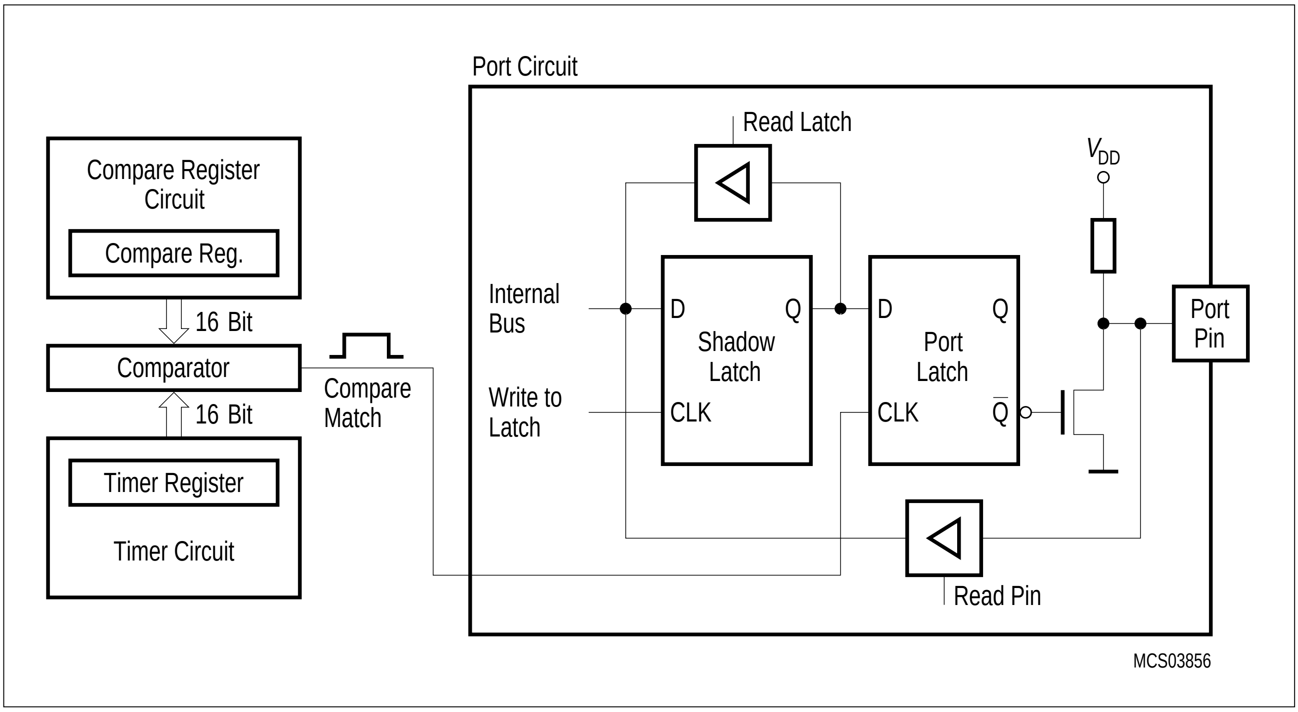


Figure 14
Compare Function in Compare Mode 1

Timer 2 Capture Modes

Each of the compare/capture registers CC1 to CC3 and the CRC register can be used to latch the current 16-bit value of the timer 2 registers TL2 and TH2. Two different modes are provided for this function.

In mode 0, the external event causing a capture is:

– for CC registers 1 to 3: a positive transition at pins CC1 to CC3 of port 1
– for the CRC register: a positive or negative transition at the corresponding pin, depending on the status of the bit I3FR in SFR T2CON.

In mode 1 a capture occurs in response to a write instruction to the low order byte of a capture register. The write-to-register signal (e.g. write-to-CRCL) is used to initiate a capture. The timer 2 contents will be latched into the appropriate capture register in the cycle following the write instruction. In this mode no interrupt request will be generated.

Serial Interface (USART)

The serial port is full duplex and can operate in four modes (one synchronous mode, three asynchronous modes) as illustrated in **Table 7**.

Table 7
USART Operating Modes

Mode	SCON		Description
	SM0	SM1	
0	0	0	Shift register mode, fixed baud rate Serial data enters and exits through R×D; T×D outputs the shift clock; 8-bit are transmitted/received (LSB first)
1	0	1	8-bit UART, variable baud rate 10 bits are transmitted (through T×D) or received (at R×D)
2	1	0	9-bit UART, fixed baud rate 11 bits are transmitted (through T×D) or received (at R×D)
3	1	1	9-bit UART, variable baud rate Like mode 2

For clarification some terms regarding the difference between “baud rate clock” and “baud rate” should be mentioned. In the asynchronous modes the serial interfaces require a clock rate which is 16 times the baud rate for internal synchronization. Therefore, the baud rate generators/timers have to provide a “baud rate clock” (output signal in **Figure 15**) to the serial interface which - divided by 16 - results in the actual “baud rate”. Further, the abbrevation f_{OSC} refers to the oscillator frequency (crystal or external clock operation).

The variable baud rates for modes 1 and 3 of the serial interface can be derived either from timer 1 or from a dedicated baud rate generator (see **Figure 15**).

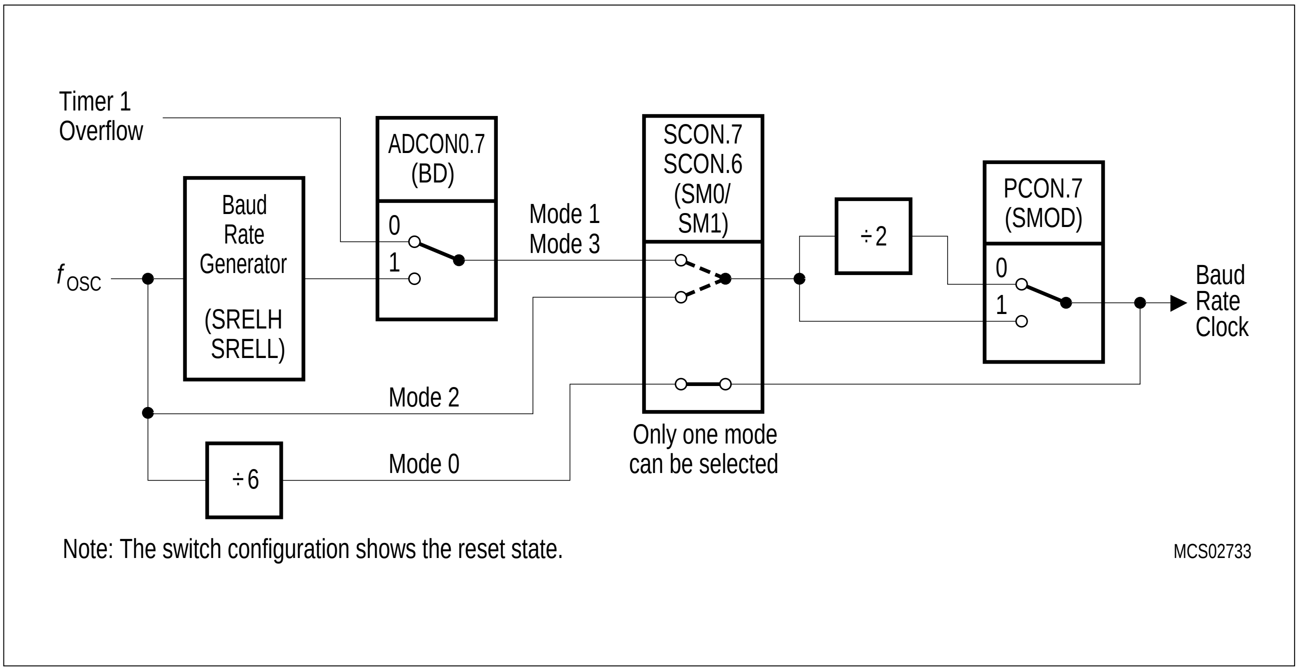


Figure 15
Block Diagram of Baud Rate Generation for the Serial Interface

Table 8 below lists the values/formulas for the baud rate calculation of the serial interface with its dependencies of the control bits BD and SMOD.

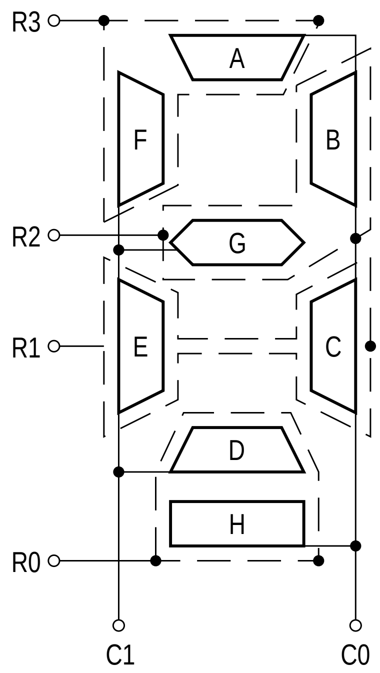
Table 8
Serial Interface - Baud Rate Dependencies

Serial Interface Operating Modes	Active Control Bits		Baud Rate Calculation
	BD	SMOD	
Mode 0 (Shift Register)	–	–	f_{OSC} / 6
Mode 1 (8-bit UART) Mode 3 (9-bit UART)	0	X	Controlled by timer 1 overflow: (2^{SMOD} × timer 1 overflow rate) / 32
	1	X	Controlled by baud rate generator (2^{SMOD} × f_{OSC}) / (32 × baud rate generator overflow rate)
Mode 2 (9-bit UART)	–	0 1	f_{OSC} / 32 f_{OSC} / 16

LCD Controller Unit

The Liquid Crystal Display (LCD) controller unit in the C505L is designed for the control of an LCD display module of 128 display segments (4 rows and 32 columns) using the 1/4 duty-cycle driving method. The C505L can be programmed to generate reference voltages for adjusting the contrast of the display.

An example of a typical LCD module is shown in **Figure 16**. The table describes the different combinations of the row and column signals required to activate a particular segment. The signals R0-R3 and C0-C31 are the row and column signals, respectively, connected to the display module.



Rows	Columns	
	C1	C0
R3	F	A
R2	G	B
R1	E	C
R0	D	H

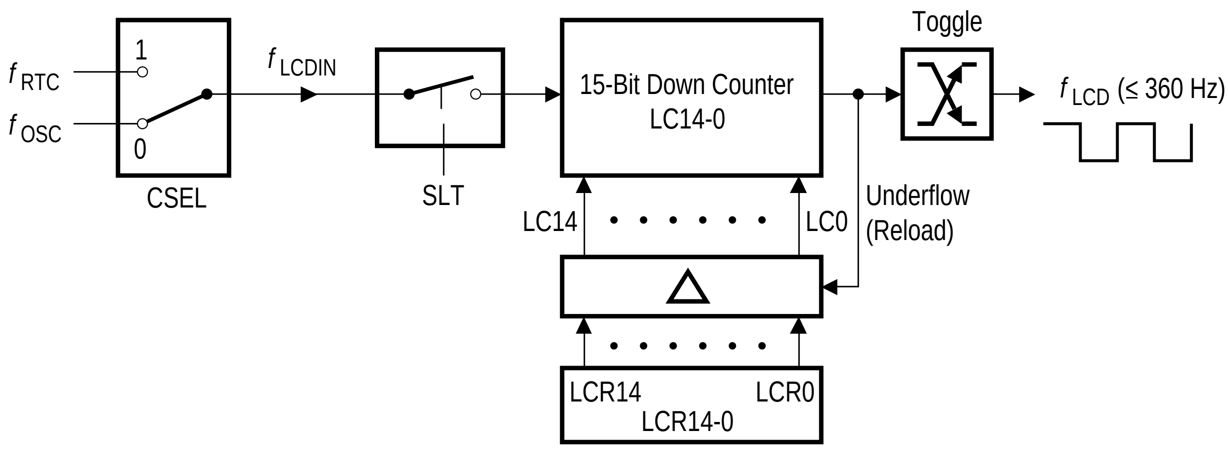
MCD03858

Figure 16
Organization of a Typical LCD Display Module

The memory required by the LCD controller includes a control register, LCON, the D/A Converter register DAC0 and 16 individual digit registers (DIGx, x = 0 to F). These registers are implemented in the on-chip external data memory area. Accesses to these registers are similar to on-chip XRAM accesses (MOVX instructions) and therefore must be preceded by an enable operation on the on-chip XRAM.

Note: The actual segment organization within the display unit could be different from the example considered here. In such cases, the segment names/positions may vary. The user should consult the manufacturer of the LCD display unit used regarding its segment organization.

The LCD outputs of the C505L must work at a frequency which is not more than 360 Hz in order to activate a display segment. To achieve this 360-Hz frequency limit, the LCD controller uses a scheme as shown in **Figure 17**.



f_{LCDIN}	LCR (15-Bit reload)	f_{LCD} (in Hz)
32.768 kHz	$002E_H$	356.17
2 MHz	$0ADA_H$	359.97
4 MHz	$15B4_H$	359.97
6 MHz	$208E_H$	359.97
10 MHz	3642_H	359.97
12 MHz	$411C_H$	359.97
16 MHz	$56D0_H$	359.97
20 MHz	$6C84_H$	359.97

MCD03859

Figure 17
LCD Clocking

The generated LCD clock has a duty-cycle of 50%. The table in **Figure 17** shows the recommended reload values at different input frequencies (f_{LCDIN}) to generate LCD clocks of frequencies less than 360 Hz.

The frequency of the LCD clock could be calculated by:

$$f_{LCD} = \frac{f_{LCDIN}}{2 \times \text{(15-bit reload value)}} \text{ Hz}$$

Display Voltage Levels

The LCD controller outputs three voltage levels required for driving the LCD display module. These voltage levels are generated by a programmable 8-bit D/A converter via the register DAC0 and a resistive divider network. The D/A converter is enabled by the LCD controller enable bit LCEN (LCON.0). Any write operation to the register DAC0 with the LCD controller enabled, starts the D/A conversion and thereby the display outputs. Therefore, the C505L can be used with a wide range of LCD display modules.

LCD Controller in Power Saving Mode

In order to reduce power consumption, the C505L can be put into the software power down mode 2. In this mode, the LCD controller and the D/A converter do not lose their register contents and remain in operation, provided the following conditions are satisfied:

– The input clock to the LCD is the 32.768 kHz real-time clock input, and
– The real-time clock input at XTAL3 and XTAL4 pins is still valid.

Real-Time Clock

The real-time clock unit of the C505L contains a dedicated oscillator and a 47-bit timer which is used to count time elapsed with respect to an initial time. The C505L real-time clock does not provide for any error correction. Any such corrections can be done by software only.

Functionality

The real-time clock can be initialized to a 40-bit initial value, which are loaded into the upper 40-bits of the timer. The lower 7 bits of the counter are never accessible by the user and merely act as prescalers that are initialized to 0000000_B after a start operation on the real-time clock. One increment of the clock register is made for every cycle of the input clock (32.768 kHz). The functionality of the real-time clock is shown in **Figure 18**.

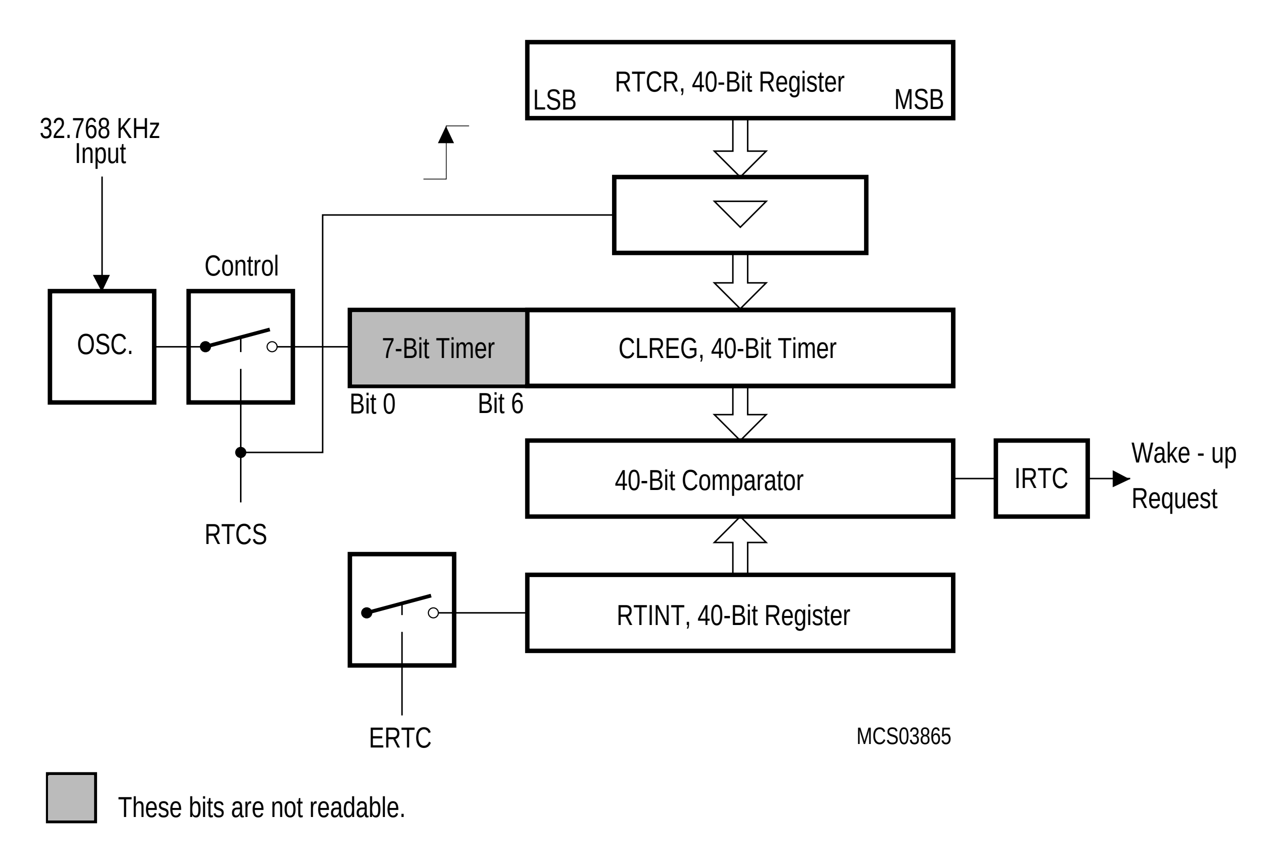


Figure 18
Real-Time Clock

The register memory for the real-time clock is implemented in the on-chip external data memory area. Accesses to these registers are similar to on-chip XRAM accesses (MOVX instructions) and therefore must be preceded by an enable operation on the on-chip XRAM. These registers include the RTCON, RTCR0 to RTCR4 (RTCR), CLREG0 to CLREG4 (CLREG) and RTINT0 to RTINT4 (RTINT) registers.

Real-Time Clock in Power Saving Modes

Once started in the normal mode, the oscillator as well as the whole real-time clock could remain in operation during certain power-down modes where the power supply could be reduced to a minimum of **3 V**. These are the power down modes 2 and 3, where other functional units of the C505L are powered down (**See "Power Saving Modes" on Page 50.**).

The upper 40-bit content of the real-time clock counter can be compared with the content of the programmable RTINT register in order to generate an interrupt request while the C505L is in one of software power-down modes 2 or 3, provided all of the following conditions are fulfilled:

- The C505L is in one of the software power-down modes 2 or 3,
- Wake-up from software power-down is enabled (bit EWPD = 1 in SFR PCON1)
- Real-time clock wake-up source is selected (bit WS = 1 in SFR PCON1),
- The real-time clock interrupt is enabled (bit ERTC = 1 of RTCON), and
- Normally operating V_{DD} levels are maintained

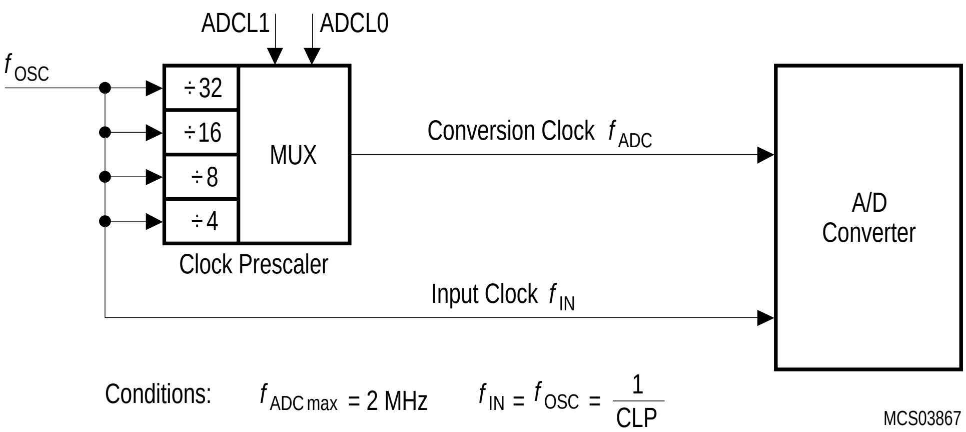
In this case, the handling is similar to the wake-up from power-down through P3.2/$\overline{\text{INT0}}$.

10-Bit A/D Converter

The C505L includes a high performance / high speed 10-bit A/D-Converter (ADC) with 8 analog input channels. It operates with a successive approximation technique and uses self calibration mechanisms for reduction and compensation of offset and linearity errors. The A/D converter provides the following features:

- 8 multiplexed input channels (port 1), which can also be used as digital inputs/outputs
- 10-bit resolution
- Single or continuous conversion mode
- Internal start-of-conversion trigger capability
- Interrupt request generation after each conversion
- Using successive approximation conversion technique via a capacitor array
- Built-in hidden calibration of offset and linearity errors

The 10-bit ADC uses two clock signals for operation: the conversion clock f_{ADC} (= $1/t_{ADC}$) and the input clock f_{IN} (= $1/t_{IN}$). f_{ADC} is derived from the C505L system clock f_{OSC} which is applied at the XTAL pins. The input clock f_{IN} is equal to f_{OSC} The conversion f_{ADC} clock is limited to a maximum frequency of 2 MHz. Therefore, the ADC clock prescaler must be programmed to a value which assures that the conversion clock does not exceed 2 MHz. The prescaler ratio is selected by the bits ADCL1 and ADCL0 of SFR ADCON1.



MCU System Clock Rate (f_{OSC})	f_{IN} [MHz]	Prescaler Ratio	f_{ADC} [MHz]	ADCL1	ADCL0
2 MHz	2	÷ 4	0.5	0	0
6 MHz	6	÷ 4	1.5	0	0
8 MHz	8	÷ 4	2	0	0
12 MHz	12	÷ 8	1.5	0	1
16 MHz	16	÷ 8	2	0	1
20 MHz	20	÷ 16	1.25	1	0

Figure 19
10-Bit A/D Converter Clock Selection

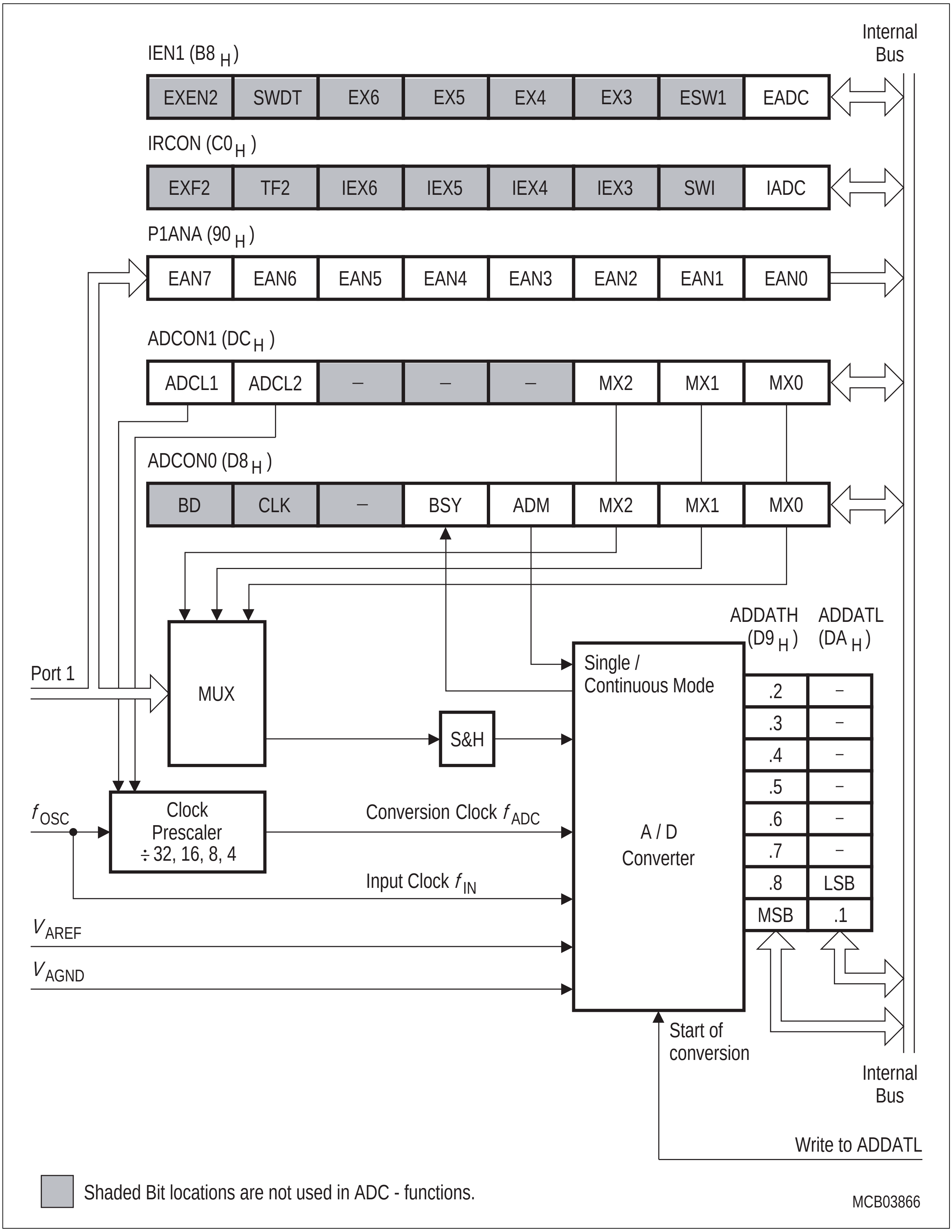


Figure 20
Block Diagram of the 10-Bit A/D Converter

Interrupt System

The C505L provides 12 interrupt vectors with four priority levels. Five interrupt requests can be generated by the on-chip peripherals (timer 0, timer 1, timer 2, serial interface, A/D converter) and six interrupts may be triggered externally (P3.2/$\overline{\text{INT0}}$, P3.3/$\overline{\text{INT1}}$, P1.0/AN0/$\overline{\text{INT3}}$/CC0, P1.1/AN1/INT4/CC1, P1.2/AN2/INT5/CC2, P1.3/AN3/INT6/CC3). Additionally, the P1.5/AN5/T2EX can trigger an interrupt. There is one software-generated interrupt (bit SWI in SFR IEN1) in addition to the above interrupts. The wake-up from power-down mode interrupt has a special functionality which allows an exit from the software power-down mode by a short low pulse at either pin P3.2/$\overline{\text{INT0}}$ or by the real-time clock interrupt.

Figure 21 to **Figure 23** give a general overview of the interrupt sources and illustrate the corresponding request and the control flags. **Table 9** lists all interrupt sources with the corresponding request flags and interrupt vector addresses.

Table 9
Interrupt Source and Vectors

Interrupt Source	Interrupt Vector Address	Interrupt Request Flags
External Interrupt 0	0003_H	IE0
Timer 0 Overflow	$000B_H$	TF0
External Interrupt 1	0013_H	IE1
Timer 1 Overflow	$001B_H$	TF1
Serial Channel	0023_H	RI / TI
Timer 2 Overflow / Ext. Reload	$002B_H$	TF2 / EXF2
A/D Converter	0043_H	IADC
Software Interrupt	$004B_H$	SWI
External interrupt 3	0053_H	IEX3
External Interrupt 4	$005B_H$	IEX4
External Interrupt 5	0063_H	IEX5
External interrupt 6	$006B_H$	IEX6
Wake-up from power-down mode	$007B_H$	IRTC (real-time clock wake-up only)

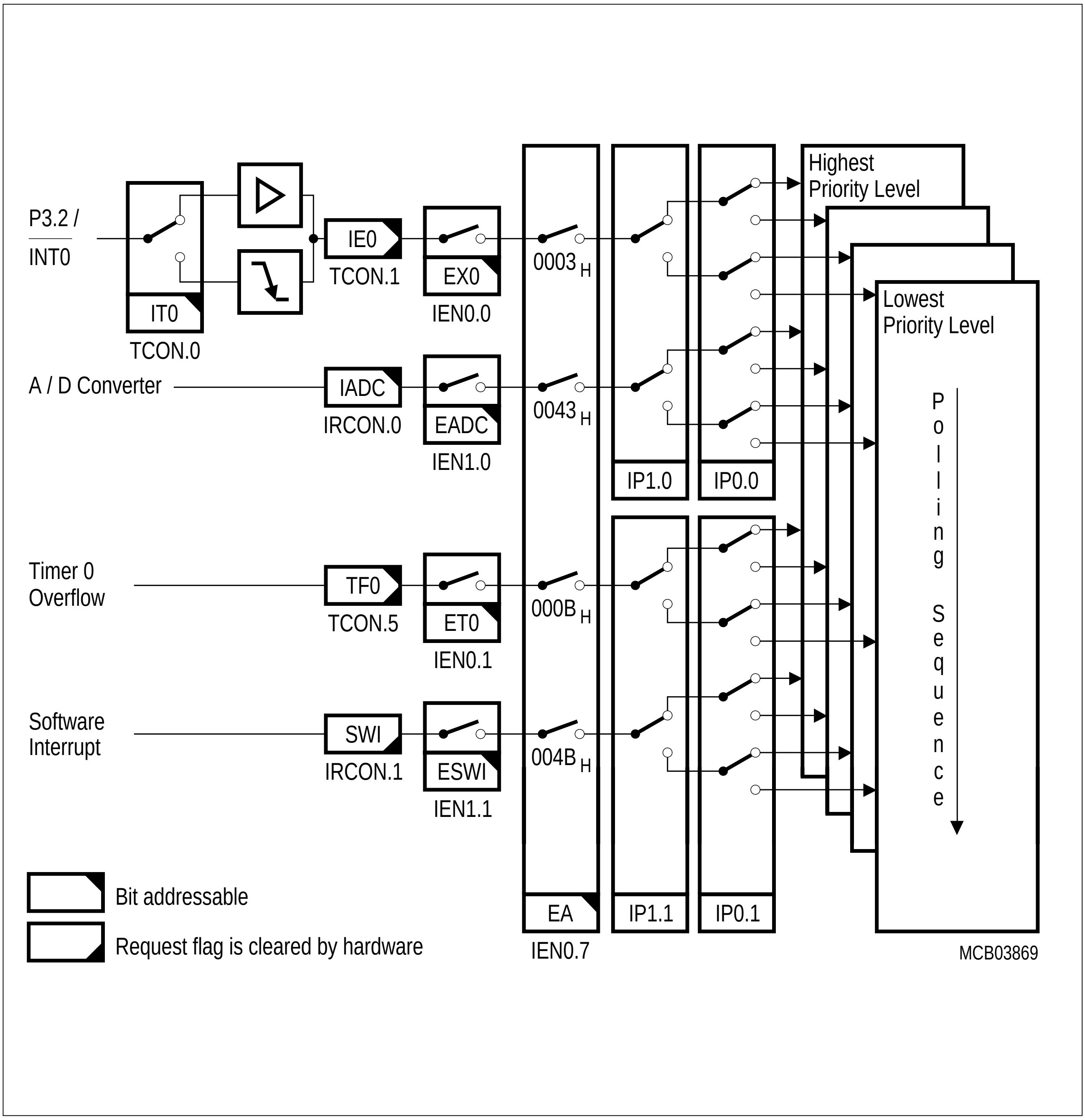


Figure 21
Interrupt Structure, Overview Part 1

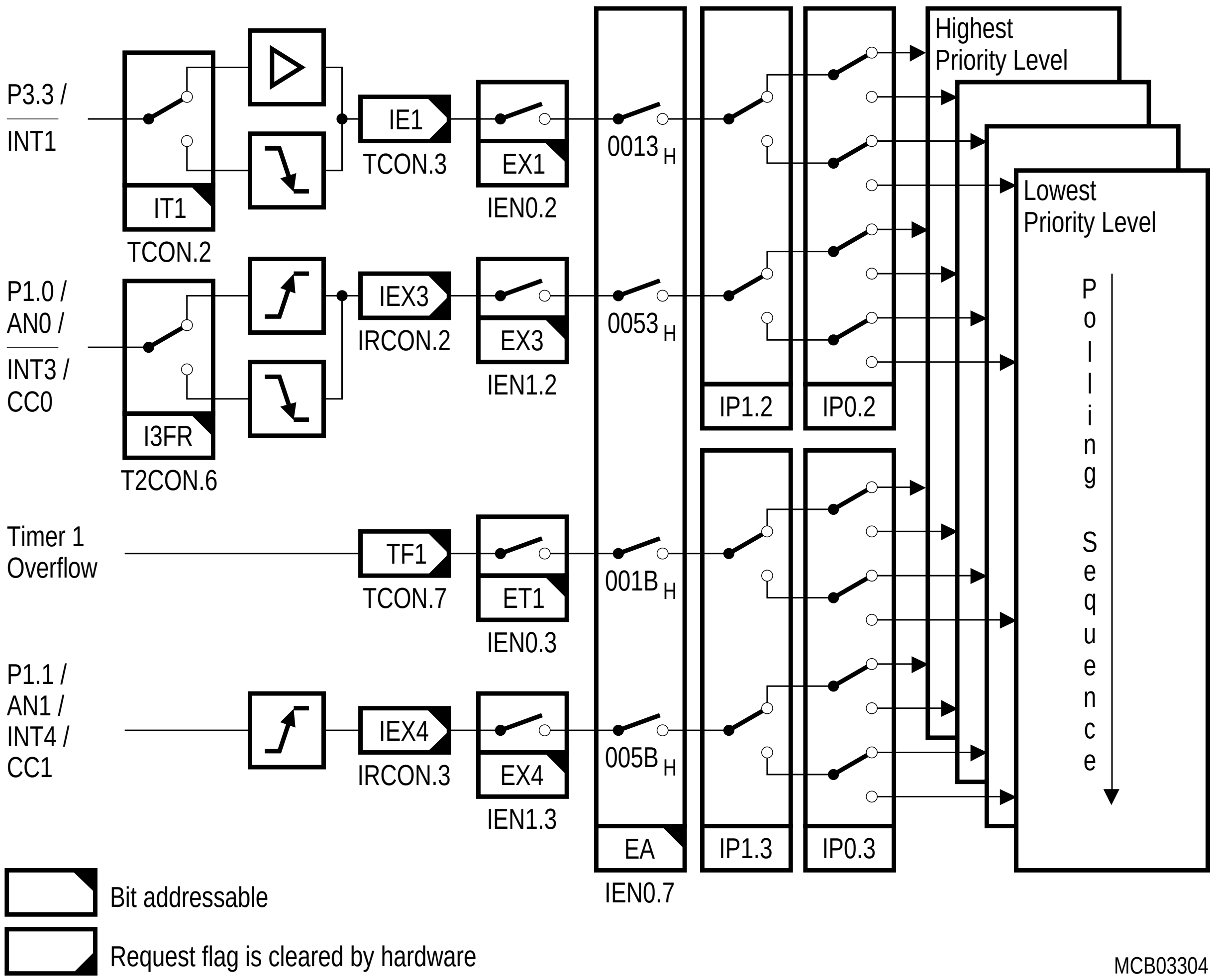


Figure 22
Interrupt Structure, Overview Part 2

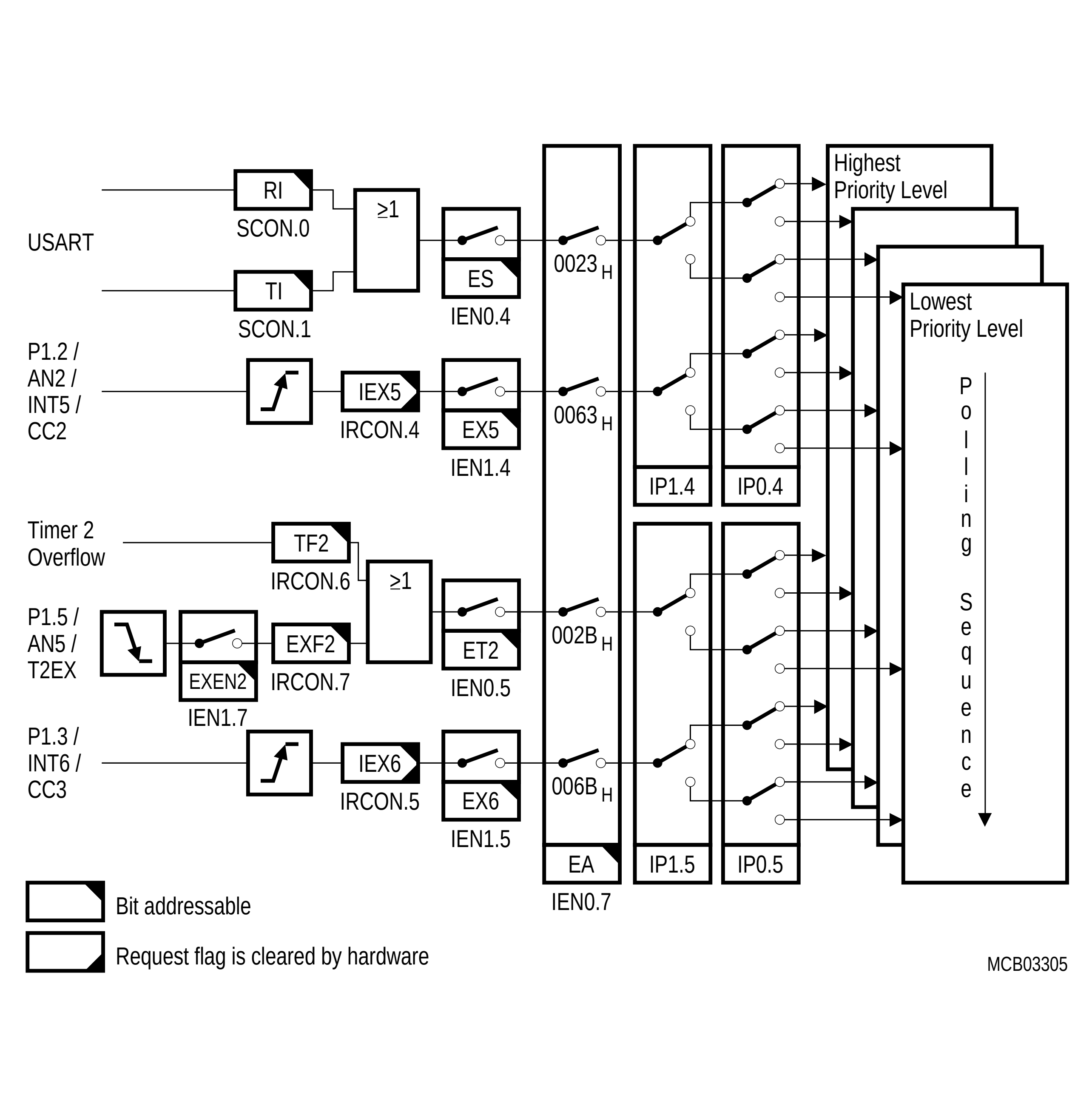


Figure 23
Interrupt Structure, Overview Part 3

Fail Save Mechanisms

The C505L offers enhanced fail safe mechanisms, which allow an automatic recovery from software upset or hardware failure:

- a programmable watchdog timer (WDT), with variable time-out period from 192 µs up to approx. 393.2 ms at 16 MHz (314.5 ms at 20 MHz).
- an oscillator watchdog (OWD) which monitors the on-chip oscillator and forces the microcontroller into reset state in case the on-chip oscillator fails; it also provides the clock for a fast internal reset after power-on.

The watchdog timer in the C505L is a 15-bit timer, which is incremented by a count rate of $f_{OSC}/12$ up to $f_{OSC}/192$. The system clock of the C505L is divided by two prescalers, a divide-by-two and a divide-by-16 prescaler. For programming of the watchdog timer overflow rate, the upper 7 bits of the watchdog timer can be written. **Figure 24** shows the block diagram of the watchdog timer unit.

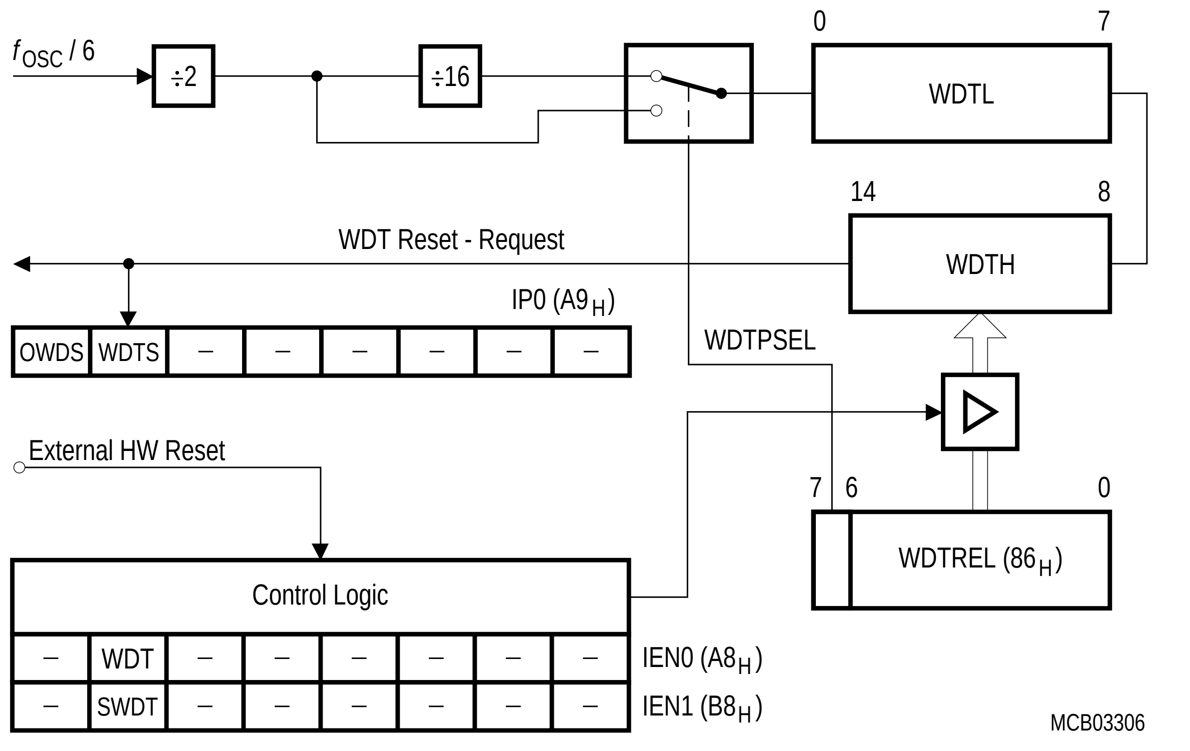


Figure 24
Block Diagram of the Watchdog Timer

The watchdog timer can be started by software (bit SWDT in SFR IEN1) but it cannot be stopped during active mode of the device. If the software fails to refresh the running watchdog timer an internal reset will be initiated on watchdog timer overflow. For refreshing of the watchdog timer the content of the SFR WDTREL is transferred to the upper 7-bit of the watchdog timer. The refresh sequence consists of two consecutive instructions which set the bits WDT and SWDT each. The reset cause (external reset or reset caused by the watchdog) can be examined by software (flag WDTS). It must be noted, however, that the watchdog timer is halted during the idle mode and power down mode of the processor.

Oscillator Watchdog

The oscillator watchdog unit serves for four functions:

– **Monitoring of the on-chip oscillator’s function**
  The watchdog supervises the on-chip oscillator’s frequency; if it is lower than the frequency of the auxiliary RC oscillator in the watchdog unit, the internal clock is supplied by the RC oscillator and the device is brought into reset; if the failure condition disappears (i.e. the on-chip oscillator has a higher frequency than the RC oscillator), the part executes a final reset phase of typ. 1 ms in order to allow the oscillator to stabilize; then the oscillator watchdog reset is released and the part starts program execution again.
– **Fast internal reset after power-on**
  The oscillator watchdog unit provides a clock supply for the reset before the on-chip oscillator has started. The oscillator watchdog unit also works identically to the monitoring function.
– **Control of wake-up from software power-down mode**
  When the software power-down mode is left by a low level at the P3.2/$\overline{\text{INT0}}$ pin or an active Real-Time Clock Interrupt Request flag IRTC, the oscillator watchdog unit assures that the microcontroller resumes operation (execution of the power-down wake-up interrupt) with the nominal clock rate. In the power-down mode the RC oscillator and the on-chip oscillator are stopped. Both oscillators are started again when power-down mode is released. When the on-chip oscillator has a higher frequency than the RC oscillator, the microcontroller starts operation after a final delay of typ. 1 ms in order to allow the on-chip oscillator to stabilize.

  Note: The oscillator watchdog unit is always enabled.

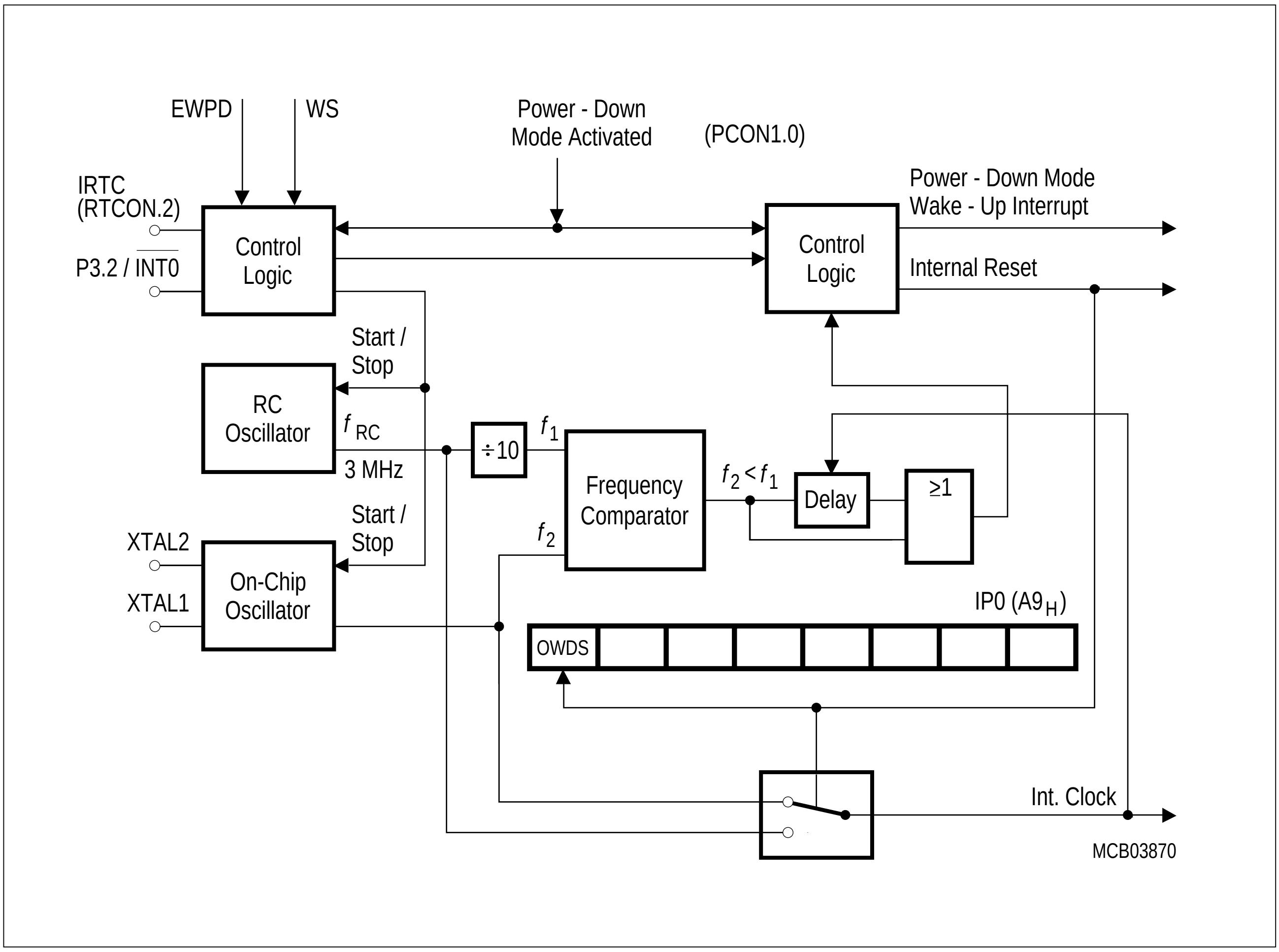


Figure 25
Block Diagram of the Oscillator Watchdog

Power Saving Modes

The C505L provides three basic power saving modes, the idle mode, the slow-down mode and the software power down mode.

- **Idle mode**
  The CPU is gated off from the oscillator. All peripherals are still provided with the clock and are able to work. Idle mode is entered by software and can be left by an interrupt or reset.
- **Slow down mode**
  The controller remains fully functional, but its normal clock frequency is internally divided by 32. This slows down all parts of the controller, the CPU and all peripherals, to 1/32 of their normal operating frequency and also reduces power consumption.
- **Software power down modes:**
  Software power-down mode 1, in which all the peripheral blocks and the CPU are stopped. This mode is used to save contents of internal RAM, XRAM and SFRs with a very low standby current.
  Software power-down mode 2, in which only the Real-time clock and LCD controller are operating. In this mode, the CPU and the rest of the peripherals are stopped. The RC oscillator and the on-chip oscillator are stopped, the real-time clock oscillator that operates with the XTAL3 and XTAL4 pins is still running and the real-time count is maintained in this mode.
  Software power-down mode 3, in which only the real-time clock is operating. In this mode, the clock input into the CPU, LCD controller and the rest of the peripherals are stopped. The only difference between this mode and mode 2 is that the LCD controller is also stopped in this mode.

In all the software power-down modes, V_{DD} can be reduced to minimize power consumption. In the case of the software power-down mode 3, V_{DD} can be reduced to **3 V** (lower specification limit). It must be ensured, however, that V_{DD} is not reduced before any of the power-down modes is invoked, and that V_{DD} is restored to its normal operating level before leaving the power-down mode.

Any of these software power-down modes can be exited either by an active reset signal or by a wake-up request. Using reset to leave power-down mode puts the microcontroller with its SFRs into the reset state. Program execution then starts from the address 0000_H. Using a wake-up request to exit the power-down mode starts the RC oscillator and the on-chip oscillator and maintains the state of the SFRs, which were frozen when power-down mode was entered.

When the C505L is in software power-down mode 1, a wake-up operation is possible only through P3.2/$\overline{\text{INT0}}$. There are two ways to use a wake-up request to exit power-down modes 2 and 3:

- Wake-up via P3.2/$\overline{\text{INT0}}$ pin, or
- Wake-up via the real-time clock interrupt

Table 10
Power Saving Modes Overview

Mode	Entering Sequence Example	Leaving by	Remarks
Idle mode	ORL PCON, #01H ORL PCON, #20H	Occurrence of an interrupt from a peripheral unit Hardware Reset	CPU clock is stopped; CPU maintains their data; peripheral units are active (if enabled) and provided with clock
Slow Down Mode	In normal mode: ORL PCON, #10H	ANL PCON,#0EFH Hardware Reset	Internal clock rate is reduced to 1/32 of its nominal frequency
	With idle mode: ORL PCON, #01H ORL PCON, #30H	Occurrence of an interrupt from a peripheral unit Hardware reset	CPU clock is stopped; CPU maintains their data; peripheral units are active (if enabled) and provided with 1/32 of its nominal frequency
Software Power Down Mode1	... bit LCEN (LCON register) is cleared; bit RTPD (RTCON register) is set; ORL PCON, #02H ORL PCON, #40H	Short low pulse at pin P3.2/$\overline{INT0}$ Hardware Reset	Oscillator is stopped; contents of on-chip RAM, XRAM and SFR's are maintained;
Software Power Down Mode 2	... bits LCEN and CSEL (LCON register) are set, bit RTPD (RTCON register) is cleared; ... ORL PCON, #02H ORL PCON, #40H	Short low pulse at pin P3.2/$\overline{INT0}$ or real-time clock wake-up interrupt Hardware Reset	Oscillator is stopped; contents of on-chip RAM, XRAM and SFR's are maintained; LCD Controller and real-time clock are functioning
Software Power Down Mode 3	... bit LCEN (LCON register) is cleared; bit RTPD (RTCON register) is cleared; ... ORL PCON, #02H ORL PCON, #40H	Short low pulse at pin P3.2/$\overline{INT0}$ or real-time clock wake-up interrupt Hardware Reset	Oscillator is stopped; contents of on-chip RAM, XRAM and SFR's are maintained; real-time clock is functioning

OTP Memory Operation

The C505L contains a 32 Kbyte one-time programmable (OTP) program memory. With the C505L fast programming cycles are achieved (1 byte in 100 µs). Also several levels of OTP memory protection can be selected.

For programming of the device, the C505L must be put into the programming mode. This typically is done not in-system but in a special programming hardware. In the programming mode the C505L operates as a slave device similar as an EPROM stand-alone memory device and must be controlled with address/data information, control lines, and an external 11.5 V programming voltage. **Figure 26** shows the pins of the C505L which are required for controlling of the OTP programming mode.

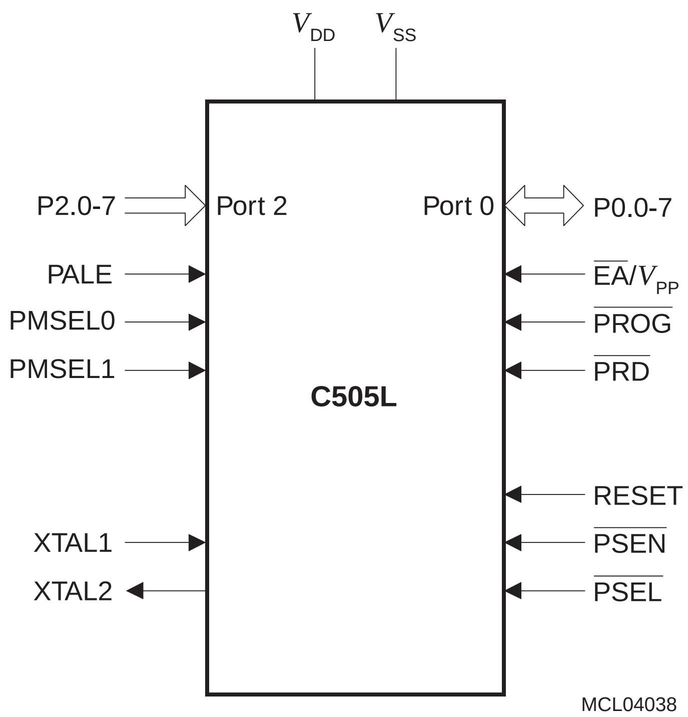


Figure 26
Programming Mode Configuration

Pin Configuration in Programming Mode

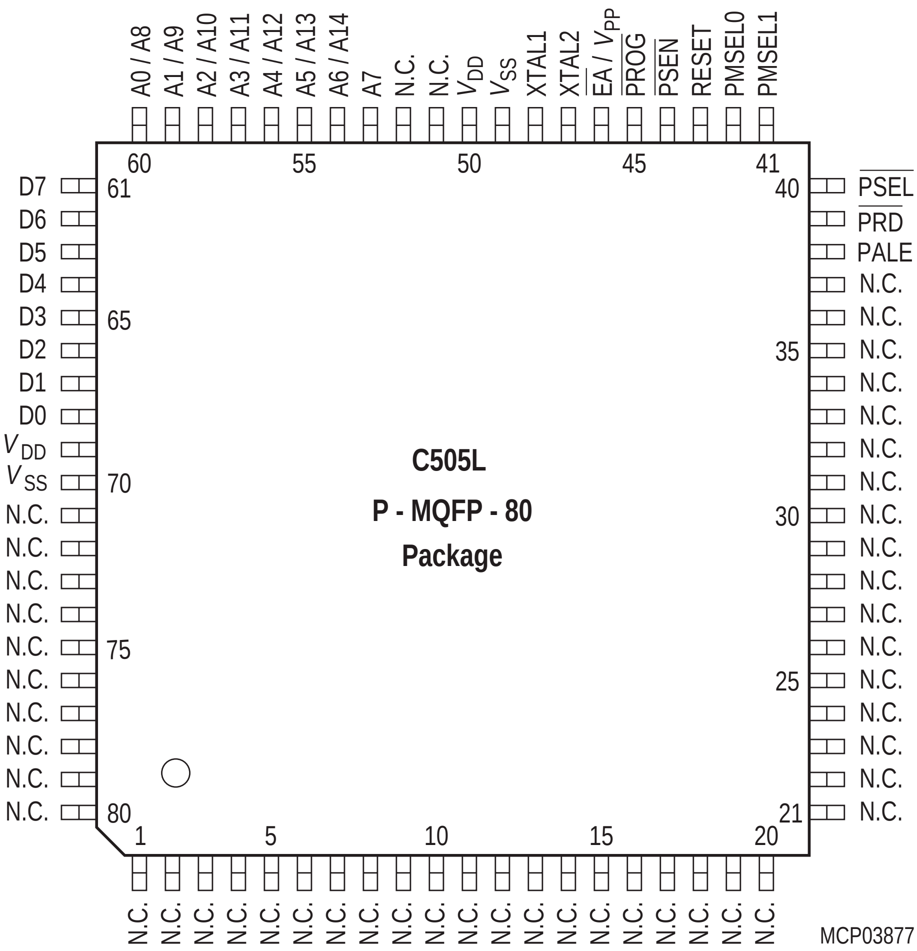


Figure 27
P-MQFP-80 Pin Configuration of the C505L in Programming Mode (top view)

Table 11 is a functional description of all C505L pins that are required for OTP memory programming.

Table 11
Pin Definitions and Functions of the C505L in Programming Mode

<table>
<tr><th rowspan="2">Symbol</th><th>Pin Number</th><th rowspan="2">I/O *)</th><th rowspan="2">Function</th></tr>
<tr><th>P-MQFP-80</th></tr>
<tr><td>RESET</td><td>43</td><td>I</td><td>Reset
This input must be at static “1” (active) level during the whole programming mode.</td></tr>
<tr><td>PMSEL0
PMSEL1</td><td>42
41</td><td>I
I</td><td>Programming Mode SELection pins
These pins are used to select the different access modes in programming mode. PMSEL1,0 must satisfy a setup time to the rising edge of PALE. When the logic level of PMSEL1,0 is changed, PALE must be at low level.
<table>
<tr><th>PMSEL1</th><th>PMSEL0</th><th>Access Mode</th></tr>
<tr><td>0</td><td>0</td><td>Reserved</td></tr>
<tr><td>0</td><td>1</td><td>Read signature bytes</td></tr>
<tr><td>1</td><td>0</td><td>Program/read lock-bits</td></tr>
<tr><td>1</td><td>1</td><td>Program/read OTP memory byte</td></tr>
</table></td></tr>
<tr><td>$\overline{\text{PSEL}}$</td><td>40</td><td>I</td><td>Basic Programming Mode SELect
This input is used for the basic programming mode selection and must be switched according to Figure 28.</td></tr>
<tr><td>$\overline{\text{PRD}}$</td><td>39</td><td>I</td><td>Programming mode ReaD strobe
This input is used for read access control for OTP memory read, version byte read, and lock-bit read operations.</td></tr>
<tr><td>PALE</td><td>38</td><td>I</td><td>Programming Address Latch Enable
PALE is used to latch the high address lines. The high address lines must satisfy a setup and hold time to/from the falling edge of PALE. PALE must be at a low level when the logic level of PMSEL1,0 is changed.</td></tr>
<tr><td>XTAL2</td><td>47</td><td>O</td><td>XTAL2
Output of the inverting oscillator amplifier.</td></tr>
<tr><td>XTAL1</td><td>48</td><td>I</td><td>XTAL1
Input to the oscillator amplifier.</td></tr>
</table>

*) I = Input
O = Output

Table 11
Pin Definitions and Functions of the C505L in Programming Mode (cont'd)

Symbol	Pin Number P-MQFP-80	I/O *)	Function
V_{SS}	49, 70	–	**Circuit ground potential** Must be applied in programming mode.
V_{DD}	50, 69	–	**Power supply terminal** Must be applied in programming mode.
A0-A7, A8-A14 (Port 2)	60-53	I	**Address lines** Multiplexed address input lines A0-A7 and A8-A14. A8-A14 must be latched with PALE.
$\overline{\text{PSEN}}$	44	I	**Program Store ENable** This input must be at static "0" level during the whole programming mode.
$\overline{\text{PROG}}$	45	I	**PROGramming mode write strobe** This input is used in programming mode as a write strobe for OTP memory program, and lock-bit write operations. During basic programming mode selection a low level must be applied to $\overline{\text{PROG}}$.
$\overline{\text{EA}}/V_{PP}$	46	–	**Programming voltage** This pin must be at 11.5 V (V_{PP}) voltage level during programming of an OTP memory byte or lock-bit. During an OTP memory read operation, this pin must be at V_{IH} high level. This pin is also used for basic programming mode selection. At basic programming mode selection a low level must be applied to $\overline{\text{EA}}/V_{PP}$.
D7-D0 (Port 0)	68-61	I/O	**Data lines 0-7** During programming mode, data bytes are transferred via the bidirectional D7-D0 lines that are located at port 0 pins.
N.C.	1-37, 51-52, 71-80	–	**Not Connected** These pins should not be connected in programming mode.

*) I = Input
O = Output

Basic Programming Mode Selection

The basic programming mode selection scheme is shown in **Figure 28**.

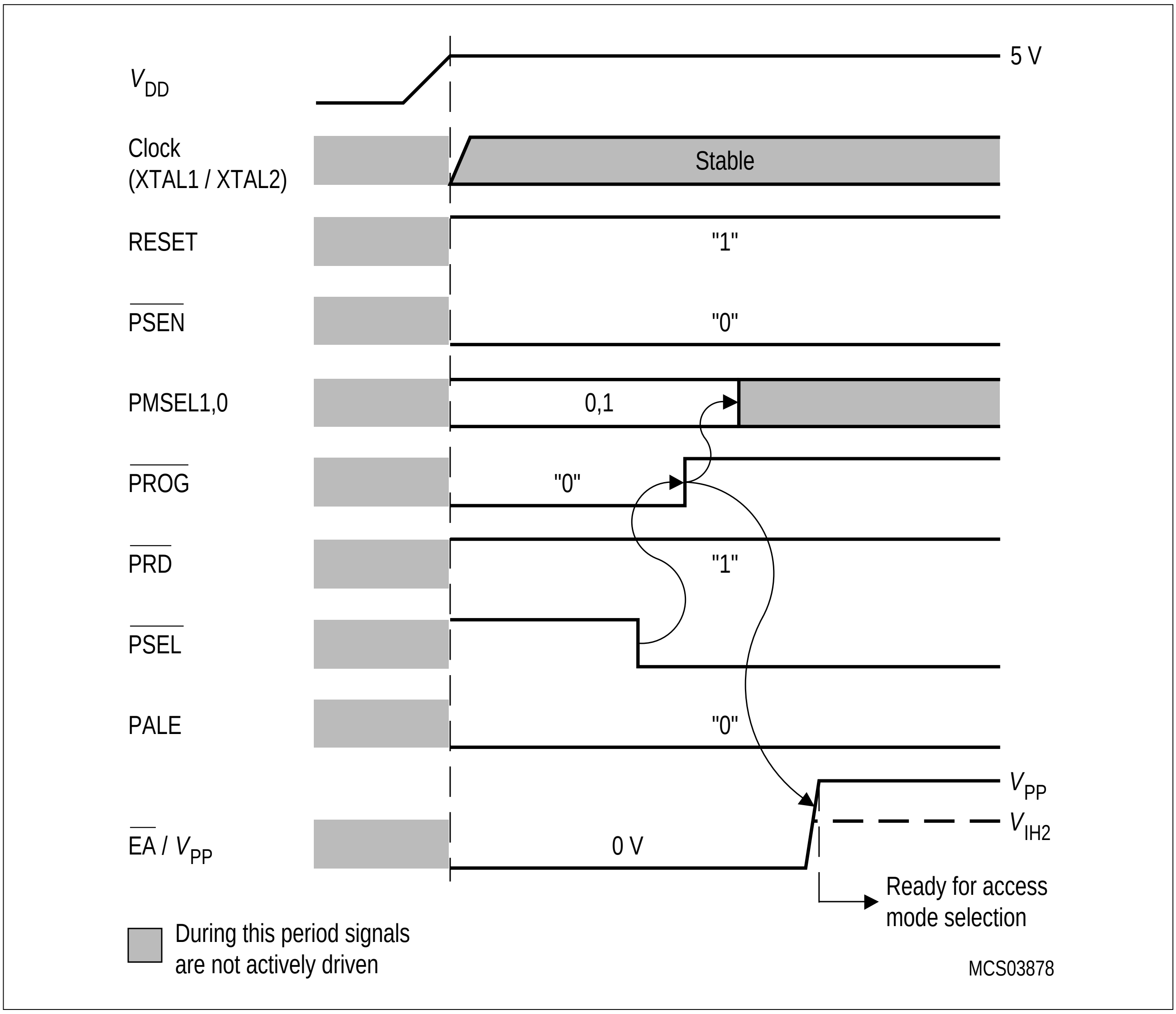


Figure 28
Basic Programming Mode Selection

Table 12
Access Modes Selection

Access Mode	$\overline{\text{EA}}$/ V_{PP}	$\overline{\text{PROG}}$	$\overline{\text{PRD}}$	**PMSEL**		Address (Port 2)	Data (Port 0)
				1	**0**		
Program OTP memory byte	V_{PP}	‾_‾	H	H	H	A0-7 A8-14	D0-7
Read OTP memory byte	V_{IH}	H	‾_‾				
Program OTP lock bits	V_{PP}	‾_‾	H	H	L	–	D1,D0 see **Table 13**
Read OTP lock bits	V_{IH}	H	‾_‾				
Read OTP version byte	V_{IH}	H	‾_‾	L	H	Byte addr. of sign. byte	D0-7

Lock Bits Programming / Read

The C505L has two programmable lock-bits that, when programmed according to **Table 13**, provide four levels of protection for the on-chip OTP code memory.

Table 13
Lock Bit Protection Types

Lock Bits at D1,D0		**Protection Level**	**Protection Type**
D1	**D0**		
1	1	Level 0	The OTP lock feature is disabled. During normal operation of the C505L, the state of the $\overline{\text{EA}}$ pin is not latched on reset.
1	0	Level 1	During normal operation of the C505L, MOVC instructions executed from external program memory are prevented from fetching code bytes from internal memory. $\overline{\text{EA}}$ is sampled and latched on reset. An OTP memory read operation is only possible in the OTP verification mode. Further programming of the OTP memory is disabled (reprogramming security).
0	1	Level 2	Same as level 1, but OTP memory read operation using OTP verification mode is disabled.
0	0	Level 3	Same as level 2, but external code execution by setting $\overline{\text{EA}}$ = low during normal operation of the C505L is not possible. External code execution, which is initiated by an internal program (e.g. by an internal jump instruction above the OTP memory boundary), is still possible.

Note: A "1" means that the lock-bit is not programmed. A "0" means that lock-bit is programmed.

Version Bytes

The steppings of the C505L versions will contain the following version register/byte information:

Stepping	Version Byte 0 = VR0 (mapped addr. FC_H)	Version Byte 1 = VR1 (mapped addr. FD_H)	Version Byte 2 = VR2 (mapped addr. FE_H)
C505L CA-Step	$C5_H$	85_H	04_H

Note: Future steppings of C505L would have a different version byte 2 content.

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Storage temperature	T_{ST}	– 40	150	°C	–
Voltage on V_{DD} pins with respect to ground (V_{SS})	V_{DD}	– 0.5	6.5	V	–
Voltage on any pin with respect to ground (V_{SS})	V_{IN}	– 0.5	V_{DD} + 0.5	V	–
Input current on any pin during overload condition	–	– 10	10	mA	–
Absolute sum of all input currents during overload condition	–	–	| 100 mA |	mA	–
Power dissipation	P_{DISS}	–	1	W	–

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for longer periods may affect device reliability. During absolute maximum rating overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$) the voltage on V_{DD} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

Operating Conditions

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Supply Voltage (Normal mode)	V_{DD}	4.25	5.5	V	–
Supply Voltage (Software Power down mode 3 only)		3		V	Not during wake-up sequence.
Ground voltage	V_{SS}	0		V	–
Ambient temperature				°C	–
SAB-C505L	T_A	0	70		
SAF-C505L	T_A	– 40	85		
SAK-C505L	T_A	– 40	125		
Analog reference voltage	V_{AREF}	4	V_{DD} + 0.1	V	–
Analog ground voltage	V_{AGND}	V_{SS} – 0.1	V_{SS} + 0.2	V	–
Analog input voltage	V_{AIN}	V_{AGND}	V_{AREF}	V	–
CPU clock	f_{CPU}	2	20	MHz	–

DC Characteristics
(Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltages all except $\overline{\text{EA}}$, RESET, XTAL3 $\overline{\text{EA}}$ pin RESET pin XTAL3	 V_{IL} V_{IL1} V_{IL2} V_{IL3}	 – 0.5 – 0.5 – 0.5 – 0.5	 0.2 V_{DD} – 0.1 0.2 V_{DD} – 0.3 0.2 V_{DD} + 0.1 0.7 V_{DD}	 V V V V	 – – – –
Input high voltages except XTAL1, RESET, XTAL3 and $\overline{\text{EA}}$ XTAL1 RESET, $\overline{\text{EA}}$ XTAL3	 V_{IH} V_{IH1} V_{IH2} V_{IH3}	 0.2 V_{DD} + 0.9 0.7 V_{DD} 0.6 V_{DD} 0.9 V_{DD}	 V_{DD} + 0.5 V_{DD} + 0.5 V_{DD} + 0.5 V_{DD} + 0.5	 V V V V	 – – – –
Output low voltages Ports 1, 2, 3, 4, 5 Port 0, ALE, $\overline{\text{PSEN}}$	 V_{OL} V_{OL1}	 – –	 0.45 0.45	 V V	 I_{OL} = 1.6 mA [1] I_{OL} = 3.2 mA [1]
Output high voltages Ports 1, 2, 3, 4, 5 Port 0 in external bus mode, ALE, $\overline{\text{PSEN}}$	 V_{OH} V_{OH2}	 2.4 0.9 V_{DD} 2.4 0.9 V_{DD}	 – – – –	 V V V V	 I_{OH} = – 80 µA I_{OH} = – 10 µA I_{OH} = – 800 µA [2] I_{OH} = – 80 µA [2]
Logic 0 input current Ports 1, 2, 3, 4, 5	 I_{IL}	 – 10	 – 70	 µA	 V_{IN} = 0.45 V
Logical 0-to-1 transition current Ports 1, 2, 3, 4, 5	I_{TL}	– 65	– 650	µA	V_{IN} = 2 V
Input leakage current Port 0, AN0-7(Port 1), $\overline{\text{EA}}$	 I_{LI}	 –	 ± 1	 µA	 0.45 < V_{IN} < V_{DD}
Pin capacitance	C_{IO}	–	10	pF	f_c = 1 MHz, T_A = 25 °C
Overload current	I_{OV}	–	± 5	mA	[8] [9]
Programming voltage	V_{PP}	10.9	12.1	V	11.5 V 5% [12]
Supply current at $\overline{\text{EA}}$/V_{PP}	–	–	30	mA	[12]

Notes see **Page 63**.

Power Supply Current

(Operating Conditions apply)

Parameter		Symbol	Limit Values		Unit	Test Condition
			typ.[10]	max.[11]		
Active Mode	16 MHz 20 MHz	I_{DD} I_{DD}	28.7 34.0	36.6 43.0	mA	[4]
Idle Mode	16 MHz 20 MHz	I_{DD} I_{DD}	13.7 15.9	19.4 22.0	mA	[5]
Active Mode with slow-down enabled	16 MHz 20 MHz	I_{DD} I_{DD}	5.7 6.2	7.6 8.1	mA	[6]
Idle Mode with slow-down enabled	16 MHz 20 MHz	I_{DD} I_{DD}	4.7 4.9	7.5 8.0	mA	[7]
Power down current: Software Power-down mode 1 Software Power-down mode 2 Software Power-down mode 3		 I_{PD1} I_{PD2} I_{PD3}	 20 250 20	 50 300 50	 µA µA µA	 V_{DD} = 2…5.5 V[3] V_{DD} = 4.25 – 5.5 V[3] V_{DD} = 3…5.5 V[3]

Notes see next page.

Notes:

1) Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and port 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation. In the worst case (capacitive loading > 100 pF), the noise pulse on ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a schmitt-trigger, or use an address latch with a schmitt-trigger strobe input.

2) Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the 0.9 V_{DD} specification when the address lines are stabilizing.

3) Power-down modes:
I_{PD1} is measured under following conditions:
$\overline{EA}$ = Port 0 = V_{DD} ; RESET = V_{SS}.; XTAL2 = XTAL4 = N.C.; XTAL1 = XTAL3 =V_{SS} ; V_{AGND} = V_{SS}; V_{AREF} = V_{DD} ; all other pins are disconnected.

Conditions for I_{PD2} and I_{PD3} are similar except that XTAL3 and XTAL4 have a valid input from the 32.768 KHz crystal and the power supply limits.

4) I_{DD} (active mode) is measured with:
XTAL1 driven with t_R /t_F = 5 ns, 50% duty cycle , V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{DD} – 0.5 V; XTAL2 = N.C.; $\overline{EA}$ = Port0 = RESET = V_{DD}; all other pins are disconnected. I_{DD} would be slightly higher if a crystal oscillator is used (approx. 1 mA)

5) I_{DD} (idle mode) is measured with all output pins disconnected and with all peripherals disabled;
XTAL1 driven with t_R/t_F = 5 ns, 50% duty cycle, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{DD} – 0.5 V; XTAL2 = N.C.;
RESET = $\overline{EA}$ = V_{SS} ; Port0 = V_{DD} ; all other pins are disconnected; the microcontroller is put into idle mode by software;

6) I_{DD} (active mode with slow-down) is measured with all output pins disconnected and with all peripherals disabled; XTAL1 driven with t_R/t_F = 5 ns, 50% duty cycle, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{DD} – 0.5 V; XTAL2 = N.C.;
RESET = $\overline{EA}$ = V_{SS} ; all other pins are disconnected; the microcontroller is put into slow-down mode by software;

7) I_{DD} (idle mode with slow-down) is measured with all output pins disconnected and with all peripherals disabled;
XTAL1 driven with t_R/t_F = 5 ns, 50% duty cycle, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{DD} – 0.5 V; XTAL2 = N.C.;
RESET = $\overline{EA}$ = V_{SS} ; Port0 = V_{DD} ; all other pins are disconnected; the microcontroller is put into idle mode with slow-down enabled by software;

8) Overload conditions under operating conditions occur if the voltage on the respective pin exceeds the specified operating range (i.e. $V_{OV} > V_{DD} + 0.5V$ or $V_{OV} < V_{SS} - 0.5V$). The absolute sum of input overload currents on all port pins may not exceed **50 mA**. The supply voltage (V_{DD} and V_{SS}) must remain within the specified limits.

9) Not 100% tested, guaranteed by design characterization

10) The typical I_{DD} values are periodically measured at T_A = + 25 °C but not 100% tested.

11) The maximum I_{DD} values are measured under worst case conditions (T_A = 0 °C or – 40 °C and V_{DD} = 5.5 V)

12) Only valid in programming mode.

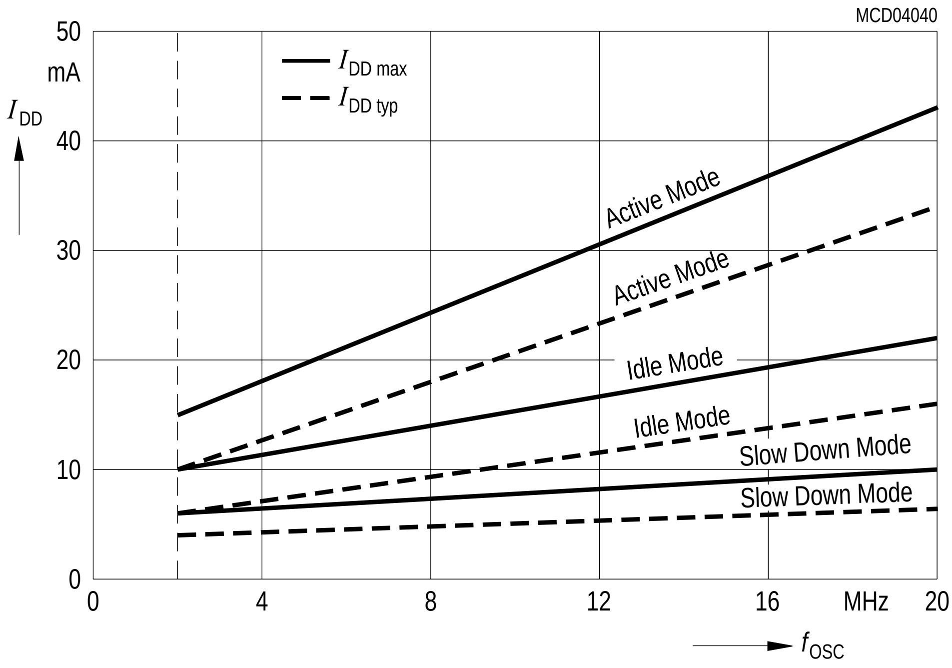


Figure 29
I_{DD} Diagram

Table 14
Power Supply Current Calculation Formulas

Parameter	**Symbol**	**Formula**
Active mode	$I_{DD\,typ}$ $I_{DD\,max}$	$1.33 \times f_{OSC} + 7.33$ $1.61 \times f_{OSC} + 10.8$
Idle mode	$I_{DD\,typ}$ $I_{DD\,max}$	$0.54 \times f_{OSC} + 5.07$ $0.66 \times f_{OSC} + 8.83$
Active mode with slow-down enabled	$I_{DD\,typ}$ $I_{DD\,max}$	$0.12 \times f_{OSC} + 3.87$ $0.12 \times f_{OSC} + 5.77$
Idle mode with slow-down enabled	$I_{DD\,typ}$ $I_{DD\,max}$	$0.05 \times f_{OSC} + 3.9$ $0.12 \times f_{OSC} + 5.67$

Note: 1. f_{OSC} is the oscillator frequency in MHz. I_{DD} values are given in mA.
2. I_{DD} graph for idle mode with slow-down enabled is not shown since it is very similar to active mode with slow-down enabled.

LCD-Output Characteristics

(Operating Conditions apply)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Full range output voltage, of D/A Converter	V_O	0	–	4.75 ± 7%	V V	Normal mode V_{DD} range (operating conditions)
Settling Time of D/A Converter Output	t_{SET}	–	–	350	S	V_{DD} = 5 V
DC differential non-linearity of D/A Converter	*DNL*	–	–	1	LSB	–
DC integral non-linearity of D/A Converter	*INL*	–	–	6	%	V_{DD} = 5 V
DC Offset Voltage of D/A Converter	–	–	–	15	mV	–
LCD Voltage levels	V_{LCD1} V_{LCD2} V_{LCD3}	–	V_O $2 \times V_O/3$ $V_O/3$	–	V	1)

Note: 1) Conditions as in V_O apply.

A/D Converter Characteristics

(Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Analog input voltage	V_{AIN}	V_{AGND}	V_{AREF}	V	1)
Sample time	t_S	–	$64 \times t_{IN}$ $32 \times t_{IN}$ $16 \times t_{IN}$ $8 \times t_{IN}$	ns	Prescaler ÷ 32 Prescaler ÷ 16 Prescaler ÷ 8 Prescaler ÷ 4 2)
Conversion cycle time	t_{ADCC}	–	$384 \times t_{IN}$ $192 \times t_{IN}$ $96 \times t_{IN}$ $48 \times t_{IN}$	ns	Prescaler ÷ 32 Prescaler ÷ 16 Prescaler ÷ 8 Prescaler ÷ 4 3)
Total unadjusted error	T_{UE}	–	± 2	LSB	V_{SS} + 0.5 V ≤ V_{AIN} ≤ V_{DD} – 0.5 V 4)
		–	± 4	LSB	V_{SS} < V_{AIN} < V_{DD} + 0.5 V V_{DD} – 0.5 V < V_{AIN} < V_{DD} 4)
Internal resistance of reference voltage source	R_{AREF}	–	t_{ADC} / 250 – 0.25	kΩ	t_{ADC} in [ns] 5) 6)
Internal resistance of analog source	R_{ASRC}	–	t_S / 500 – 0.25	kΩ	t_S in [ns] 2) 6)

Notes see next page.

Clock Calculation Table:

Clock Prescaler Ratio	ADCL1, 0		t_{ADC}	t_S	t_{ADCC}
÷ 32	1	1	$32 \times t_{IN}$	$64 \times t_{IN}$	$384 \times t_{IN}$
÷ 16	1	0	$16 \times t_{IN}$	$32 \times t_{IN}$	$192 \times t_{IN}$
÷ 8	0	1	$8 \times t_{IN}$	$16 \times t_{IN}$	$96 \times t_{IN}$
÷ 4	0	0	$4 \times t_{IN}$	$8 \times t_{IN}$	$48 \times t_{IN}$

Further timing conditions: t_{ADC} min = 500 ns
$t_{IN} = 1 / f_{OSC} = t_{CLP}$

Notes:

1) V_{AIN} may exceed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be $X000_H$ or $X3FF_H$, respectively.

2) During the sample time the input capacitance C_{AIN} must be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach their final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result.

3) This parameter includes the sample time t_S, the time for determining the digital result and the time for the calibration. Values for the conversion clock t_{ADC} depend on programming and can be taken from the table on the previous page.

4) T_{UE} is tested at V_{AREF} = 5.0 V, V_{AGND} = 0 V, V_{DD} = 4.9 V. It is guaranteed by design characterization for all other voltages within the defined voltage range.
If an overload condition occurs on maximum 2 unused analog input pins and the absolute sum of input overload currents on all analog input pins does not exceed 10 mA, an additional conversion error of 1/2 LSB is permissible.

5) During the conversion the ADC's capacitance must be repeatedly charged or discharged. The internal resistance of the reference source must allow the capacitance to reach their final voltage level within the indicated time. The maximum internal resistance results from the programmed conversion timing.

6) Not 100% tested, but guaranteed by design characterization.

AC Characteristics (16 MHz, 0.4 to 0.6 Duty Cycle)

(Operating Conditions apply)

(C_L for port 0, ALE and $\overline{\text{PSEN}}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		16-MHz clock Duty Cycle 0.4 to 0.6		Variable Clock 1/CLP= 2 MHz to 16 MHz		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	48	–	CLP – 15	–	ns
Address setup to ALE	t_{AVLL}	10	–	TCL_{Hmin} – 15	–	ns
Address hold after ALE	t_{LLAX}	10	–	TCL_{Hmin} – 15	–	ns
ALE to valid instruction in	t_{LLIV}	–	75	–	2 CLP – 50	ns
ALE to $\overline{\text{PSEN}}$	t_{LLPL}	10	–	TCL_{Lmin} – 15	–	ns
$\overline{\text{PSEN}}$ pulse width	t_{PLPH}	73	–	CLP+ TCL_{Hmin} – 15	–	ns
$\overline{\text{PSEN}}$ to valid instruction in	t_{PLIV}	–	38	–	CLP + TCL_{Hmin} – 50	ns
Input instruction hold after $\overline{\text{PSEN}}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{\text{PSEN}}$	t_{PXIZ} *)	–	15	–	TCL_{Lmin} – 10	ns
Address valid after $\overline{\text{PSEN}}$	t_{PXAV} *)	20	–	TCL_{Lmin} – 5	–	ns
Address to valid instruction in	t_{AVIV}	–	95	–	2 CLP + TCL_{Hmin} – 55	ns
Address float to $\overline{\text{PSEN}}$	t_{AZPL}	– 5	–	– 5	–	ns

*) Interfacing the C505L to devices with float times up to 20 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics (16 MHz, 0.4 to 0.6 Duty Cycle) (cont'd)

External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		16-MHz clock Duty Cycle 0.4 to 0.6		Variable Clock 1/CLP= 2 MHz to 16 MHz		
		min.	max.	min.	max.	
RD pulse width	t_{RLRH}	158	–	3 CLP – 30	–	ns
WR pulse width	t_{WLWH}	158	–	3 CLP – 30	–	ns
Address hold after ALE	t_{LLAX2}	48	–	CLP – 15	–	ns
RD to valid data in	t_{RLDV}	–	100	–	2 CLP + TCL_{Hmin} – 50	ns
Data hold after RD	t_{RHDX}	0	–	0	–	ns
Data float after RD	t_{RHDZ}	–	51	–	CLP – 12	ns
ALE to valid data in	t_{LLDV}	–	200	–	4 CLP – 50	ns
Address to valid data in	t_{AVDV}	–	200	–	4 CLP + TCL_{Hmin} – 75	ns
ALE to WR or RD	t_{LLWL}	73	103	CLP + TCL_{Lmin} – 15	CLP+ TCL_{Lmin} + 15	ns
Address valid to WR	t_{AVWL}	95	–	2 CLP – 30	–	ns
WR or RD high to ALE high	t_{WHLH}	10	40	TCL_{Hmin} – 15	TCL_{Hmin} + 15	ns
Data valid to WR transition	t_{QVWX}	5	–	TCL_{Lmin} – 20	–	ns
Data setup before WR	t_{QVWH}	163	–	3 CLP + TCL_{Lmin} – 50	–	ns
Data hold after WR	t_{WHQX}	5	–	TCL_{Hmin} – 20	–	ns
Address float after RD	t_{RLAZ}	–	0	–	0	ns

AC Characteristics (16 MHz, 0.4 to 0.6 Duty Cycle) (cont'd)

External Clock Drive Characteristics

Parameter	Symbol	CPU Clock = 16 MHz Duty Cycle 0.4 to 0.6		Variable CPU Clock 1/CLP = 2 to 16 MHz		Unit
		min.	**max.**	**min.**	**max.**	
Oscillator period	CLP	62.5	62.5	62.5	500	ns
High time	TCL_H	25	–	25	$CLP - TCL_L$	ns
Low time	TCL_L	25	–	25	$CLP - TCL_H$	ns
Rise time	t_R	–	10	–	10	ns
Fall time	t_F	–	10	–	10	ns
Oscillator duty cycle	DC	0.4	0.6	25 / CLP	1 – 25 / CLP	–
Clock cycle	TCL	25	37.5	$CLP \times DC_{min}$	$CLP \times DC_{max}$	ns

Note: The 16 MHz values in the tables are given as an example for a typical duty cycle variation of the oscillator clock from 0.4 to 0.6.

AC Characteristics (20 MHz, 0.5 Duty Cycle)

(Operating Conditions apply)

C_L for port 0, ALE and $\overline{\text{PSEN}}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		20 MHz clock 0.5 Duty Cycle		Variable Clock 1/CLP = 2 MHz to 20 MHz		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	35	–	CLP – 15	–	ns
Address setup to ALE	t_{AVLL}	10	–	CLP/2 – 15	–	ns
Address hold after ALE	t_{LLAX}	10	–	CLP/2 – 15	–	ns
ALE to valid instruction in	t_{LLIV}	–	55	–	2 CLP – 45	ns
ALE to $\overline{\text{PSEN}}$	t_{LLPL}	10	–	CLP/2 – 15	–	ns
$\overline{\text{PSEN}}$ pulse width	t_{PLPH}	60	–	3/2 CLP – 15	–	ns
$\overline{\text{PSEN}}$ to valid instruction in	t_{PLIV}	–	25	–	3/2 CLP – 50	ns
Input instruction hold after $\overline{\text{PSEN}}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{\text{PSEN}}$	t_{PXIZ} *)	–	20	–	CLP/2 – 5	ns
Address valid after $\overline{\text{PSEN}}$	t_{PXAV} *)	20	–	CLP/2 – 5	–	ns
Address to valid instruction in	t_{AVIV}	–	65	–	5/2 CLP – 60	ns
Address float to $\overline{\text{PSEN}}$	t_{AZPL}	– 5	–	– 5	–	ns

*) Interfacing the C505L to devices with float times up to 20 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics (20 MHz, 0.5 Duty Cycle) (cont'd)

External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		20 MHz clock 0.5 Duty Cycle		Variable Clock 1/CLP = 2 MHz to 20 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	120	–	3 CLP – 30	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	120	–	3 CLP – 30	–	ns
Address hold after ALE	t_{LLAX2}	35	–	CLP – 15	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	75	–	5/2 CLP– 50	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	38	–	CLP – 12	ns
ALE to valid data in	t_{LLDV}	–	150	–	4 CLP – 50	ns
Address to valid data in	t_{AVDV}	–	150	–	9/2 CLP – 75	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	60	90	3/2 CLP – 15	3/2 CLP + 15	ns
Address valid to $\overline{WR}$	t_{AVWL}	70	–	2 CLP – 30	–	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	10	40	CLP/2 – 15	CLP/2 + 15	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	5	–	CLP/2 – 20	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	125	–	7/2 CLP – 50	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	5	–	CLP/2 – 20	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

External Clock Drive Characteristics

Parameter	Symbol	Limit Values		Unit
		Variable Clock Freq. = 2 MHz to 20 MHz		
		min.	max.	
Oscillator period	CLP	50	500	ns
High time	TCL_H	15	CLP – TCL_L	ns
Low time	TCL_L	15	CLP – TCL_H	ns
Rise time	t_R	–	10	ns
Fall time	t_F	–	10	ns
Oscillator duty cycle	DC	0.5	0.5	–

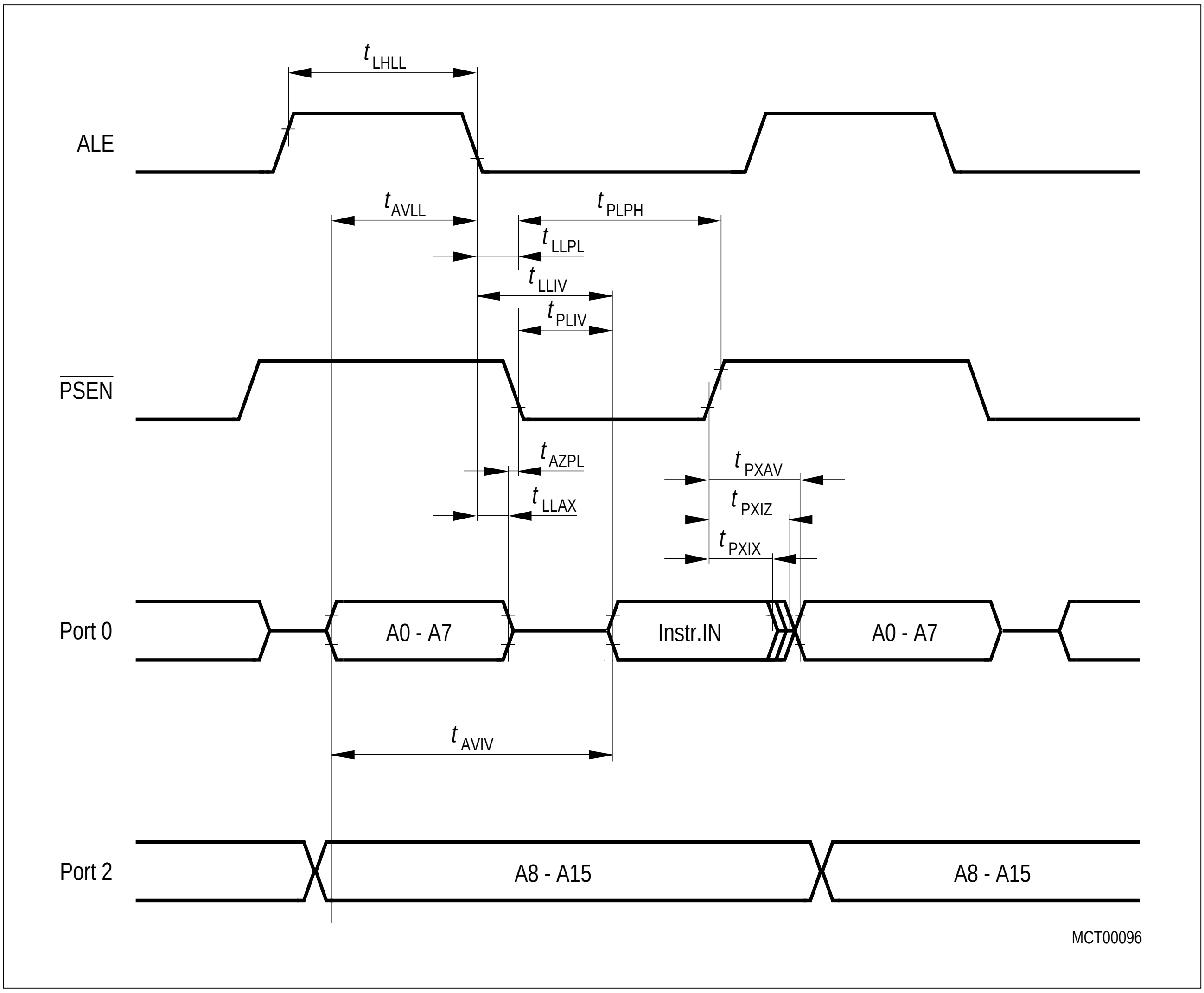


Figure 30
Program Memory Read Cycle

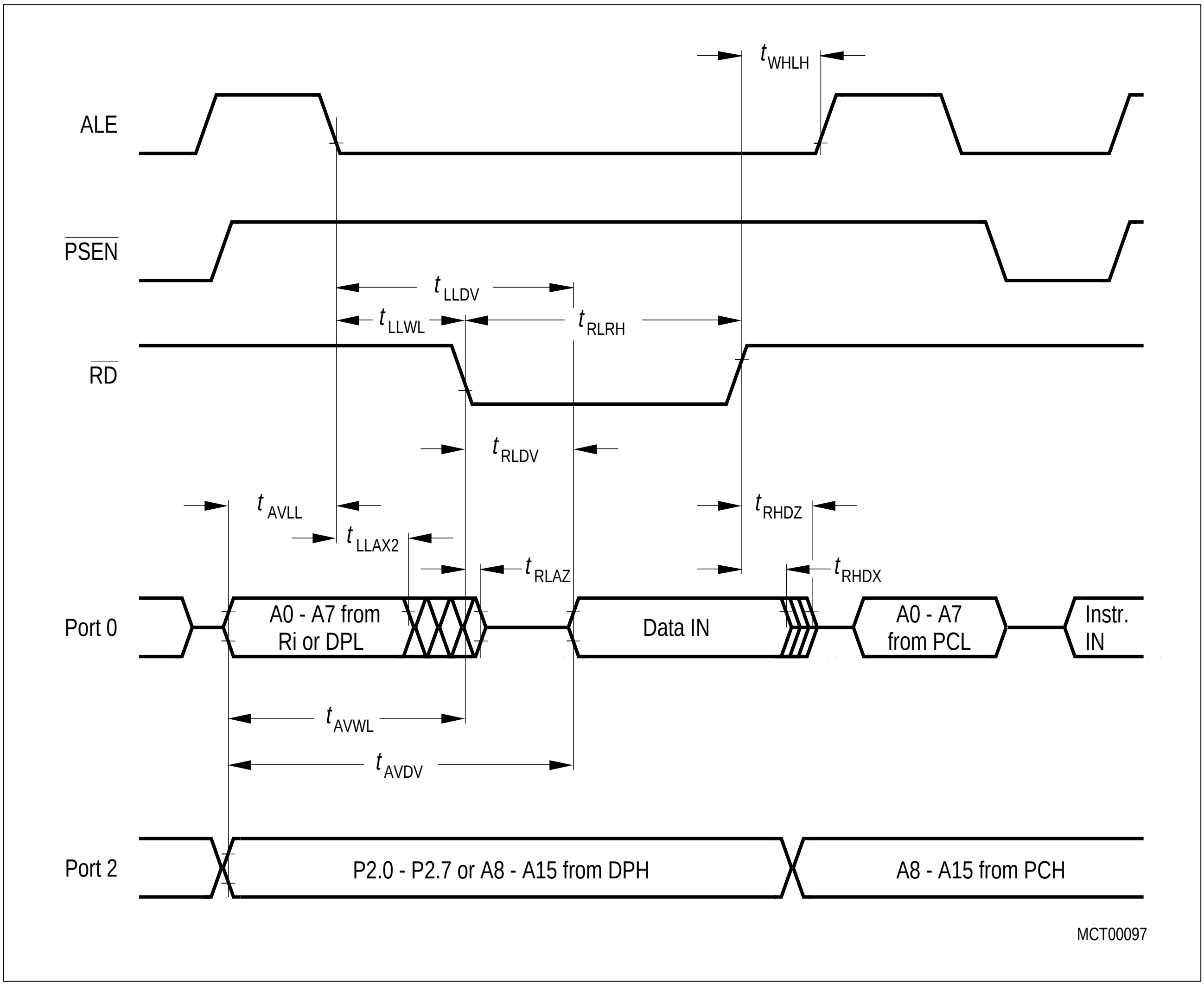


Figure 31
Data Memory Read Cycle

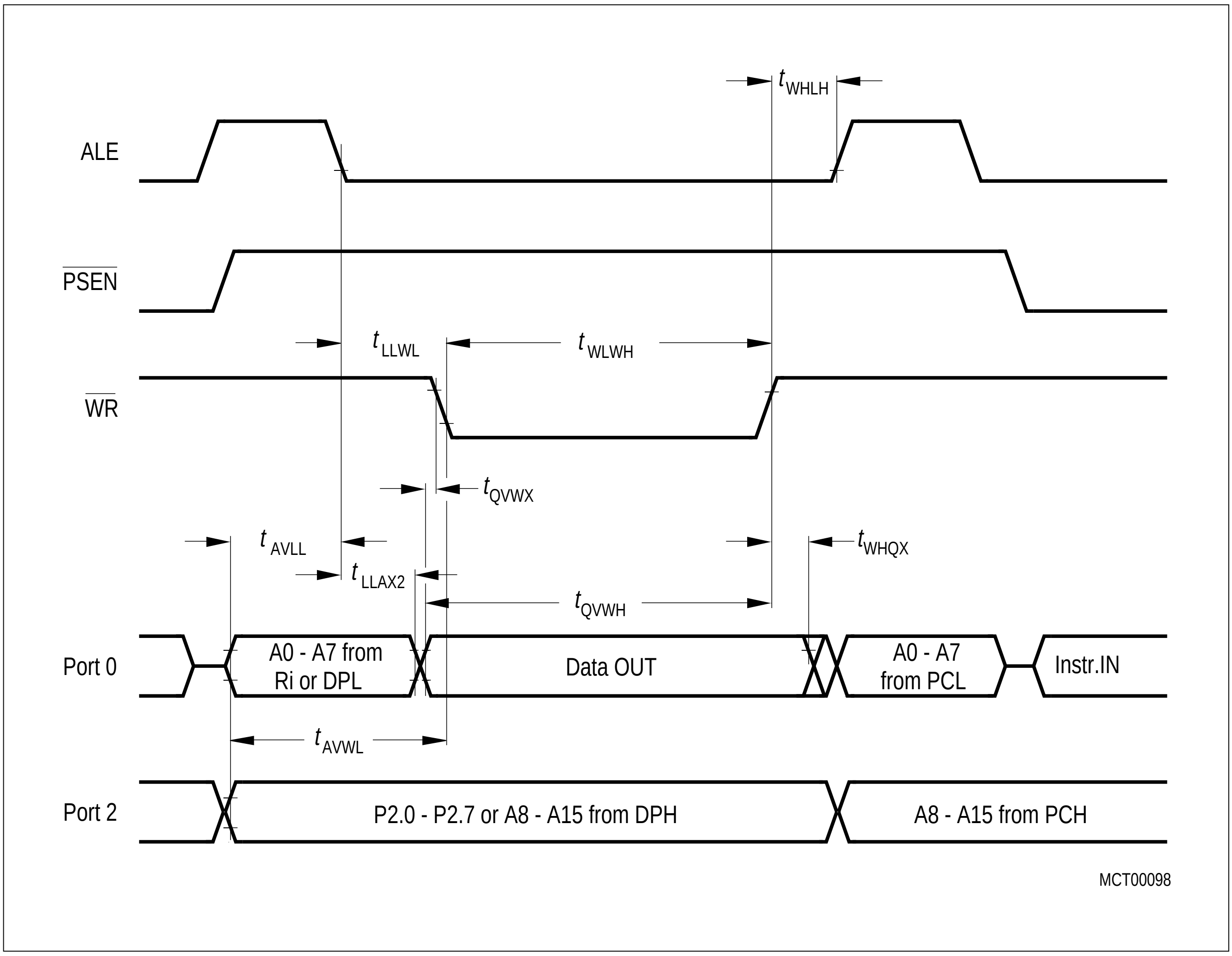


Figure 32
Data Memory Write Cycle

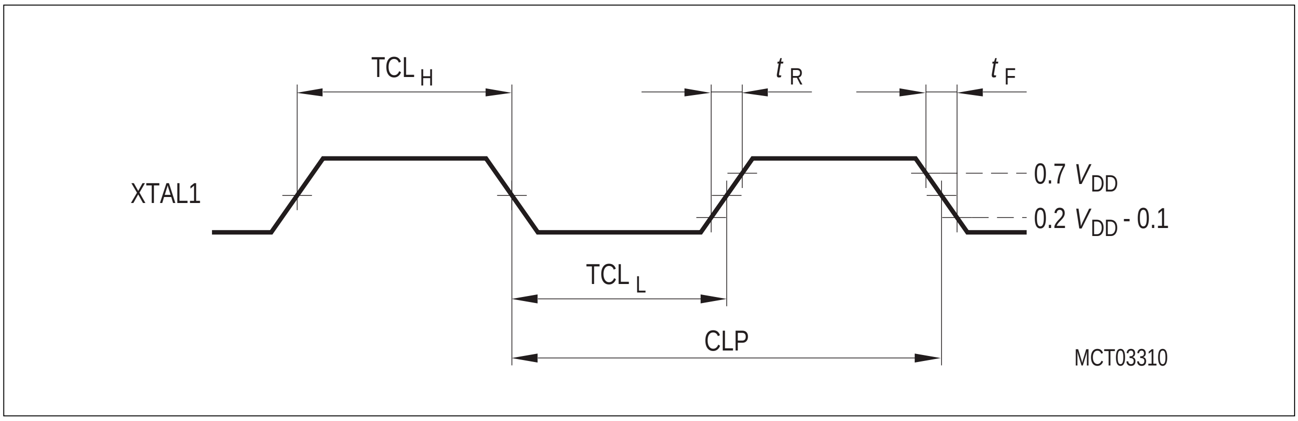
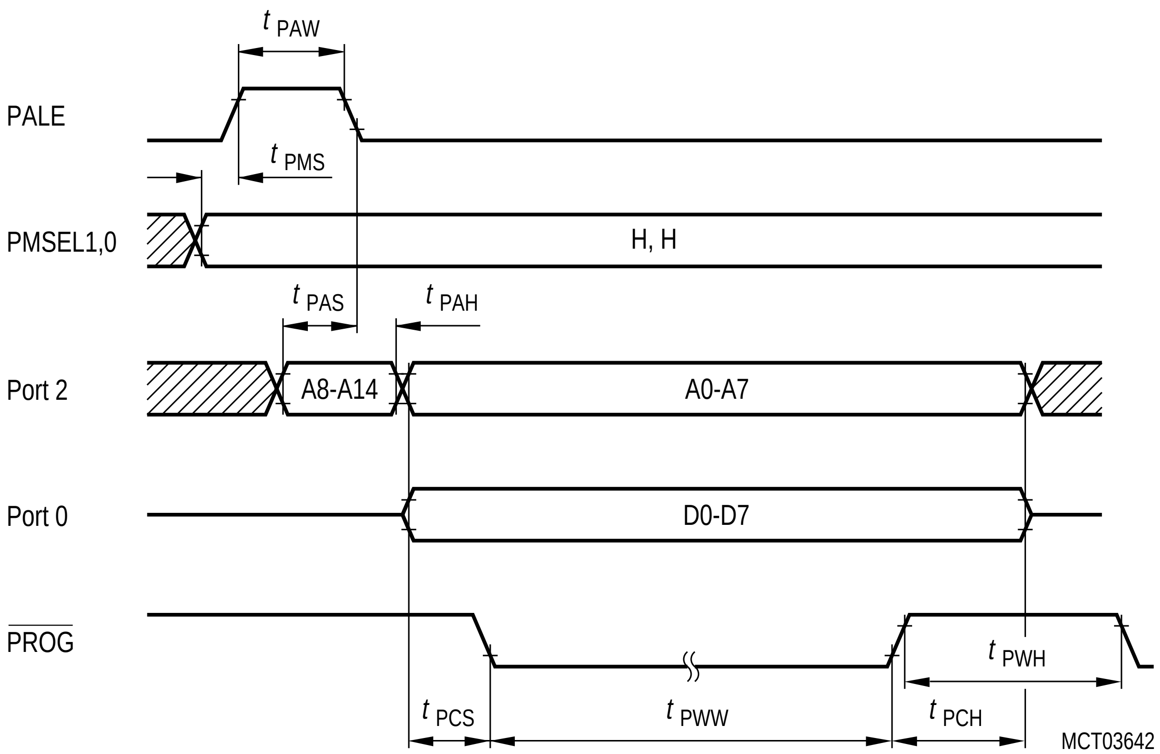


Figure 33
External Clock Drive on XTAL1

AC Characteristics of Programming Mode

V_{DD} = 5 V 10 %; V_{PP} = 11.5 V 5 %; T_A = 25 °C ± 10 °C

Parameter	Symbol	Limit Values		Unit
		min.	**max.**	
PALE pulse width	t_{PAW}	35	–	ns
PMSEL setup to PALE rising edge	t_{PMS}	10	–	–
Address setup to PALE, $\overline{\text{PROG}}$, or $\overline{\text{PRD}}$ falling edge	t_{PAS}	10	–	ns
Address hold after PALE, $\overline{\text{PROG}}$, or $\overline{\text{PRD}}$ falling edge	t_{PAH}	10	–	ns
Address, data setup to $\overline{\text{PROG}}$ or $\overline{\text{PRD}}$	t_{PCS}	100	–	ns
Address, data hold after $\overline{\text{PROG}}$ or $\overline{\text{PRD}}$	t_{PCH}	0	–	ns
PMSEL setup to $\overline{\text{PROG}}$ or $\overline{\text{PRD}}$	t_{PMS}	10	–	ns
PMSEL hold after $\overline{\text{PROG}}$ or $\overline{\text{PRD}}$	t_{PMH}	10	–	ns
$\overline{\text{PROG}}$ pulse width	t_{PWW}	100	–	µs
$\overline{\text{PRD}}$ pulse width	t_{PRW}	100	–	ns
Address to valid data out	t_{PAD}	–	75	ns
$\overline{\text{PRD}}$ to valid data out	t_{PRD}	–	20	ns
Data hold after $\overline{\text{PRD}}$	t_{PDH}	0	–	ns
Data float after $\overline{\text{PRD}}$	t_{PDF}	–	20	ns
$\overline{\text{PROG}}$ high between two consecutive $\overline{\text{PROG}}$ low pulses	t_{PWH1}	1	–	µs
$\overline{\text{PRD}}$ high between two consecutive $\overline{\text{PRD}}$ low pulses	t_{PWH2}	100	–	ns
XTAL clock period	t_{CLKP}	83.3	500	ns



Notes: PRD must be high during a programming write cycle.

Figure 34
Programming Code Byte - Write Cycle Timing

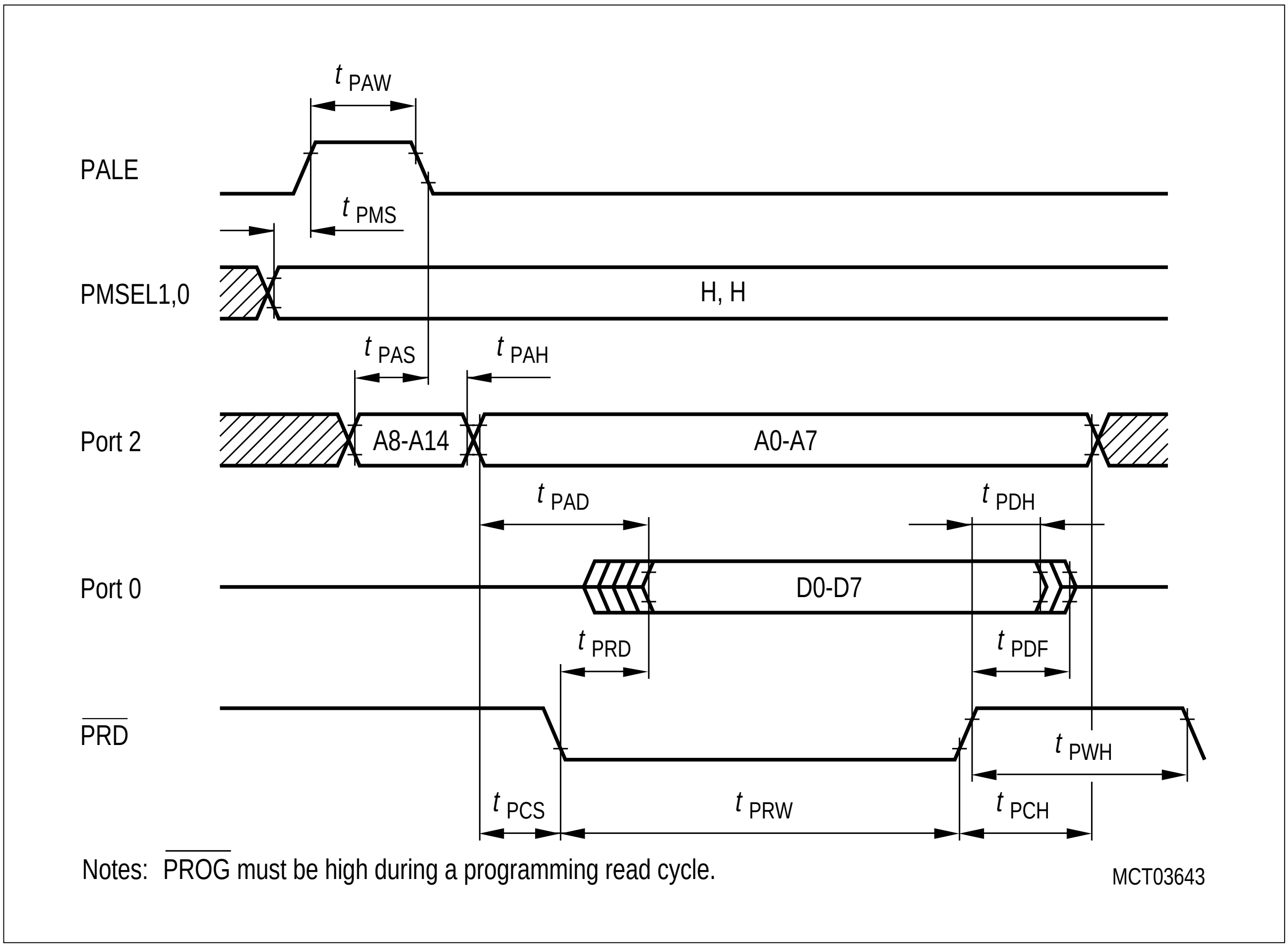
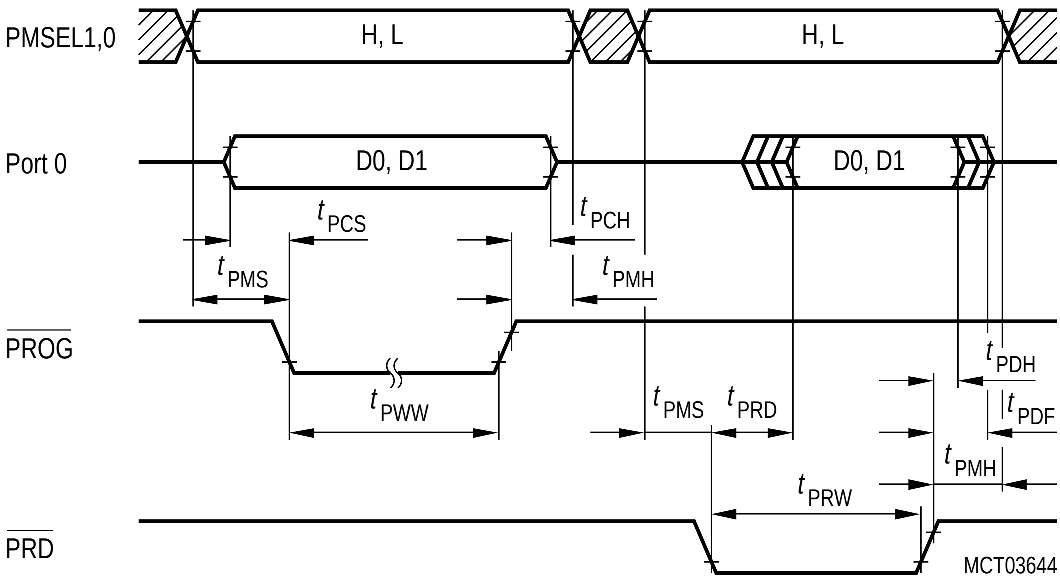
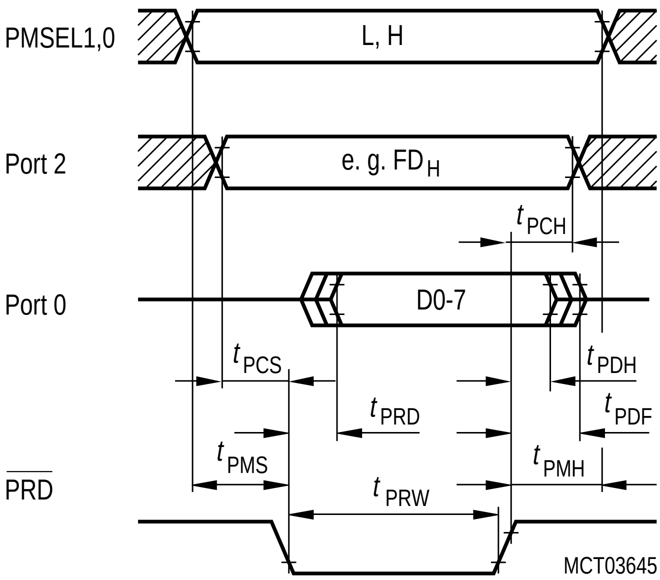


Figure 35
Verify Code Byte - Read Cycle Timing



Note: PALE should be low during a lock bit read / write cycle.

Figure 36
Lock Bit Access Timing



Note: PROG must be high during a programming read cycle.

Figure 37
Version Byte Read Timing

OTP Verification Mode Characteristics

Note: ALE pin described below is the pin 45.

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
ALE pulse width	t_{AWD}	–	CLP	–	ns
ALE period	t_{ACY}	–	6 CLP	–	ns
Data valid after ALE	t_{DVA}	–	–	2 CLP	ns
Data stable after ALE	t_{DSA}	4 CLP	–	–	ns
P3.5 setup to ALE low	t_{AS}	–	TCL_H	–	ns
Oscillator frequency	1/ CLP	4	–	6	MHz

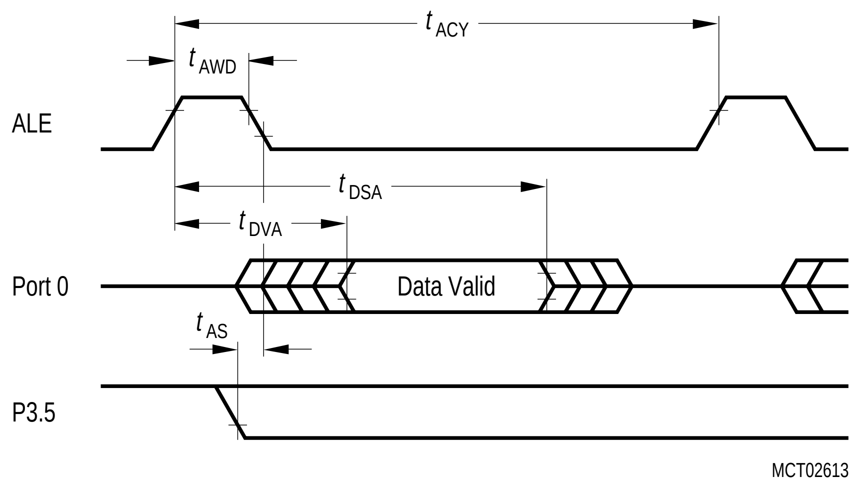
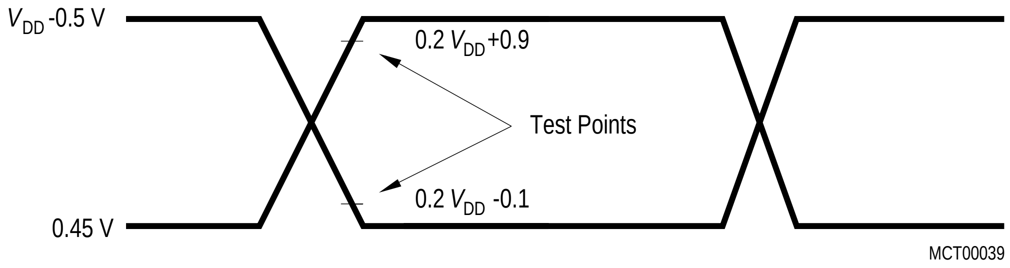


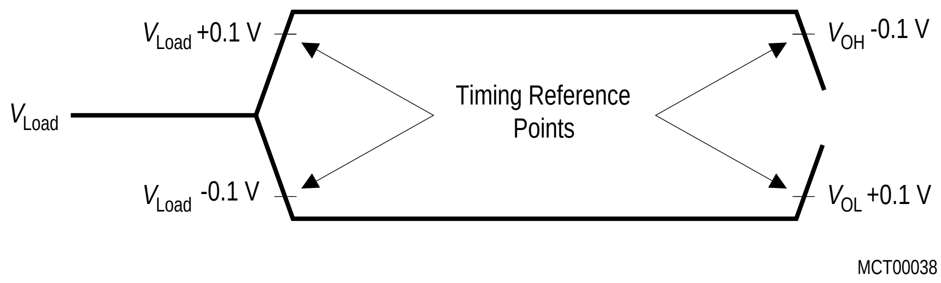
Figure 38
OTP Verification Mode

Note: This mode cannot be entered if OTP protection levels of 1 to 3 are programmed.



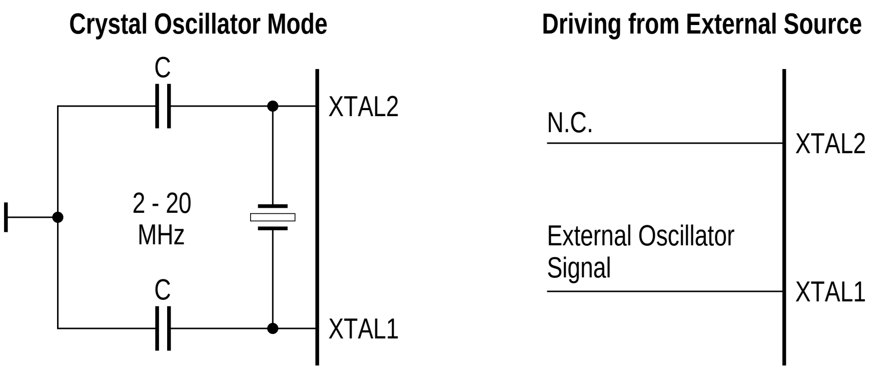
AC Inputs during testing are driven at V_{DD} – 0.5 V for a logic '1' and 0.45 V for a logic '0'. Timing measurements are made at V_{IHmin} for a logic '1' and V_{ILmax} for a logic '0'.

Figure 39
AC Testing: Input, Output Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.
$I_{OL}/I_{OH} \geq \pm$ 20 mA

Figure 40
AC Testing: Float Waveforms



Crystal Mode: C = 20 pF ± 10 pF (incl. stray capacitance)

Figure 41
Recommended Oscillator Circuits for Crystal Oscillator at XTAL1

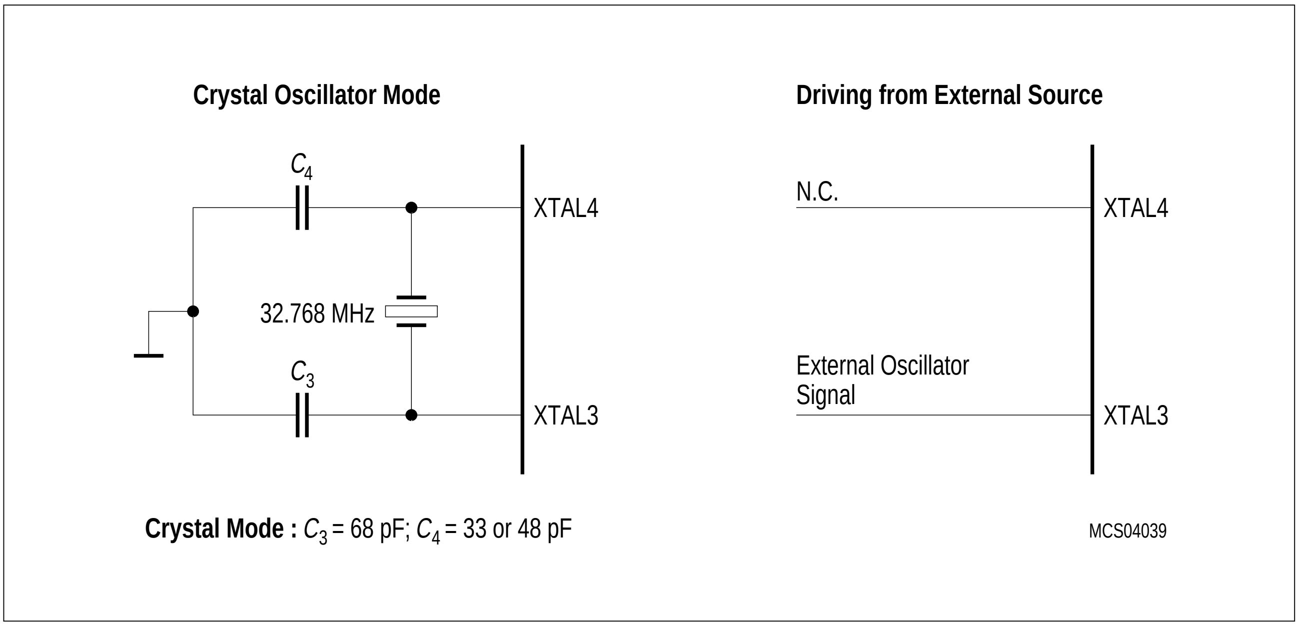


Figure 42
Recommended Oscillator Circuits for Real-Time Clock Oscillator at XTAL3

The recommended oscillator circuitry for the Real-Time Clock oscillator configuration using a crystal oscillator of 32.768 KHz.

Plastic Package, P-MQFP-80-1 (SMD)
(Plastic Metric Quad Flat Pack)

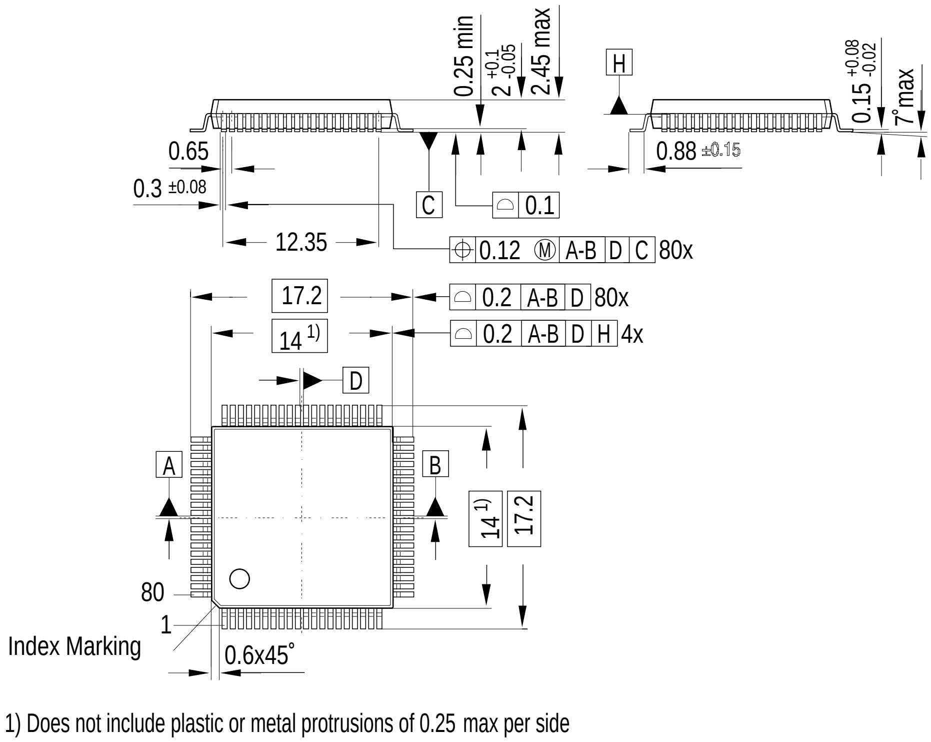


Figure 43
P-MQFP-80-1 Package Outline

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book "Package Information"

SMD = Surface Mounted Device

Dimensions in mm