

PAL/NTSC SYSTEM SINGLE-CHIP COLOR TV SIGNAL PROCESSOR

DESCRIPTION

The M52727SP is an I²C bus interface built-in semiconductor IC designed to process PAL/NTSC type image signals, color signals and deflection signals. Provided with a switch for both S input and AV, black extension function, etc., the M52727SP can meet a wide range of devices from diffusion machines to large screen TV sets. The addition of SECAM chroma-decoder M52325AP will enable the M52727SP to completely and automatically identify the TV systems used all over the world.

FEATURES

- Is capable of reading/writing data with the I²C bus control circuit.
- Built-in AV-SW (with volume control) that is also available for S input
- Complete and automatic identification of color signals and vertical synchronous frequencies of a TV system
- Improvement in the synchronization separation facility at the time of synchronous compression by auto slicer
- Built-in black expansion circuit
- Built-in vertical phase adjustment function
- Built-in two SW systems (ON/OFF by bus control)

APPLICATION

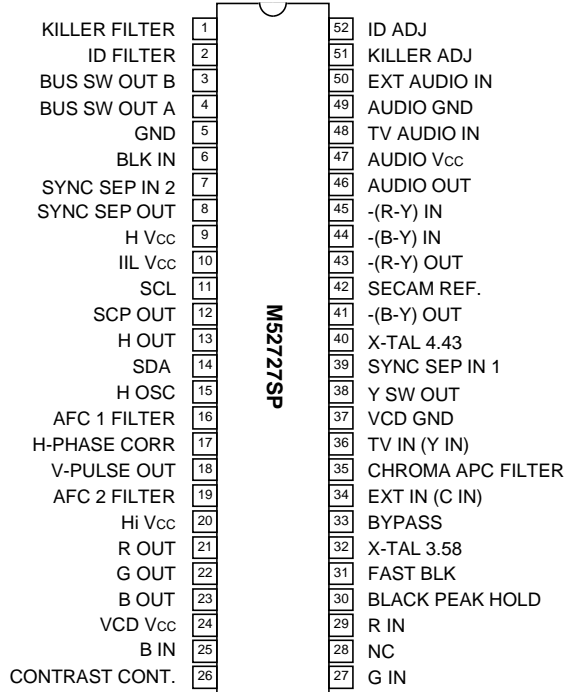
PAL/NTSC Type Color TV, Projector

RECOMMENDED OPERATING CONDITION

Recommended supply voltage V₂₄=5V, V_{9.47}=8.2V, V₂₀=9V
 Operating supply voltage range ... V₂₄=4.75 to 5.25V
 V_{9.47}=7.6 to 8.8V
 V₂₀=8.6 to 9.4V
 Maximum Current 5.0mA (Pin ⑱ current)
 5.0mA (Pin ⑬ current)
 8.0mA (RGB current)
 3.0mA (AUDIO OUT current)
 1.0mA (Pin ⑫ current)

Note: Do not use the M52727SP when only the deflection type power supply (pin ⑨) is made to rise. If so, normal horizontal output pulse width cannot be obtained. Keep away 1 m or more from the IC when using a portable telephone.

PIN CONFIGURATION (TOP VIEW)

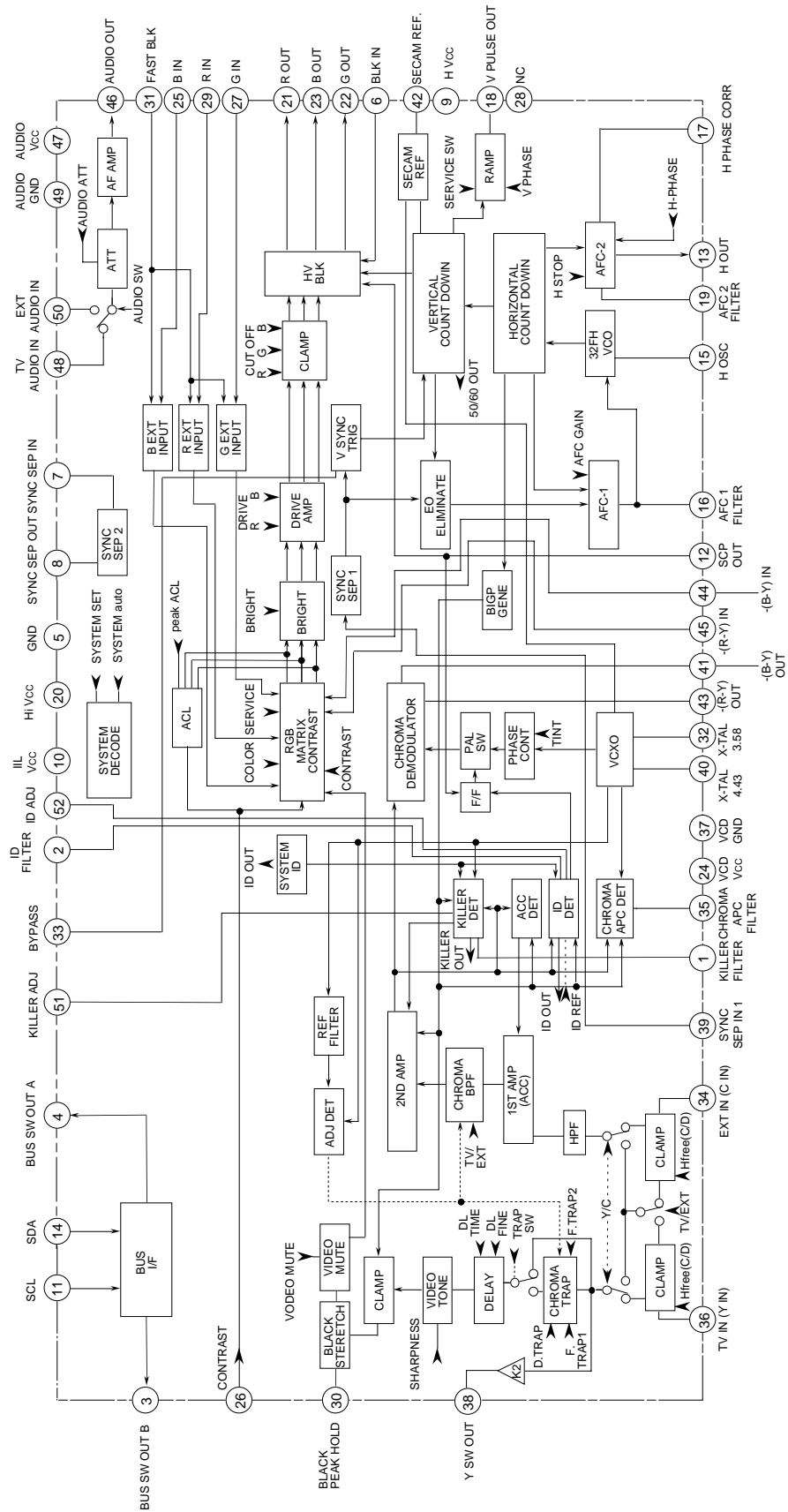


Outline 52P4B

NC : NO CONNECTION

PAL/NTSC SYSTEM SINGLE-CHIP COLOR TV SIGNAL PROCESSOR

BLOCK DIAGRAM



PAL/NTSC SYSTEM SINGLE-CHIP COLOR TV SIGNAL PROCESSOR

ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Symbol	Parameter	Ratings	Unit
V _{CC}	Supply voltage	6.0, 9.0, 10.0	V
P _d	Power dissipation	1.572	W
T _{opr}	Operating temperature	-20 to +65	°C
T _{stg}	Storage temperature	-55 to +150	°C
Surge	Electrostatic discharge	±200	V

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ELECTRICAL CHARACTERISTICS (cont.)

Symbol	Parameter	Test conditions																Limits			Unit												
		Input signal		V _{CC}														Min.	Typ.	Max.													
		SG P/in	condition	SW condition	1	2	3	4	8	12	13	16	18	21	22	23	26					28	38	39	41	42	43	44	9	20	24	47	
kilP	Killer color residual (PAL)	36 34	SGa VS4P ec=0V	SW PIN																											-41	-30	dB
APC1	APC Pull-in range 1	36 34	SGa VS4P (variable)	SW PIN																										±300	±600	±1500	Hz
θR-Y P	Demodulated phase angle θ R-Y	36 34	SGa VS4P (p variable)	SW PIN																			M							82	90	98	deg
R/BP	Demodulation ratio R-Y/B-Y	36 34	SGa VS4P ec=unity	SW PIN																			M							0.45	0.56	0.68	—
CLP	Demodulated output carrier leak	36 34	SGa SS4P	SW PIN																											5	15	mVp-p
DDH	Demodulated output 1H level difference	36 34	SGa VS4P ec=0V	SW PIN																			M								11	30	mVp-p
B/T	BPF/TOF switching	36 34	SGa VS4P (-25dB)	SW PIN																											2	6	mVp-p
ACC3	ACC characteristics 3 (EXT)	36 34	SGa VS4P (+6dB)	SW PIN																			M							-4.5	-2.5	-0.5	dB
ACC4	ACC characteristics 4 (EXT)	36 34	SGa VS4P (-20dB)	SW PIN																			M							-2	0	2	dB
HBLK PAL	PAL with HBLK level difference	36 34	SGa VS4P ec=0mV	SW PIN																			M								1	5	mV
BPF C1	BPF characteristics 1	36 34	SGa VS4P ec f variable	SW PIN																										350	500	690	mVp-p
TOF C1	TOF characteristics 1	36 34	SGa VS4P ec f variable	SW PIN																			M							260	420	580	mVp-p
DCIN Hold PALL	C input D range APC Hold range	36 34	SGa VS4P SYNC variable SGa VS4P ec f variable	SW PIN																													Hz
																														220	370	530	mVp-p
																														350	500	690	mVp-p
																							M							400	580	800	mVp-p
																														190	330	470	mVp-p
																														-1.0	0	1.0	dB
																															±600	±1600	Hz

PAL/NTSC SYSTEM SINGLE-CHIP COLOR TV SIGNAL PROCESSOR

ELECTRICAL CHARACTERISTICS (cont.)

Symbol	Parameter	Test conditions																				Limits			
		Input signal SG Pin	SW condition	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	Min.	Typ.	Max.	Unit
				16	44	45	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P				
BPF C2	BPF characteristics 2	36 34	SW PIN	1	0	0															320	480	620	mVp-p	
TOF C2	TOF characteristics 2	36 34	SW PIN																		190	320	470	mVp-p	
f free	VCXO Free run frequency condition	—	—																		-500	0	500	Hz	
ACC5	ACC	36 34	SWG SGG PIN																		-3	0	3	dB	

Symbol	Parameter	Test conditions																				Limits			
		Input signal SG Pin	SW condition	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	Min.	Typ.	Max.	Unit
				16	44	45	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P				
—	Chroma (SECAM) typical condition	—	SW PIN	1	0	0															—	—	—	—	
SRA	SECAM REF output AC voltage	—	SW PIN																		230	400	500	mVp-p	
SRDL	SECAM REF output DC voltage L	—	SW PIN																		1.2	1.5	1.8	V	
SRDH	SECAM REF output DC voltage H	—	SW PIN																		4.6	5.0	5.6	V	

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ELECTRICAL CHARACTERISTICS (cont.)

Symbol	Parameter	Test conditions																Limits						
		Input signal condition	SW condition	S 44	S 45	P 7	P 8	P 12	P 13	P 16	P 17	P 18	P 21	P 22	P 23	P 28	P 39	Vcc	Min.	Typ.	Max.	Unit		
SYSH	Sync. separation output H	SG PIN	SW PIN																8.1	8.2	8.3	V		
SYSL	Sync. separation output L	SG PIN	SW PIN																		0.1	0.4	V	
HLV	Maximum sync. detection level	36	SW PIN						M								M				7	18	%	
fV	Vertical free run frequency	—	SW PIN																41	44	47	Hz		
VVL	Vertical output minimum voltage	—	SW PIN																0	0.3	0.7	V		
SSV	Service switch operation 2	—	SW PIN																	0	0.5	V		
FPV	Vertical pull-in range	36	SGd (fv variable) PIN																65	—	—	Hz		
VW	Vertical output pulse width	—	SW PIN																0.35	0.52	0.65	msec		
VBLK W	Vertical BLK width	—	SW PIN																1.35	1.5	1.6	msec		
BLK IN	Vertical BLK input	—	SW PIN																	—	—	0.5	V	
AV ER1	50/60 decision 1	36	SGd (fv63Hz) PIN																		63	—	Hz	
AV ER2	50/60 decision 2	36	SGd (fv57Hz) PIN																		57	—	Hz	
AV ER3	50/60 decision 3	36	SGd (fv53Hz) PIN																		53	—	Hz	
AV ER4	50/60 decision 4	36	SGd (fv47Hz) PIN																		47	—	Hz	
VW SS	Minimum sync. detection width	36	SGd (Vw variable) V=0.28V PIN																		10	15	μsec	
SCP G	SCP wave height value GP	—	SW PIN																		4.21	4.5	6.5	V
SCP H	SCP wave height value H-BLK	—	SW PIN																		2.5	2.9	3.3	V
SCP V	SCP wave height value V-BLK	—	SW PIN																		1.35	1.55	1.80	V

PAL/NTSC SYSTEM SINGLE-CHIP COLOR TV SIGNAL PROCESSOR

ELECTRICAL CHARACTERISTICS TEST METHOD

Icc** Circuit Current

1. Test each pin current, and make it Icc**
2. Standard

Icc** Expressed as (mA)

IILcc BUS IIL Lowest Operation Current

1. Gradually reduce the current from 13.6 mA at pin ⑩, measure the current that causes malfunction to occur at BUS, and specify the value as IILcc.
2. Standard

IILICC** Expressed as (mA)

VEAgmax EXT AUDIO Maximum Gain

1. Input SG1 into pin ⑤① and test P-P value of pin ④⑥ output signal, and make it VA1.
- 2.

$$VEAgmax=20 \log \frac{VA1}{\sqrt{VIN}} \text{ (dB)}$$

ATT1 Maximum Attenuation 1

1. Input SG1 into pin ⑤① and test P-P value of pin ④⑥ output signal.
- 2.

$$ATT1=20 \log \frac{\text{Test value (mVP-P)}}{VA1(mVP-P)} \text{ (dB)}$$

CTET EXT → T V Cross Talk

1. Input SG1 into pin ⑤① and test P-P value of pin ④⑥ output signal.
- 2.

$$CTET=20 \log \frac{\text{Test value (mVP-P)}}{VA1(mVP-P)} \text{ (dB)}$$

VTAgmax TV AUDIO Maximum Gain

1. Input SG1 into pin ④⑧ and test P-P value of pin ④⑥ output signal, and make it VA4.
- 2.

$$VTAgmax=20 \log \frac{VA4}{\sqrt{VIN}} \text{ (dB)}$$

ATT2 Maximum Attenuation 2

1. Input SG1 into pin ④⑧ and test P-P value of pin ④⑥ output signal.
- 2.

$$ATT2=20 \log \frac{\text{Test value (mVP-P)}}{VA4(mVP-P)} \text{ (dB)}$$

CTTE TV → EXT Cross Talk

1. Input SG1 into pin ④⑧ and test rms value of pin ④⑥ output signal.
- 2.

$$CTTE=20 \log \frac{\text{Test value (mVP-P)}}{VA4(mVP-P)} \text{ (dB)}$$

OFTE TV EXT Offset

1. Test output voltage difference of pin ④⑥ without input.

VEATyp EXT AUDIO Normal Gain

1. Input SG1 (Typ) into pin ⑤① and test P-P value of pin ④⑥ output signal, and make it VA8.
- 2.

$$VEATyp=20 \log \frac{VA8}{\sqrt{VIN}} \text{ (dB)}$$

VTATyp TV AUDIO Normal Gain

1. Input SG1 (Typ) into pin ④⑧ and test P-P value of pin ④⑥ output signal, and make it VA9.
- 2.

$$VTATyp=20 \log \frac{VA9}{\sqrt{VIN}} \text{ (dB)}$$

VEAmax EXT AUDIO Maximum Output

1. Input SG1 (V=3VP-P) into pin ⑤① and test P-P value of pin ④⑥ output signal.

VEAlmax EXT AUDIO Input D Range

1. Input SG1 (level variable) into pin ⑤① and then measure the distortion factor of the output signal at pin ④⑥.
2. Gradually increase the input and measure the input level when the distortion factor is 1%.

VTAmmax TV AUDIO Maximum Output

1. Input SG1 (V=3VP-P) into pin ④⑧ and test P-P value of pin ④⑥ output signal.

VTAlmax TV AUDIO Input D Range

1. Input SG1 (level variable) into pin ④⑧ and then measure the distortion factor of the output signal at pin ④⑥.
2. Gradually increase the input and measure the input level when the distortion factor is 1%.

S/NT Sound S/N TV

1. Test the noise level of pin ④⑥.

S/NE Sound S/N EXT

1. Test the noise level of pin ④⑥.

PAL/NTSC SYSTEM SINGLE-CHIP COLOR TV SIGNAL PROCESSOR

TV OFATT ATT max min Offset TV

1. Test DC offset of pin ④⑥ at ATT max min.
2. TV OFATT=ATTmin - ATTmax

fTV TV f Specific

1. Input SG1(f specific) into pin ④⑧.
2. Measure the frequency whose amplitude takes -3dB of VA8 at pin ④⑥.

fEXT EXT f Specific

1. Input SG1(f variable) into pin ⑤⑩.
2. Measure the frequency whose amplitude takes -3dB of VA9 at pin ④⑥.

EXT OFATT ATT max min Offset EXT

1. Test DC offset of pin ④⑥ at ATT max min.
2. EXT OFATT=ATTmin - ATTmax

Cn1 Chroma Normal Output 1 (PAL)

Cn2 Chroma Normal Output 2 (PAL)

1. Input SS4P into pin ③④, SG.A into pin ③⑥ .
2. Test the output amplitude of pin ④①, ④③ and make Cn1,Cn2.
3. At the same time, test the output amplitude of pin ④④ and make it Vcn1.

ACC1 ACC Characteristics 1

1. Input VS4P(eb=570mV: Input level+6dB) into pin ③④, SG.A into pin ③⑥ .
2. Test the output amplitude of pin ④①.
- 3.

$$ACC1 = 20 \log \frac{\text{Test value}(V_{P-P})}{Cn1 (V_{P-P})} \text{ (dB)}$$

ACC2 ACC Characteristics 2

1. Input VS4P(Input level -20dB) into pin ③④, SG.A into pin ③⑥ .
2. Test the output amplitude of pin ④①.
- 3.

$$ACC2 = 20 \log \frac{\text{Test value}(V_{P-P})}{Cn1 (V_{P-P})} \text{ (dB)}$$

OV Overload Characteristics

1. Input VS4P (ec=800mV_{P-P}: Croma +3dB) into pin ③④, SG.A into pin ③⑥ .
2. Test the output amplitude of pin ④①.
- 3.

$$OL = 20 \log \frac{\text{Test value}(V_{P-P})}{Cn1 (V_{P-P})} \text{ (dB)}$$

VikP Killer Operation Input Level (PAL)

1. Input VS4P (level variable) into pin ③④ with level 0 dB and input SG.A into pin ③⑥.
2. Lower the input level while monitoring the output amplitude at pin ④①, and then measure the input level when no output amplitude is generated.

KilP Killer Color Residual (PAL)

1. Input VS4P(eb=0V) into pin ③④, SG.A into pin ③⑥ .
2. Test the output amplitude of pin ④①.

Note.) Take measurements in the auto color mode. KILLER malfunction may occur in the forced color mode.

APC1 APC Pull-in Range 1

1. Input VS4P (f=eb=ec=variable) into pin ③④, SG.a into pin ③⑥ .
2. Change the input signal frequency and measure the frequency range when the output signal at pin ④① comes into existence (is placed in the pull-in status). The basic value shall be 4.433619 MHz.

θR-Y P Demodulated Phase Angle θ P-Y

1. Input VS4P (ec=Single Chroma, phase variable) into pin ③④, SG.a into pin ③⑥.
2. Measure the output at pin ④③ make the ec phase variable and specify 0 deg for the phase where the output is zero.
3. Measure the output at pin ④①, advance the ec phase, and measure the phase where the output becomes zero.

R//BP Demodulated Ratio R-Y/B-Y

1. Input VS4P (ec=Single Chroma=eb+50kHz) into pin ③④, SG.a into pin ③⑥ .
2. Test the output amplitude of pin ④① and make it V41.
3. Test the output amplitude of pin ④③ and make it V43.
- 4.

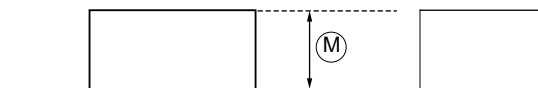
$$R/BP = 20 \log \frac{V43 (V_{P-P})}{V41 (V_{P-P})} \text{ (dB)}$$

CLP Demodulated Output Carrier Leak

1. Input SS4P into pin ③④, SG.a into pin ③⑥.
2. Measure each of 4.43MHz element and 8.86MHz element of demodulation output at pin ④① .

DDH Demodulated Output 1H Level Difference

1. Input VS4P(ec=0V) into pin ③④, SG.a into pin ③⑥ .
2. Measure the 1H level difference at pins ④① and ④③ .



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B/T BPF/TOP Switching

1. Input VS4P(input level-25dB) into pin ③④ , SG.a into pin ③⑥.
2. Test the output amplitude of pin ④① on TV, EXT.
- 3.

$$B/T = 20 \log \frac{EXT (V_{P-P})}{TV (V_{P-P})} \text{ (dB)}$$

ACC3 ACC Characteristics 3 (EXT)

1. Input VS4P(input level+6dB) into pin ③④ , SG.a into pin ③⑥.
2. Test the output amplitude of pin ④①.
- 3.

$$ACC3 = 20 \log \frac{Test \ value(V_{P-P})}{Cn1} \text{ (dB)}$$

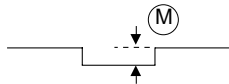
ACC4 ACC Characteristics 4 (EXT)

1. Input VS4P(input level-20dB) into pin ③④ , SG.a into pin ③⑥.
2. Test the output amplitude of pin ④①.
- 3.

$$ACC4 = 20 \log \frac{Test \ value(V_{P-P})}{Cn1} \text{ (dB)}$$

HBLK PAL HBLK. Level Difference PAL

1. Input VS4P(ec=0mV) into pin ③④, SG.a into pin ③⑥.
2. Measure the level difference between the output color pattern period of pin ④① and the BLK period.



BPFC1 BPF Characteristics 1

1. Input VS4P (ec single frequency, 0.3 V_{P-P}, _f variable) and SG.a into pins ③④ and ③⑥, respectively.
2. Measure the output amplitude at pin ④① with ec=fsc+10kHz, +800 kHz, or -800 kHz.

TOFC1 TOF Characteristics 1

1. Input VS4P (ec single frequency, 0.3 V_{P-P}, _f variable) and SG.a into pins ③④ and ③⑥, respectively.
2. Measure the output amplitude at pin ④① with ec=fsc+10kHz, +800 kHz, or -800 kHz.

DCIN C Input D Range

1. Input VS4P (SYNC 1V) into pin ③④, SG.a into pin ③⑥ .
- 2.

$$DCIN = 20 \log \frac{Test \ value}{Cn1} \text{ (dB)}$$

Hold PALL APC Hold Range

1. Input VS4P (f=eb=ec=variable) into pin ③④, SG.a into pin ③⑥.
2. Change the input signal frequency range and then measure the frequency range when the output signal at pin ④① comes into existence (is placed in the pull-in status).

Cn3 Chroma Normal Output 3 (NTSC)

Cn4 Chroma Normal Output 4 (NTSC)

1. Input SS3N into pin ③④ , SG.b into pin ③⑥.
2. Test the output amplitude of pin ④①, ④③ and make Cn3,Cn4.

VikN Killer Operation Input Level (NTSC)

1. Input VS3N (level variable) into pin ③④ with the input level of 0 dB and input SG.b into pin ③⑥ .
2. Lower the input level while monitoring the output amplitude at pin ④①, and then measure the input level when no output amplitude is generated.

KiIN Killer Color Residual (NTSC)

1. Input VS3N (eb=0V) into pin ③④, SG.b into pin ③⑥.
2. Test the output amplitude of pin ④①.

APC2 APC Pull-in Range 2

1. Input VS3N (f=eb=ec=variable) into pin ③④, SG.b into pin ③⑥.
2. Change the input signal frequency and measure the frequency range when the output signal at pin ④① comes into existence (is placed in the pull-in status). The basic value shall be 3.579545 MHz.

Note: When measuring 3.58 MHz APC pull-in, set the APC pin to high-level, supply the signal to the pin, and then take measurements with the APC pin OPEN. When the APC pin is set to high-level, oscillation of 3.58 MHz may stop. Use the above conditions for the measurement to check that this status is not held.

θR-Y N Demodulated Phase Angle θR-Y N

1. Input VS3N (eb=unity Chroma, phase variable) into pin ③④ , SG.b into pin ③⑥ .
2. Measure the output at pin ④③ , make the ec phase variable, and specify 0 deg for the phase where the output is zero.
3. Observe the output at pin ④①, advance the ec phase and measure the position where the output is 0.

R/BN Demodulated Ratio R-Y/B-Y

1. Input VS3N(ec=unity Chroma=eb+50kHz) and SG.b into pin ③④.
2. Test the output amplitude of pin ④① and make V41.
3. Test the output amplitude of pin ④③ and make V43.
- 4.

$$R/BN = 20 \log \frac{V43(V_{P-P})}{V41(V_{P-P})} \text{ (dB)}$$

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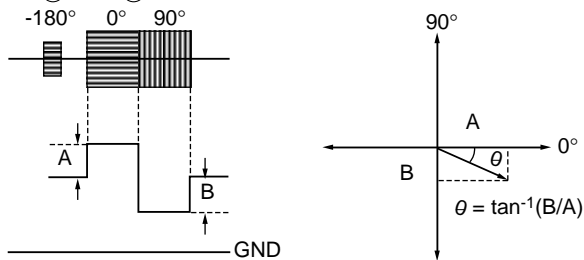
CLN Demodulated Output Carrier Leak

1. Input SS3N into pin ③④, SG.b into pin ③⑥ .
2. Measure each of 3.58MHz element and 7.16MHz element of demodulation output at pin ④①

T1 TINT Control Characteristics 1

T2 TINT Control Characteristics 2

1. Input VS3N (see the diagram below) and SG.b into pins ③④ and ③⑥, respectively.



Find the absolute angle from the output at pin ④① according to the diagram above.

2. Assuming the TINT DATA center (64) as the basic angle (TC), find the angle for TINT DATA MAX and MIN and express with the difference in angle between them. (MAX = TC_{MAX}, MIN = TC_{MIN})
3. TC₁=TC_{MAX}-TC (deg)
TC₂=TC-TC_{MIN} (deg)

T3 TINT Center Position

1. Shall be the basic angle for the TINT data center.
2. T₃=TC

HBLK NT H-BLK Level Difference

1. Input VS3N(ec=0mV) into pin ③④, SG.b into pin ③⑥.
2. Measure the level difference between the output pattern period and the BLK period at pin ④① .

Hold NT APC Hold Range

1. Input VS3N(.f=eb=ec=variable) into pin ③④, SG.b into pin ③⑥.
2. Change the input signal frequency and measure the frequency range when the output signal at pin ④① comes into existence (is placed in the pull-in status). The basic value shall be 3.579545 MHz.

BPFC2 BPF Characteristics 2

1. Input VS3N (ec single frequency, 0.3 V_{P-P}, _f variable) and SG.a into pins ③④ and ③⑥, respectively.
2. Measure the output amplitude at pin ④① with ec=fsc+10 kHz, +800 kHz, or -800 kHz.

TOFC2 TOF Characteristics 2

1. Input VS3N (ec single frequency, 0.3 V_{P-P}, _f variable) and SG.a into pins ③④ and ③⑥, respectively.
2. Measure the output amplitude at pin ④① with ec=fsc+10 kHz, +800 kHz, or -800 kHz.

f free VCXO Free Run Frequency

1. Test the oscillate frequency of pin ③② and make f CN16.
2. f free = f CN16-3579545 (Hz)

ACC5 ACC Lock

1. Input SG.G(f=3.579545MHz, V variable) into pin ③④, SG.b into pin ③⑥.
2. When the amplitude of SG.G is switched to 0.5 V_{P-P} or 2.0 V_{P-P}, the output at pin ④① shall be V_{cn17a} or V_{cn17b}, respectively.

3.
$$ACC5 = 20 \log \frac{V_{cn17b}}{V_{cn17a}} \text{ (dB)}$$

SRA SECAM REF Output AC Voltage

1. Measure the amplitude (SRA) of 4.43 MHz element of the output at pin ④②.

SRDL SECAM REF Output DC voltage L

1. Test the output DC voltage of pin ④②.

SRDH SECAM REF Output DC voltage H

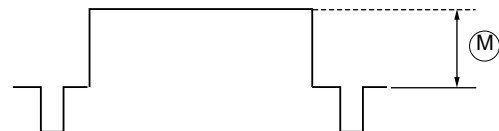
1. Test the output DC voltage of pin ④②.

AUTO1~6 System Distinction 1~6

1. Place the IC in the AUTO mode and then check that BUS reads input signals appropriately.

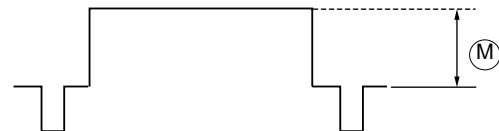
ACL1 Peak ACL "H" Level

1. Input SGA into pin ③⑧.
2. Measure the amplitude (P-P) except for the blanking block of the output at pin ②①



GY Video Normal Gain

1. Input SGA into pin ③⑧.
2. Measure the amplitude (P-P) except for the blanking block of the output at pin ②①.



3.
$$GY = 20 \log \frac{\text{Test value}}{\sqrt{IN}(0.714V)} \text{ (dB)}$$

FBY Video Frequency Characteristics

1. Input SGB (5MHz, 0.714V_{P-P}) into pin ③⑧.
2. Measure the amplitude (P-P) except for the blanking block of the output at pin ②①.

3.
$$FBY = 20 \log \frac{\text{Test value (V}_{P-P})}{GY \text{ (V}_{P-P})} \text{ (dB)}$$

PAL/NTSC SYSTEM SINGLE-CHIP COLOR TV SIGNAL PROCESSOR

FBYRGB Video Frequency Characteristics RGB Difference

1. Input SGB (5MHz, 0.4VP-P) into pin ③⑥.
2. Measure the amplitude (P-P) except for the blanking block of the output at pins ⑳①, ㉒ and ㉓.
3. The maximum test value and the minimum test value are assumed to be MRGB and SRGB, respectively.

$$FBYRGB = 20 \log \frac{SRGB (VP-P)}{MRGB (VP-P)} \text{ (dB)}$$

2AGY Double Amplifier Standard Output

1. Input SGA into pin ③⑥.
2. Test the output amplitude (P-P) of pin ③⑧.
- 3.

$$2AGY = 20 \log \frac{\text{Test value}}{VIN (1VP-P)} \text{ (dB)}$$

CTR1 Chroma Trap Attenuation 1 (pin ㉑ output)

1. Input SGF (f = 3.58 MHz) into pin ③⑥, measure the output amplitude at pin ㉑ with TRAP DATA 0, and specify the value as VY60OFF.
2. Set TRAP DATA to 1, switch f TRAP1/f TRAP2 to 0/1, and then measure the respective output amplitude values at pin ㉑.

fTRAP1	fTRAP2	→	Vf
0	0	→	Vf00
0	1	→	Vf01
1	0	→	Vf10
1	1	→	Vf11

$$CTR1 = 20 \log \frac{Vf00, Vf01, Vf10, Vf11 (mVP-P)}{VY60OFF (mVP-P)} \text{ (dB)}$$

4. Specify TRAP01 as the attenuation for fixing.
5. Of the values from TRAP00 to TRAP11, the maximum attenuation value shall be specified as the attenuation for arrangement.

CTR2 Chroma Trap Attenuation 2 (pin ㉑ output)

1. Input SGF (f = 4.43 MHz) into pin ③⑥, measure the output amplitude at pin ㉑ with TRAP DATA 0, and specify the value as VY7OFF.
2. Set TRAP DATA to 1, switch f TRAP1 and f TRAP2 to 0/1, and then measure the respective output amplitude values at pin ㉑.

fTRAP1	fTRAP2	→	Vf
0	0	→	Vf00
0	1	→	Vf01
1	0	→	Vf10
1	1	→	Vf11

$$CTR2 = 20 \log \frac{Vf00, Vf01, Vf10, Vf11 (mVP-P)}{VY7OFF (mVP-P)} \text{ (dB)}$$

4. Specify TRAP401 as the attenuation for fixing.
5. Of the values from TRAP400 to TRAP411, the maximum attenuation value shall be specified as the attenuation for arrangement.

DTR1 D. TRAP Attenuation 1 (pin ㉑ output)

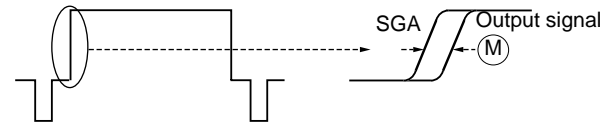
1. Set D.TRAP DATA to 1, and take measurement as in the case of CTR1.

DTR2 D. TRAP Attenuation 2 (pin ㉑ output)

1. Set D.TRAP DATA to 1, and take measurement as in the case of CTR2.

YDL1 Y delay time 1

1. Input SGA into pin ③⑥.
2. Measure the delay time of output from pin ㉑ against input signal.



Measure the delay time at the center of the rising portion.

YDL2~4 Y delay time 2 to 4

1. Input SGA into pin ③⑥.
2. Measure the delay time between the signal output from pin ㉑ and Y10 YDL1.

YDL5 Y delay time 5

1. Input SGA into pin ③⑥.
2. Measure the absolute value of difference in time between the output signal at pin ㉑ and Y13YDL4.

GTnor Video Tone 1

1. Input SGB (f=100kHz, 0.4VP-P, 3MHz) into pin ③⑥. Test the output amplitude of each pin ㉑ and make VY100K, VY3M.

$$GTnor = 20 \log \frac{VY3M}{VY100K} \text{ (dB)}$$

GTmax Video Tone 2

1. Input SGB (f= 3MHz, 0.4VP-P) into pin ③⑥.
2. Test the output amplitude of pin ㉑.
- 3.

$$GTmax = 20 \log \frac{\text{Test value (VP-P)}}{VY100K} \text{ (dB)}$$

GTmin Video Tone 3

1. Input SGB (f= 3MHz, 0.4VP-P) into pin ③⑥.
2. Test the output amplitude of pin ㉑.
- 3.

$$GTmin = 20 \log \frac{\text{Test value (VP-P)}}{VY100K} \text{ (dB)}$$

GT1M Video Tone 4

1. Input SGB (f= 1MHz, 0.4VP-P) into pin ③⑥.
2. Test the output amplitude of pin ㉑.
- 3.

$$GT1M = 20 \log \frac{\text{Test value (VP-P)}}{VY100K} \text{ (dB)}$$

PAL/NTSC SYSTEM SINGLE-CHIP COLOR TV SIGNAL PROCESSOR

GT5M Video Tone 5

1. Input SGB (f= 5MHz, 0.4V_{P-P}) into pin ③⑥ .
2. Test the output amplitude of pin ②①.
3. $GT5M = 20 \log \frac{\text{Test value (V}_{P-P})}{VY100K}$ (dB)

ACL2 Peak ACL "L" Level

1. Input SGA into pin ③⑥.
2. Test the output amplitude of pin ②①.

SSW1 Service Switch Operation 1

1. Input SGB (f= 5MHz) into pin ③⑥ .
2. Measure the output amplitude at pin ②① with the service SW set to OFF.
3. Measure the output amplitude at pin ②① with the service SW set to ON.
4. $GY1 = 20 \log \frac{\text{Test value}}{VY21}$ (dB)

GY1 Contrast Control Characteristics 1

1. Input SGB (f= 5MHz) into pin ③⑥ .
2. Test the output amplitude of pin ②①.
3. $GY1 = 20 \log \frac{\text{Test value}}{VY21}$ (dB)

GY2 Contrast Control Characteristics 2

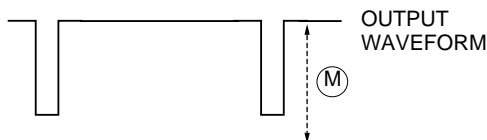
1. Input SGB (f= 5MHz) into pin ③⑥.
2. Measure the output amplitude at pin ②① when 0V is applied to pin ②⑥ from outside.
3. $GY2 = 20 \log \frac{\text{Test value}}{VY21}$ (dB)

Lum nor Brightness Control Characteristics 1

Lum max Brightness Control Characteristics 2

Lum min Brightness Control Characteristics 3

1. No input.
2. Test the output DC voltage of pin ②① except blanking part.
3. Lum max=Test value-Lum nor



D(G) Drive Control Characteristics G

1. Input SGA into pin ③⑥ .
2. Measure the output amplitude at pin ②② with D(G) DATA min and max. Specify the measured values as Dgmin and Dgmax, respectively.
3. $D(G) = 20 \log \frac{DG_{max}(V_{P-P})}{DG_{min}(V_{P-P})}$ (dB)

D(B) Drive Control Characteristics B

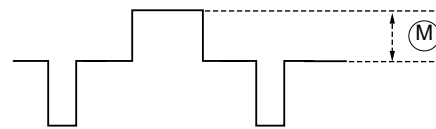
1. Input SGA into pin ③⑥ .
2. Measure the output amplitude at pin ②③ with D(B) DATA min and max. Specify the measured values as DBmin and DBmax, respectively.
3. $D(B) = 20 \log \frac{DB_{max}(V_{P-P})}{DB_{min}(V_{P-P})}$ (dB)

EX(R) EXT(R) Normal Gain

EX(G) EXT(G) Normal Gain

EX(B) EXT(B) Normal Gain

1. Input SG50 and SGD (V=0.7V) into pin ③⑥ and FB, respectively. Input SGD (V=0.35V) into each of ER, EG and EB.
2. Measure the amplitude over the pedestal level except for the blanking block of the outputs at pins ②①, ②② and ②③. Specify the respective values as VY31R, VY31G and VY31B.



3. $EXT(R), EXT(G), EXT(B) = 20 \log \frac{\text{Test value}}{0.35}$ (dB)

OFRG R-G Offset Voltage

OFBG B-G Offset Voltage

1. Test the output DC voltage of pin ②①, ②②, ②③ except blanking part.
2. $OFRG = (\text{pin } ②① \text{ Test voltage}) - (\text{pin } ②② \text{ Test voltage})$ (mV)
 $OFBG = (\text{pin } ②③ \text{ Test voltage}) - (\text{pin } ②② \text{ Test voltage})$ (mV)

C(R) R Cut-off Characteristics

C(G) G Cut-off Characteristics

C(B) B Cut-off Characteristics

1. Test the output DC voltage of pin ②①, ②②, ②③ except blanking part when each of C(R), C(G), C(B) DATA is max, min.
2. $C(R), C(G), C(B) = (\text{DATA}_{max} \text{ voltage}) - (\text{DATA}_{min} \text{ voltage})$ (V)

Ccon0 Color Regulation Characteristics 0

1. Input SGE (V=1.3V) into -B IN (pin ④④).
2. Test the output amplitude of pin ②③ and make VY37.

Ccon1 Color Regulation Characteristics 1

Ccon2 Color Regulation Characteristics 2

1. Input SGE into -B IN (pin ④④).
2. Test the output amplitude of pin ②③ and make VY38, VY39.
3. $Ccon1, Ccon2 = 20 \log \frac{VY38, VY39}{VY37}$ (dB)

PAL/NTSC SYSTEM SINGLE-CHIP COLOR TV SIGNAL PROCESSOR

VMF Video Mute Characteristics

1. Input SGB(f=5MHz) into pin ③⑥ .
2. Test the output amplitude of pin ②① .
3.
$$VMF = 20 \log \frac{\text{Test value}}{V_{Y21}} \text{ (dB)}$$

R-Y PAL R-Y/B-Y PAL Relative Amplitude

R-Y NTSC R-Y/B-Y PAL Relative Amplitude

G-Y /B-Y R-Y/B-Y PAL Relative Amplitude

<G-Y <G-Y Relative Phase

1. Input SGE(V=1VP-P)into -B IN (pin ④④) .
2. Test the output amplitude of pin ②② , ②③ .
(and make B-Y, G-Y ← B)
3. Input SGE(V=0.56V) into -R IN (pin ④⑤) .
4. Test the output amplitude of pin ②① , ②② .
(and make R-Y, G-Y ← R)
5. Change into NTSC mode and test the output amplitude of pin ②①. (and make R-Y n)

6.
$$R-Y \text{ PAL} = \frac{R-Y_P}{B-Y} \text{ (-)}$$

$$R-Y \text{ NTSC} = \frac{R-Y_N}{B-Y} \text{ (-)}$$

7.
$$G-Y \leftarrow RNT = G-Y \leftarrow R \times \cos 7^\circ$$

$$G-Y \leftarrow BNT = G-Y \leftarrow B - G-Y \leftarrow R \times \sin 7^\circ$$

8.
$$\text{PAL } G-Y/B-Y = \frac{\sqrt{(G-Y \leftarrow R)^2 + (G-Y \leftarrow B)^2}}{B-Y} \text{ (-)}$$

$$\text{NTSC } G-Y/B-Y = \frac{\sqrt{(G-Y \leftarrow RNT)^2 + (G-Y \leftarrow BNT)^2}}{B-Y} \text{ (-)}$$

$$\text{PAL} <G-Y = \tan^{-1} \frac{G-Y \leftarrow R}{G-Y \leftarrow B} \text{ (deg)}$$

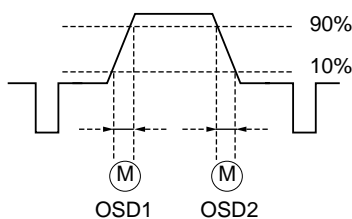
$$\text{NTSC} <G-Y = \tan^{-1} \frac{G-Y \leftarrow RNT}{G-Y \leftarrow BNT} \text{ (deg)}$$

OSD1 OSD Speed Characteristics 1

OSD2 OSD Speed Characteristics 2

1. Input SG50 into pin ③⑥ . Input SGD into each of FB, ER, EG and EB.
2. Measure the signal rising/falling time above the pedestal level except for the blanking block of the output at pins ②①, ②② and ②③ .

PIN ②①, ②②, ②③ OUTPUT WAVEFORM



CLS Input Cut Switch Operation

1. Test the output DC of pin ③⑧ .

CLV1 Input Cramp Potencial 1

1. Test the output DC of pin ③⑧ .

BLS1 Black Expanding Operation 1

BLS2 Black Expanding Operation 2

BLS3 Black Expanding Operation 3

1. Input SGC (Y49 0.2V, Y50 0.4V, Y51 0V) into pin ③⑥ .
2. Specify DC except for BLK of BLS 0 (OFF) as BLS off.
3. Specify DC except for BLK of BLS 1 (ON) as BLS on.
4. BLS1, 2, 3=BLS off-BLS on

S/N RGB RGB Output Noise

1. Test the output noise level of pin ②① except BLK part.

Tc RGB RGB Output Temperature Characteristics

1. Measure the voltage except for BLK block of the output at pin ②① when the ambient temperature is -20°C and specify the value as V-20°C.
2. Measure the voltage except for BLK block of the output at pin ②① when the ambient temperature is 65°C and specify the value as V-65°C.

3.
$$Tc_{RGB} = \frac{(V_{65^\circ C}) - (V_{-20^\circ C})}{85^\circ C} \text{ (mV/}^\circ\text{C)}$$

HBLKL HBLK "L" Level

VBLKL VBLK "L" Level

1. Test the output voltage of pin ②① on the term of HBLK, VBLK.

Vamax Analog RGB Maximum Output

1. Input SG50 into pin ③⑥ . Input SGD into each of ER, EG, EB and FB.
2. Test the output amplitude of pin ②①, ②②, ②③ except BLK part.

VDRGB Analog RGB Input D Range

1. Input SG50 into pin ③⑥ . Input SGD (level 0.5V, 1.0V) into each of ER, EG, EB and FB.
2. Test of the output aplitude of pin ②①, ②②, ②③ and make VY57RT, VY57GT, VY57BT, VY57RH, VY57GH, VY57BH .
- 3.

$$VDRGB = 20 \log \left(\frac{V_{Y57RH}, V_{Y57GH}, V_{Y57BH}}{V_{Y57RT}, V_{Y57GT}, V_{Y57BT}} \right) \text{ (dB)}$$

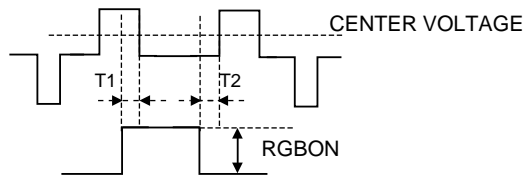
PAL/NTSC SYSTEM SINGLE-CHIP COLOR TV SIGNAL PROCESSOR

RGBON Analog RGB ON Voltage

RGBON BLK RGB ON Voltage

ARGB DL Analog RGB Transmission Characteristics

1. Input SGA into pin ⑳ and SGD(level variable) into FB.
2. Observing the output at pin ㉑, measure the SGD level that keeps pedestal electric potential for the period of SGD "H".
3. At the same time, measure the delay time between SGD and pin ㉑.
4. Increasing SGD, measure the SGD level where BLK of SGD "H" period takes place.



CTAT Analog RGB →TV Crosstalk

1. Input SG50 into pin ㉞ and SGB (f=5MHz) into ER.
2. When the voltages of 0V and 0.7V are applied to FB, the amplitude except for BLK portion of the output at pin ㉑ are specified as V_{0V} and $V_{0.7V}$, respectively.
3. $CTAT=20 \log \frac{V_{0V}}{V_{0.7V}}$ (dB)

CTTA TV →Analog RGB Crosstalk

1. Input SGB(f=5MHz) into pin ㉞.
2. When the voltages of 0V and 0.7V are applied to FB, the amplitude except for BLK portion of the output at pin ㉑ are specified as V_{Y0V} and $V_{Y0.7V}$, respectively.
3. $CTTA=20 \log \frac{V_{Y0V}}{V_{Y0.7V}}$ (dB)

VDY Video Input D Range

1. Input SGB(f=100kHz, level variable Lumi:0.714,1.428V) into pin ㉞.
2. Test the output amplitude of pin ㉑ except BLK part, and make V_{Y63T} , V_{Y63H} .
3. $VDY=20 \log \left(\frac{V_{Y63H}}{V_{Y63T}} \right)$ (dB)

VDCO Color Input D Range

1. Input SGE(1.0VP-P, 2.0VP-P) into -B.
2. Test the output amplitude of pin ㉑ except BLK part.
3. $VDCO=20 \log \left(\frac{V_{Y64H}}{V_{Y64T} \times V_{YCN1}} \right)$ (dB)

Zcor Color Output Impedance

1. Test the output impedance of pin ㉑ and ㉒ as SECAM, NO SECAM.

Ygmax Video Maximum Gain

1. Input SGB(f=100kHz, $V=0.4VP-P$) into pin ㉞.
2. Test the output amplitude into pin ㉑ except BLK part.
3. $Ygmax = 20 \log \frac{\text{Test value}}{0.4VP-P}$ (dB)

f tone Tone Control Peaking Frequency

1. Input SGB (0.714V f variable) into pin ㉞.
2. Varying the frequency of SGB, find the frequency where output amplitude takes a maximum value at pin ㉑.

BLS start Black Expansion Start Point

1. Input SGC (level variable) into pin ㉞.
2. Make V_{Y68A} the output amplitude when SGC level is 0.
3. Gradually changing the SGC level largely, measure the amplitude at which the output at pin ㉑ does not change with the black expansion is turned on/off (specified to be V_{Y68}).
4. Measure the output at pin ㉑ when the SGC level set to 0.714 (specified to be V_{Y68} TYP).
5. $BLS \text{ start} = \frac{V_{Y68}-V_{Y68A}}{V_{Y68TYP}-V_{Y68A}} \times 100$ (IRE)

BLS max Maximum Gain of Black Expansion Amplifier

1. Input SGB (level 0.3VP-P) into pin ㉞.
2. When 5V and OPEN are applied to pin ㉞, the output at pin ㉑ is specified to be $V_{Y69 5V}$ and $V_{Y69 OPEN}$, respectively.
3. $BLS \text{ max}=20 \log \frac{V_{Y69 5V}}{V_{Y69 OPEN}}$ (dB)

CTR3 Chroma Trap Attenuation 3

1. Perform TRAP CONT. of trap data for the attenuation when adjustments are made at Y7.
2. Standard CTR3 shall be specified to be a value given in (dB) when TRAP CONT. is performed on the trap data at Y6.

VYSW Y SW OUT Input D Range

1. Input SGB(f=100kHz level variable Lumi:0.714, 1.428V) into pin ㉞.
2. Test the output Lumi level of pin ㉞ and make V_{Y71T} , V_{Y71H} .
3. $VYSW=20 \log \frac{V_{Y71H}}{V_{Y71T}}$ (dB)

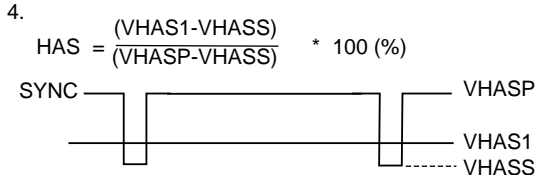
DVY Video Amplitude with Voltage Reducing SW Set to ON

1. Input SGB(f=100kHz Lumi:0.714) into pin ㉞
2. For standard DVY, switch the voltage at pin ㉑ to 0V and 4.5V, measure the output at pin ㉑, and then give the value in (VP-P).

PAL/NTSC SYSTEM SINGLE-CHIP COLOR TV SIGNAL PROCESSOR

HAS Auto Slice Slice Level

1. Test the output voltage of pin ③⑨ as no input and make VHAS1.
2. Input SG50(V=286mV_{P-P}) into ③⑥.
3. Test the sink-chip and pedestal potential of pin ③⑨ and make VHASS, VHASP.



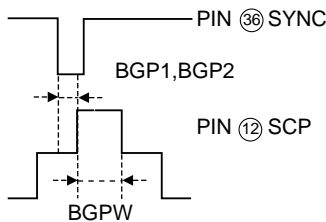
ISS Sync. Separation Input Sensitivity Current

Supply current from pin ⑦, then measure the flow current when the voltage at pin ⑧ is 0.5 VDC or less.

BGP1 BGP Timing 1

BGP2 BGP Timing 2

BGPW BGP Pulse Width



FH Horizontal Freerun Frequency

Test the output frequency of pin ⑬ as no input.

FPH1 Horizontal Pull-in Range 1

FPH2 Horizontal Pull-in Range 2

Change the SGc frequency and then calculate the difference in test value from 15.625 kHz of the frequency range pull in by output signal at pin ⑬ and input signal at pin ③⑥.

$$15.625\text{kHz} - \text{Test value (Hz)}$$

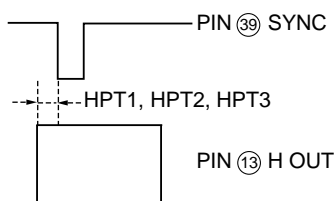
HPT1 Horizontal Pulse Timing 1

HPT2 Horizontal Pulse Timing 2 HPT2-HPT1

HPT3 Horizontal Pulse Timing 3 HPT3-HPT1

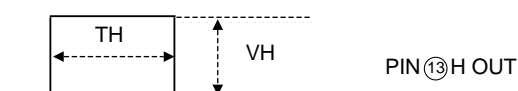
HPT4 Horizontal Pulse Timing 4 HPT4-HPT1

HPT5 Horizontal Pulse Timing 5 HPT5-HPT1



TH Horizontal Pulse Width

VH Horizontal Pulse Amplitude



SH Horizontal Stop Operation

When lowering the voltage at pin ⑨, measure the voltage at which H.OUT output stops.

AFCG AFC Gain Operation

1. Test the output amplitude of pin ⑩ when AFC Gain Switch is changed and make AFCon when SW is ON and AFCoff when SW is OFF.

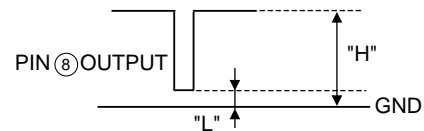
$$2. \text{AFCG} = 20 \log \frac{\text{AFCon (V}_{P-P})}{\text{AFCoff (V}_{P-P})} \text{ (dB)}$$

FS H-V Free Operation

Test the voltage difference of pin ③⑨ when H.FREE SW is ON and OFF.

SYSH SYNC SEP Output "H"

SYSL SYNC SEP Output "L"



HLV Minimum Sync. Detection Level

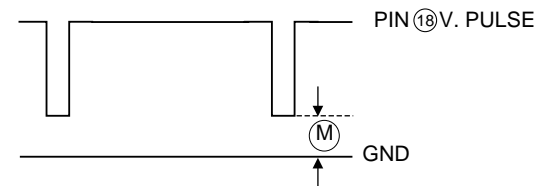
1. Input SG50 (V=variable) into pin ③⑥ .
2. Gradually reduce the SG50 amplitude from 286 mV_{P-P}, measure the amplitude where the horizontal synchronization is put out of the range and specify the value to be HL_{V1}.

$$3. \text{HLV} = \frac{\text{HLV}_1}{286} * 100 (\%)$$

FV Vertical Free-run Frequency

Test the output frequency of pin ⑱ as no input.

VVL Vertical Output Minimum Voltage



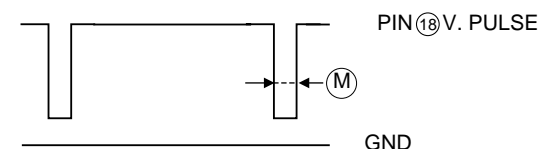
SW Service Switch Operation 2

Test the output DC voltage of pin ⑱ when the service switch DATA ON.

FPV Vertical Pull-in Range

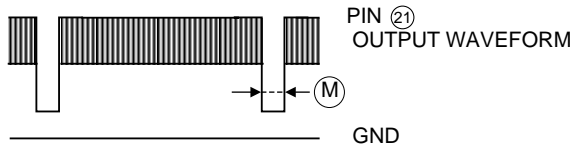
Lower frequencies of SG.d at pin ③⑨ from higher frequency and then measure the frequency when the output waveform at pin ⑱ is pulled in.

VW Vertical Output Pulse Width



PAL/NTSC SYSTEM SINGLE-CHIP COLOR TV SIGNAL PROCESSOR

VBLKW Vertical BLK Width



BLK IN Vertical BLK Input

Apply 5V to BLK IN and test the output DC voltage into pin (21).

AVER1 50/60 Decision 1

AVER2 50/60 Decision 2

AVER3 50/60 Decision 3

AVER4 50/60 Decision 4

For input frequencies, check that the output frequencies at pin (18) are the same (put in the same pull-in status).

At the same time, check the status of BUS write mode (D7).

WVSS Minimum Sync. Detection Width

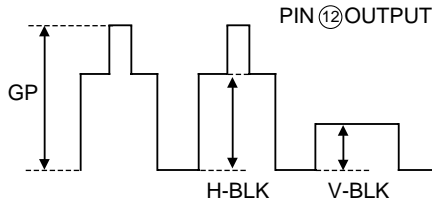
Narrowing the width of SG.d signal at pin (36), measure the input signal width when the output at pin (16) becomes out of synchronization.

SCPG SCP Wave Height Value GP

SCPH SCP Wave Height Value H-BLK

SCPV SCP Wave Height Value V-BLK

Test the output waveform of pin (12) as no input.



VSH1 Vertical Shift Operation 1

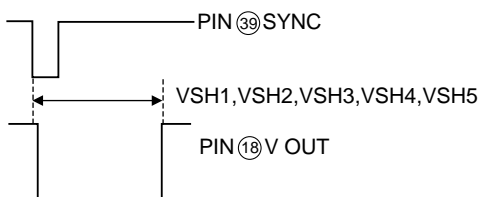
VSH2 Vertical Shift Operation 2

VSH3 Vertical Shift Operation 3

VSH4 Vertical Shift Operation 4

VSH5 Vertical Shift Operation 5

1. Input SG.d(f=50Hz,V=285mVP-P) into pin (36).
2. Measure the delay time from signal input at the center point of falling portion at pin (39) to signal output at the center point of rising portion at pin (18).
3. Make VSH1,VSH2,VSH3,VSH4 and VSH5(nsec) each value.



SWA SW A

Test the voltage of pin (4) when SW A is DATA ON and OFF at no input.

SWB SW B

Test the voltage of pin (4) when SW B is DATA ON and OFF at no input.

IDADJ1 ID ADJ 1 "M"

Test the output DC voltage of pin (52).

IDADJ2 ID ADJ 2 "H"

1. Test the output DC voltage of pin (52).

IDADJ3 ID ADJ 3 "L"

1. Test the output DC voltage of pin (52).

ICVOL IC BUS VOL

Supply a current of 3 mA to pin (14) and then measure the voltage of acknowledge bit.

I²CV_{TH} I²C BUS V_{TH}

Lowering the "H" voltage of SDA/SCL input, measure the voltage at which BUS does not operate.

C_{I²C} I²C BUS Pin Input Capacity

Test the capacity of pin (11) and (14) on OPEN.

fSCL SCL Clock Maximum Operation Frequency

Test the SCL maximum operation frequency BUS reacted.

IBUS IC BUS 0.4V Current

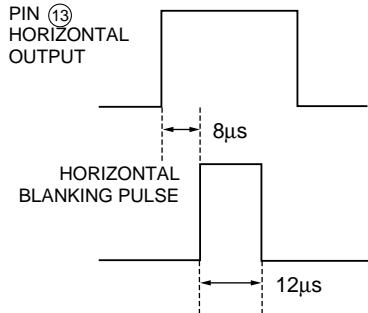
Test the current of pin (11) and (14) when 0.4V is applied.

IDADJ4 ID ADJ 4 "L" 2

Measure the voltage when a current of 180μA flows from pin (52).

PAL/NTSC SYSTEM SINGLE-CHIP COLOR TV SIGNAL PROCESSOR

Note 1. Adjust the one-shot multivibrator's potentiometer so that the timing of the horizontal blanking pulse and pulse width are as shown in the figure below.



Set 8µs via the pin 15 potentiometer of TTL IC, M74LS221P, and set 12µs via the pin 7 potentiometer.

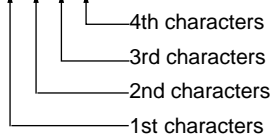
About Input Signal Parameter Including Color Signal

1. The name of input signal is made of 4 alphanumeric characters.

Note)

S	S	4	P
---	---	---	---

 Standard Signal 4.43MHz PAL system



1st Characters : Standard=S , No standard=V (however, the part of change is specified.)

2nd Characters : Meanings of signal

3rd Characters : Expressed as burst and chroma frequency.

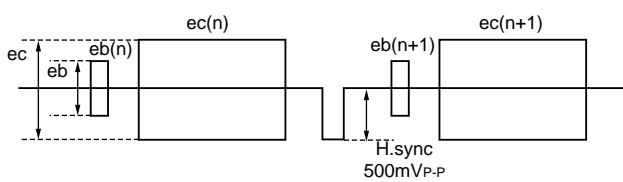
4(4.433619MHz), 3(3.579545MHz) (however, this is treated the same as SECAM standard signal in case of "S")

4th Characters : Expressed as color system.

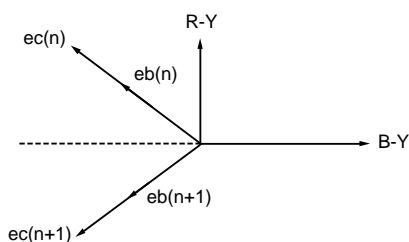
N(NTSC), P(PAL)

2. Configuration of input color signal.

Configurations of color signal are shown in the figure below.



1. If the first character of a signal name is S (standard), the signal conforms to the standard color bar signal in types. However, H.sync is to be added for input clamp. (The frequency of H.sync conforms to the 4th character. P: 50 Hz, N: 60 Hz)
2. The amplitude of burst and the frequency are given in eb. If they are standardized, the amplitude is 285 mVp-p and the frequency conforms to the 3rd character of the signal name.
3. The amplitude of chroma and the frequency are given in ec. If they are standardized, the amplitude is 570 mVp-p and the frequency conforms to the 3rd character of the signal name.
4. The phase correlation on the PAL type signal is shown in the figure below.



PAL/NTSC SYSTEM SINGLE-CHIP COLOR TV SIGNAL PROCESSOR

Video/Interface

SG. No.	Signals (50Ω termination)	
SG. A	<p>PAL type Make input for sync separation PAL type APL 100% normal video signal shown in the figure on the right. Vertical must be inter laced at 50Hz.</p>	
SG. B	<p>On the SGA signal, Lumi. signal frequency and amplitude are variable. However, standard amplitude is 0.714 V_{P-P}</p>	
SG. C		
SG. D		
SG. E		
SG. 50	<p>Level variable typ = 0.3V_{P-P} H = 15.625kHz, V = 50Hz</p>	<p>STANDARD PAL SYNC</p>
SG. F	<p>NTSC type</p>	
SG. 60	<p>Level variable typ = 0.3V_{P-P} H = 15.734kHz, V = 60Hz</p>	<p>STANDARD NTSC SYNC</p>
SG. G	<p>Level variable CW</p>	<p>f = 3.579545MHz</p>

PAL/NTSC SYSTEM SINGLE-CHIP COLOR TV SIGNAL PROCESSOR

AUDIO

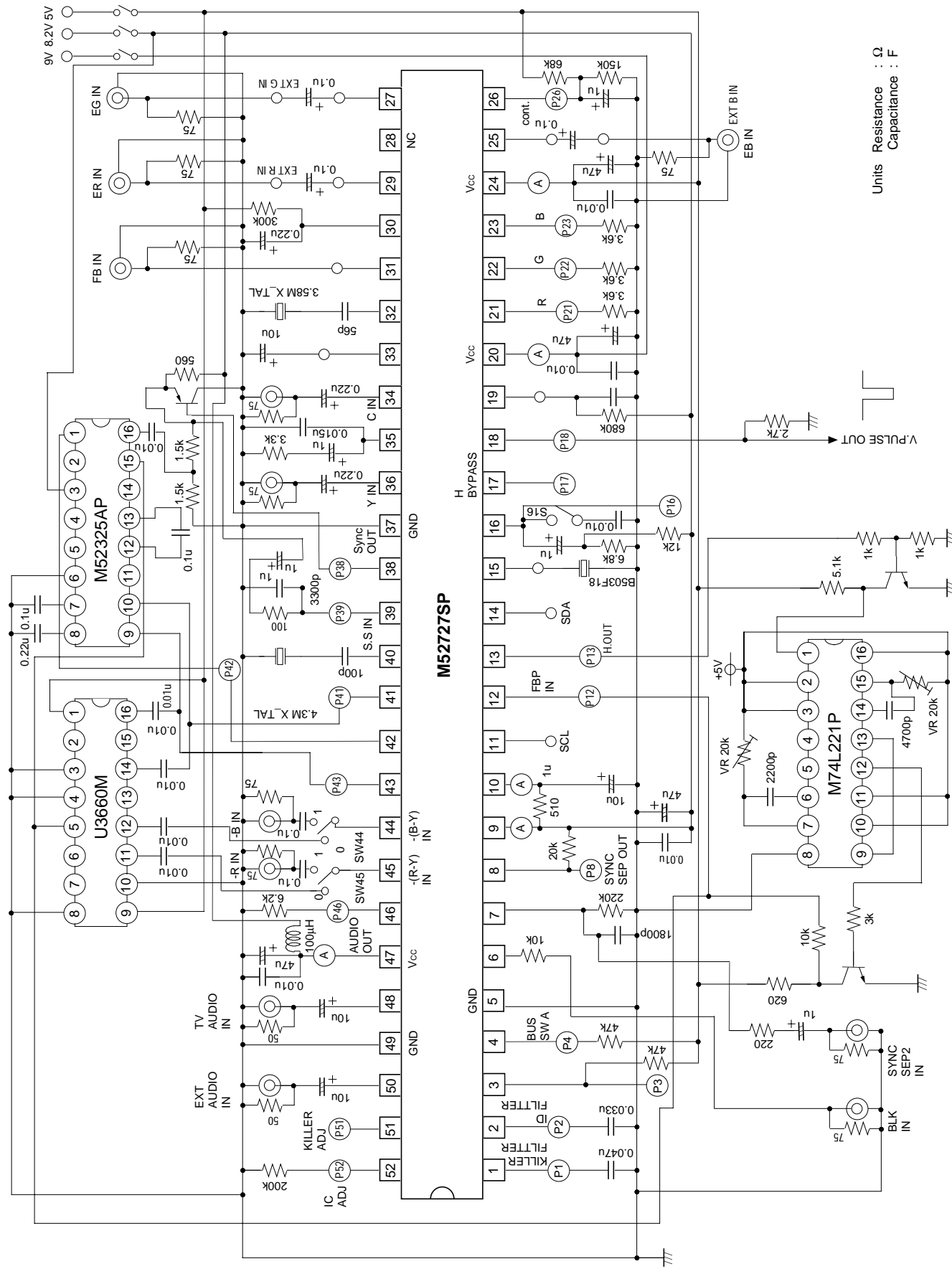
SG. No.	Signals (50Ω termination)
SG. 1	f=1kHz, 1V _{P-P} , CW 50Ωtermination f variable Level variable (TYP f=1kHz, 1V _{P-P})

TENDENCY

SG. No.	Signals (50Ω termination)
SG. a	<p>Make SG.a PAL type APL variable video signal. Vertical must be interlaced at 50Hz.</p>
SG. b	<p>Make SG.b NTSC type APL variable video signal. Vertical must be interlaced at 50Hz.</p>
SG. c	<p>Duty 90% Frequency variable Level variable (standard 1V_{P-P})</p>
SG. d	<p>Duty 95% Frequency variable Level variable (standard 1V_{P-P}) Duty variable (standard : 95%)</p>

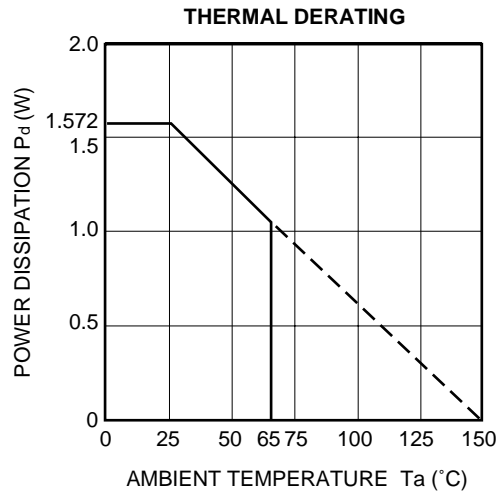
PAL/NTSC SYSTEM SINGLE-CHIP COLOR TV SIGNAL PROCESSOR

TEST CIRCUIT DIAGRAM



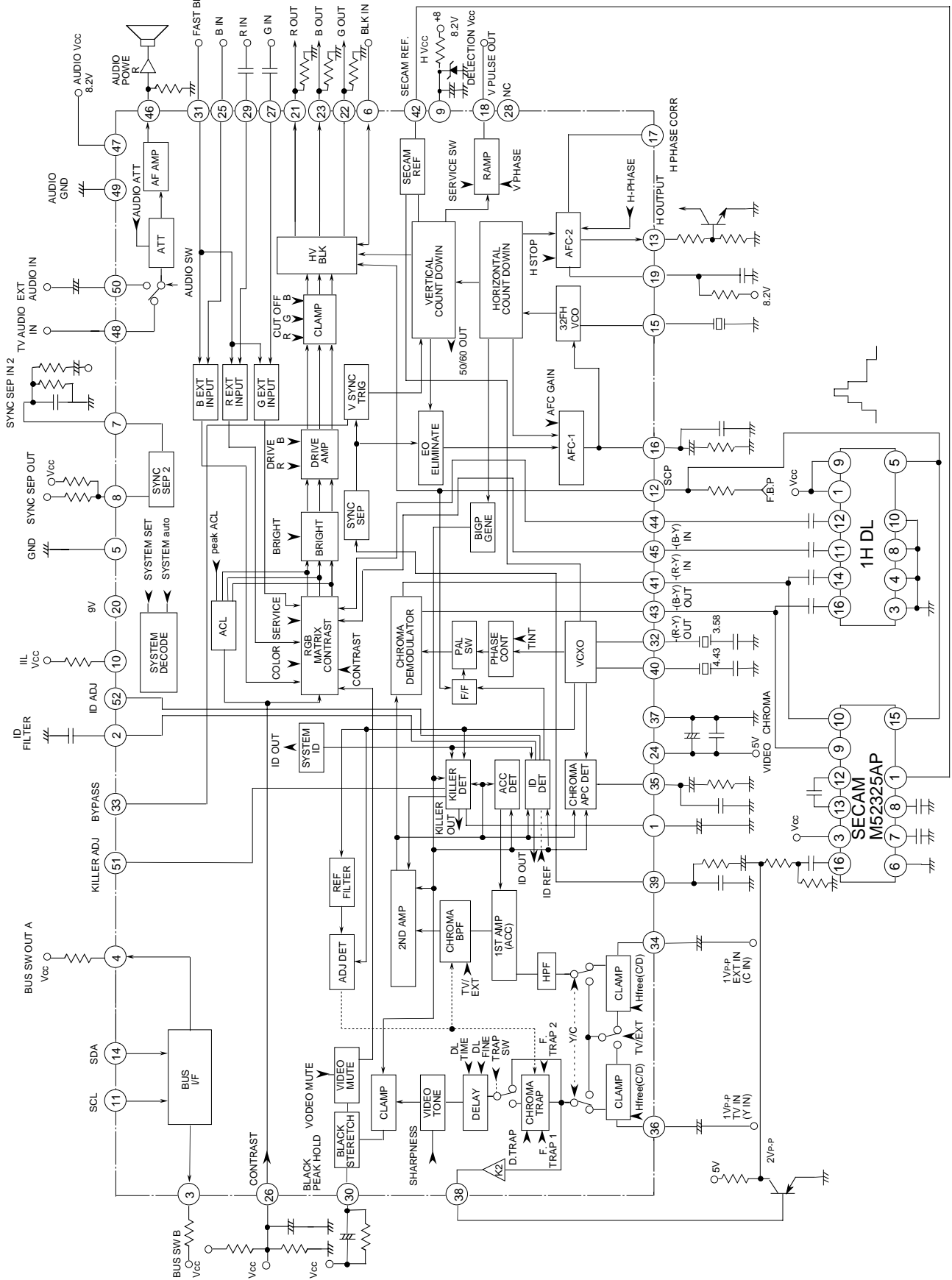
PAL/NTSC SYSTEM SINGLE-CHIP COLOR TV SIGNAL PROCESSOR

TYPICAL CHARACTERISTICS



PAL/NTSC SYSTEM SINGLE-CHIP COLOR TV SIGNAL PROCESSOR

APPLICATION EXAMPLE



PAL/NTSC SYSTEM SINGLE-CHIP COLOR TV SIGNAL PROCESSOR

DESCRIPTION OF PIN

Pin No.	Name	Peripheral circuit of pins	Pin waveform	DC voltage (V)		Note
				Min.	Typ.	
①	KILLER FILTER			Min.	1.90	
				Typ.	2.40	
				Max.	2.90	
②	ID FILTER			Min.	2.20	
				Typ.	2.70	
				Max.	3.20	
③	SUB SWB			Min.	4.80	BUS SW B H
					0	BUS SW B L
				Typ.	5.00	BUS SW B H
					0.30	BUS SW B L
				Max.	5.10	BUS SW B H
					0.50	BUS SW B L
④	BUS SWA			Min.	4.80	BUS SW A H
					0	BUS SW A L
				Typ.	5.00	BUS SW A H
					0.30	BUS SW A L
				Max.	5.10	BUS SW A H
					0.50	BUS SW A L
⑤	GND			Min.	—	
				Typ.	0	
				Max.	—	

PAL/NTSC SYSTEM SINGLE-CHIP COLOR TV SIGNAL PROCESSOR

DESCRIPTION OF PIN (cont.)

Pin No.	Name	Peripheral circuit of pins	Pin waveform	DC voltage (V)		Note
				Min.	Typ.	
⑥	BLK IN			Min.	0	
				Typ.	0	
				Max.	0.3	
⑦	SYNC SEP 2 IN			Min.	5.50	
				Typ.	6.10	
				Max.	6.70	
⑧	SYNC SEP OUT			Min.	8.00	
				Typ.	8.20	
				Max.	8.40	
⑨	H Vcc			Min.	—	
				Typ.	8.20	
				Max.	—	
⑩	IIL Vcc			Min.	1.10	
				Typ.	1.40	
				Max.	1.70	

PAL/NTSC SYSTEM SINGLE-CHIP COLOR TV SIGNAL PROCESSOR

DESCRIPTION OF PIN (cont.)

Pin No.	Name	Peripheral circuit of pins	Pin waveform	DC voltage (V)		Note
				Min.	Typ.	
⑪	SCL			Min.	—	
				Typ.	—	
				Max.	—	
⑫	SCP OUT			Min.	4.21	BGP
					2.50	HBLK
					1.35	VBLK
				Typ.	5.00	BGP
					2.90	HBLK
					1.55	VBLK
Max.	6.50	BGP				
	3.30	HBLK				
	1.80	VBLK				
⑬	H OUT			Min.	3.90	H
					0	L
				Typ.	4.40	H
					0.30	L
Max.	—	H				
	0.50	L				
⑭	SDA			Min.	—	
				Typ.	—	
				Max.	—	
⑮	H OSC			Min.	4.80	
				Typ.	5.4	
				Max.	5.9	

PAL/NTSC SYSTEM SINGLE-CHIP COLOR TV SIGNAL PROCESSOR

DESCRIPTION OF PIN (cont.)

Pin No.	Name	Peripheral circuit of pins	Pin waveform	DC voltage (V)		Note
				Min.	Typ.	
①⑥	AFC 1 ALTER			Min.	4.80	
				Typ.	5.50	
				Max.	6.20	
①⑦	H PHASE CORR			Min.	2.20	
				Typ.	2.70	
				Max.	3.20	
①⑧	V.PULSE OUT			Min.	5.20	H
					—	L
				Typ.	5.80	H
					0	L
				Max.	6.40	H
	0.50	L				
①⑨	AFC2 FILTER			Min.	3.60	
				Typ.	4.20	
				Max.	4.80	
②⑩	HI Vcc			Min.	—	
				Typ.	9.00	
				Max.	—	

PAL/NTSC SYSTEM SINGLE-CHIP COLOR TV SIGNAL PROCESSOR

DESCRIPTION OF PIN (cont.)

Pin No.	Name	Peripheral circuit of pins	Pin waveform	DC voltage (V)		Note
				Min.	Typ.	
(21) (22) (23)	R OUT G OUT B OUT			Min.	1.75	H
					—	L
				Typ.	2.25	H
					0.10	L
			Max.	2.75	H	
				0.50	L	
(24)	VCD Vcc			Min.	—	
				Typ.	5.00	
				Max.	—	
(25) (27) (29)	B IN G IN R IN			Min.	2.20	
				Typ.	2.80	
				Max.	3.40	
(26)	CONTRAST CONT			Min.	2.90	
				Typ.	3.40	
				Max.	3.90	
(28)	N.C			Min.	—	
				Typ.	—	
				Max.	—	

PAL/NTSC SYSTEM SINGLE-CHIP COLOR TV SIGNAL PROCESSOR

DESCRIPTION OF PIN (cont.)

Pin No.	Name	Peripheral circuit of pins	Pin waveform	DC voltage (V)		Note
				Min.	Typ.	
③①	BLACK PEAK FILTER			Min.	2.40	
				Typ.	3.10	
				Max.	3.80	
③②	FAST BLK			Min.	—	
				Typ.	—	
				Max.	—	
③③	X-ral 3.58MHz			Min.	2.80	
				Typ.	3.10	
				Max.	3.60	
③④	BYPASS			Min.	1.50	
				Typ.	2.00	
				Max.	2.50	
③⑤	EXT IN (C IN)			Min.	1.35	
				Typ.	1.85	
				Max.	2.35	

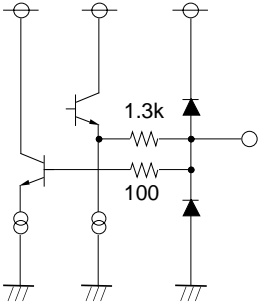

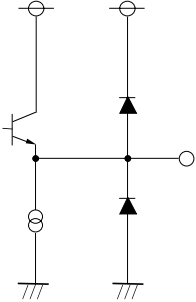

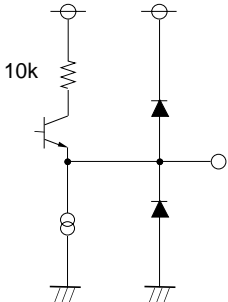
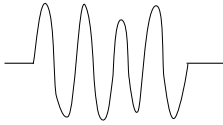
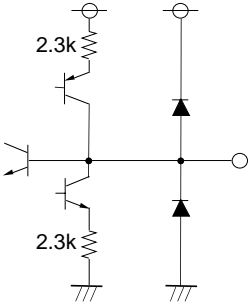

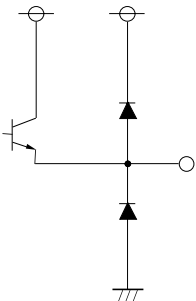

PAL/NTSC SYSTEM SINGLE-CHIP COLOR TV SIGNAL PROCESSOR

DESCRIPTION OF PIN (cont.)

Pin No.	Name	Peripheral circuit of pins	Pin waveform	DC voltage (V)		Note
				Min.	Typ.	
35	CHTROMA APC FILTER			Min.	2.55	
				Typ.	3.05	
				Max.	3.55	
36	TV IN (Y IN)			Min.	1.50	
					3.90	
				Typ.	2.40	
				Max.	2.90	
	5.00					
37	VCD GND			Min.	—	
				Typ.	0	
				Max.	—	
33	V(Y)SW OUT			Min.	1.85	
				Typ.	2.15	
				Max.	2.45	
39	SYNC SEP 1 IN			Min.	1.65	
				Typ.	2.10	
				Max.	2.55	

PAL/NTSC SYSTEM SINGLE-CHIP COLOR TV SIGNAL PROCESSOR

DESCRIPTION OF PIN (cont.)

Pin No.	Name	Peripheral circuit of pins	Pin waveform	DC voltage (V)		Note
				Min.	Typ.	
④①	X-TAL 4.03MHz			Min.	2.70	
				Typ.	3.20	
				Max.	3.70	
④② ④③	-(B-Y) OUT -(R-Y) OUT			Min.	2.45	
				Typ.	2.95	
				Max.	3.45	
④④	SECAM REF			Min.	1.10	
				Typ.	1.50	
				Max.	1.90	
④④ ④⑤	-(B-Y) IN -(R-Y) IN			Min.	2.50	
				Typ.	3.00	
				Max.	3.50	
④⑥	AUDIO OUT			Min.	2.90	
				Typ.	3.30	
				Max.	3.90	

PAL/NTSC SYSTEM SINGLE-CHIP COLOR TV SIGNAL PROCESSOR

DESCRIPTION OF PIN (cont.)

Pin No.	Name	Peripheral circuit of pins	Pin waveform	DC voltage (V)		Note
				Min.	Typ.	
④7	AUDIO Vcc			Min.	—	
				Typ.	8.20	
				Max.	—	
④8	TV AUDIO IN			Min.	2.50	
				Typ.	3.00	
				Max.	3.50	
④9	AUDIO GND			Min.	—	
				Typ.	0	
				Max.	—	
⑤0	EXT AUDIO IN			Min.	2.50	
				Typ.	3.00	
				Max.	3.50	
⑤1	KILLER ADJ			Min.	1.35	
				Typ.	1.80	
				Max.	2.35	

PAL/NTSC SYSTEM SINGLE-CHIP COLOR TV SIGNAL PROCESSOR

DESCRIPTION OF PIN (cont.)

Pin No.	Name	Peripheral circuit of pins	Pin waveform	DC voltage (V)		Note
52	ID ADJ			Min.	1.55	
				Typ.	2.0	
				Max.	2.45	

PIN VOLTAGE STANDARD CONDITION

Sub address	00H	01H		02H						
Function	SWB	IDADJ	AUDsw	SWA	TRAP	D. TRAP	F. TRAP2	ACL	DLFA	SWK
DATA	A0	A6		A3						
Function	0	32	0	0	0	0	0	1	0	0

Sub address	03H	04H	05H	06H					07H
Function	ATT	SHARP	CONT	DLTA	AUTO	TVEXT	Y/C	BLACK	TINT
DATA	A0	A0	A6	A2					A7
Function	0	0	32	2	0	0	0	0	64

Sub address	08H	09H		0AH	0BH		0CH	0DH	0EH	0FH
Function	COLOR	SET	HP	BRI	DG	MUTE	DB	CR	CG	CB
DATA	A0	A7		A6	A6		A6	A8	A8	A8
Function	0	0	8	32	32	0	32	128	128	128

Sub address	10H		13H			
Function	FTR1	CLOFF	SESW	Hfr	AFCG	V Phase
DATA	A6		A0			
Function	1	0	0	0	0	0

PAL/NTSC SYSTEM SINGLE-CHIP COLOR TV SIGNAL PROCESSOR

INITIAL CONDITION

█ : No Function

	D7	D6	D5	D4	D3	D2	D1	D0	DATA
00H	0	SW B 0	1	0	0	0	0	0	A6
01H	0	A UD SW 0	1	0	0	0	0	0	A6
02H	0	SWA 0	TRAP 0	DBF 0	F TRAP2 0	ACL 0	DFA 0	0	A0
03H	0	1	0	0	0	0	0	0	A7
04H	0	0	1	0	0	0	0	0	A6
05H	0	0	1	0	0	0	0	0	A6
06H	0	0	AUTO 0	BLACK 0	Y/C 0	TV/EXT 0	DL TIME 1	0	A2
07H	0	1	0	0	0	0	0	0	A7
08H	0	0	1	0	0	0	0	0	A6
09H	0	1	0	0	0	3.58 0	NTSC 0	SECAM 0	A7
0AH	0	0	1	0	0	0	0	0	A6
0BH	0	MUTE 0	1	0	0	0	0	0	A6
0CH	0	0	1	0	0	0	0	0	A6
0DH	1	0	0	0	0	0	0	0	A8
0EH	1	0	0	0	0	0	0	0	A8
0FH	1	0	0	0	0	0	0	0	A8
10H	0	C OFF 0	F TRAP 0	0	0	0	0	0	A0
13H	0	0	AFCG 0	H Free 0	SERSW 0	V Phase 0	V Phase 0	V Phase 0	A0

PAL/NTSC SYSTEM SINGLE-CHIP COLOR TV SIGNAL PROCESSOR

M52727SP I²C - BUS Format

Sub address byte and data byte format :
read

* SW

	No.	Functions	BIT	SUB ADD	Data byte								
					D7	D6	D5	D4	D3	D2	D1	D0	
OTHER	1												
	2	BUS SWB*	1	00H		SWB							
	3	IDADJ	6	01H	0	-	A15	A14	A13	A12	A11	A10	
	4	AUDIO SW*	1	01H		AUDIO SW							
	5												
	6												
	7	AUDIO ATT	7	03H	0	A36	A35	A34	A33	A32	A31	A30	
VIDEO	8	sharpness	6	04H	0	-	A45	A44	A43	A42	A41	A40	
	9	contrast cont	7	05H	0	A56	A55	A54	A53	A52	A51	A50	
	10	DL time ADJ*	2	06H	0	-	-	-	-	-	A61	A60	
	11	TV/EXT*	1	06H						TV/EXT			
	12	Y/C IN*	1	06H					Y/C				
CHROMA	13	black stretch*	1	06H				black					
	14	TORAP SW*	1	02H			TRAP						
	15	tint cont	7	07H	0	A76	A75	A74	A73	A72	A71	A70	
	16	color cont	7	08H	0	A86	A85	A84	A83	A82	A81	A80	
INTER FACE	17	SYSTEM auto*	1	06H			auto						
	18	SYSTEM SET*	3	09H	0	-	-	-	-	3.58	NTSC	SECAM	
	19	bright cont	7	0AH	0	AA6	AA5	AA4	AA3	AA2	AA1	AA0	
	20	drive (R)	6	0BH	0	0	AB5	AB4	AB3	AB2	AB1	AB0	
	21	drive (B)	6	0CH	0	0	AC5	AC4	AC3	AC2	AC1	AC0	
	22	cut off (R)	8	0DH	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	
	23	cut off (G)	8	0EH	AE7	AE6	AE5	AE4	AE3	AE2	AE1	AE0	
	24	cut off (B)	8	0FH	AF7	AF6	AF5	AF4	AF3	AF2	AF1	AF0	
DEFLECTION	25	DL fine ADJ	+40ns Ons	1	02H						0	1	
	26	peak ACL	Lo Hi	1	02H					0	1		
	27	AFC-2 H phase		4	09H	0	A96	A95	A94	A93	-	-	
	28												
	29												
	30												
	31	V phase		3	13H						AG2	AG1	AG0
	32												
OTHER	33	Service SW*		1	13H				Service SW				
	34	H free*		1	13H			H free					
	35	AFC GAIN*		1	13H			AFC GAIN					
	36												
	37	VIDEO MUTE*		1	0BH		MUTE						
OTHER	38	DOUBLE TRAP*		1	02H			D.TRAP					
	39	TRAP fine ADJ1*		1	10H			F.TRAP1					
	40	BUS SWA*		1	02H		SWA						
	41	TRAP fine ADJ2*		1	02H					F.TRAP2			
	42	CLAMP OFF*		1	10H		CLAMP						

write

Data byte							
D7	D6	D5	D4	D3	D2	D1	D0
50/60	—	KILLER	ID	3.58	NTSC	SECAM	CONDITION

PAL/NTSC SYSTEM SINGLE-CHIP COLOR TV SIGNAL PROCESSOR

Initial Data byte Conditions at Power-ON M52727SP

	Functions	Data	Condition	Initial condition	
OTHER	BUS SWA	SWA	0	H	H
			1	L	
	AUDIO SW	AUDIO SW	0	TV	TV
			1	EXT	
	BUS SWB	SWB	0	H	H
1			L		
VIDEO	DL TIME ADJ	A71 , A70	0 0	170nsec	330nsec
			0 1	200nsec	
			1 0	330nsec	
			1 1	430nsec	
	TV/EXT	TV/EXT	0	TV	TV
			1	EXT	
	Y/C IN	Y/C IN			
	black stretch	black	0	OFF	OFF
			1	ON	
	TRAP SW	TRAP	0	OFF	OFF
1			ON		
INTER FACE	DL fine ADJ	DLf	0	+40nsec	+40nsec
			1	0nsec	
	peak ACL	ACL	0	Lo	Hi
			1	Hi	
CHROMA	SYSTEM auto	auto	0	manual	manual
			1	auto	
	SYSTEM SET	3.58,NTSC,SECAM	0 0 0	4.43 PAL	4.43 PAL
			1 0 0	3.58 PAL	
			1 1 0	3.58 NTSC	
			0 1 0	4.43 NTSC	
0 0 1			SECAM		
DEFLECTION	Service SW	Service SW	0	OFF	OFF
			1	ON	
	H free	H free	0	OFF	OFF
			1	ON	
AFC GAIN	AFC GAIN	0	NORMAL	NORMAL	
		1	HIGH		
OTHER	clamp off	clamp	0	OFF	OFF
			1	ON	
	Video mute	mute	0	OFF	OFF
			1	ON	
	double trap	d.trap	0	single	single
			1	double	
	trap fine adj1	f.trap1	0	low	high
			1	high	
	trap fine adj2	f.trap2	0	low	low
			1	high	

PAL/NTSC SYSTEM SINGLE-CHIP COLOR TV SIGNAL PROCESSOR**Data byte Conditions at D/A**

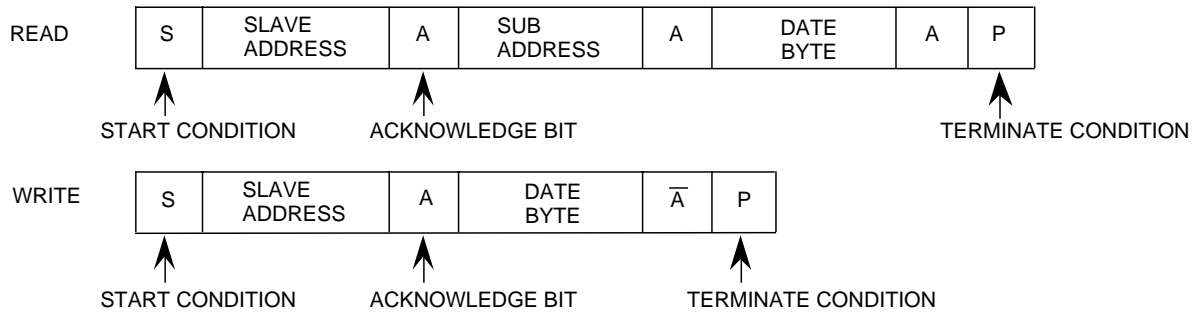
	Functions	BIT	Data	Condition	Initial condition
OTHER	IDADJ	6	0 ~ 63	0 → 63 DC Lo → Hi	32
	AUDIO ATT	7	0 ~ 127	0 → 127 Gain min → max	0
VIDEO	sharpness	6	0 ~ 63	0 → 63 f soft → sharp	0
	contrast cont	7	0 ~ 127	0 → 127 Gain min → max	32
CHROMA	tint cont	7	0 ~ 127	0 → 127 Phase Red → Green	64
	color cont	7	0 ~ 127	0 → 127 Gain min → max	0
INTER FACE	bright cont	7	0 ~ 127	0 → 127 DC Lo → Hi	32
	drive (R)	6	0 ~ 63	0 → 63 Gain min → max	32
	drive (B)	6	0 ~ 63	0 → 63 Gain min → max	32
	cut off (R)	8	0 ~ 255	0 → 255 DC min → max	128
	cut off (G)	8	0 ~ 255	0 → 255 DC min → max	128
	cut off (B)	8	0 ~ 255	0 → 255 DC min → max	128
DEFLE CTION	AFC-2 H phase	4	0 ~ 15	0 → 15 delay min → max	8
	V phase	3	0 ~ 7	0 → 4 delay min → max	0

PAL/NTSC SYSTEM SINGLE-CHIP COLOR TV SIGNAL PROCESSOR

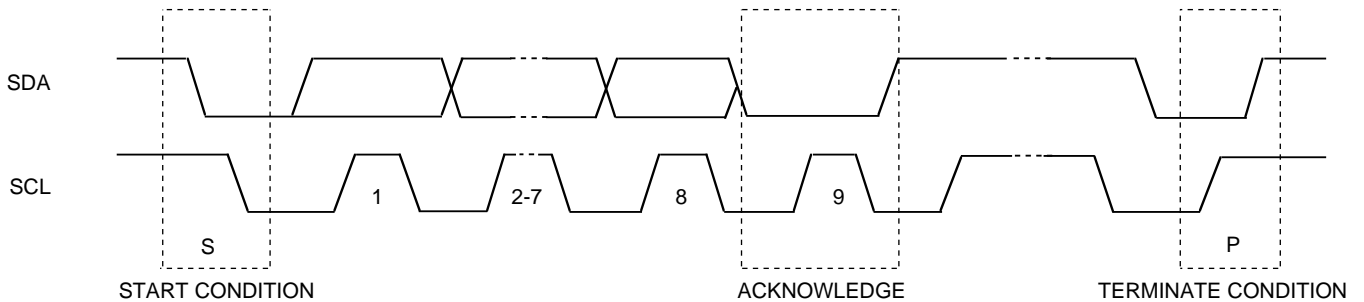
Slave Address

A6	A5	A4	A3	A2	A1	A0	R / W	
1	0	1	1	1	0	1	0	(= B A H) READ
							1	(= B B H) WRITE

DATA Format



Information consists of 8-bit bytes. Each byte is followed by Acknowledge.



NORMAL Condition

Both SDA and SCL are set to HIGH when I²C bus is not used.

Start Condition

Is defined at the falling edge of SDA when SCL is set to HIGH.

Terminate Condition

Is defined at the rising edge of SDA when SCL is set to HIGH.

(Caution)

Except for start condition and termination condition, the SDA level must not change when SCL is set to HIGH.

DATA Transfer

The DATA line level must not be changed during data transfer or when the CLOCK line is set to HIGH. Data is effective only when the clock pulse is set to HIGH (including rising and falling edges to cover areas that are not clear).

Acknowledge

Sending device sends HIGH for the portion of the 9th clock pulse of each byte. In the WRITE operation, this IC pulls down the DATA line for the portion of the 9th clock pulse to keep acknowledging.

READ

The READ status allows data to be input into this IC. In this status, pull-down of Acknowledge bits to this IC keeps the bits LOW.

WRITE

The WRITE status allows data to be output from this IC. In this status, pull-down of Acknowledge bits after data byte to the microcomputer keeps the bits LOW. (The output of the M52727SP is set to HIGH.)

PAL/NTSC SYSTEM SINGLE-CHIP COLOR TV SIGNAL PROCESSOR

Cautions for applications

- When using the IC, keep setting the ID filter at pin ② to 0.033 μ F or less.
 - For output of color difference, add low pass filter, if necessary.
 - The constant of the XTAL (4.43M/3.58M) circumference differs depending on the characteristics of XTAL in use.
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