

SANYO

No. 5082A

LC321664BJ, BM, BT-70/80**1 MEG (65536 words × 16 bits) DRAM
Fast Page Mode, Byte Write**

Overview

The LC321664BJ, BM, BT is a CMOS dynamic RAM operating on a single 5 V power source and having a 65536 words × 16 bits configuration. Equipped with large capacity capabilities, high speed transfer rates and low power dissipation, this series is suited for a wide variety of applications ranging from computer main memory and expansion memory to commercial equipment.

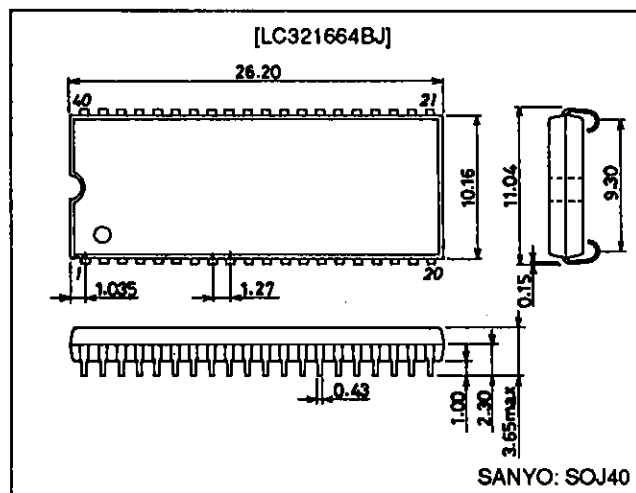
Address input utilizes a multiplexed address bus which permits it to be enclosed in a compact plastic package of 40-pin SOJ. Refresh rates are within 4 ms with 256 row address (A0 to A7) selection and support Row Address Strobe ($\overline{\text{RAS}}$)-only refresh, Column Address Strobe ($\overline{\text{CAS}}$)-before- $\overline{\text{RAS}}$ refresh and hidden refresh settings. There are functions such as fast page mode, read-modify-write and byte write.

Features

- 65536 words × 16 bits configuration.
- Single 5 V ± 10% power supply.
- All input and output (I/O) TTL compatible.
- Supports fast page mode, read-modify-write and byte write.
- Supports output buffer control using early write and Output Enable ($\overline{\text{OE}}$) control.
- 4 ms refresh using 256 refresh cycles.
- Supports $\overline{\text{RAS}}$ -only refresh, $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh and hidden refresh.
- Packages
 - SOJ 40-pin (400 mil) plastic package : LC321664BJ
 - SOP 40-pin (525 mil) plastic package : LC321664BM
 - TSOP 44-pin (400 mil) plastic package : LC321664BT
- $\overline{\text{RAS}}$ access time/column address access time/ $\overline{\text{CAS}}$ access time/cycle time/power dissipation

Package Dimensions

unit: mm

3200-SOJ40

Parameter	LC321664BJ, BM, BT	
	-70	-80
$\overline{\text{RAS}}$ access time	70 ns	80 ns
Column address access time	40 ns	45 ns
$\overline{\text{CAS}}$ access time	25 ns	25 ns
Cycle time	125 ns	135 ns
Power dissipation (max)	During operation	688 mW
	During standby	5.5 mW (CMOS level)/11 mW (TTL level)

SANYO Electric Co., Ltd. Semiconductor Business Headquarters

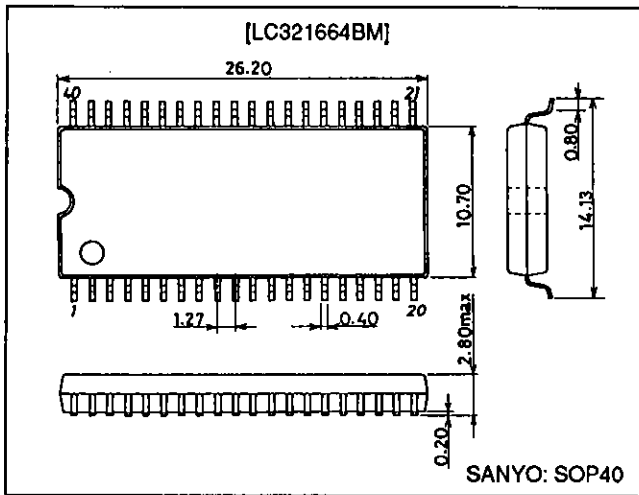
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

LC321664BJ, BM, BT-70/80

Package Dimensions

unit: mm

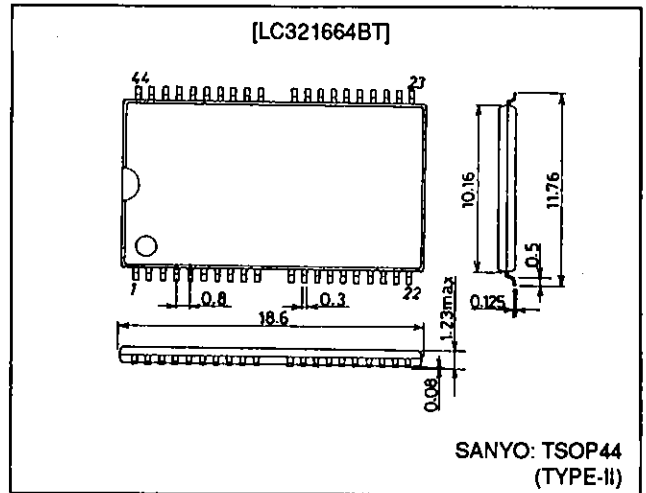
3195-SOP40



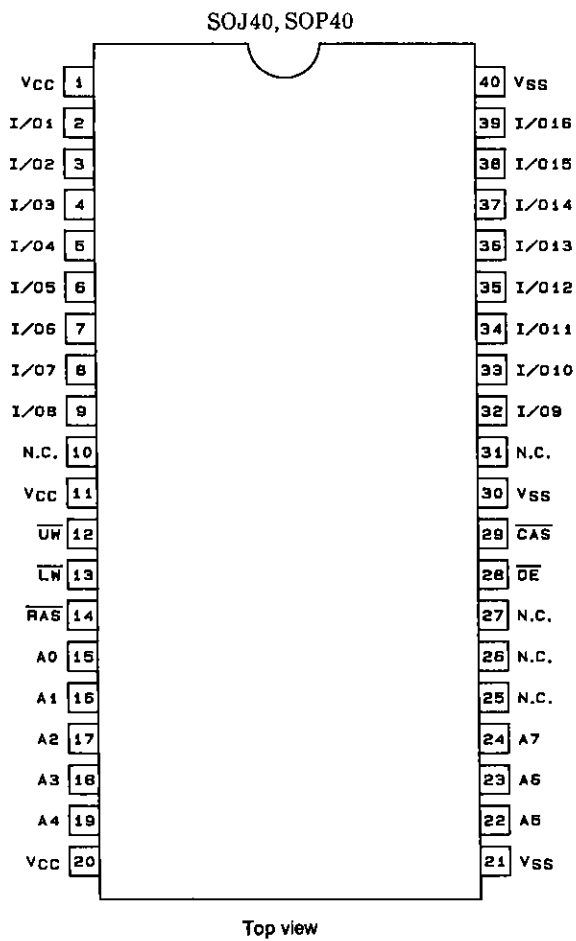
Package Dimensions

unit: mm

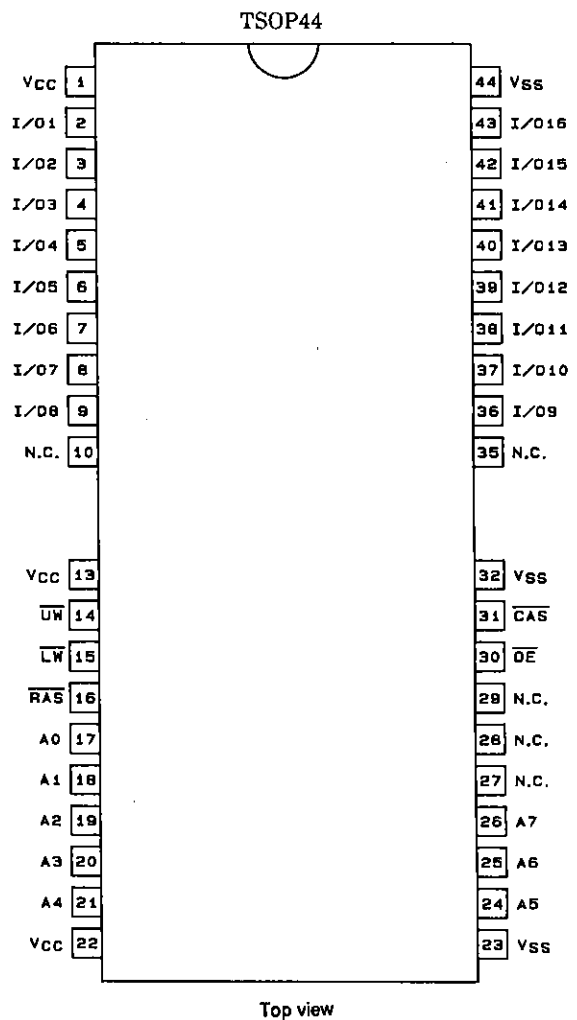
3207-TSOP44



Pin Assignments

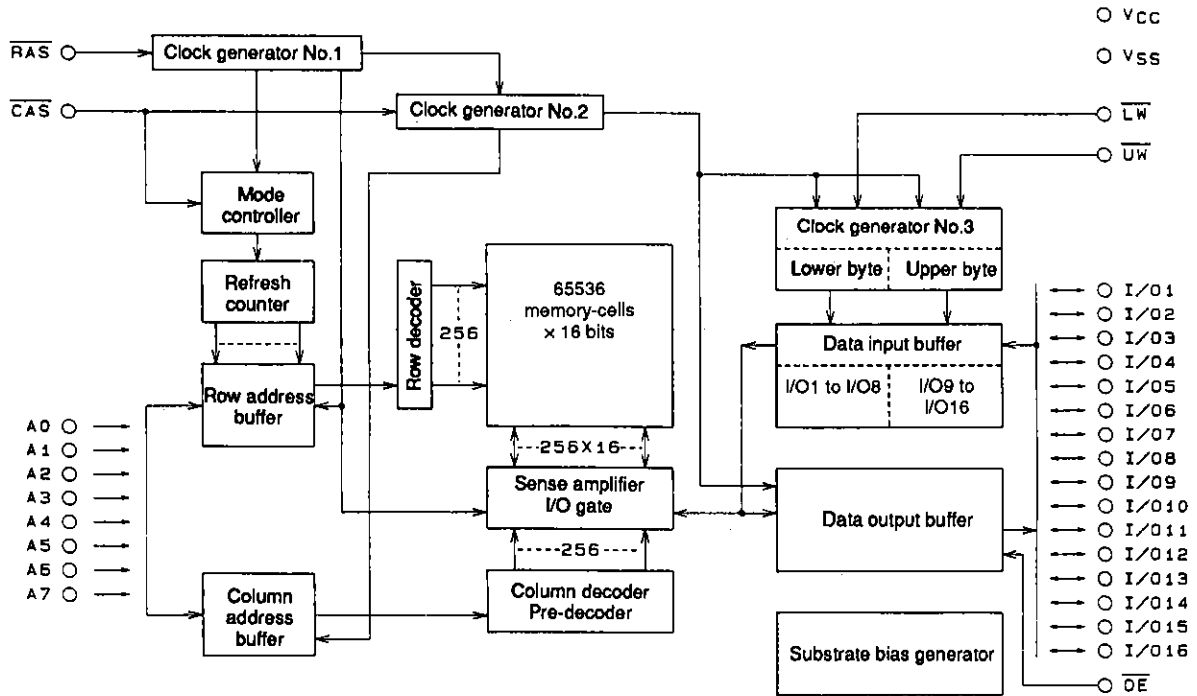


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Block Diagram



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Specifications

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note	
Maximum supply voltage	V _{CC} max	-1.0 to +7.0	V	1	
Input voltage	V _{IN}	-1.0 to +7.0	V	1	
Output voltage	V _{OUT}	-1.0 to +7.0	V	1	
Allowable power dissipation	Pd max	LC321664BJ, BM	800	mW	1
		LC321664BT	700		
Output short-circuit current	I _{OUT}	50	mA	1	
Operating temperature range	T _{opr}	0 to +70	°C	1	
Storage temperature range	T _{stg}	-55 to +150	°C	1	

Note: 1. Stresses greater than the above listed maximum values may result in damage to the device.

DC Recommended Operating Ranges at Ta = 0 to +70°C

Parameter	Symbol	min	typ	max	Unit	Note
Power supply voltage	V _{CC}	4.5	5.0	5.5	V	2
Input high level voltage	V _{IH}	2.4		6.5	V	2
Input low level voltage (A0 to A7, RAS, CAS, UW, LW, OE)	V _{IL}	-1.0*		+0.8	V	2
Input low level voltage (I/O1 to I/O16)	V _{IL}	-0.5*		+0.8	V	2

Note: 2. All voltages are referenced to V_{SS}.
 A bypass capacitor of about 0.1 μF should be connected between V_{CC} and V_{SS} of the device.
 *: -2.0 V when pulse width is less than 20 ns.

LC321664BJ, BM, BT-70/80

DC Electrical Characteristics at Ta = 0 to +70°C, VCC = 5 V ± 10%

Parameter	Symbol	Conditions	LC321664BJ, BM, BT				Unit	Note
			-70		-80			
			min	max	min	max		
Operating current (Average current during operation)	I _{CC1}	RAS, CAS, address cycling: t _{RC} = t _{RC} min		125		115	mA	3, 4, 5
Standby current	I _{CC2}	RAS = CAS = V _{IH}		2		2	mA	
RAS-only refresh current	I _{CC3}	RAS cycling, CAS = V _{IH} : t _{RC} = t _{RC} min		125		115	mA	3, 5
Fast page mode current	I _{CC4}	RAS = V _{IL} , CAS, address cycling: t _{PC} = t _{PC} min		80		70	mA	3, 4, 5
Standby current	I _{CC5}	RAS = CAS = V _{CC} - 0.2 V		1		1	mA	
CAS-before-RAS refresh current	I _{CC6}	RAS, CAS cycling: t _{RC} = t _{RC} min		125		115	mA	3
Input leakage current	I _{IL}	0 V ≤ V _{IN} ≤ 6.5 V, pins other than test pin = 0 V	-10	+10	-10	+10	μA	
Output leakage current	I _{OL}	D _{OUT} disable, 0 V ≤ V _{OUT} ≤ 5.5 V	-10	+10	-10	+10	μA	
Output high level voltage	V _{OH}	I _{OUT} = -2.5 mA	2.4		2.4		V	
Output low level voltage	V _{OL}	I _{OUT} = 2.1 mA		0.4		0.4	V	

Note: 3. All current values are measured at minimum cycle rate. Since current flows immoderately, if cycle time is longer than shown here, current value becomes smaller.

4. I_{CC1} and I_{CC4} are dependent on output loads. Maximum values for I_{CC1} and I_{CC4} represent values with output open.

5. Address change is less than or equal to one time during RAS = V_{IL}. Concerning I_{CC4}, it is less than or equal to one time during 1 cycle (t_{PC}).

AC Electrical Characteristics at Ta = 0 to +70°C, VCC = 5 V ± 10% (Notes 6, 7 and 8)

Parameter	Symbol	LC321664BJ, BM, BT				Unit	Note
		-70		-80			
		min	max	min	max		
Random read, write cycle time	t _{RC}	125		135		ns	
Read-write/read-modify-write cycle time	t _{RWC}	170		180		ns	
Fast page mode cycle time	t _{PC}	50		55		ns	
Fast page mode read-write/read-modify-write cycle time	t _{PRWC}	95		100		ns	
RAS access time	t _{RAC}		70		80	ns	9, 14, 15
CAS access time	t _{CAC}		25		25	ns	9, 14
Column address access time	t _{AA}		40		45	ns	9, 15
CAS precharge access time	t _{CPA}		45		50	ns	9
Output low-impedance time from CAS low	t _{CLZ}	0		0		ns	9
Output buffer turn-off delay time	t _{OFF}	0	20	0	20	ns	10
Rise, fall time	t _T	3	50	3	50	ns	
RAS precharge time	t _{RP}	45		45		ns	
RAS pulse width	t _{RAS}	70	10000	80	10000	ns	
RAS pulse width for fast page mode only	t _{RASP}	70	100000	80	100000	ns	
RAS hold time	t _{RSH}	25		25		ns	
CAS hold time	t _{CSH}	70		80		ns	
CAS pulse width	t _{CAS}	25	10000	25	10000	ns	
RAS to CAS delay time	t _{RCD}	20	45	20	55	ns	14
RAS to column address delay time	t _{RAD}	15	30	15	35	ns	15
CAS to RAS precharge time	t _{CRP}	10		10		ns	
CAS precharge time	t _{CP}	10		10		ns	
Row address setup time	t _{ASR}	0		0		ns	
Row address hold time	t _{RAH}	10		10		ns	
Column address setup time	t _{ASC}	0		0		ns	
Column address hold time	t _{CAH}	15		15		ns	
Column address hold time referenced to RAS	t _{AR}	50		55		ns	
Column address to RAS lead time	t _{RAL}	35		40		ns	
Read command setup time	t _{RCS}	0		0		ns	
Read command hold time referenced to CAS	t _{RCH}	0		0		ns	11
Read command hold time referenced to RAS	t _{RRH}	0		0		ns	11
Write command hold time	t _{WCH}	15		15		ns	
Write command hold time referenced to RAS	t _{WCR}	50		55		ns	

Continued on next page.

LC321664BJ, BM, BT-70/80

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Parameter	Symbol	LC321664BJ, BM, BT				Unit	Note
		-70		-80			
		min	max	min	max		
Write command pulse width	t_{WP}	15		15		ns	
Write command to \overline{RAS} lead time	t_{RWL}	20		20		ns	
Write command to \overline{CAS} lead time	t_{CWL}	20		20		ns	
Data input setup time	t_{DS}	0		0		ns	12
Data input hold time	t_{DH}	15		15		ns	12
Data input hold time referenced to \overline{RAS}	t_{DHR}	50		55		ns	
Refresh time	t_{REF}		4		4	ms	
Write command setup time	t_{WCS}	0		0		ns	13
\overline{CAS} to \overline{UW} , \overline{LW} delay time	t_{CWD}	45		45		ns	13
\overline{RAS} to \overline{UW} , \overline{LW} delay time	t_{RWD}	90		100		ns	13
Column address to \overline{UW} , \overline{LW} delay time	t_{AWD}	60		65		ns	13
\overline{CAS} precharge \overline{UW} , \overline{LW} delay time for fast page mode cycle only	t_{CPWD}	65		70		ns	13
\overline{CAS} setup time for \overline{CAS} -before- \overline{RAS}	t_{CSR}	10		10		ns	
\overline{CAS} hold time for \overline{CAS} -before- \overline{RAS}	t_{CHR}	10		10		ns	
\overline{RAS} precharge \overline{CAS} active time	t_{RPC}	10		10		ns	
\overline{CAS} precharge time for \overline{CAS} -before- \overline{RAS} counter test	t_{CPT}	40		40		ns	
\overline{RAS} hold time referenced to \overline{OE}	t_{ROH}	15		15		ns	
\overline{OE} access time	t_{OEA}		25		25	ns	9
\overline{OE} delay time	t_{OED}	15		15		ns	
\overline{OE} output buffer turn-off delay time	t_{OEZ}	0	15	0	15	ns	10
\overline{OE} command hold time	t_{OEH}	20		20		ns	
Data input to \overline{CAS} delay time	t_{DZC}	0		0		ns	16
Data input to \overline{OE} delay time	t_{DZO}	0		0		ns	16
Masked write setup time	t_{MCS}	0		0		ns	
Masked write hold time referenced to \overline{RAS}	t_{MRH}	0		0		ns	
Masked write hold time referenced to \overline{CAS}	t_{MCH}	0		0		ns	

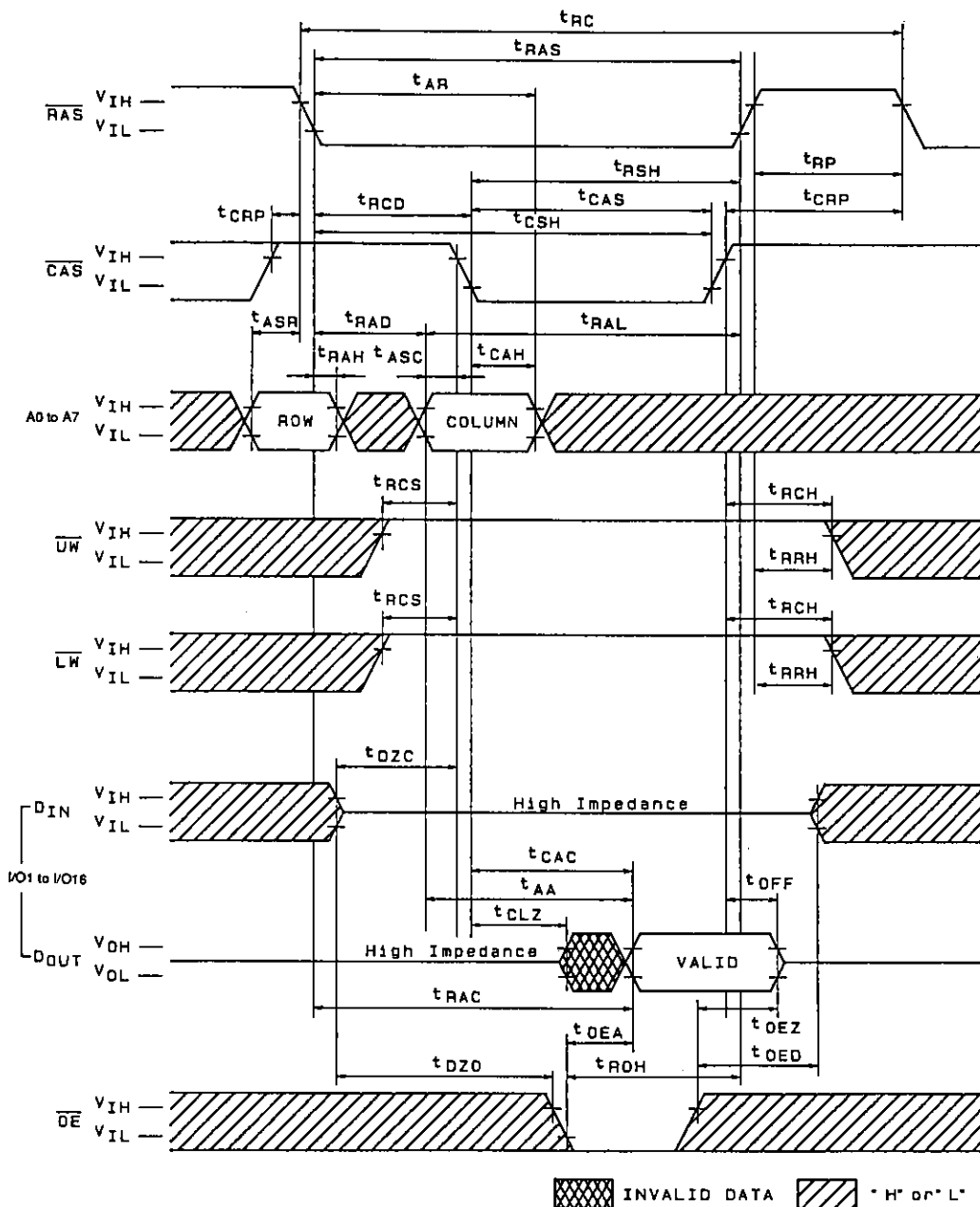
Input/Output Capacitance at $T_a = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = 5\text{ V} \pm 10\%$

Parameter	Symbol	min	max	Unit	Note
Input capacitance (A0 to A7, \overline{RAS} , \overline{CAS} , \overline{UW} , \overline{LW} , \overline{OE})	C_{IN}		7	pF	
Input/Output capacitance (I/O1 to I/O16)	C_{IO}		7	pF	

- Note:
- An initial pause of 200 μs is required after power-up followed by eight \overline{RAS} -only refresh cycles before proper device operation is achieved. In case of using refresh counter, a minimum of eight \overline{CAS} -before- \overline{RAS} refresh cycles instead of eight \overline{RAS} -only refresh cycles are required.
 - Measured at $t_T = 5\text{ ns}$.
 - When measuring input signal timing, V_{IH} (min) and V_{IL} (max) are used for reference points. In addition, rise and fall time are defined between V_{IH} and V_{IL} .
 - Measured using an equivalent of 50 pF and one standard TTL loads.
 - t_{OFF} (max) and t_{OEZ} (max) are defined as the time until output voltage can no longer be measured when output switches to a high impedance condition.
 - Operation is guaranteed if either t_{RRH} or t_{RCH} is satisfied.
 - These parameters are measured from the falling edge of \overline{CAS} for an early-write cycle, and from the falling edge of \overline{UW} and \overline{LW} for a read-write/read-modify-write cycle.
 - t_{WCS} , t_{CWD} , t_{RWD} , t_{AWD} and t_{CPWD} are not restrictive operating parameters for memory in that they specify the operating mode. If $t_{WCS} \geq t_{WCS}$ (min), the cycle switches to an early-write cycle and output pins switch to high impedance throughout the cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPWD} \geq t_{CPWD}$ (min) for fast page mode cycle only, the cycle switches to a read-write/read-modify-write cycle and data output equal information in the selected cells. If neither of the above timings are satisfied, output pins are in an undefined state.
 - t_{RCD} (max) is not a restrictive operating parameter but instead represents the point at which the access time t_{RAC} (max) is guaranteed. If $t_{RCD} \geq t_{RCD}$ (max), access time is determined according to t_{CAC} .
 - t_{RAD} (max) is not a restrictive operating parameter but instead represents the point at which the access time t_{RAC} (max) is guaranteed. If $t_{RAD} \geq t_{RAD}$ (max), access time is determined according to t_{AA} .
 - Operation is guaranteed if either t_{DZC} or t_{DZO} is satisfied.

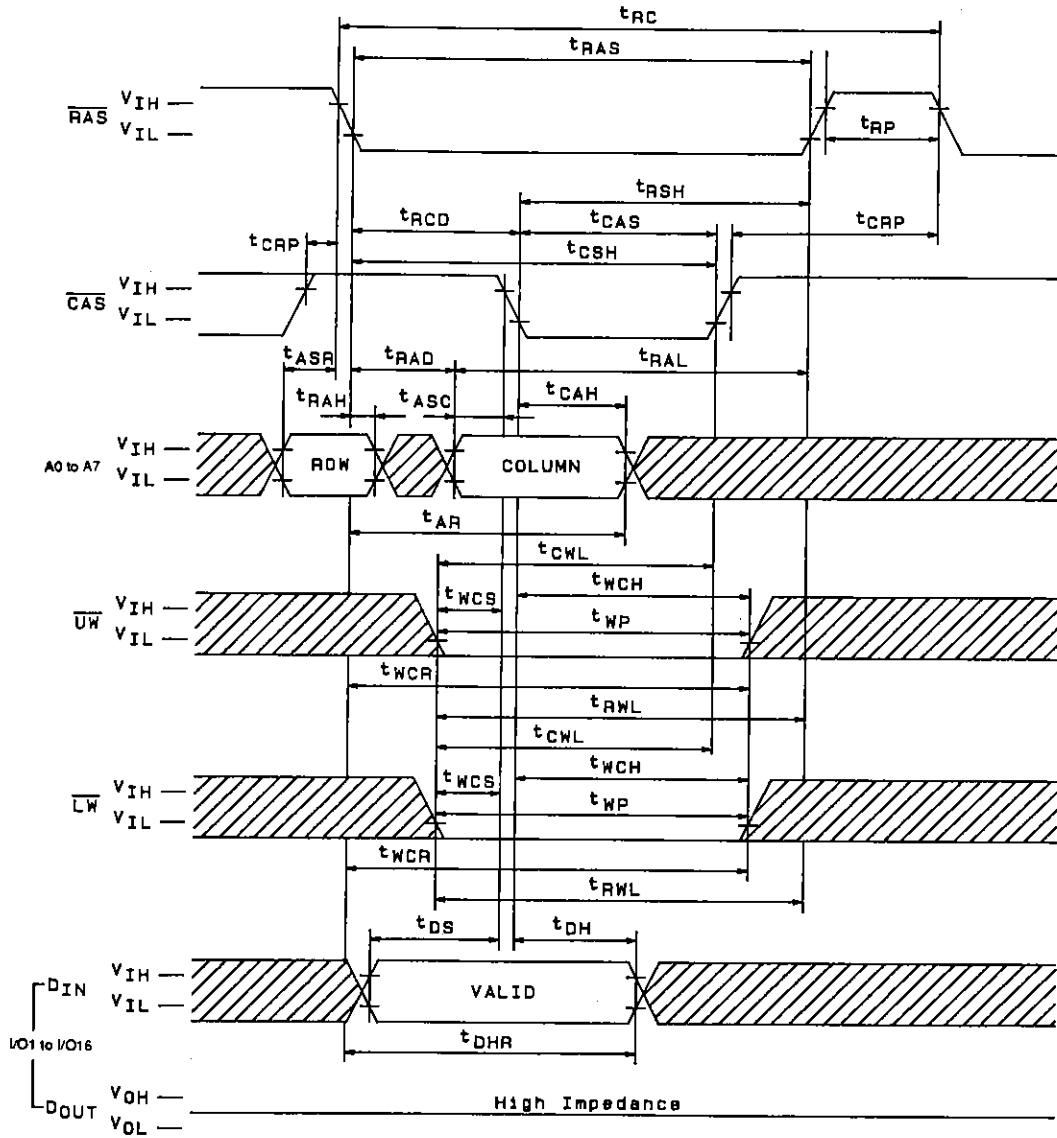
Timing Chart

Read Cycle



A02139

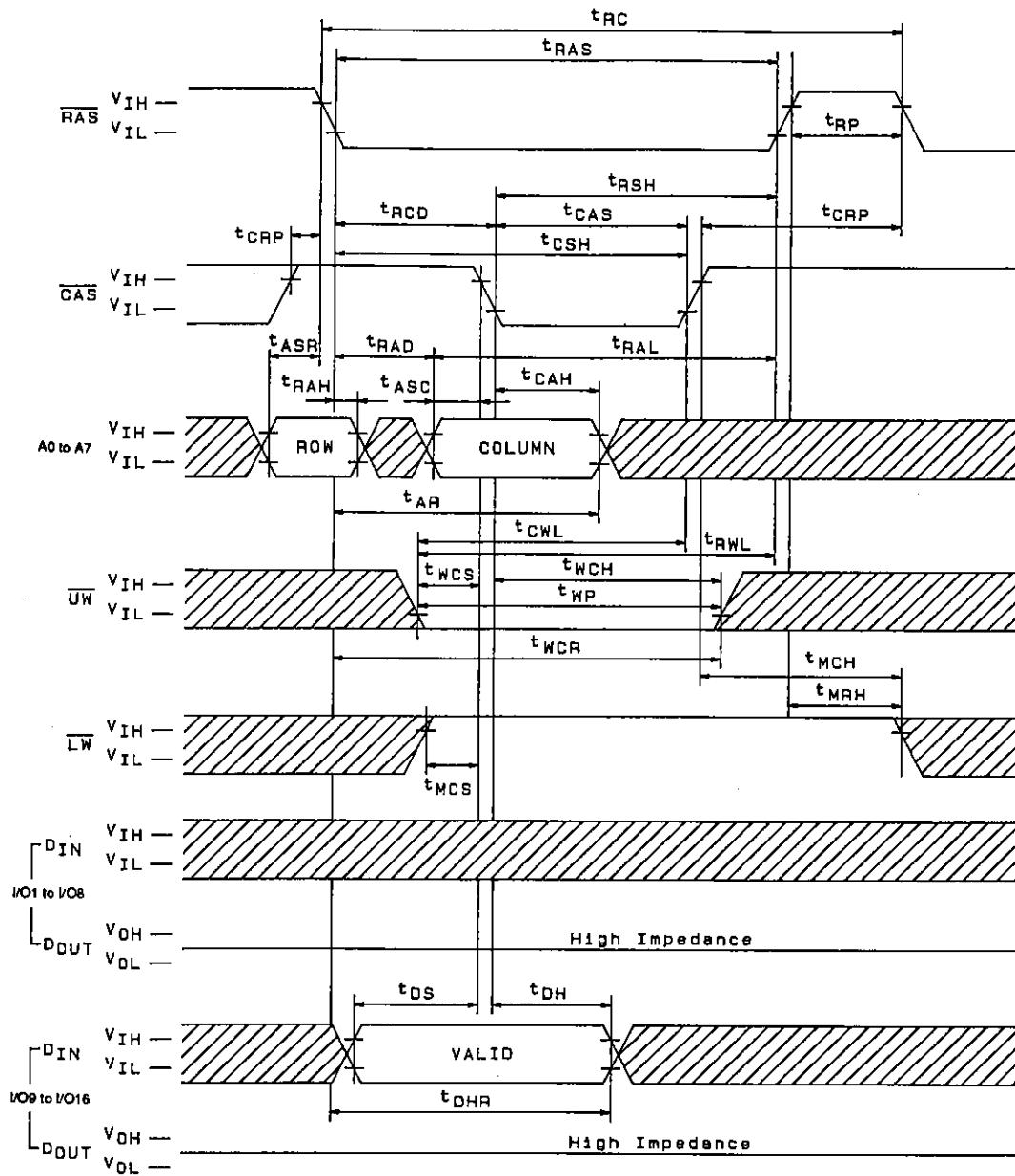
Early Write Cycle



* H* or L*
 \overline{OE} : * H* or L*

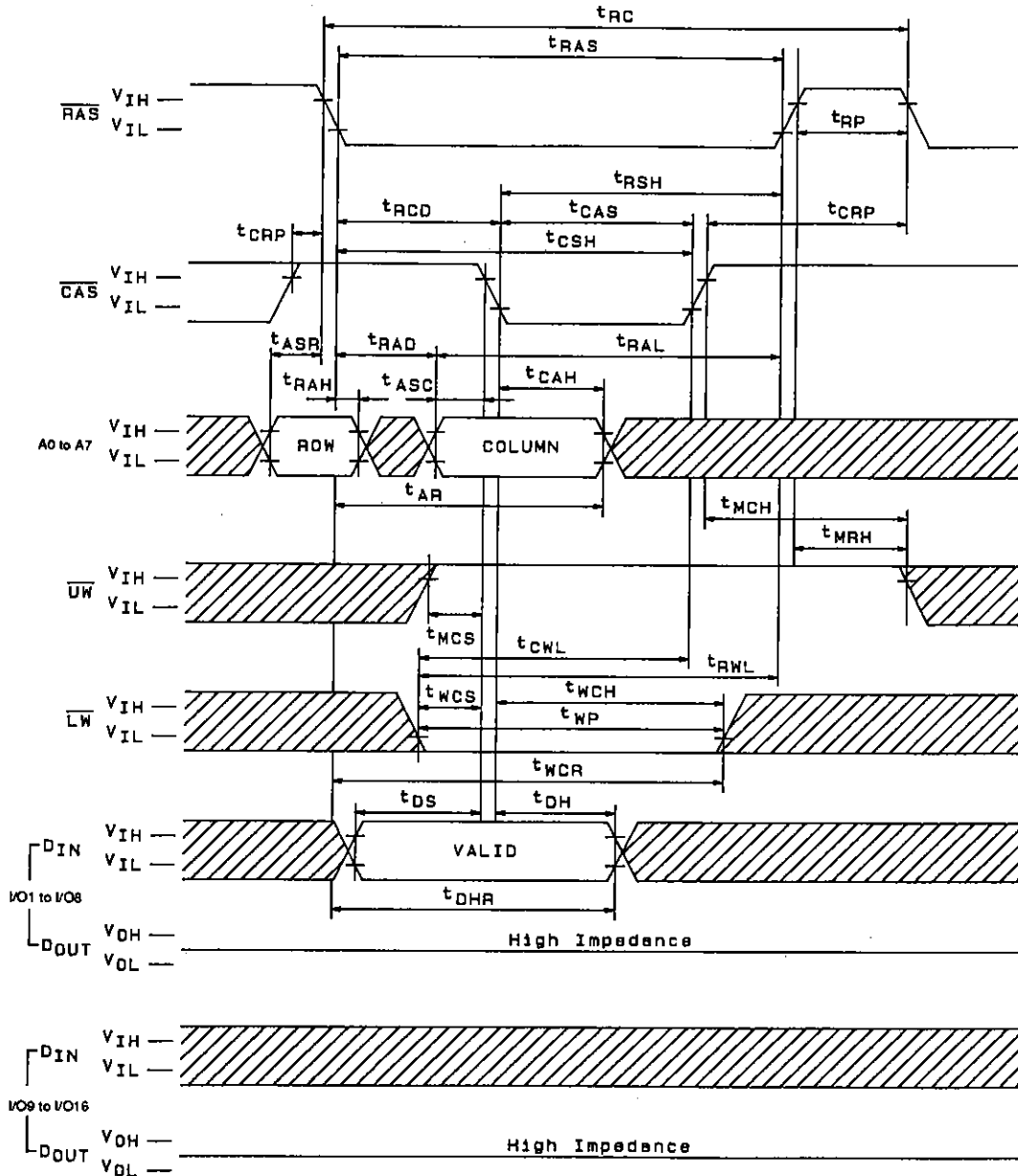
A02140

Upper Byte Early Write Cycle



A02141

Lower Byte Early Write Cycle

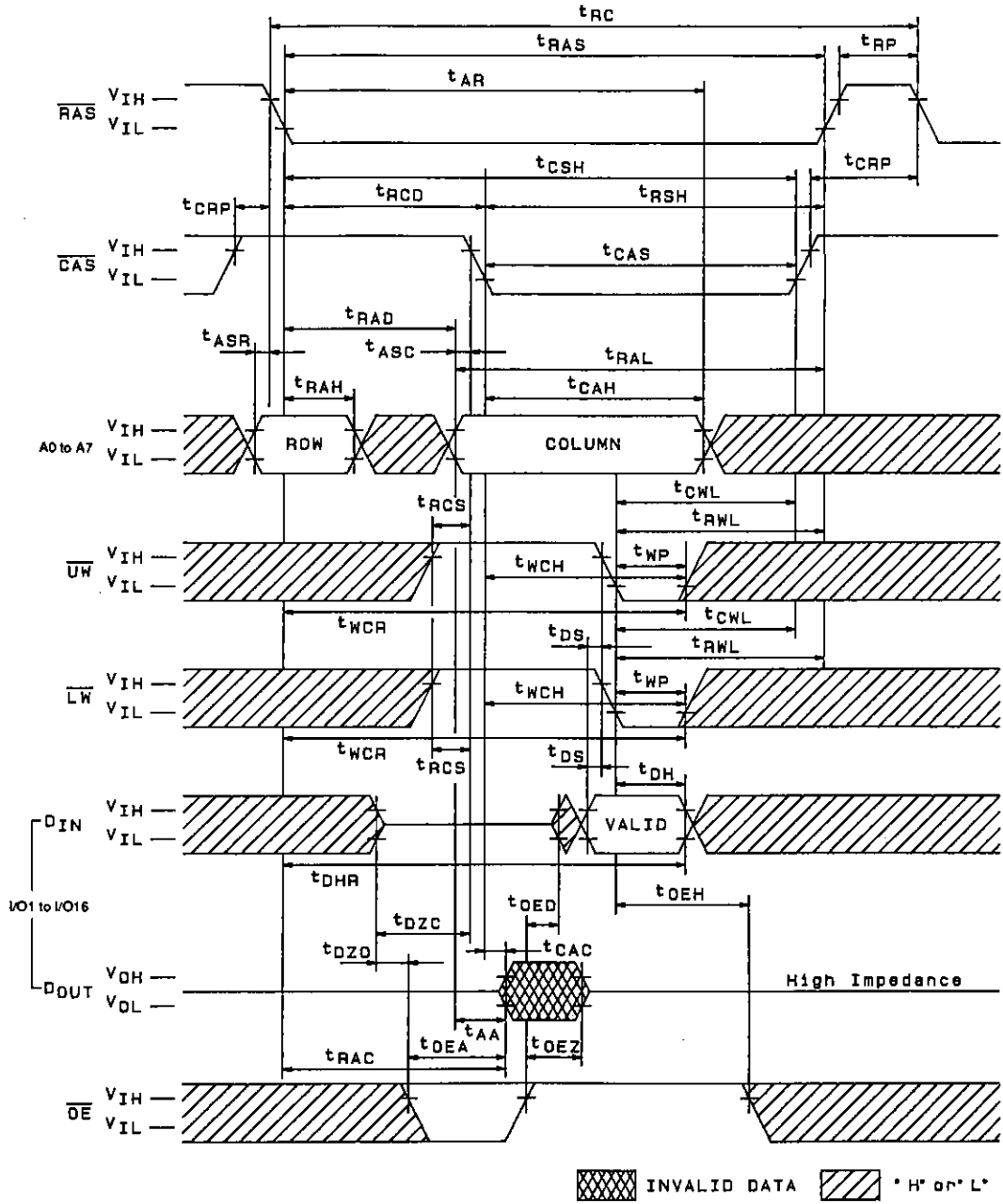


* H* or * L*

\overline{OE} : * H* or * L*

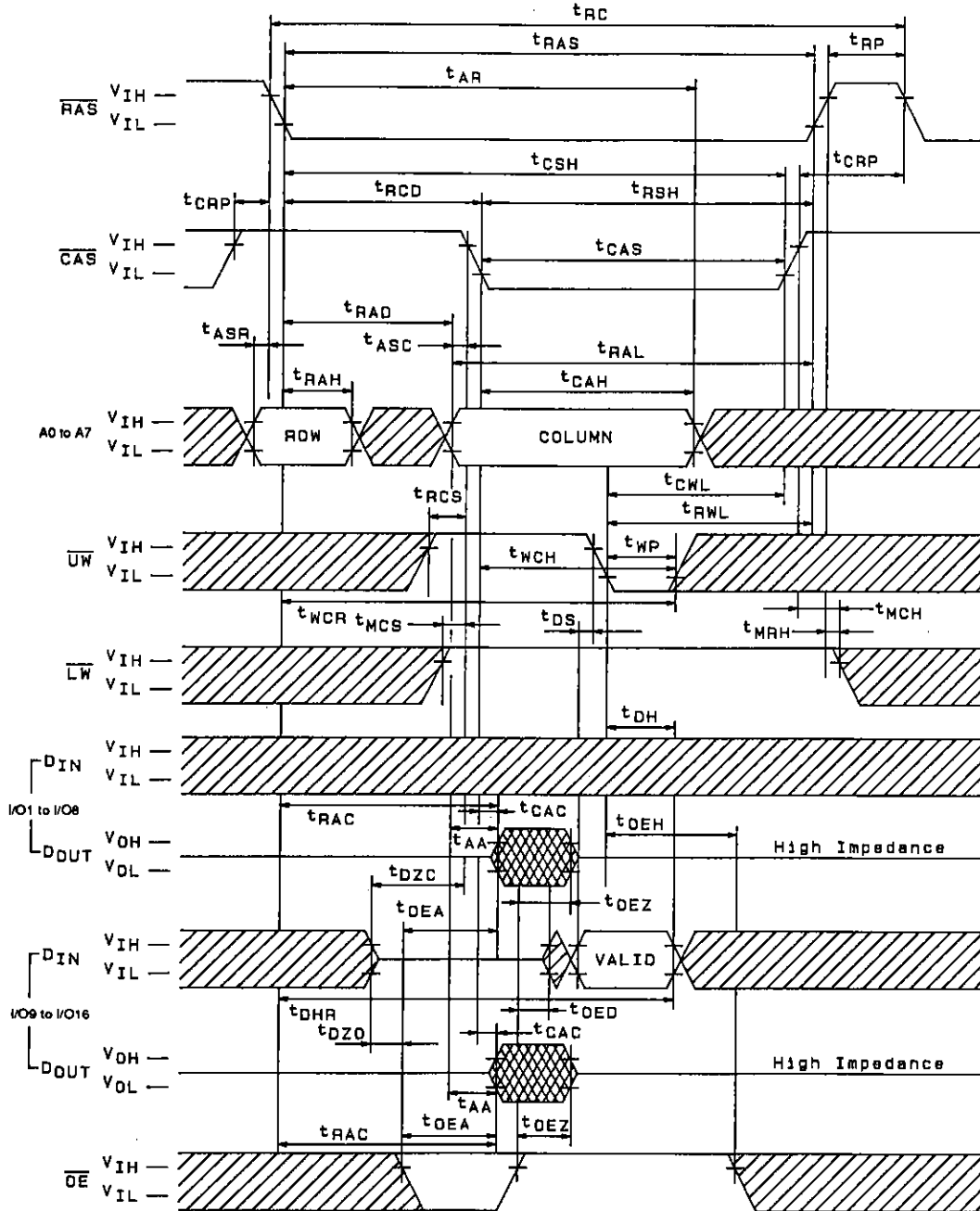
A02142

Write Cycle (\overline{OE} Control)



A02143

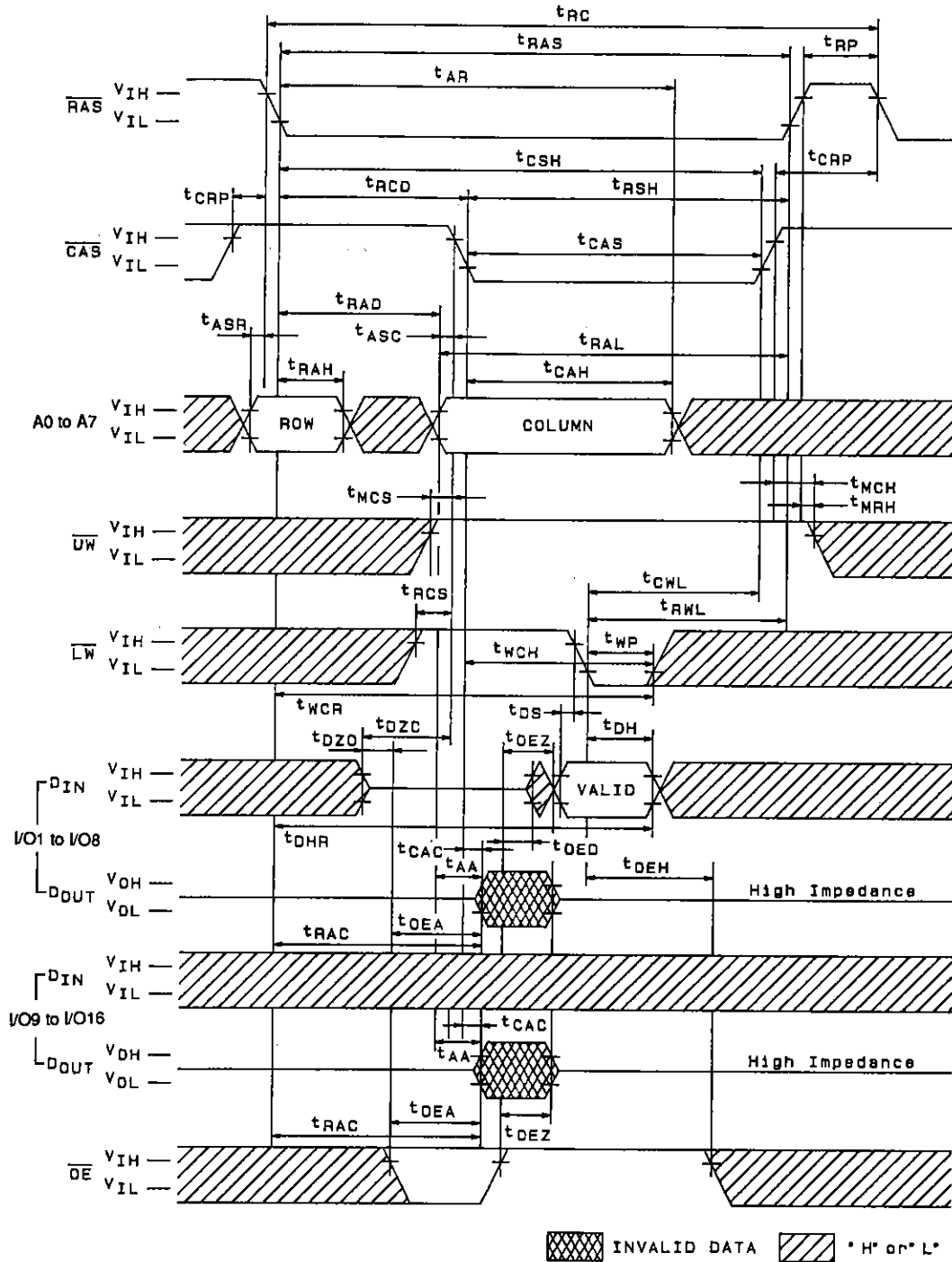
Upper Byte Write Cycle (\overline{OE} Control)



INVALID DATA "H" or "L"

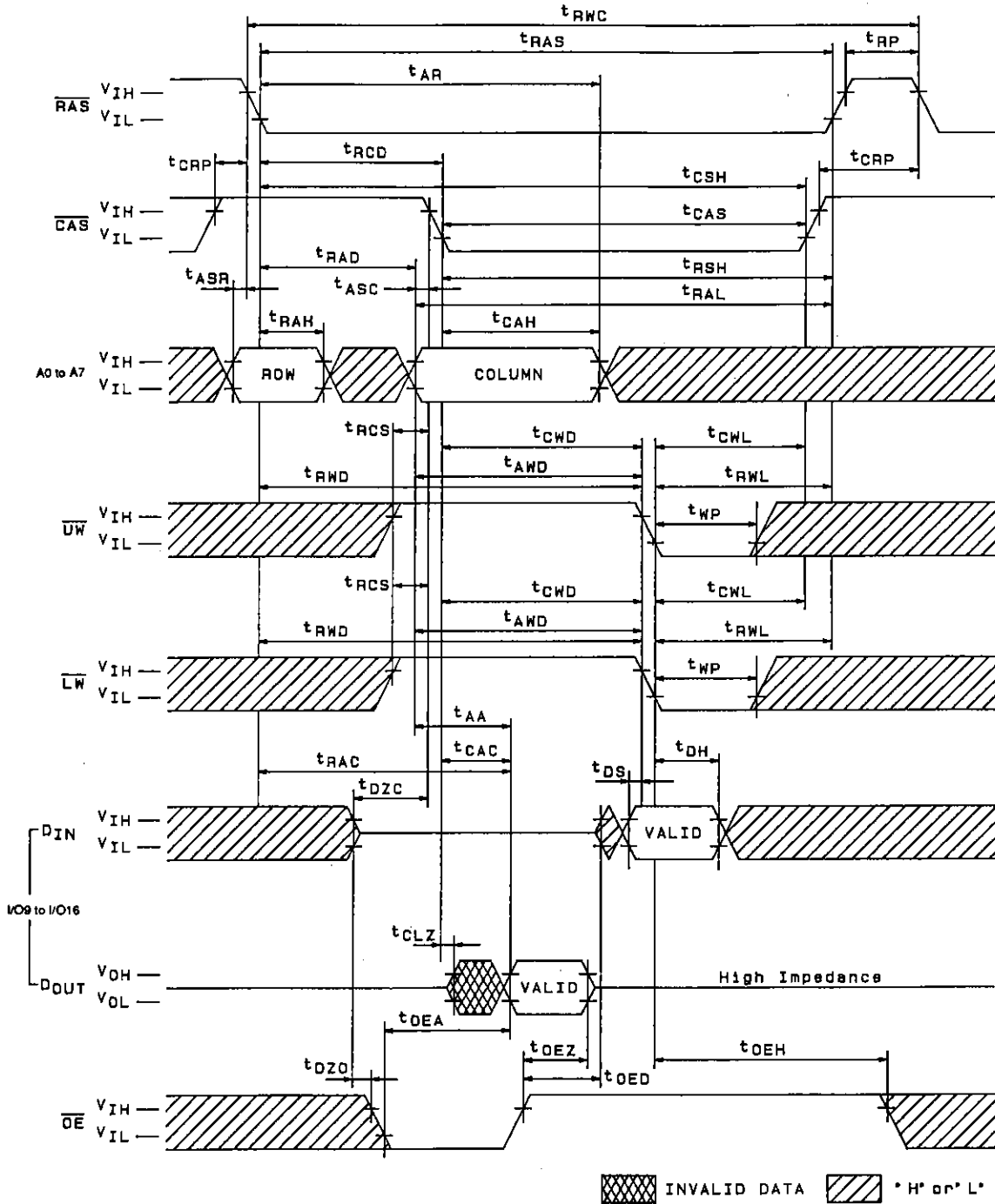
A02144

Lower Byte Write Cycle (\overline{OE} Control)



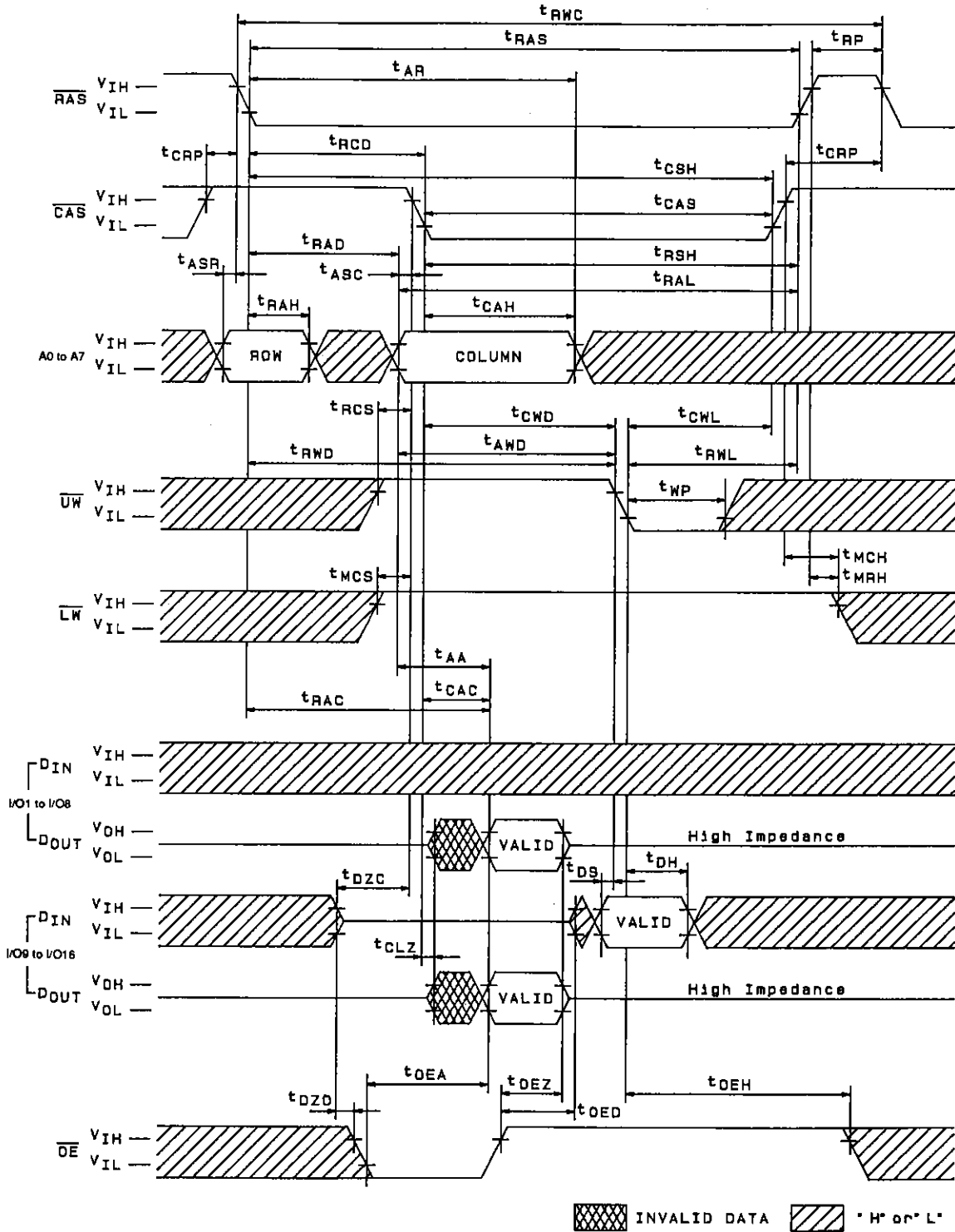
A02145

Read-Modify Write Cycle



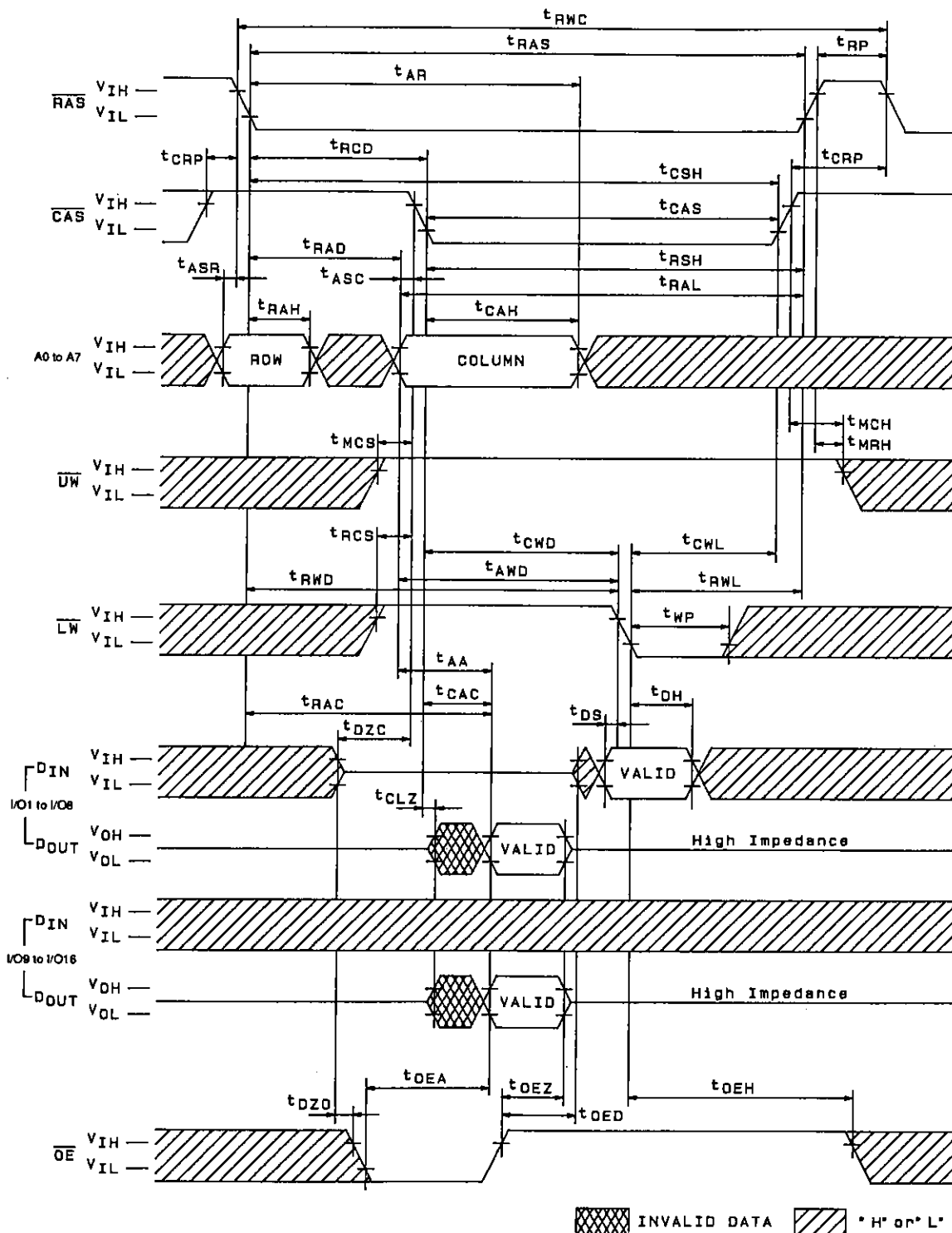
A02146

Read-Modify Upper Byte Write Cycle



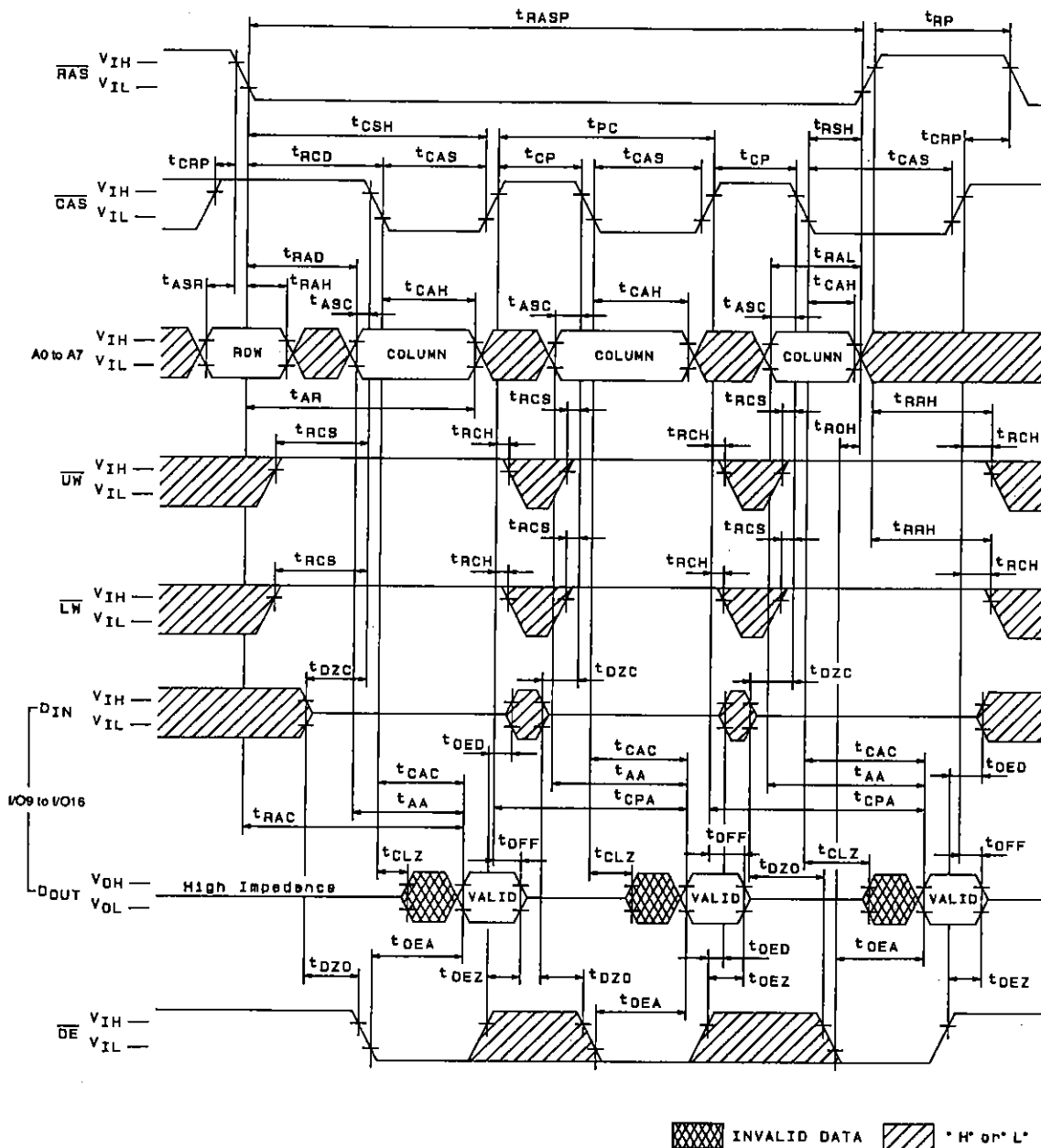
A02147

Read-Modify Lower Byte Write Cycle



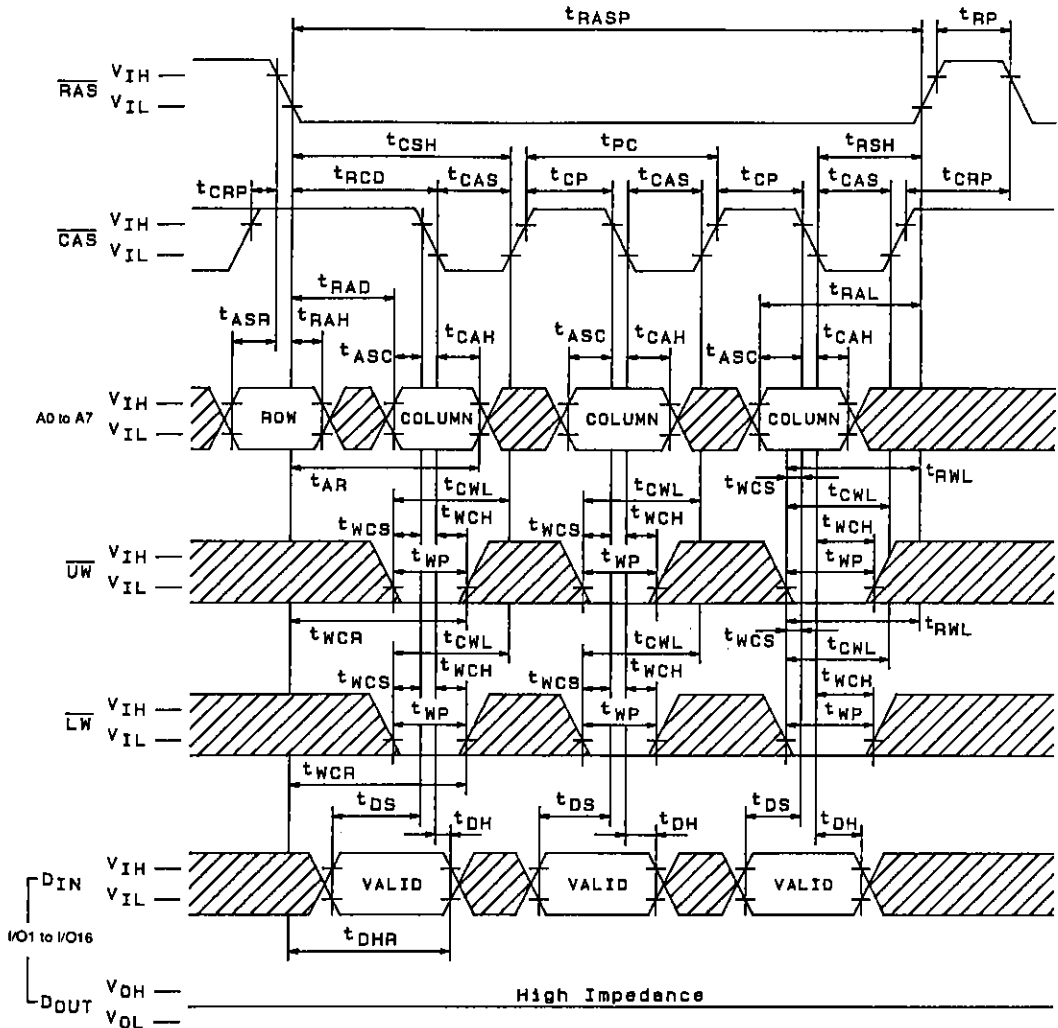
A02148

Fast Page Mode Read Cycle



A02149

Fast Page Mode Early Write Cycle

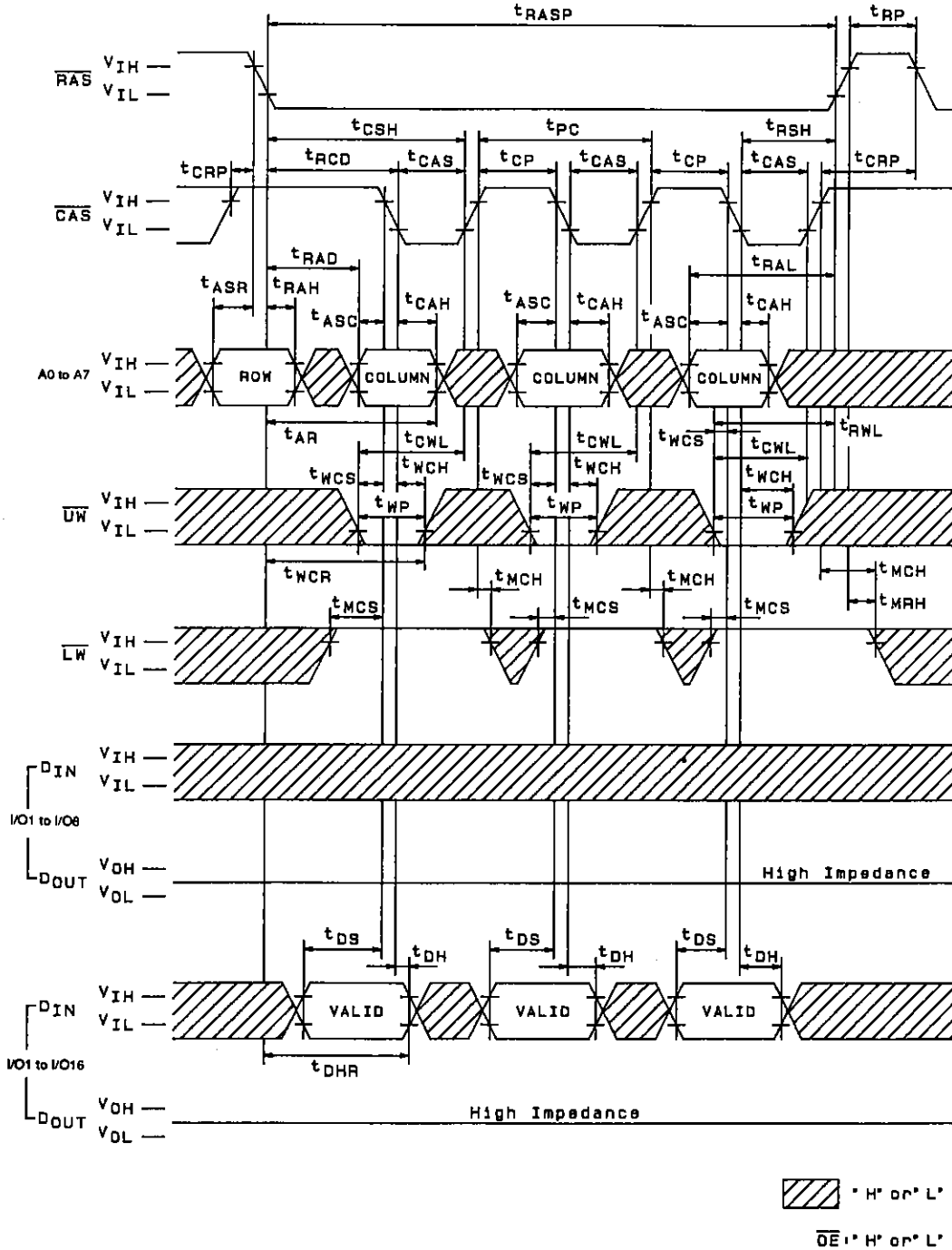


▨ * H* or L*

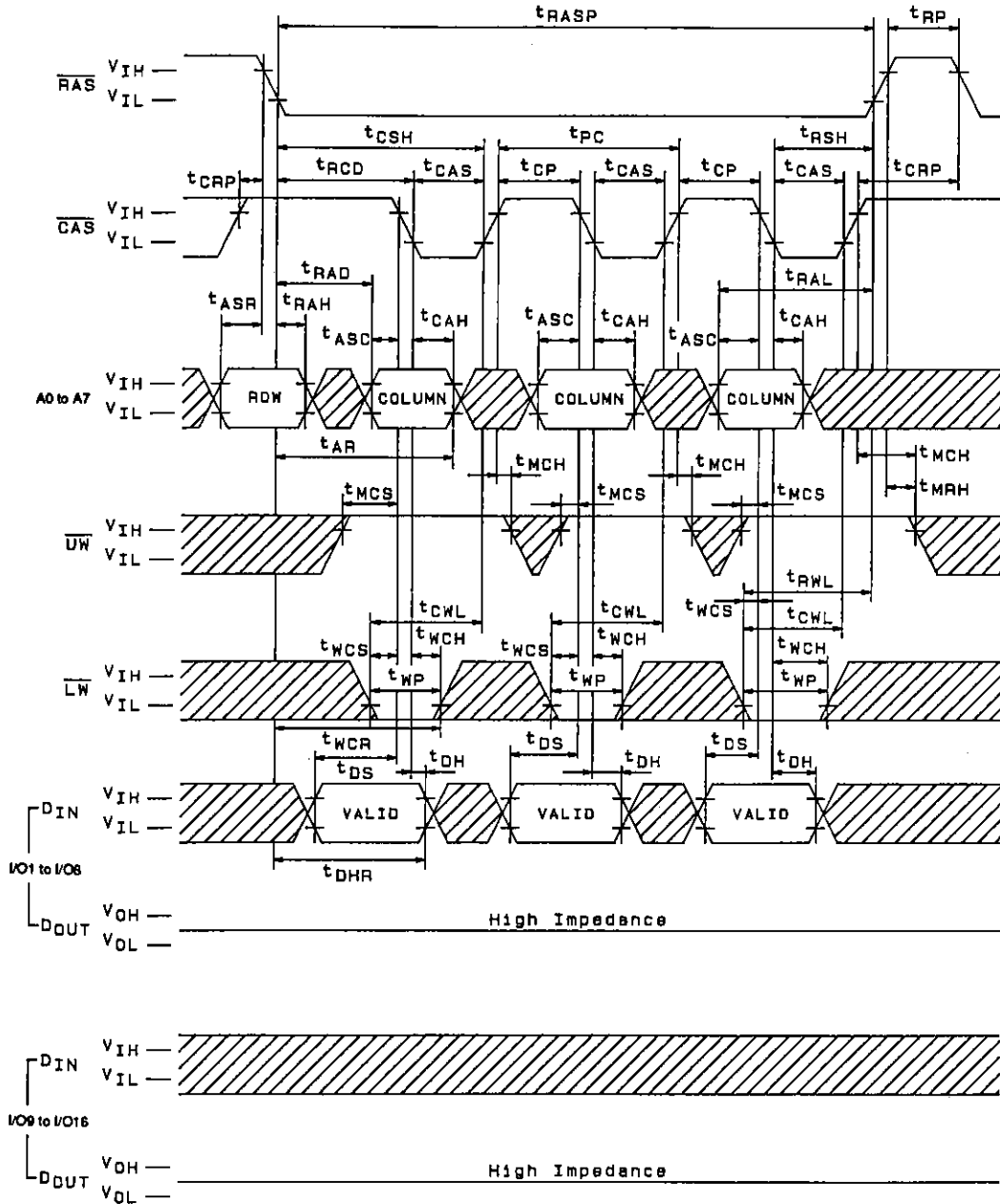
\overline{OE} : * H* or L*



A02180

Fast Page Mode Upper Byte Early Write Cycle



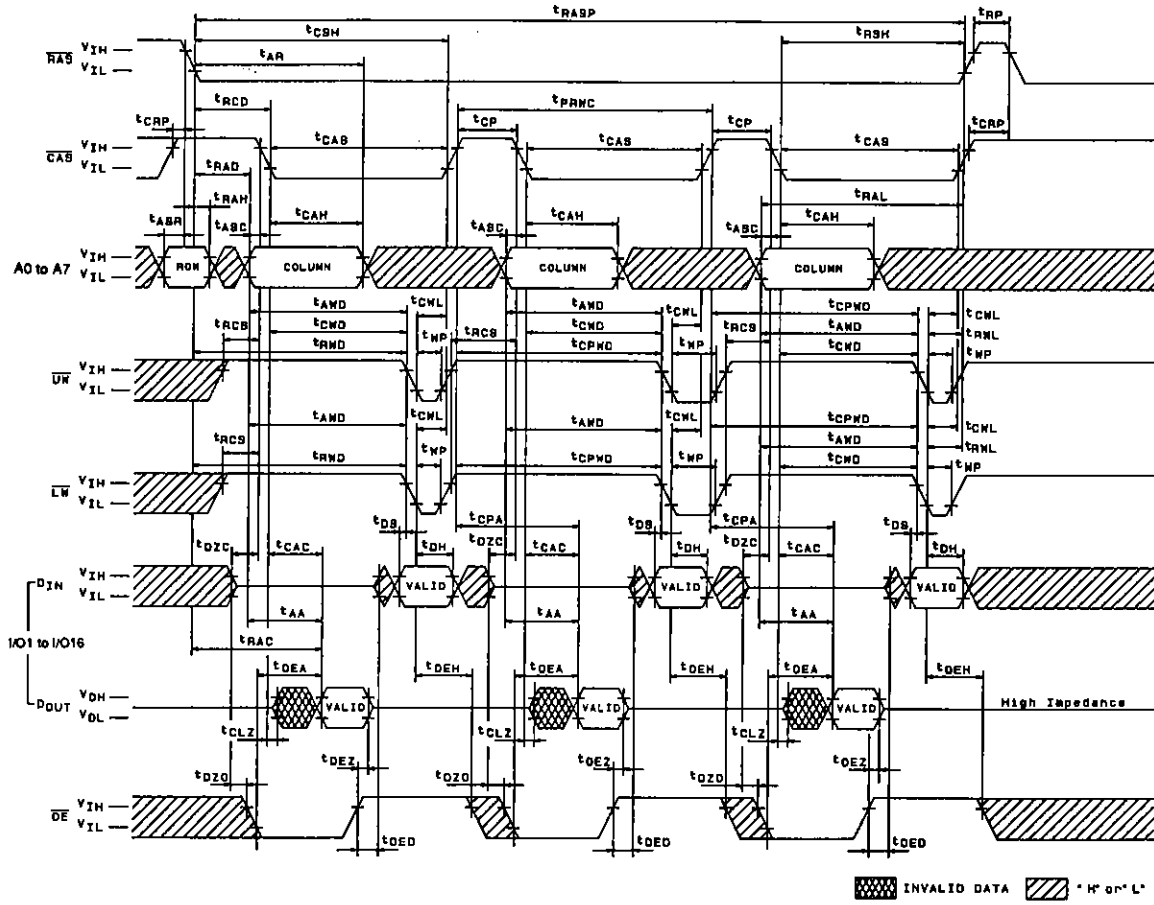
Fast Page Mode Lower Byte Early Write Cycle



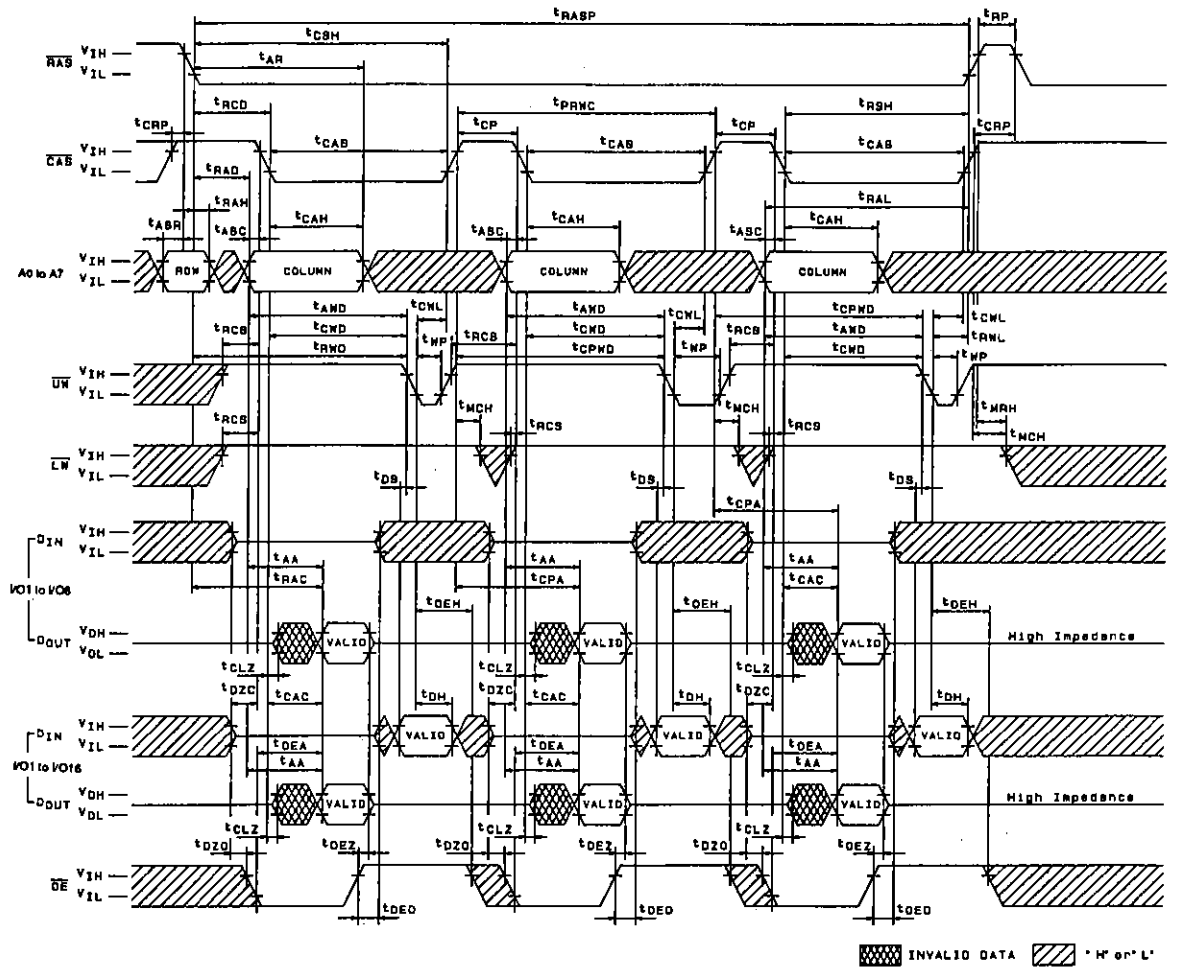
 H or L
 OE, H or L

A02162

Fast Page Mode Read-Modify-Write Cycle

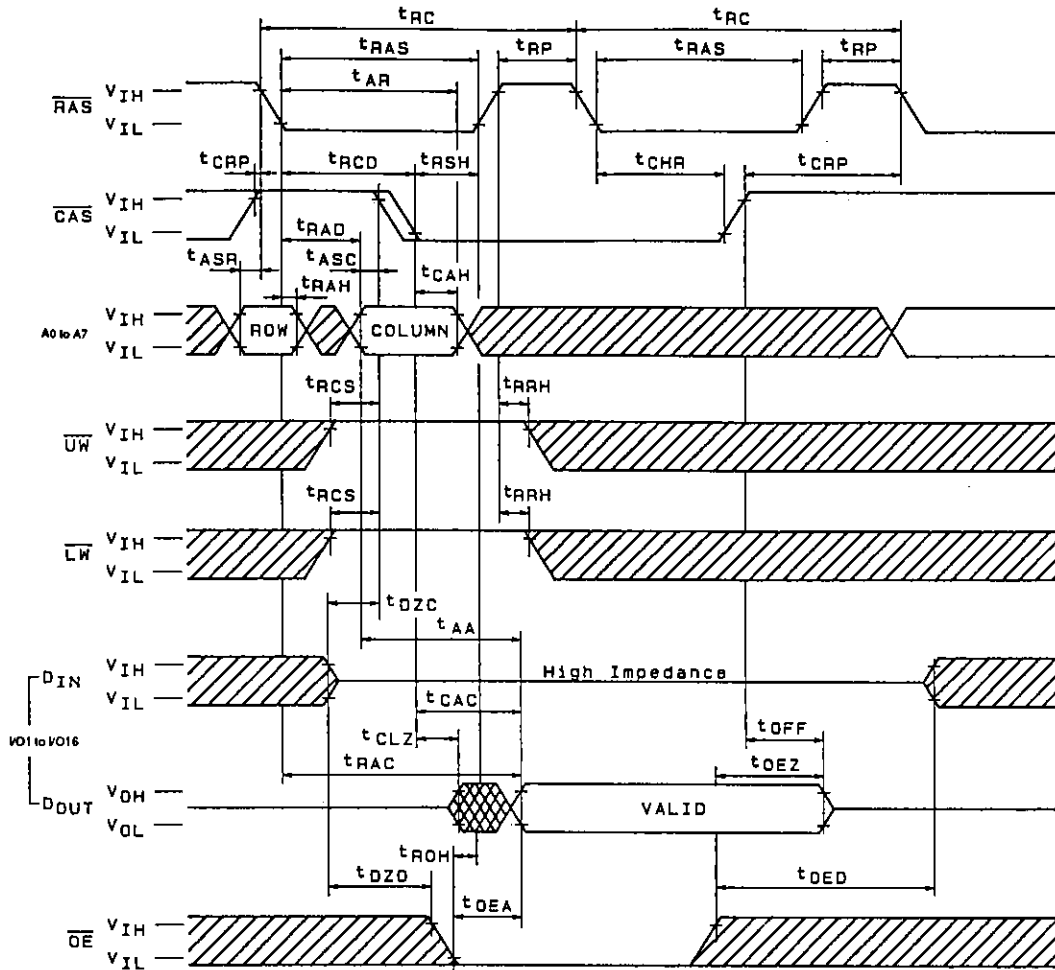


Fast Page Mode Read-Modify Upper Byte Write Cycle



A03278

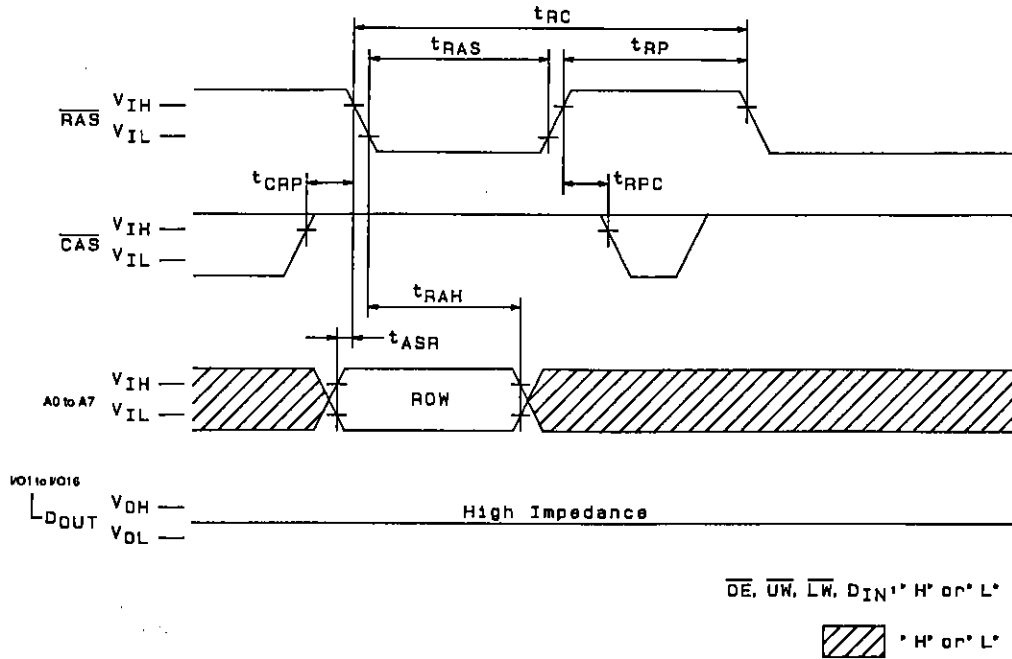
Hidden Refresh Cycle



INVALID DATA "H" or "L"

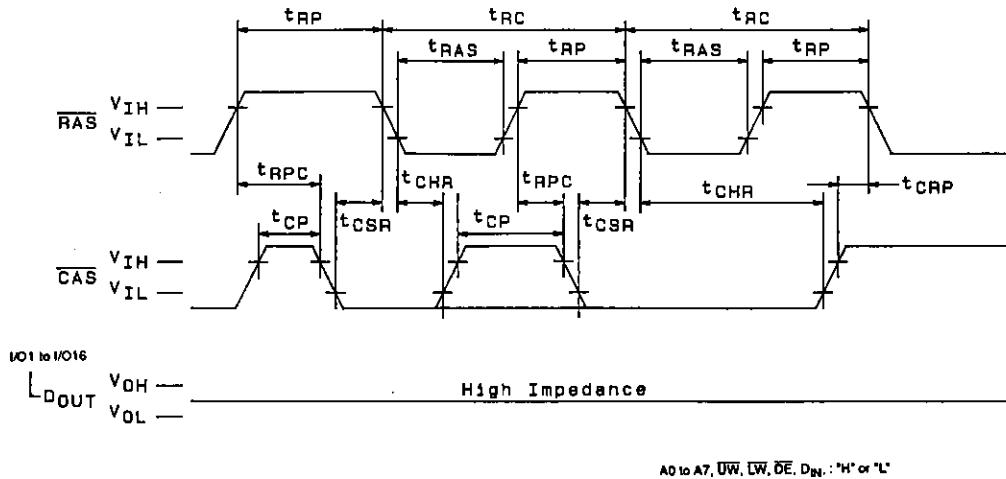
A03280

RAS-Only Refresh Cycle



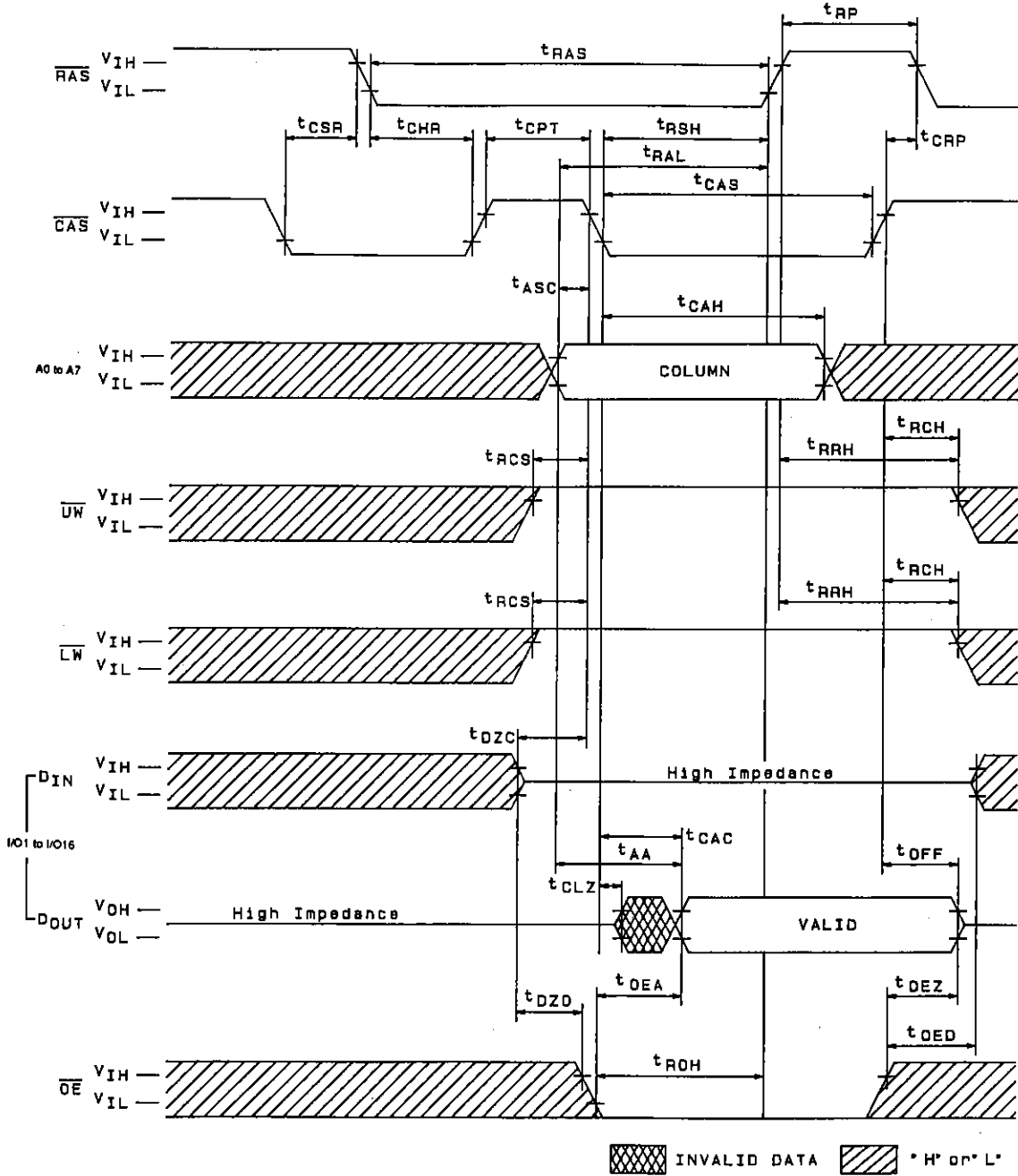
A02157

CAS-Before-RAS Refresh Cycle



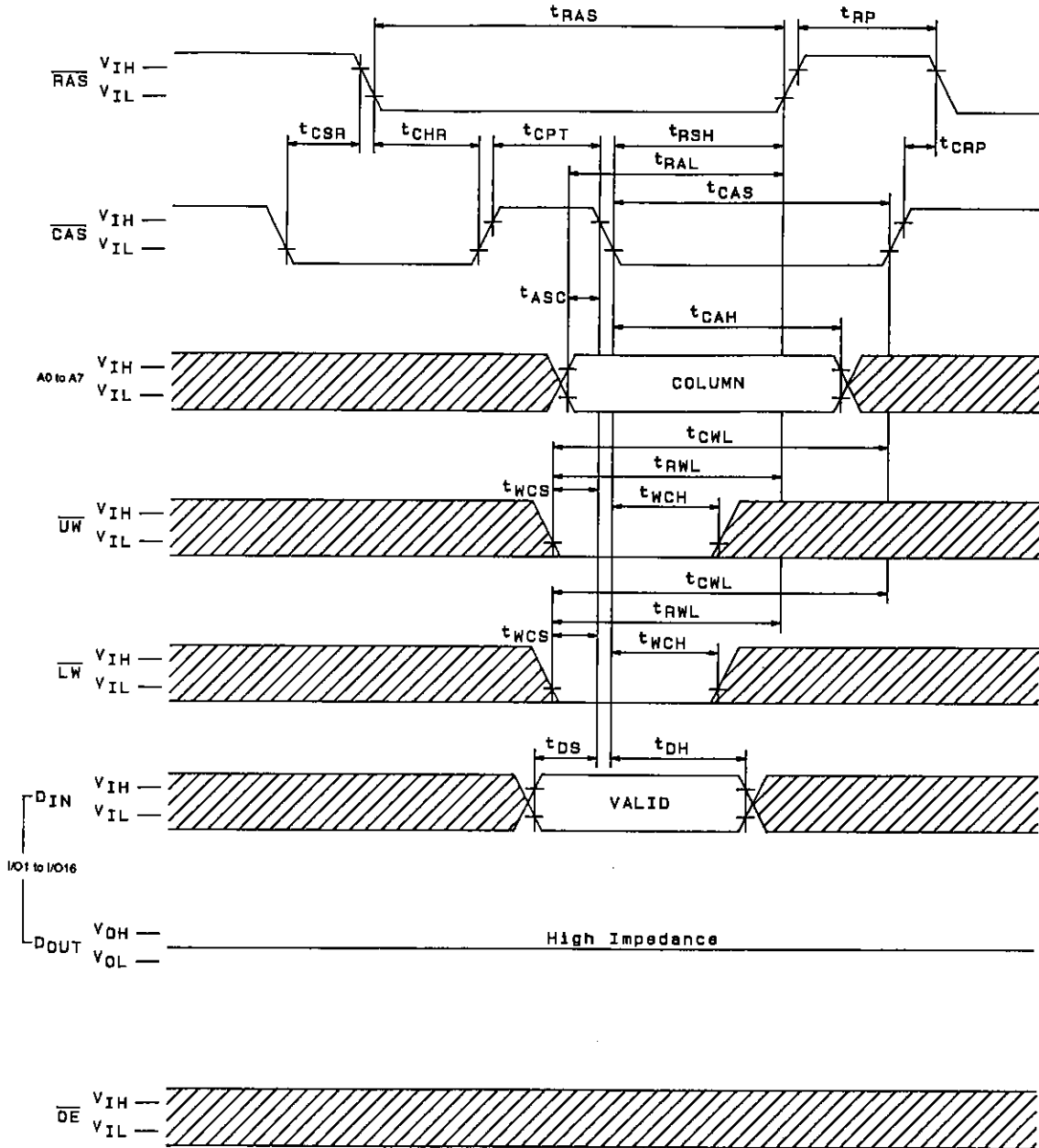
A02158

CAS-Before-RAS Refresh Counter Test Cycle (Read)



A02158

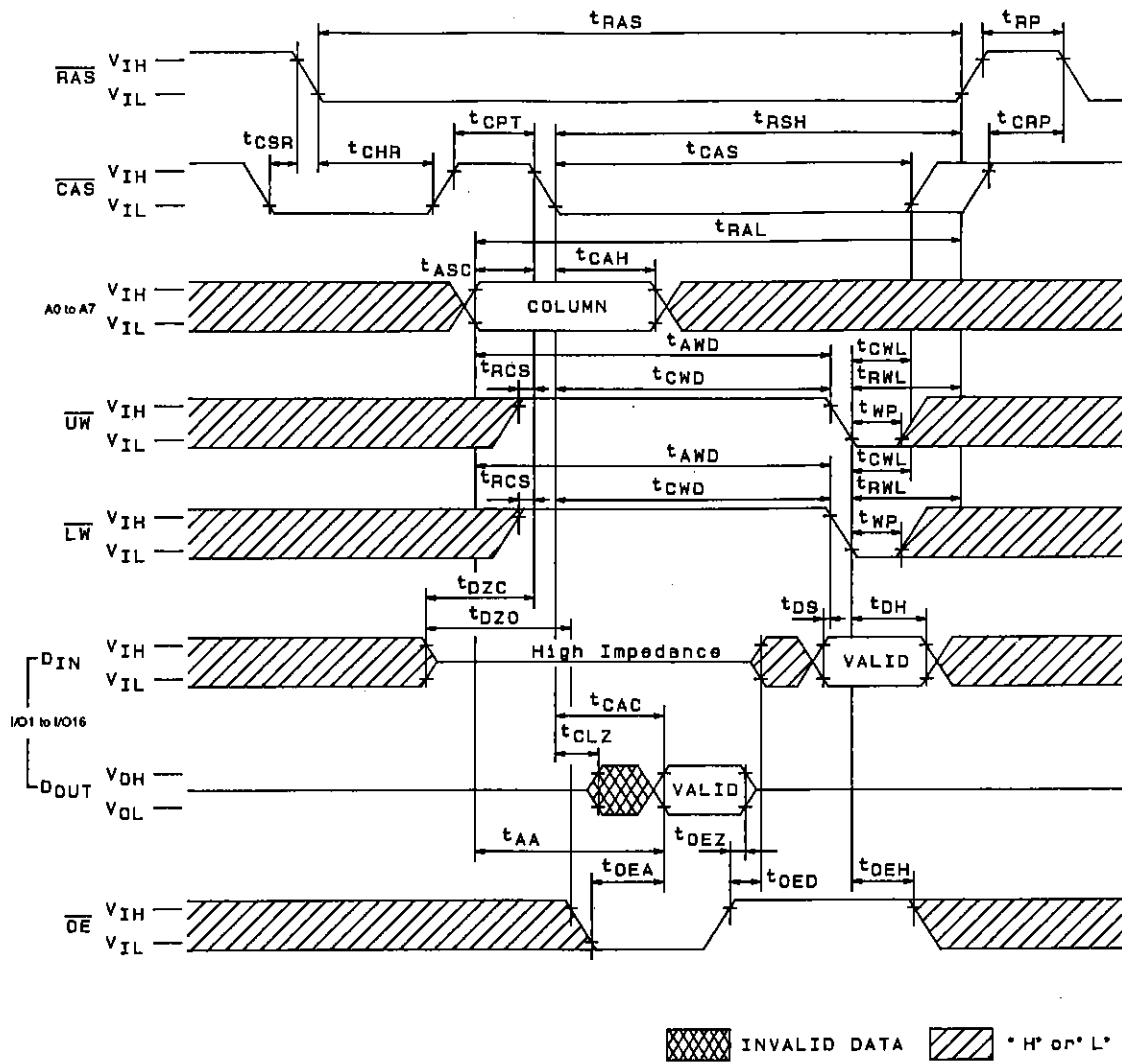
CAS-Before-RAS Refresh Counter Test Cycle (Write)



'H' or 'L'

A02180

CAS-Before-RAS Refresh Counter Test Cycle (Read-Modify-Write)



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