CY62147DV18
MoBL2™
4-Mb (256K x 16) Static RAM

Features

- **Very high speed: 55 ns and 70 ns**
- **Wide voltage range: 1.65V – 2.25V**
- **Pin-compatible with CY62147CV18**
- **Ultra-low active power**
  - **Typical active current: 1 mA @ f = 1 MHz**
  - **Typical active current: 6 mA @ f = f_{max}**
- **Ultra low standby power**
- **Easy memory expansion with $\overline{CE}$, and $\overline{OE}$ features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Packages offered 48-ball BGA**

Functional Description[1]

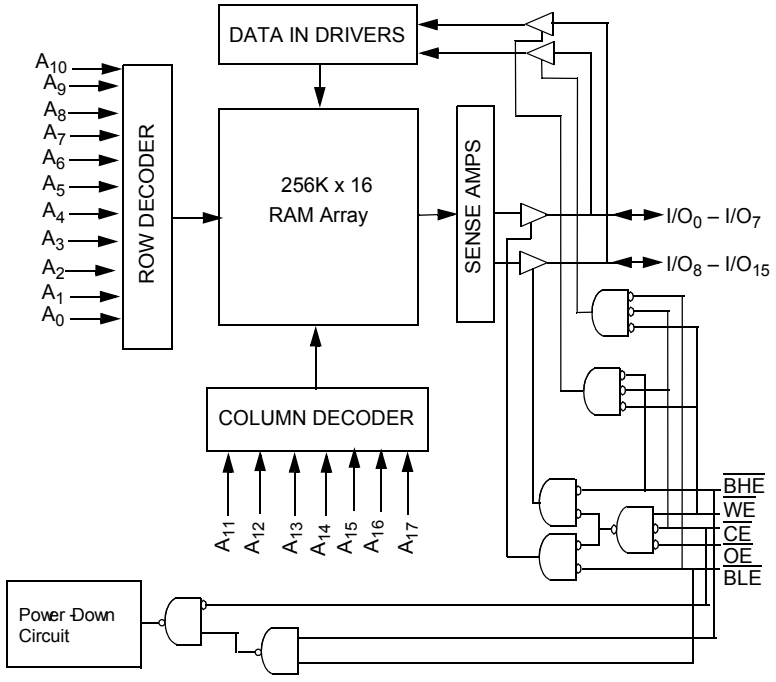
The CY62147DV18 is a high-performance CMOS static RAM organized as 256K words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL™) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption. The device can also be put into standby mode reducing power consumption by more than 99% when deselected ($\overline{CE}$ HIGH or both $\overline{BLE}$ and $\overline{BHE}$ are HIGH). The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when: deselected ($\overline{CE}$ HIGH), outputs are disabled ($\overline{OE}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

Writing to the device is accomplished by asserting Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{17}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{17}).

Reading from the device is accomplished by asserting Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory will appear on I/O_8 to I/O_{15}. See the truth table for a complete description of read and write modes.

The CY62147DV18 is available in a 48-ball FBGA package.

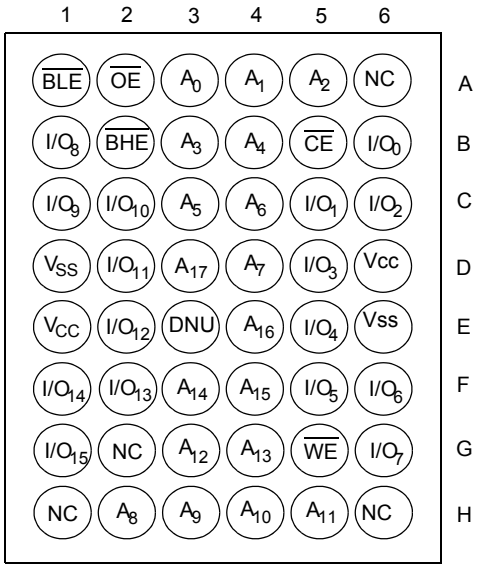
Logic Block Diagram



Note:
1. For best practice recommendations, please refer to the Cypress application note “System Design Guidelines” on http://www.cypress.com.

Pin Configuration[2, 3, 4]

FBGA (Top View)



Notes:
2. NC pins are not internally connected on the die.
3. DNU pins have to be left floating or tied to Vss to ensure proper application.
4. Pins H1, G2, and H6 in the BGA package are address expansion pins for 8 Mb, 16 Mb, and 32 Mb, respectively.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to + 150°C

Ambient Temperature with Power Applied.....–55°C to + 125°C

Supply Voltage to Ground Potential .....–0.2V to + $V_{CC(MAX)}$ + 0.2V

DC Voltage Applied to Outputs in High Z State[5,6].....–0.2V to $V_{CC(MAX)}$ + 0.2V

DC Input Voltage[5,6] .....–0.2V to $V_{CC\ (MAX)}$ + 0.2V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current..... > 200 mA

Operating Range

Device	Range	Ambient Temperature (T_A)	V_{CC}[7]
CY62147DV18L	Industrial	–40°C to +85°C	1.65V to 2.25V
CY62147DV18LL			

Product Portfolio

Product	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating I_{CC} (mA)				Standby I_{SB2} (μA)	
					f = 1MHz		f = f_{max}			
	Min.	Typ.[7]	Max.		Typ.[7]	Max.	Typ.[7]	Max.	Typ.[7]	Max.
CY62147DV18L	1.65	1.8	2.25	55	1.0	2.0	6	15	0.5	18
CY62147DV18LL								10		12
CY62147DV18L	1.65	1.8	2.25	70	1.0	2.0	6	15	0.5	18
CY62147DV18LL								10		12

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions			CY62147DV18-55			CY62147DV18-70			Unit
					Min.	Typ.[7]	Max.	Min.	Typ.[7]	Max.	
V_{OH}	Output HIGH Voltage	I_{OH} = –0.1 mA	V_{CC} = 1.65V		1.4			1.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA	V_{CC} = 1.65V				0.2			0.2	V
V_{IH}	Input HIGH Voltage	V_{CC} =1.65V to 2.25V			1.4		V_{CC}+0.2V	1.4		V_{CC} + 0.2V	V
V_{IL}	Input LOW Voltage	V_{CC} =1.65V to 2.25V			–0.2		0.4	–0.2		0.4	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}			–1		+1	–1		+1	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled			–1		+1	–1		+1	μA
I_{CC}	V_{CC} Operating Supply Current	f = f_{MAX} = 1/t_{RC}	$V_{CC(max)}$ = 1.95V I_{OUT} = 0 mA CMOS levels	L		6	12		6	12	mA
				LL			8			8	
			$V_{CC(max)}$ = 2.25V I_{OUT} = 0 mA CMOS levels	L		6	15		6	15	mA
				LL			10			10	
		f = 1 MHz	$V_{CC(max)}$ = 1.95V	L		1	1.5		1	1.5	mA
				LL							
			$V_{CC(max)}$ = 2.25V	L		1	2		1	2	mA
				LL							

Notes:

5. $V_{IL(min.)}$ = –2.0V for pulse durations less than 20 ns.
6. $V_{IH(max)}$=V_{CC}+0.75V for pulse durations less than 20ns.
7. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ.)}$, T_A = 25°C.

Electrical Characteristics Over the Operating Range (continued)

Parameter	Description	Test Conditions			CY62147DV18-55 Min.	CY62147DV18-55 Typ.[7]	CY62147DV18-55 Max.	CY62147DV18-70 Min.	CY62147DV18-70 Typ.[7]	CY62147DV18-70 Max.	Unit
I_{SB1}	Automatic CE Power-Down Current — CMOS Inputs	$\overline{CE} \geq V_{CC}-0.2V$, $V_{IN} \geq V_{CC}-0.2V$, $V_{IN} \leq 0.2V$); f = f_{MAX} (Address and Data Only), f = 0 ($\overline{OE}$, $\overline{WE}$, $\overline{BHE}$ and $\overline{BLE}$)	$V_{CC(max)}$=1.95V	L		0.5	12		0.5	12	µA
				LL			8			8	
			$V_{CC(max)}$=2.25V	L		0.5	18		0.5	18	
				LL			12			12	
I_{SB2}	Automatic CE Power-down Current — CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, f = 0	$V_{CC(max)}$=1.95V	L		0.5	12		0.5	12	µA
				LL			8			8	
			$V_{CC(max)}$=2.25V	L		0.5	18		0.5	18	
				LL			12			12	

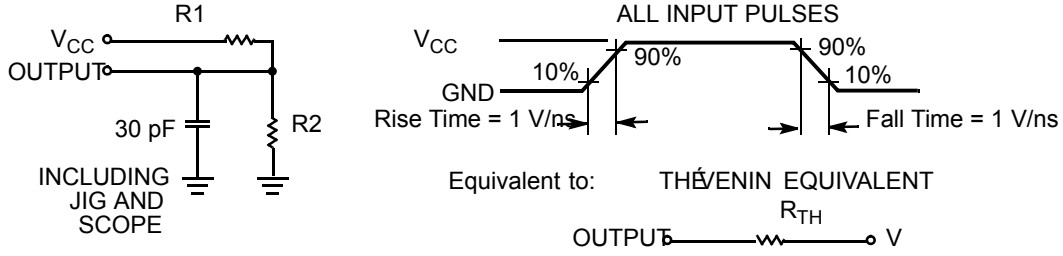
Capacitance for all Packages[8]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, $V_{CC} = V_{CC(typ)}$	10	pF
C_{OUT}	Output Capacitance		10	pF

Thermal Resistance

Parameter	Description	Test Conditions	BGA	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)[8]	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	75	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)[8]		10	°C/W

AC Test Loads and Waveforms



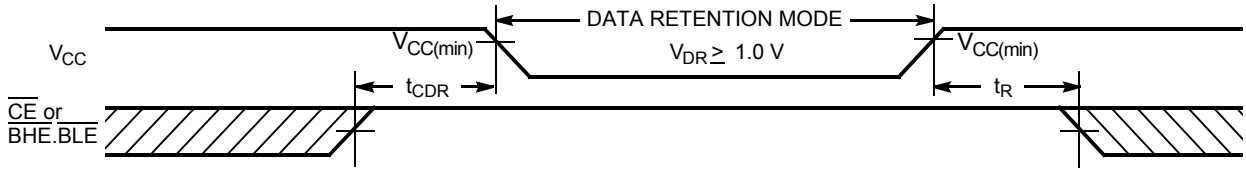
Parameters	1.80V	Unit
R1	13500	Ω
R2	10800	Ω
R_{TH}	6000	Ω
V_{TH}	0.80	V

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions		Min.	Typ.[7]	Max.	Unit
V_{DR}	V_{CC} for Data Retention			1.0			V
I_{CCDR}	Data Retention Current	V_{CC}= 1.0V $\overline{CE} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	L			6	µA
			LL			4	
t_{CDR}[8]	Chip Deselect to Data Retention Time			0			ns
t_R	Operation Recovery Time			t_{RC}			ns

Notes:
8. Tested initially and after any design or process changes that may affect these parameters.

Data Retention Waveform[9]



Switching Characteristics Over the Operating Range [10.]

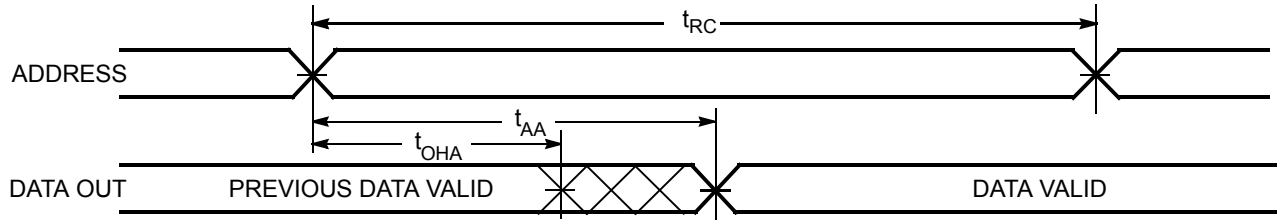
Parameter	Description	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t_{RC}	Read Cycle Time	55		70		ns
t_{AA}	Address to Data Valid		55		70	ns
t_{OHA}	Data Hold from Address Change	10		10		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		55		70	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		25		35	ns
t_{LZOE}	$\overline{OE}$ LOW to LOW Z[11]	5		5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[11, 12]		16		16	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[11]	10		10		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[11, 12]		20		25	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		55		70	ns
t_{DBE}	$\overline{BLE}$ / $\overline{BHE}$ LOW to Data Valid		55		70	ns
t_{LZBE}	$\overline{BLE}$ / $\overline{BHE}$ LOW to Low Z[11]	10		10		ns
t_{HZBE}	$\overline{BLE}$ / $\overline{BHE}$ HIGH to HIGH Z[11, 12]		20		25	ns
Write Cycle[13]						
t_{WC}	Write Cycle Time	55		70		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	40		50		ns
t_{AW}	Address Set-up to Write End	40		50		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	40		45		ns
t_{BW}	$\overline{BLE}$ / $\overline{BHE}$ LOW to Write End	40		50		ns
t_{SD}	Data Set-Up to Write End	25		30		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[11, 12]		20		25	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[11]	10		10		ns

Notes:

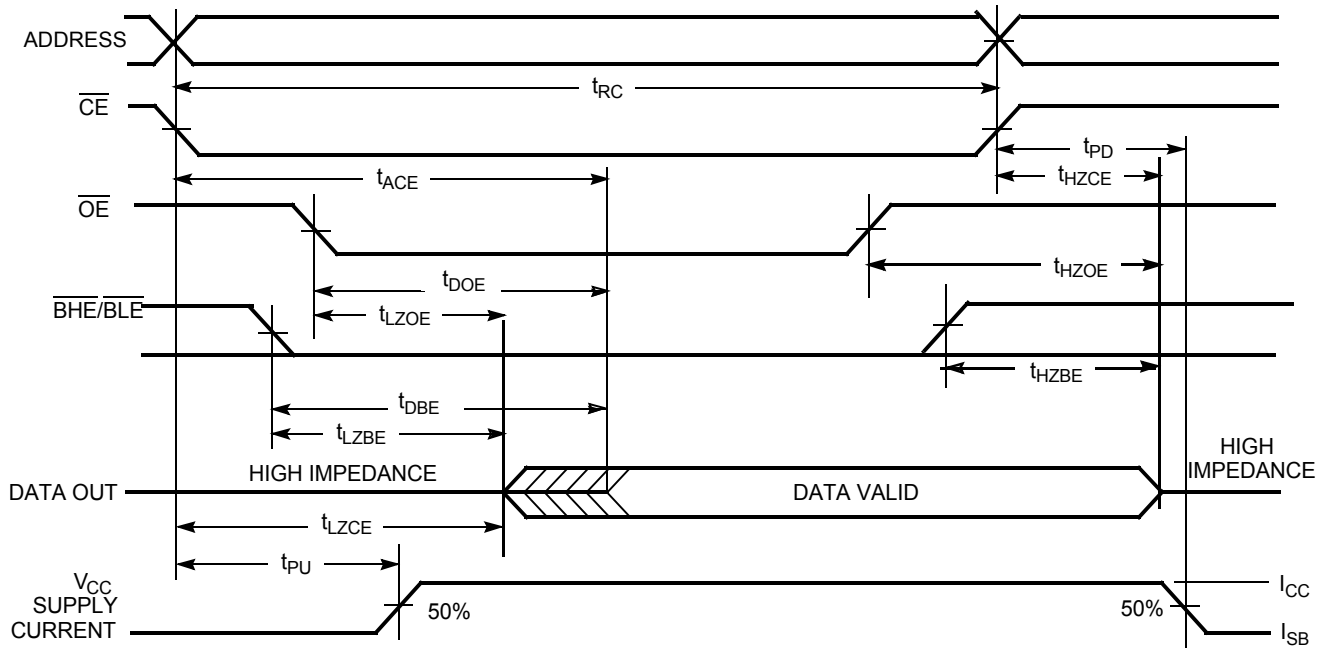
9. $\overline{BHE}.\overline{BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Chip can be deselected by either disabling the chip enable signal or by disabling both $\overline{BHE}$ and $\overline{BLE}$.
10. Test conditions for all parameters other than three-state parameters assume signal transition time of 1V/ns or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the "AC Test Loads and Waveforms" section.
11. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
12. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high impedence state.
13. The internal Write time of the memory is defined by the overlap of WE, CE = V_{IL}, BHE and/or BLE = V_{IL}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

Switching Waveforms

Read Cycle 1 (Address Transition Controlled)[14, 15]



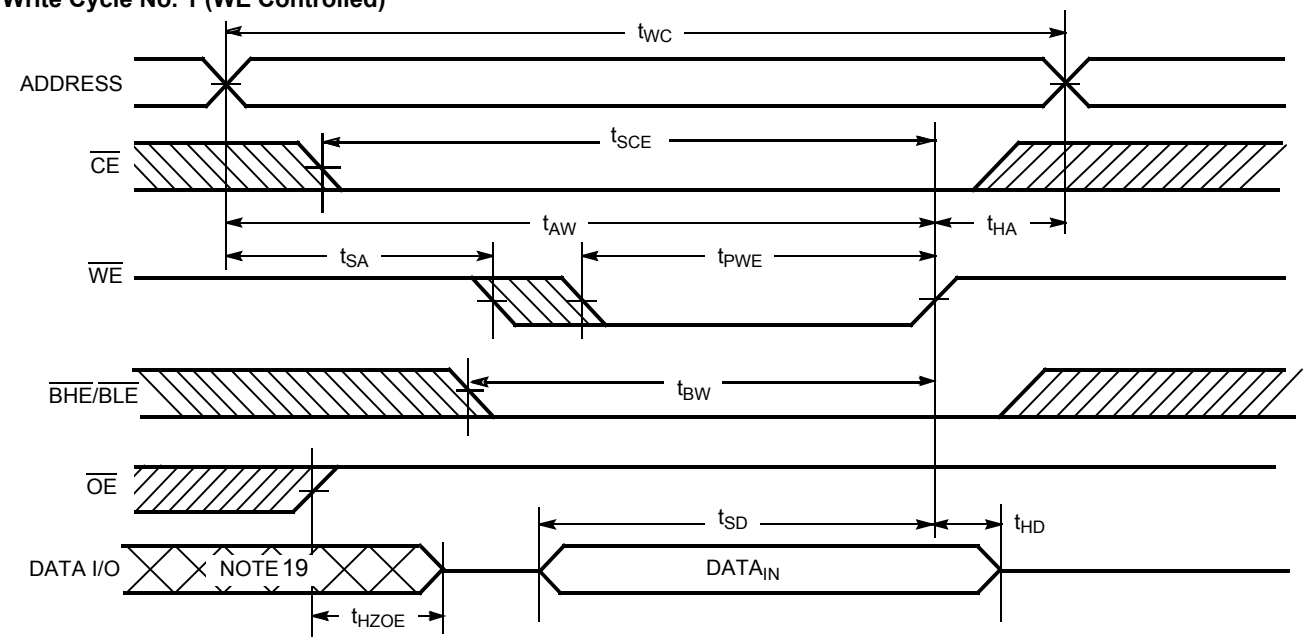
Read Cycle No. 2 (OE Controlled) [15, 16]



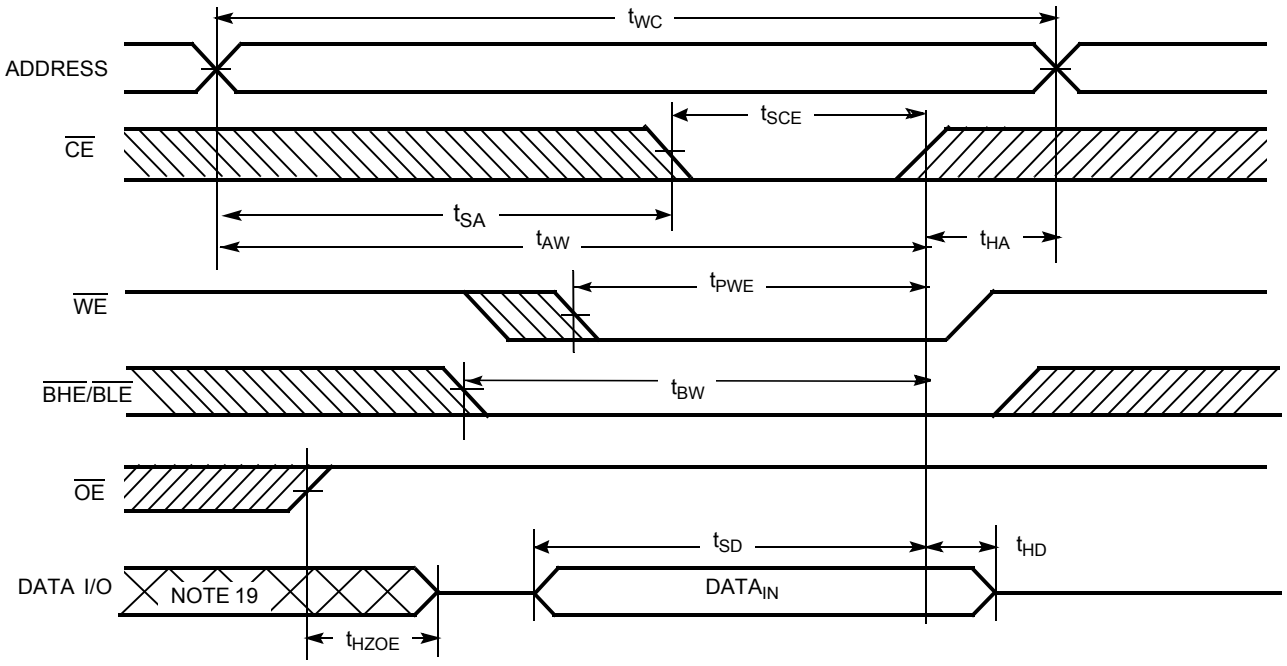
Notes:
14. The device is continuously selected. OE, CE = V_{IL}, BHE and/or BLE = V_{IL}.
15. WE is HIGH for read cycle.
16. Address valid prior to or coincident with CE and BHE, BLE transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 (WE Controlled)[13, 17, 18]



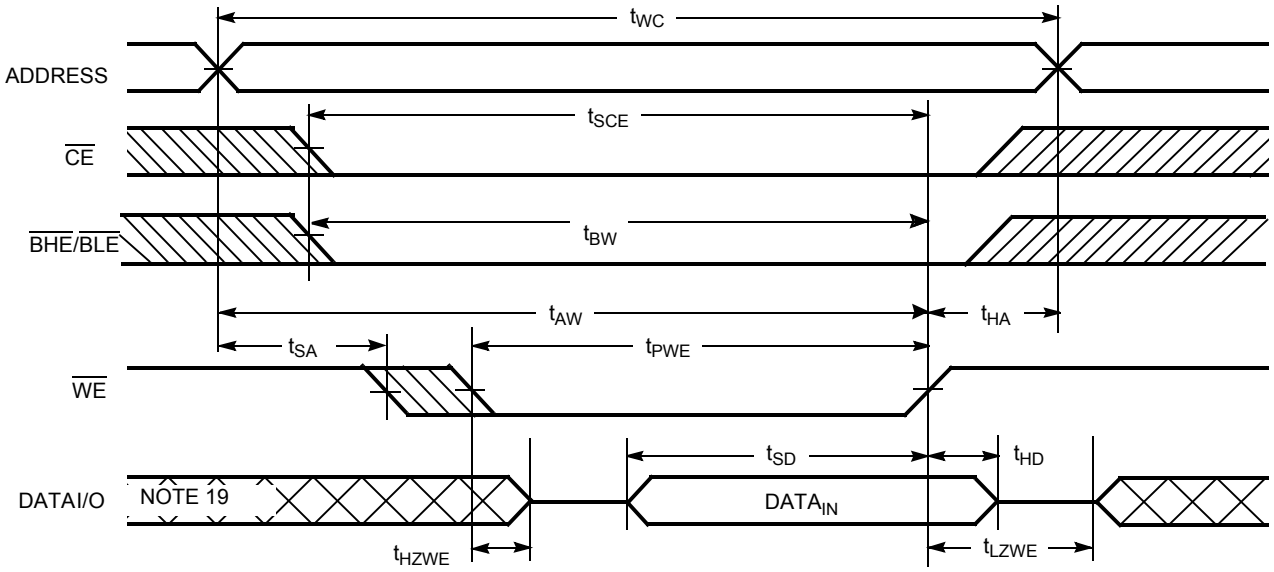
Write Cycle No. 2 (CE Controlled)[13, 17, 18]



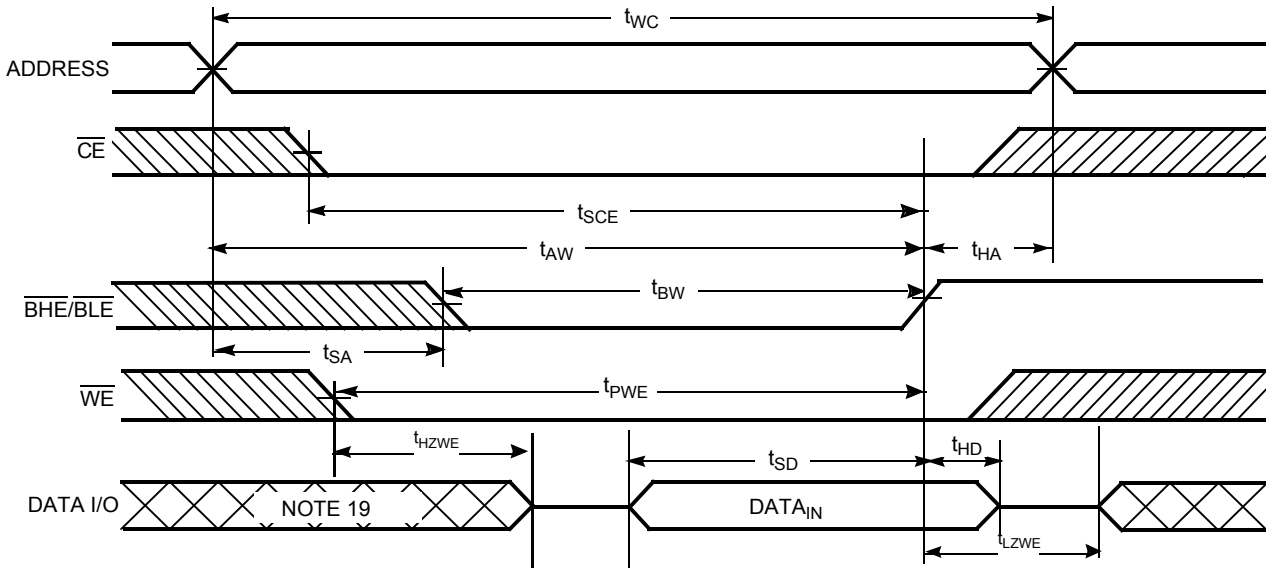
Notes:
17. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
18. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high-impedance state.
19. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle No. 3 (WE Controlled, OE LOW) [18]



Write Cycle No. 4 (BHE/BLE Controlled, OE LOW) [18]



Truth Table

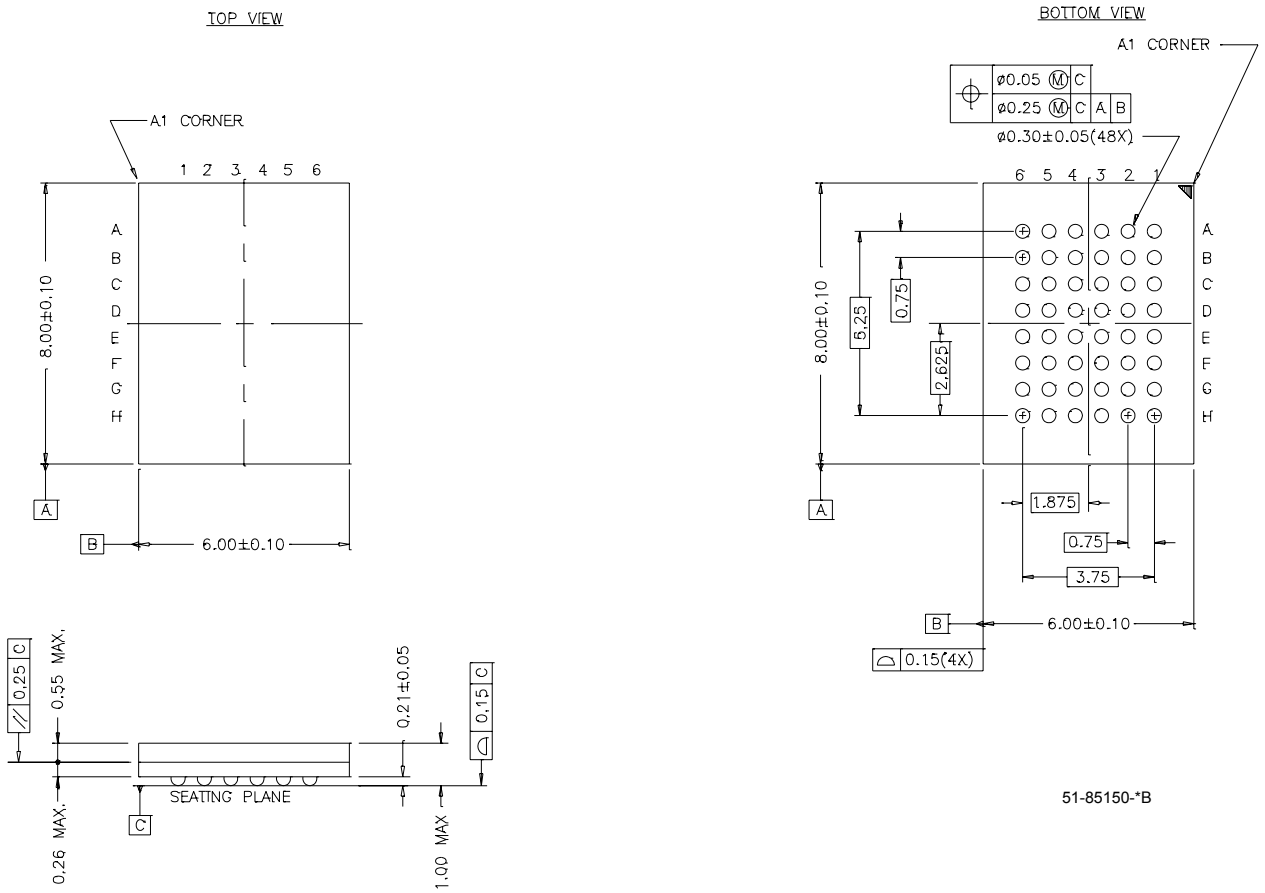
$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
X	X	X	H	H	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	L	L	L	Data Out (I/O_O–I/O_{15})	Read	Active (I_{CC})
L	H	L	H	L	Data Out (I/O_O–I/O_7); I/O_8–I/O_{15} in High Z	Read (Lower byte only)	Active (I_{CC})
L	H	L	L	H	Data Out (I/O_8–I/O_{15}); I/O_0–I/O_7 in High Z	Read (Higher byte only)	Active (I_{CC})
L	H	H	L	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	L	H	High Z	Output Disabled	Active (I_{CC})
L	L	X	L	L	Data In (I/O_O–I/O_{15})	Write	Active (I_{CC})
L	L	X	H	L	Data In (I/O_O–I/O_7); I/O_8–I/O_{15} in High Z	Write (Lower byte only)	Active (I_{CC})
L	L	X	L	H	Data In (I/O_8–I/O_{15}); I/O_0–I/O_7 in High Z	Write (Higher byte only)	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	CY62147DV18L-55BVI	BV48A	48-ball Fine Pitch BGA (6 mm × 8mm × 1 mm)	Industrial
	CY62147DV18LL-55BVI			
70	CY62147DV18L-70BVI	BV48A	48-ball Fine Pitch BGA (6 mm × 8mm × 1 mm)	Industrial
	CY62147DV18LL-70BVI			
55	CY62147DV18L-55BVXI	BV48A	48-ball Fine Pitch BGA (6 mm × 8mm × 1 mm) Pb-free	Industrial
	CY62147DV18LL-55BVXI			
70	CY62147DV18L-70BVXI	BV48A	48-ball Fine Pitch BGA (6 mm × 8mm × 1 mm) Pb-free	Industrial
	CY62147DV18LL-70BVXI			

Package Diagram

48-Lead VFBGA (6 x 8 x 1 mm) BV48A



Document History Page

Document Title:CY62147DV18 MoBL2™ 4-Mb (256K x 16) Static RAM Document Number: 38-05343				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	127482	06/17/03	HRT	New Data Sheet
*A	131009	11/26/03	CBD	Changed From Advance to Preliminary
*B	229908	See ECN	AJU	Changed From Preliminary to Final Added 70 ns speed bin Changed Vcc MAX spec from 2.20V to 2.25V Modified V_{IH} spec on footnote #6 from $V_{CC\ (MAX)}$ + 0.5V to $V_{CC\ (MAX)}$ + 0.75V Changed I_{CC} TYP values from 8 mA to 6 mA Changed I_{CC} MAX values at Vcc (max) = 1.95V from 15 mA to 12 mA (L bin) and 10 mA to 8mA (LL bin) Changed I_{CC} MAX values at Vcc (max) = 2.25V from 18 mA to 15 mA (L bin) and 12mA to 10 mA (LL bin) With modified $V_{cc\ MAX}$ spec, changed I_{SB1} and I_{SB2} MAX values from 15 uA to 18 uA (L bin) and 10 uA to 12 uA (LL bin) Modified input and output capacitance values Removed footnote #9 from earlier rev Removed MAX value for V_{DR} Modified t_{HZOE} from 20 ns to 16 ns Added Pb-free ordering information