

December 1992

Features

- High Voltage Type (20V Rating)
- Set - Reset Capability
- Static Flip-Flop Operation - Retains State Indefinitely with Clock Level Either "High" or "Low"
- Medium Speed Operation - 16MHz (typ.) Clock Toggle Rate at 10V
- Standardized Symmetrical Output Characteristics
- 100% Tested For Quiescent Current at 20V
- Maximum Input Current of 1 μ A at 18V Over Full Package-Temperature Range;
 - 100nA at 18V and +25 $^{\circ}$ C
- Noise Margin (Over Full Package Temperature Range):
 - 1V at VDD = 5V
 - 2V at VDD = 10V
 - 2.5V at VDD = 15V
- 5V, 10V and 15V Parametric Ratings
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Registers, Counters, Control Circuits

Description

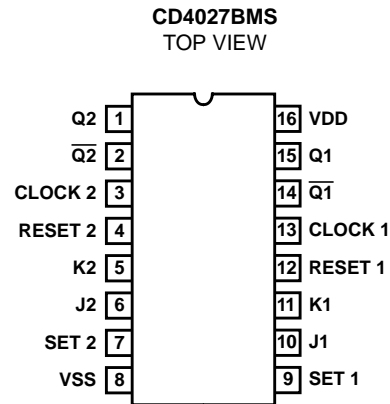
CD4027BMS is a single monolithic chip integrated circuit containing two identical complementary-symmetry J-K master-slave flip-flops. Each flip-flop has provisions for individual J, K, Set Reset, and Clock input signals. Buffered Q and \bar{Q} signals are provided as outputs. This input-output arrangement provides for compatible operation with the Intersil CD4013B dual D type flip-flop.

The CD4027BMS is useful in performing control, register, and toggle functions. Logic levels present at the J and K inputs along with internal self-steering control the state of each flip-flop; changes in the flip-flop state are synchronous with the positive-going transition of the clock pulse. Set and reset functions are independent of the clock and are initiated when a high level signal is present at either the Set or Reset input.

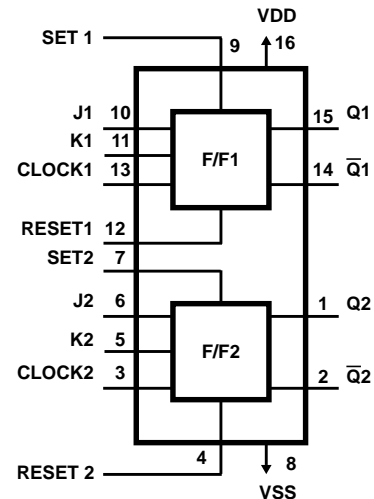
The CD4027BMS is supplied in these 16-lead outline packages:

Braze Seal DIP H4T
 Frit Seal DIP H1E
 Ceramic Flatpack H6W

Pinout



Functional Diagram



Specifications CD4027BMS

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) -0.5V to +20V
 (Voltage Referenced to VSS Terminals)
 Input Voltage Range, All Inputs -0.5V to VDD +0.5V
 DC Input Current, Any One Input ±10mA
 Operating Temperature Range -55°C to +125°C
 Package Types D, F, K, H
 Storage Temperature Range (TSTG) -65°C to +150°C
 Lead Temperature (During Soldering) +265°C
 At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for
 10s Maximum

Reliability Information

Thermal Resistance θ_{ja} θ_{jc}
 Ceramic DIP and FRIT Package 80°C/W 20°C/W
 Flatpack Package 70°C/W 20°C/W
 Maximum Package Power Dissipation (PD) at +125°C
 For TA = -55°C to +100°C (Package Type D, F, K) 500mW
 For TA = +100°C to +125°C (Package Type D, F, K) Derate
 Linearity at 12mW/°C to 200mW
 Device Dissipation per Output Transistor 100mW
 For TA = Full Package Temperature Range (All Package Types)
 Junction Temperature +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
						MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	2	µA
				2	+125°C	-	200	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	2	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
			VDD = 18V	2	+125°C	-1000	-	nA
				3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
			VDD = 18V	2	+125°C	-	1000	nA
				3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented. 2. Go/No Go test with limits applied to inputs. 3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

Specifications CD4027BMS

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay Clock To Q, \bar{Q}	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	300	ns
			10, 11	+125°C, -55°C	-	405	ns
Propagation Delay Set To Q Reset To \bar{Q}	TPLH2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	300	ns
			10, 11	+125°C, -55°C	-	405	ns
Propagation Delay Set To \bar{Q} , Reset To Q	TPHL3	VDD = 5V, VIN = VDD or GND	9	+25°C	-	400	ns
			10, 11	+125°C, -55°C	-	540	ns
Transition Time	TTLH TTHL	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Maximum Clock Input Frequency	FCL	VDD = 5V, VIN = VDD or GND	9	+25°C	3.5	-	MHz
			10, 11	+125°C, -55°C	3.5/1.35	-	MHz

NOTES:

1. VDD = 5V, CL = 50pF, RL = 200K
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	1	μA
				+125°C	-	30	μA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	μA
				+125°C	-	60	μA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	μA
				+125°C	-	120	μA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA

Specifications CD4027BMS

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Output Current (Source)	IOH15	VDD = 15V, VO _{UT} = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VO _H > 9V, VO _L < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VO _H > 9V, VO _L < 1V	1, 2	+25°C, +125°C, -55°C	7	-	V
Propagation Delay Clock To Q, \bar{Q}	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	130	ns
		VDD = 15V	1, 2, 3	+25°C	-	90	ns
Propagation Delay Set To Q, Reset To \bar{Q}	TPLH2	VDD = 10V	1, 2, 3	+25°C	-	130	ns
		VDD = 15V	1, 2, 3	+25°C	-	90	ns
Propagation Delay Set To \bar{Q} , Reset To Q	TPHL3	VDD = 10V	1, 2, 3	+25°C	-	170	ns
		VDD = 15V	1, 2, 3	+25°C	-	120	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Maximum Clock Input Frequency Toggle Mode Input TR, TF = 5ns	FCL	VDD = 10V	1, 2, 3	+25°C	8	-	MHz
		VDD = 15V	1, 2, 3	+25°C	12	-	MHz
Minimum Data Setup Time	TS	VDD = 5V	1, 2, 3	+25°C	-	200	ns
		VDD = 10V	1, 2, 3	+25°C	-	75	ns
		VDD = 15V	1, 2, 3	+25°C	-	50	ns
Minimum Set or Reset Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	180	ns
		VDD = 10V	1, 2, 3	+25°C	-	80	ns
		VDD = 15V	1, 2, 3	+25°C	-	50	ns
Minimum Clock Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	140	ns
		VDD = 10V	1, 2, 3	+25°C	-	60	ns
		VDD = 15V	1, 2, 3	+25°C	-	40	ns
Clock Input Rise Or Fall Time (Note 5)	TRCL TFCL	VDD = 5V	1, 2, 3, 4	+25°C	-	45	μs
		VDD = 10V	1, 2, 3, 4	+25°C	-	5	μs
		VDD = 15V	1, 2, 3, 4	+25°C	-	2	μs
Input Capacitance	CIN		1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
4. If more than one unit is cascaded in a parallel clocked operation, trCL should be made less than or equal to the sum of the fixed propagation delay time at 15pF and the transition time of the output driving stage for the estimated capacitive load.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	7.5	μA

Specifications CD4027BMS

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10 μ A	1, 4	+25 $^{\circ}$ C	-2.8	-0.2	V
N Threshold Voltage Delta	Δ V _{NTN}	VDD = 10V, ISS = -10 μ A	1, 4	+25 $^{\circ}$ C	-	\pm 1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10 μ A	1, 4	+25 $^{\circ}$ C	0.2	2.8	V
P Threshold Voltage Delta	Δ V _{TP}	VSS = 0V, IDD = 10 μ A	1, 4	+25 $^{\circ}$ C	-	\pm 1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25 $^{\circ}$ C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25 $^{\circ}$ C	-	1.35 x +25 $^{\circ}$ C Limit	ns

NOTES: 1. All voltages referenced to device GND. 2. CL = 50pF, RL = 200K, Input TR, TF < 20ns. 3. See Table 2 for +25 $^{\circ}$ C limit. 4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25 $^{\circ}$ C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-1	IDD	\pm 0.2 μ A
Output Current (Sink)	IOL5	\pm 20% x Pre-Test Reading
Output Current (Source)	IOH5A	\pm 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)	100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)	100% 5004	1, 7, 9, Deltas	
Final Test	100% 5004	2, 3, 8A, 8B, 10, 11	
Group A	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	1, 7, 9	
Group D	Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2, 3

NOTE: 1. 5% Parametric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

CD4027BMS

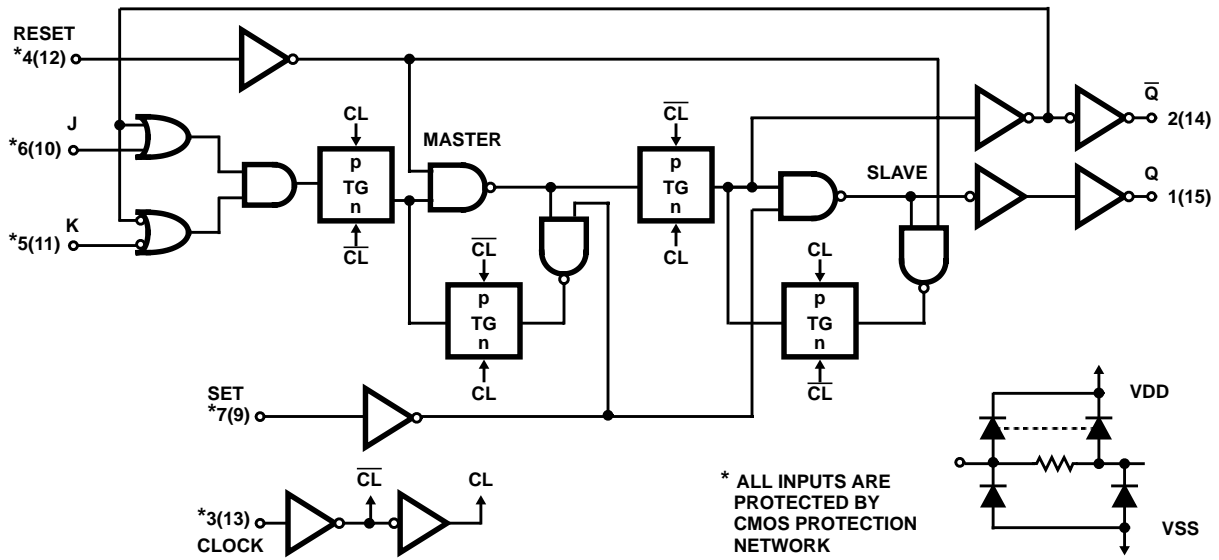
TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± 0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	1, 2, 14, 15	3 - 13	16			
Static Burn-In 2 Note 1	1, 2, 14, 15	8	3 - 7, 9 - 13, 16			
Dynamic Burn-In Note 2	-	4, 7 - 9, 12	5, 6, 10, 11, 16	12, 14, 15	3, 13	
Irradiation Note 3	1, 2, 14, 15	8	3 - 7, 9 - 13, 16			

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 4.75K ± 5%, VDD = 18V ± 0.5V
3. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagram



LOGIC DIAGRAM AND TRUTH TABLE FOR CD4027BMS (ONE OF TWO IDENTICAL J-K FLIP-FLOPS)

TRUTH TABLE

PRESENT STATE					CL*	NEXT STATE	
INPUTS				OUTPUT		OUTPUTS	
J	K	S	R	Q		Q	Q̄
1	X	0	0	0		1	0
X	0	0	0	1		1	0
0	X	0	0	0		0	1
X	1	0	0	1		0	1
X	X	0	0	X			No Change
X	X	1	0	X	X	1	0
X	X	0	1	X	X	0	1
X	X	1	1	X	X	1	1

Logic 1 = High Level
Logic 0 = Low Level

* = Level change
X = Don't care

Typical Performance Characteristics

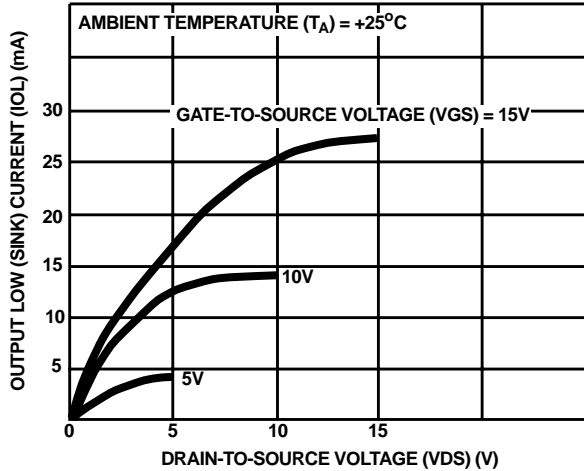


FIGURE 1. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

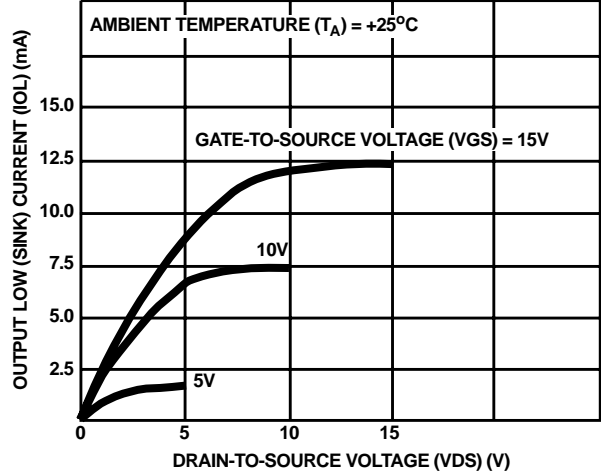


FIGURE 2. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

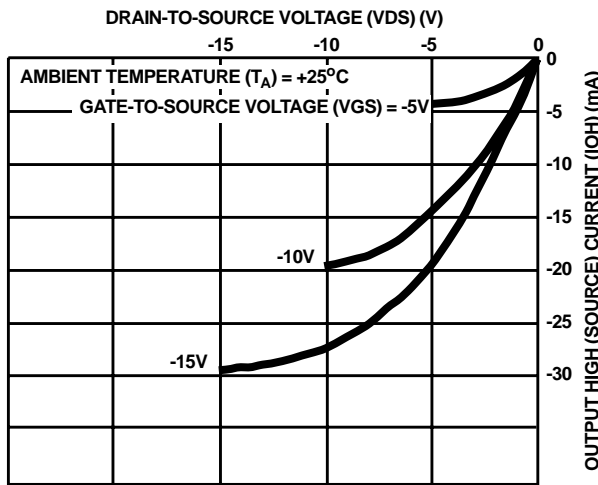


FIGURE 3. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

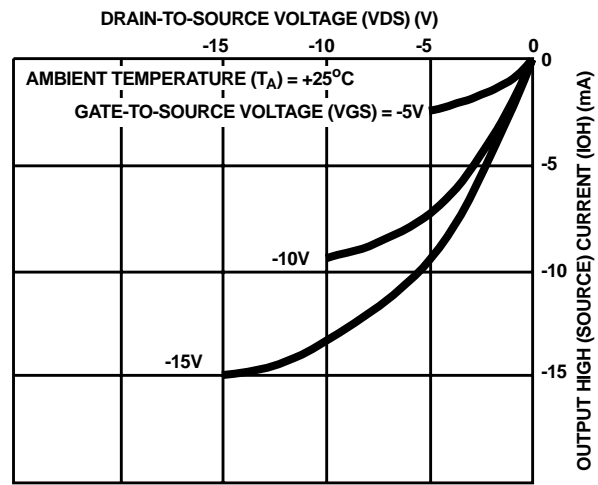


FIGURE 4. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

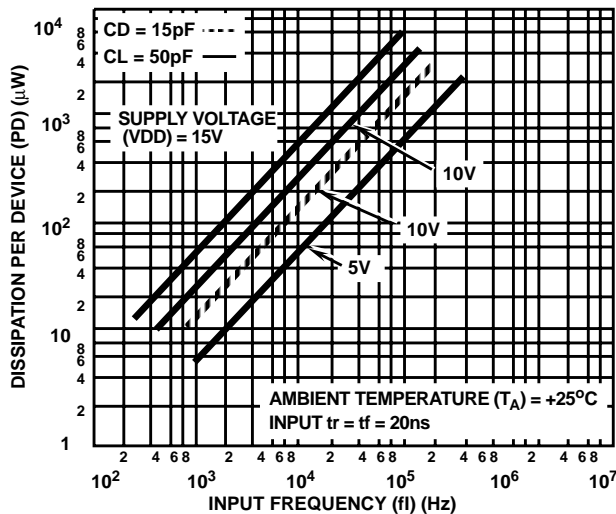


FIGURE 5. TYPICAL POWER DISSIPATION vs FREQUENCY

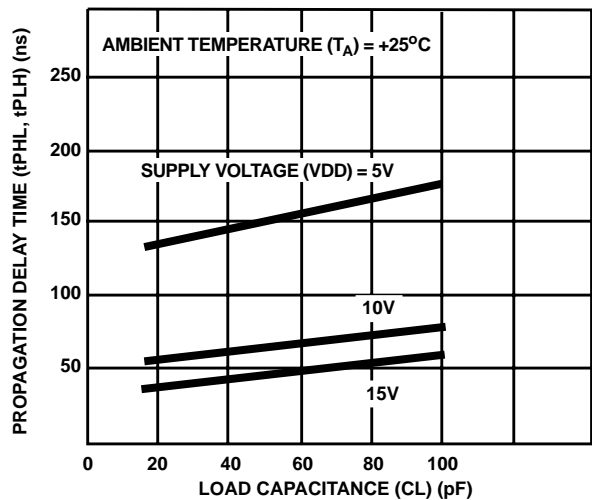


FIGURE 6. TYPICAL PROPAGATION DELAY TIME vs LOAD CAPACITANCE (CLOCK OR SET TO Q, CLOCK OR RESET TO \bar{Q})

Typical Performance Characteristics (Continued)

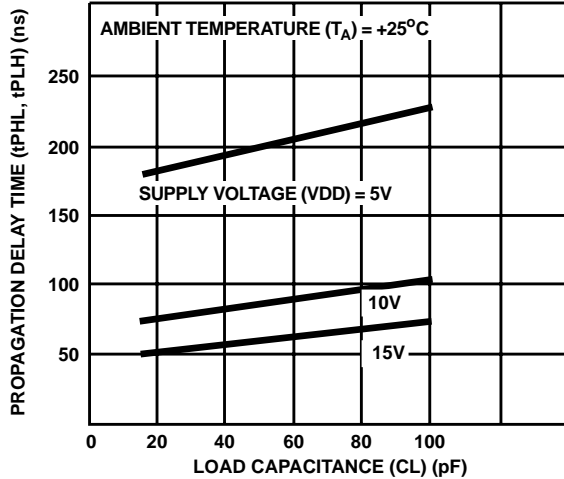


FIGURE 7. TYPICAL PROPAGATION DELAY TIME vs LOAD CAPACITANCE (SET TO Q, OR RESET TO Q)

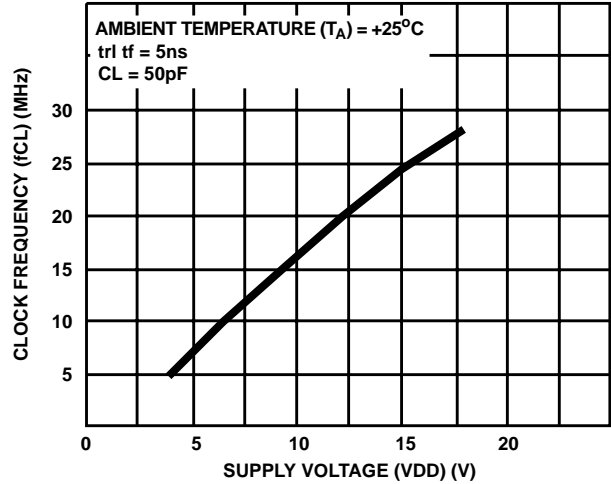
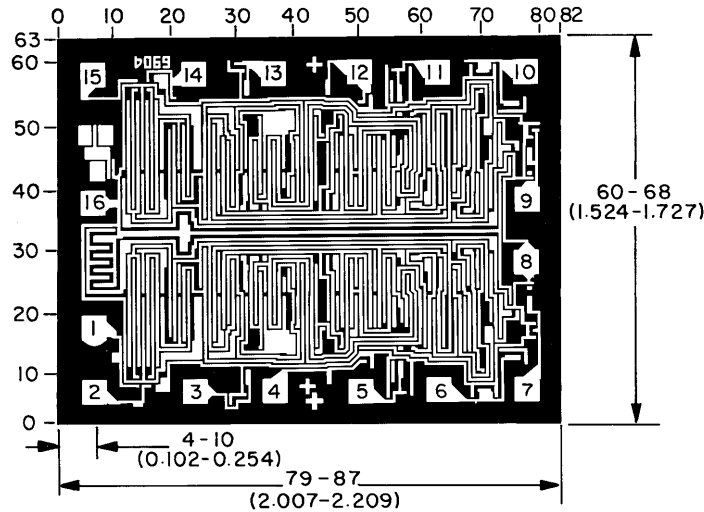


FIGURE 8. TYPICAL MAXIMUM CLOCK FREQUENCY vs SUPPLY VOLTAGE (TOGGLE MODE)

Chip Dimensions and Pad Layout



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch)

METALLIZATION: Thickness: $11\text{k}\text{\AA} - 14\text{k}\text{\AA}$, AL.

PASSIVATION: $10.4\text{k}\text{\AA} - 15.6\text{k}\text{\AA}$, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see web site <http://www.intersil.com>