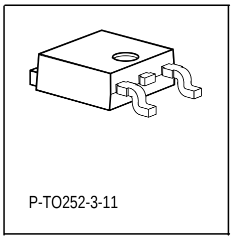
Smart Lowside Power Switch

Features

- Logic Level Input
- Input Protection (ESD)
- Thermal shutdown with auto restart
- Overload protection
- Short circuit protection
- Overvoltage protection
- Current limitation
- Analog driving possible

Product Summary

Drain source voltage	V_{DS}	42	V
On-state resistance	$R_{DS(on)}$	28	mΩ
Nominal load current	$I_{D(Nom)}$	4.6	A
Clamping energy	E_{AS}	3.5	J

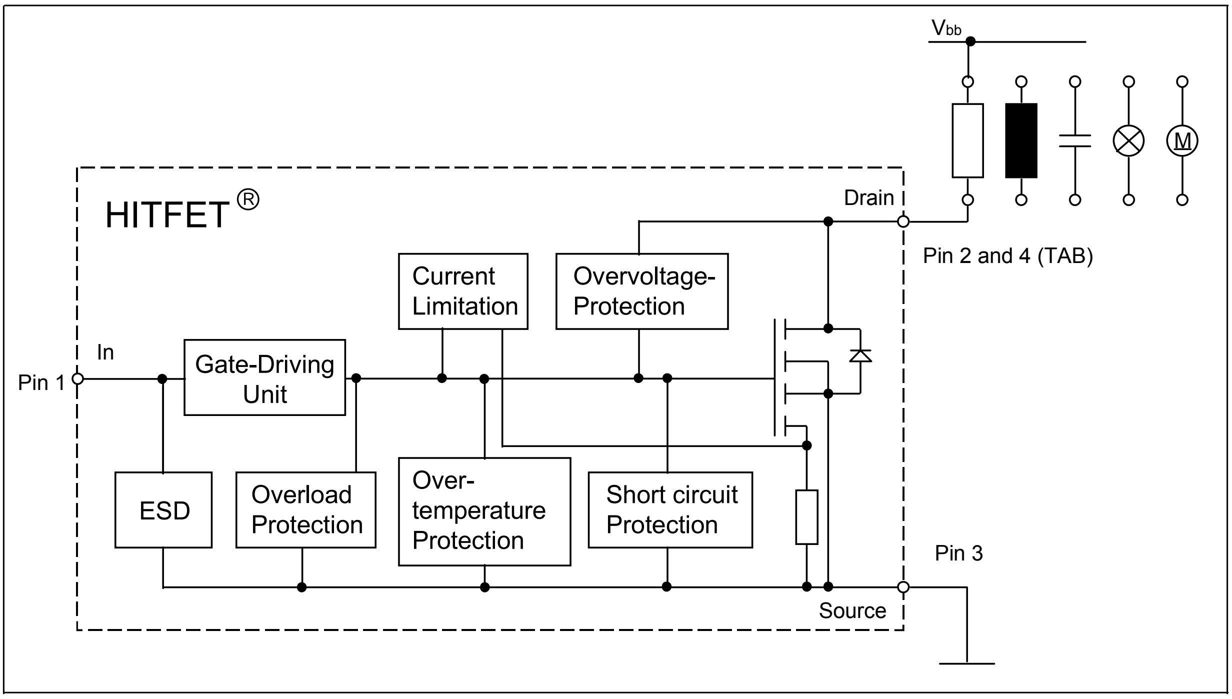


Application

- All kinds of resistive, inductive and capacitive loads in switching or linear applications
- µC compatible power switch for 12 V DC applications
- Replaces electromechanical relays and discrete circuits

General Description

N channel vertical power FET in Smart SIPMOS® technology. Fully protected by embedded protection functions.



Complete product spectrum and additional information http://www.infineon.com/hitfet

Maximum Ratings at T_j = 25°C, unless otherwise specified

Parameter	Symbol	Value	Unit
Drain source voltage	V_{DS}	42	V
Supply voltage for full short circuit protection	$V_{bb(SC)}$	42	
Continuous input voltage[1]	V_{IN}	-0.2 [2] ... +10	
Continuous input current[2] $-0.2V \le V_{IN} \le 10V$ $V_{IN} < -0.2V$ or $V_{IN} > 10V$	I_{IN}	 self limited $\vert I_{IN} \vert \le 2$	mA
Operating temperature	T_j	-40 ...+150	°C
Storage temperature	T_{stg}	-55 ... +150	
Power dissipation [5] T_C = 85 °C 6cm² cooling area , T_A = 85 °C	P_{tot}	 59 1.1	W
Unclamped single pulse inductive energy [2]	E_{AS}	3.5	J
Load dump protection $V_{LoadDump}$[2][3] = $V_A + V_S$ V_{IN} = 0 and 10 V, t_d = 400 ms, R_I = 2 Ω, R_L = 3 Ω, V_A = 13.5 V	V_{LD}	67.5	V
Electro**s**tatic **d**ischarge voltage[2] (Human Body Model) according to Jedec norm EIA/JESD22-A114-B, Section 4	V_{ESD}	2	kV
Jedec humidity category,J-STD-20-B		MSL1	
IEC climatic category; DIN EN 60068-1		40/150/56	

Thermal resistance

junction - case:	R_{thJC}	1.1	K/W
SMD: junction - ambient @ min. footprint @ 6 cm² cooling area [4]	R_{thJA}	 115 55	

[1]For input voltages beyond these limits I_{IN} has to be limited.

[2]not subject to production test, specified by design

[3]$V_{Loaddump}$ is setup without the DUT connected to the generator per ISO 7637-1 and DIN 40839

[4] Device on 50mm*50mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70µm thick) copper area for drain connection. PCB mounted vertical without blown air.

[5]not subject to production test, calculated by R_{thJA} and $R_{ds(on)}$

Electrical Characteristics

Parameter at T_j = 25°C, unless otherwise specified	Symbol	Values			Unit
		min.	typ.	max.	
Characteristics					
Drain source clamp voltage T_j = - 40 ...+ 150 °C, I_D = 10 mA	$V_{DS(AZ)}$	42	-	55	V
Off-state drain current	I_{DSS}				µA
T_j = -40...+85 °C, V_{DS} = 32 V, V_{IN} = 0 V		-	1.5	8	
T_j = 150 °C		-	10	20	
Input threshold voltage	$V_{IN(th)}$				V
I_D = 2.4 mA, T_j = 25 °C		1.3	1.7	2.2	
I_D = 2.4 mA, T_j = 150 °C		0.8	-	-	
On state input current	$I_{IN(on)}$	-	10	30	µA
On-state resistance	$R_{DS(on)}$				mΩ
V_{IN} = 5 V, I_D = 4.6 A, T_j = 25 °C		-	27	34	
V_{IN} = 5 V, I_D = 4.6 A, T_j = 150 °C		-	54	68	
On-state resistance	$R_{DS(on)}$				
V_{IN} = 10 V, I_D = 4.6 A, T_j = 25 °C		-	23	28	
V_{IN} = 10 V, I_D = 4.6 A, T_j = 150 °C		-	46	56	
Nominal load current [5] T_j < 150°C, V_{IN} = 10 V, T_A = 85 °C, SMD [1]	$I_{D(Nom)}$	4.6	5.5	-	A
Nominal load current [5] V_{IN} = 10 V, V_{DS} = 0.5 V, T_C = 85 °C, T_j < 150°C	$I_{D(ISO)}$	12.6	15.3	-	
Current limit (active if V_{DS}>2.5 V)[2] V_{IN} = 10 V, V_{DS} = 12 V, t_m = 200 µs	$I_{D(lim)}$	30	45	55	

[1] @ 6 cm² cooling area

[2] Device switched on into existing short circuit (see diagram Determination of $I_{D(lim)}$). If the device is in on condition and a short circuit occurs, these values might be exceeded for max. 50 µs.

[5] not subject to production test, calculated by R_{thJA} and $R_{ds(on)}$

Electrical Characteristics

Parameter at T_j = 25°C, unless otherwise specified	Symbol	Values			Unit
		min.	typ.	max.	
Dynamic Characteristics					
Turn-on time V_{IN} to 90% I_D: R_L = 4.7 Ω, V_{IN} = 0 to 10 V, V_{bb} = 12 V	t_{on}	-	60	120	µs
Turn-off time V_{IN} to 10% I_D: R_L = 4.7 Ω, V_{IN} = 10 to 0 V, V_{bb} = 12 V	t_{off}	-	60	120	
Slew rate on 70 to 50% V_{bb}: R_L = 4.7 Ω, V_{IN} = 0 to 10 V, V_{bb} = 12 V	$-dV_{DS}/dt_{on}$	-	0.3	1.5	V/µs
Slew rate off 50 to 70% V_{bb}: R_L = 4.7 Ω, V_{IN} = 10 to 0 V, V_{bb} = 12 V	dV_{DS}/dt_{off}	-	0.3	1.5	
Protection Functions[1]					
Thermal overload trip temperature	T_{jt}	150	175	-	°C
Thermal hysteresis [2]	ΔT_{jt}	-	10	-	K
Input current protection mode T_j = 150 °C	$I_{IN(Prot)}$	-	180	400	µA
Unclamped single pulse inductive energy [2] I_D = 4.6 A, T_j = 25 °C, V_{bb} = 12 V	E_{AS}	3.5	-	-	J

Inverse Diode

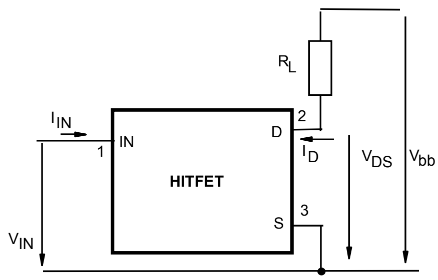
Inverse diode forward voltage I_F = 51 A, t_m = 250 µs, V_{IN} = 0 V, t_P = 300 µs	V_{SD}	-	1.0	1.5	V

[1] Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

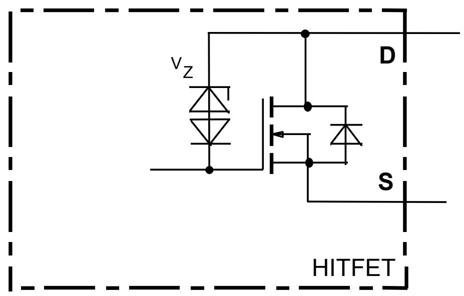
[2] not subject to production test, specified by design

Block diagram

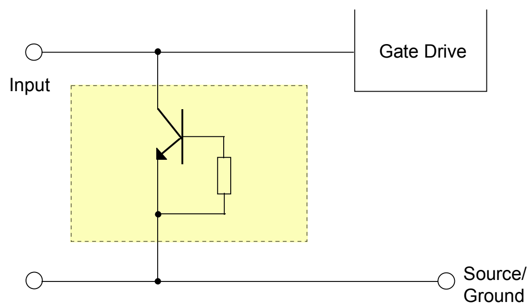
Terms



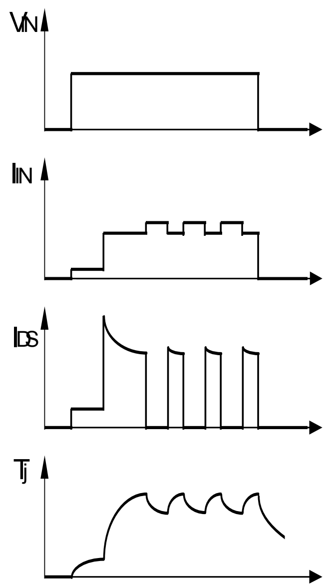
Inductive and overvoltage output clamp



Input circuit (ESD protection)



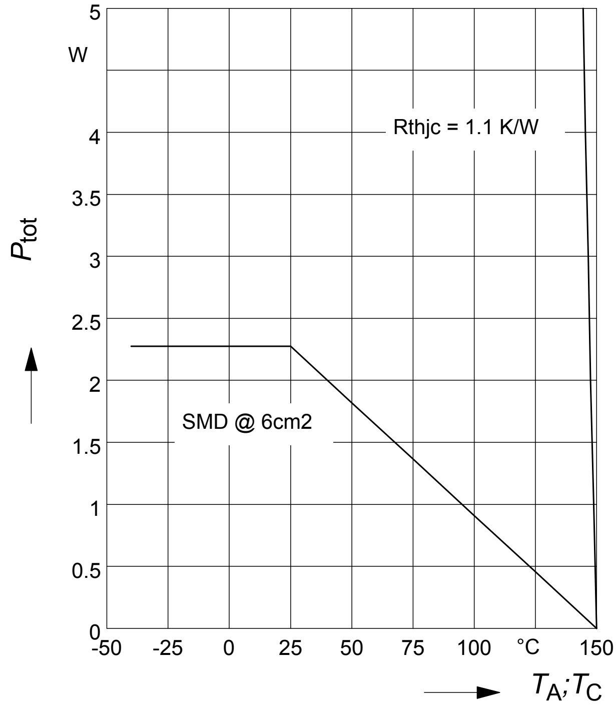
Short circuit behaviour



1 Maximum allowable power dissipation

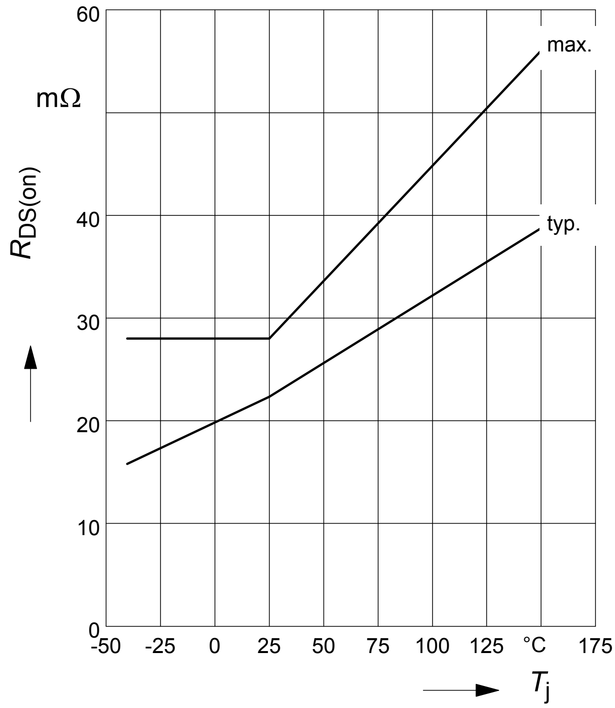
P_{tot} = f(T_C) resp.

P_{tot} = f(T_A) @ R_{thJA}=55 K/W



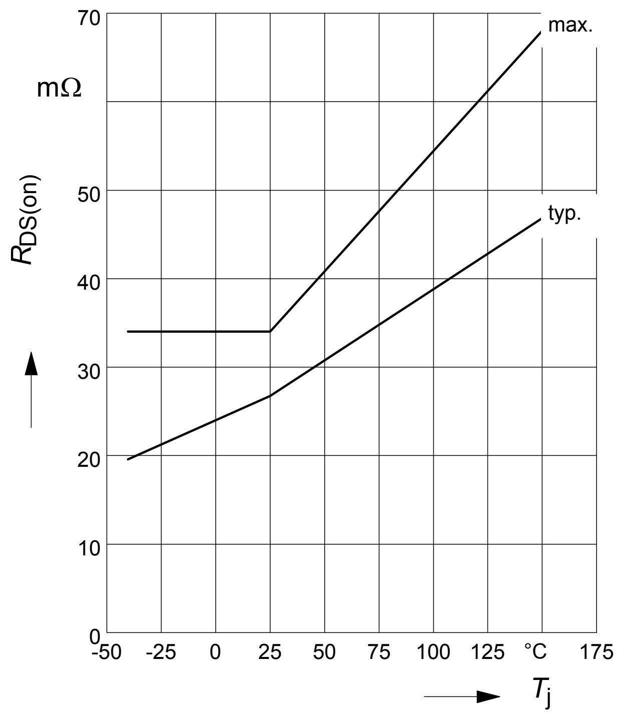
2 On-state resistance

R_{ON} = f(T_j); I_D=12.6A; V_{IN}=10V



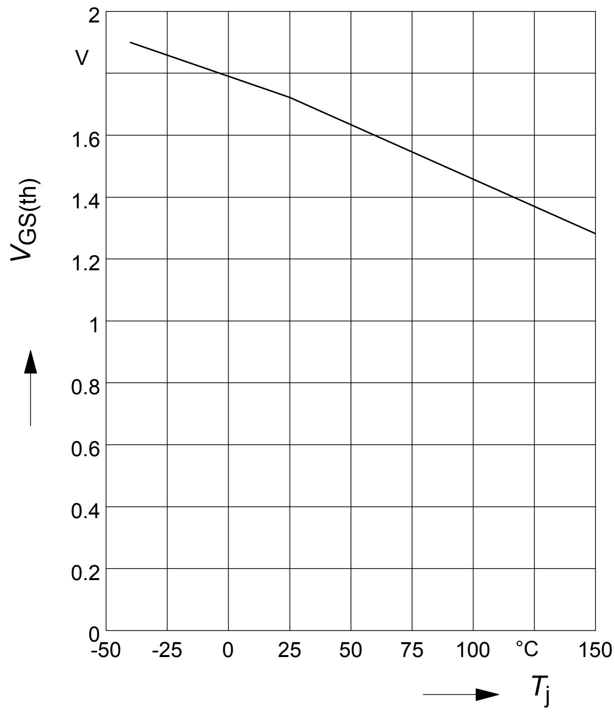
3 On-state resistance

R_{ON} = f(T_j); I_D= 12.6A; V_{IN}=5V



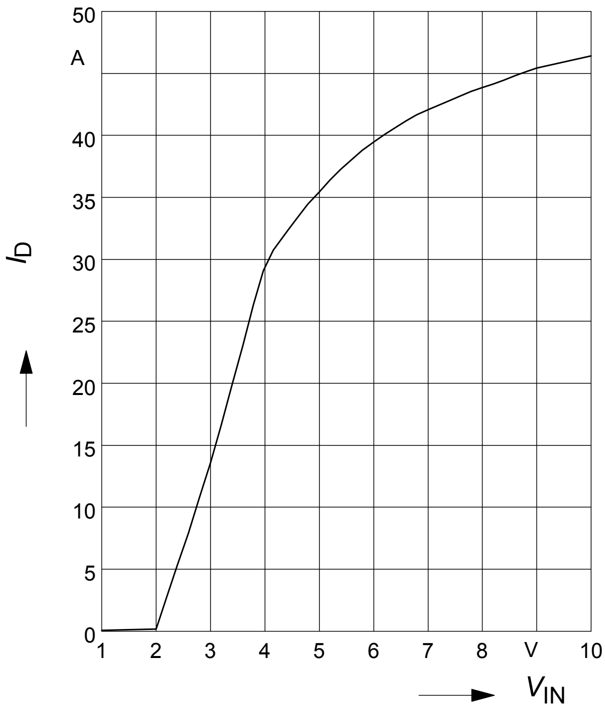
4 Typ. input threshold voltage

$V_{IN(th)}$ = f(T_j); I_D = 1.2 mA; V_{DS} = 12V



5 Typ. transfer characteristics

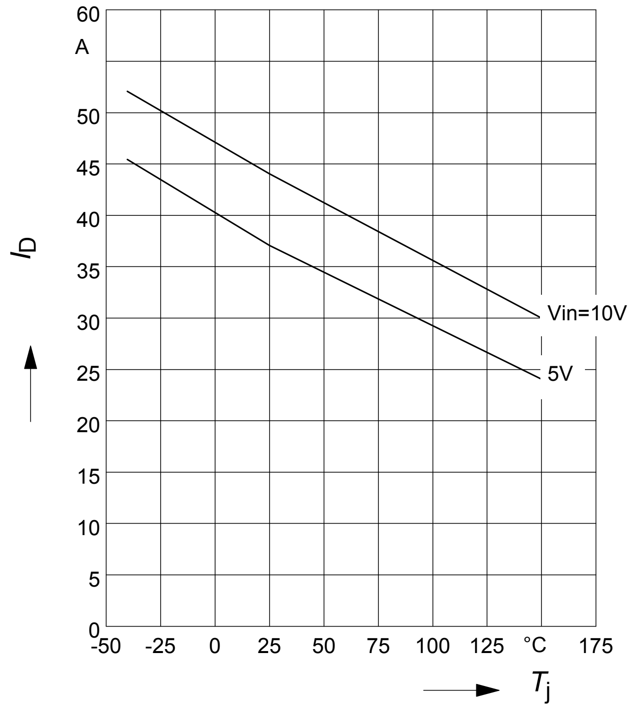
I_D=f(V_{IN}); V_{DS}=12V; T_{Jstart}=25°C



6 Typ. short circuit current

$I_{D(lim)}$ = f(T_j); V_{DS}=12V

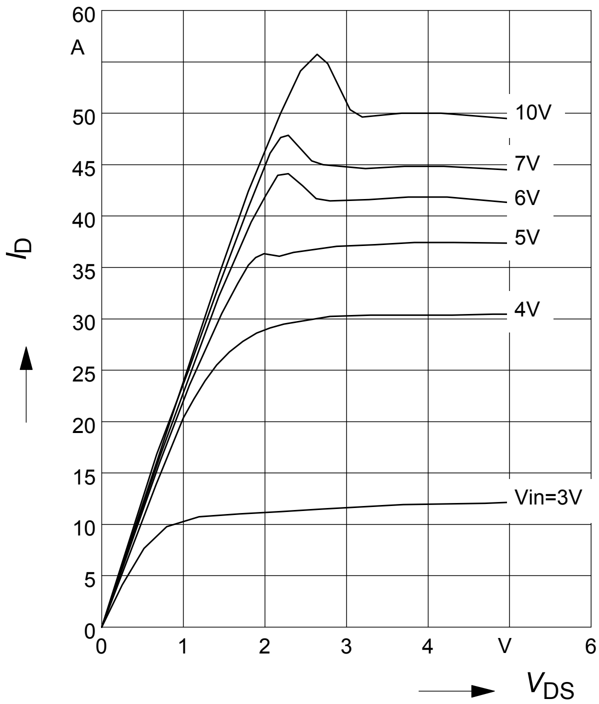
Parameter: V_{IN}



7 Typ. output characteristics

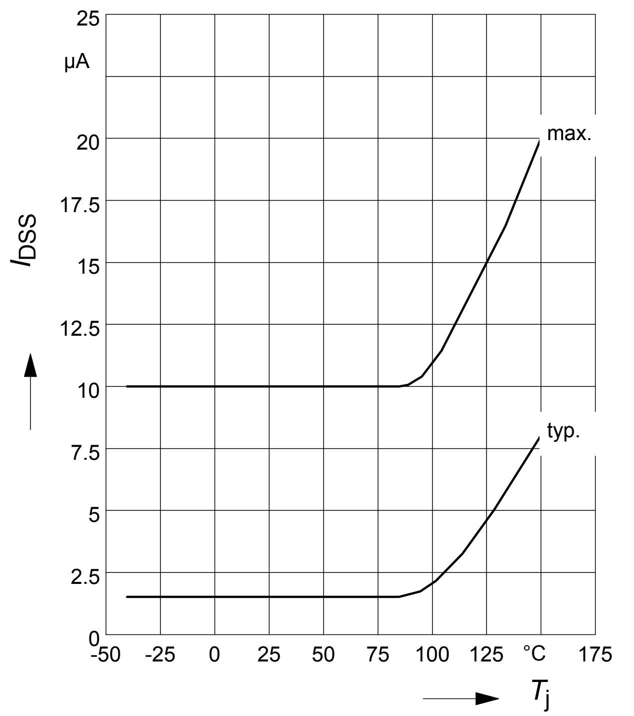
I_D=f(V_{DS}); T_{Jstart}=25°C

Parameter: V_{IN}



8 Off-state drain current

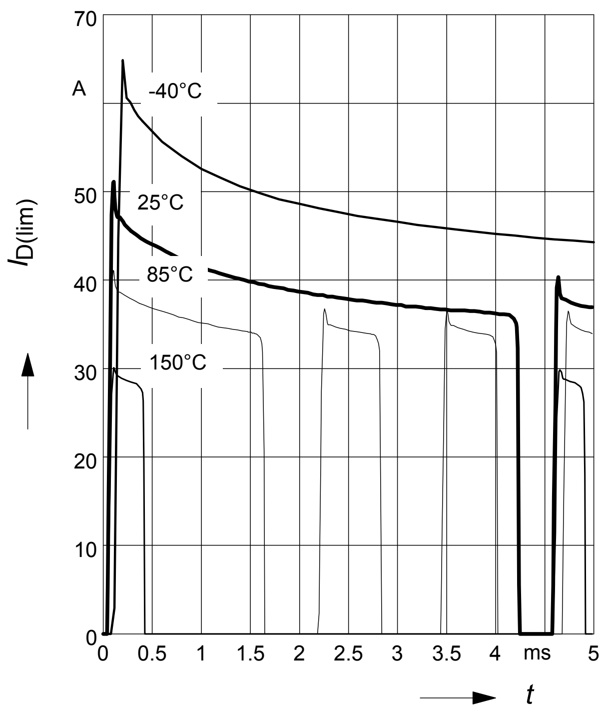
I_{DSS} = f(T_j)



9 Typ. overload current

$I_{D(lim)}$ = f(t), V_{bb}=12 V, no heatsink

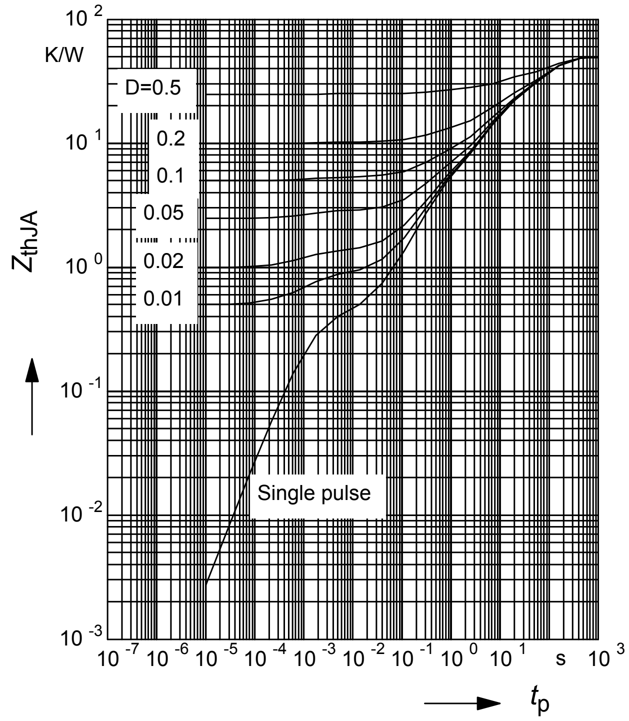
Parameter: T_{jstart}



10 Typ. transient thermal impedance

Z_{thJA}=f(t_p) @ 6 cm² cooling area

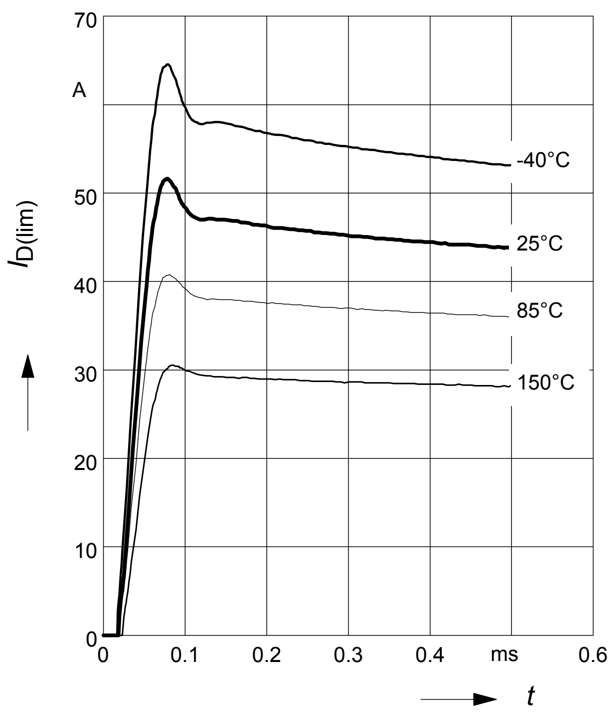
Parameter: D=t_p/T



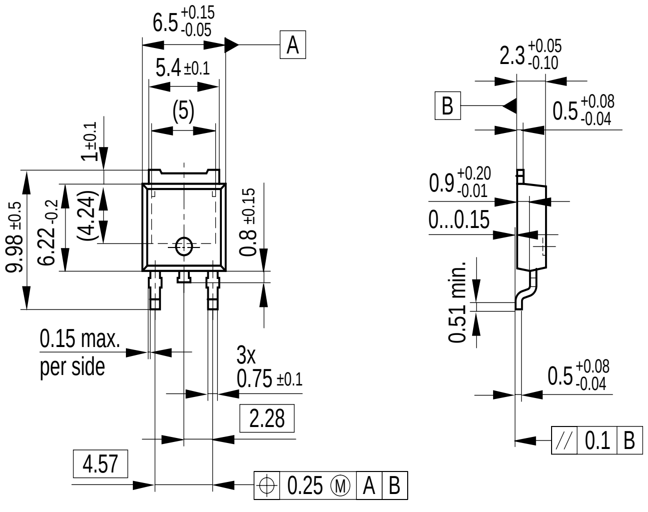
11 Determination of $I_{D(lim)}$

$I_{D(lim)}$ = f(t); t_m = 200µs

Parameter: T_{Jstart}



Package	Ordering Code
P-TO-252-3-11	Q67060-S7401-A3



All metal surfaces tin plated, except area of cut.

Revision History : **2004-03-05**
Previous version : 2003-04-22

Page	Subjects (major changes since last revision)
2, 4	Footnote 2 extended to Vin<0V, E_{tot} and ΔT_{jT}
2, 3	Footnote 5 implemented to P_{tot}, $I_{D(nom)}$ and $I_{D(ISO)}$
2	ESD test condition changed from MIL STD 883D, methode 3015.7 and EOS/ESD assn. standard S5.1-1993 to Jedec Norm EIA/JESD22-A114-B, Section 4
2	Humidity category classification changed from DIN 40040 value E to J-STD-20-B value MSL1
2	climatic category changed from DIN IEC 68-1 to DIN EN 60068-1
3	$V_{IN(th)}$ test conditions from I_D=1.2mA to I_D=2.4mA

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