DATA SHEET

MOS INTEGRATED CIRCUIT

μPD78217A,78218A

8-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μPD78217A and 78218A are members of the 78K/II series of microcontrollers featuring a high-speed high-performance CPU. The μPD78217A and 78218A are based on the μPD78213 and 78214, and feature increased memory capacity and added functions, such as a timer/counter and macro servicing.

Functions are described in detail in the following User's Manuals, which should be read when carrying out design work.

μPD78218A Subseries User's Manual: Hardware (IEU-1313)
78K/II Series User's Manual: Instruction (IEU-1311)

FEATURES

- Upper compatibility with μPD78214 subseries (pin-compatible)
- High-speed instruction execution (at 12 MHz): 333 ns (μPD78218A), 500 ns (μPD78217A)
- On-chip high-performance interrupt controller
- On-chip A/D converter: 8 bits × 8 channels
- Number of I/O pins: 54 (μPD78218A), 36 (μPD78217A)
- Real-time output ports: 8 bits × 1 channel or 4 bits × 2 channels
- Serial interface: 2 channels
- Timer/counter: 16 bits × 1 channel and 8 bits × 3 channels

APPLICATION FIELDS

Printers, typewriters, OA equipment such as plain paper copiers (PPCs) and faxes, electronic music instruments, inverters, cameras, etc.

ORDERING INFORMATION

Part Number	Package	On-Chip ROM	On-Chip RAM
μPD78217ACW	64-pin plastic shrink DIP (750 mil)	None	1024
μPD78217AGC-AB8	64-pin plastic QFP (14 x 14 mm)	None	1024
μPD78218ACW-×××	64-pin plastic shrink DIP (750 mil)	32K	1024
μPD78218AGC-×××-AB8	64-pin plastic QFP (14 x 14 mm)	32K	1024

Remark ××× is the ROM code suffix.

The information in this document is subject to change without notice.

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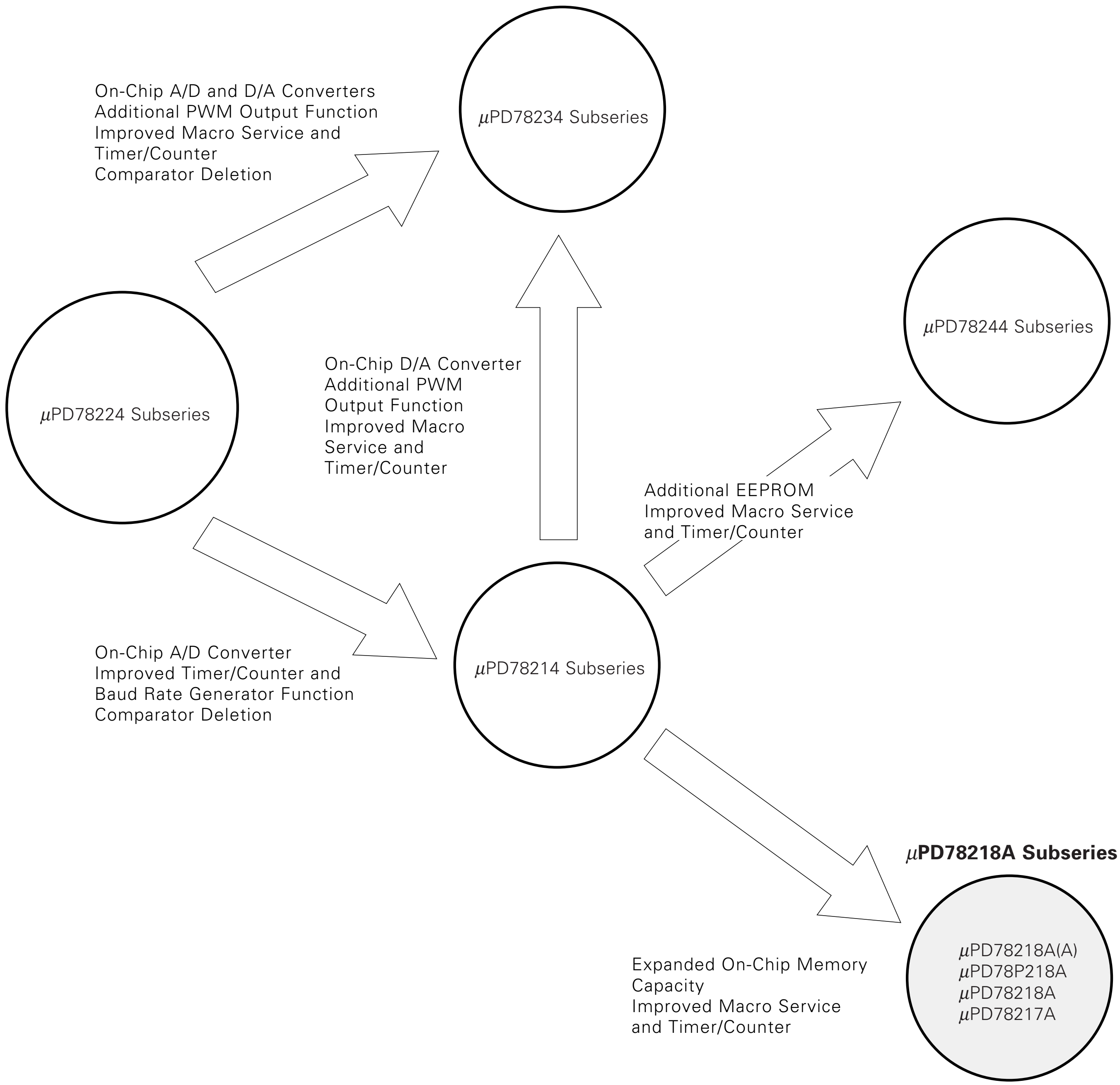
The mark ★ shows revised points.

78K/II Product Development



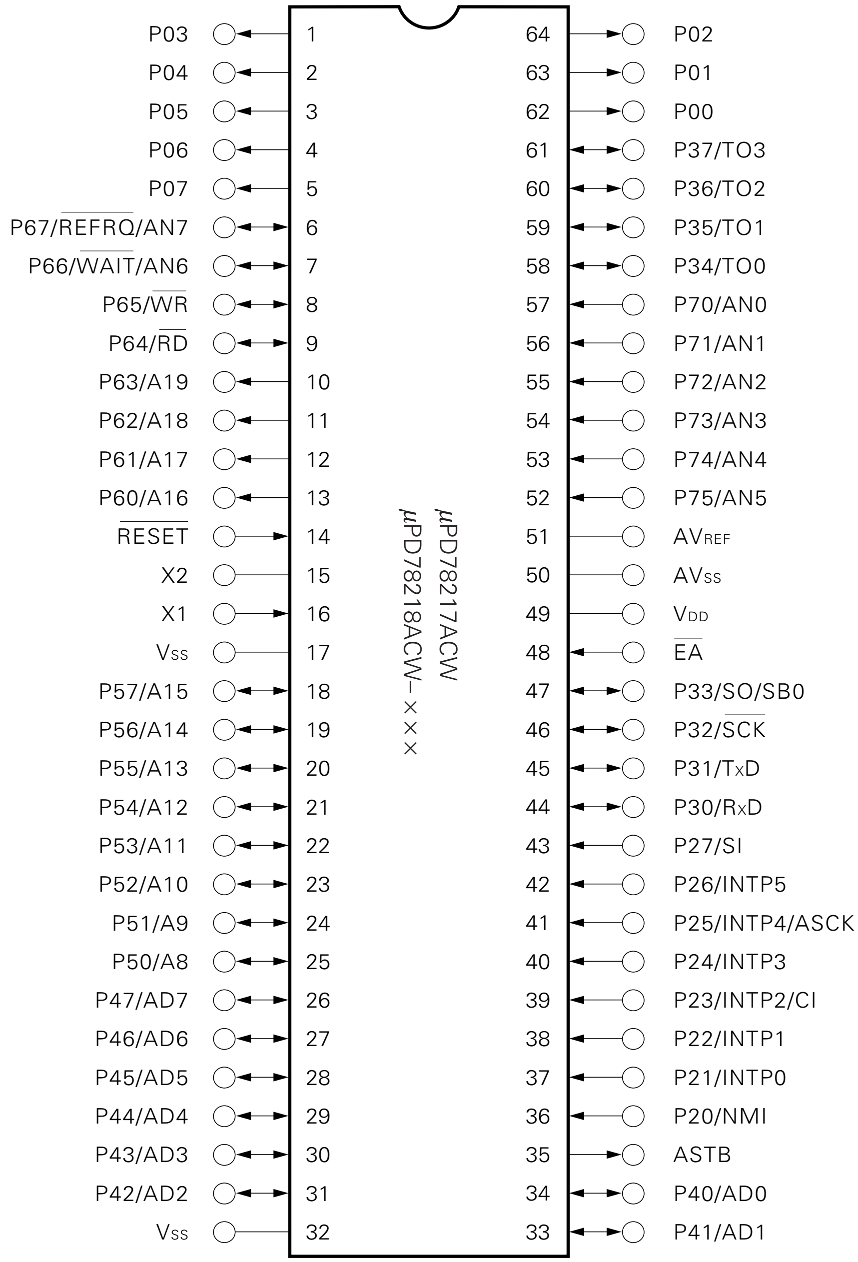
FUNCTION LIST

Item		μPD78217A	μPD78218A
Basic instructions (mnemonic)		65	
Minimum instruction execution time		333 ns (at 12-MHz)	
Instruction set		16-bit operation Multiply and divide (8 bits × 8 bits, 16 bits ÷ 8 bits) Bit manipulate BCD adjust, etc.	
On-chip memory capacity	ROM	None	32 Kbytes
	RAM	1024 bytes	
Address space		Program memory: 64 Kbytes, data memory: 1 Mbytes	
I/O pins	Input	14	
	Output	12	
	Input/Output	10	28
	Total	36	54
Additional function pins Note	Pins with pull-up resistor	16	34
	LED direct drive outputs	—	16
	Transistor direct drive outputs	8	
ROM-less mode setting		ROM-less version	$\overline{EA}$ pin = low level
General registers		8 bits × 8 × 4 banks (memory mapping)	
Timer/counter		16-bit timer/counter: Timer register × 1, Capture register × 1, Compare register × 2 Pulse output capability (Toggle output, PWM/PPG × 2, One-shot pulse output)	
		8-bit timer/counter 1: Timer register × 1, Capture/compare register × 1, Compare register × 1 Pulse output capability (Real-time outputs, 4 bits × 2)	
		8-bit timer/counter 2: Timer register × 1, Capture register × 1, Compare register × 2 Pulse output capability (Toggle output, PWM/PPG × 2)	
		8-bit timer/counter 3: Timer register × 1, Compare register × 1 —	
Real-time output port		Output port linked 8-bit timer/counter 1 4 bits × 2 channels	
Serial interface		UART : 1 channel (on-chip dedicated baud rate generator) CSI (3-wire serial I/O, SBI) : 1 channel	
A/D converter		8-bit resolution × 8 channels	
Interrupt		19 sources (external 7, internal 12) + BRK instruction 2-level priority order (programmable) 2 servicing modes (vectored interrupt, macro service)	
Package		64-pin plastic shrink DIP (750 mil) 64-pin plastic QFP (14 x 14 mm)	

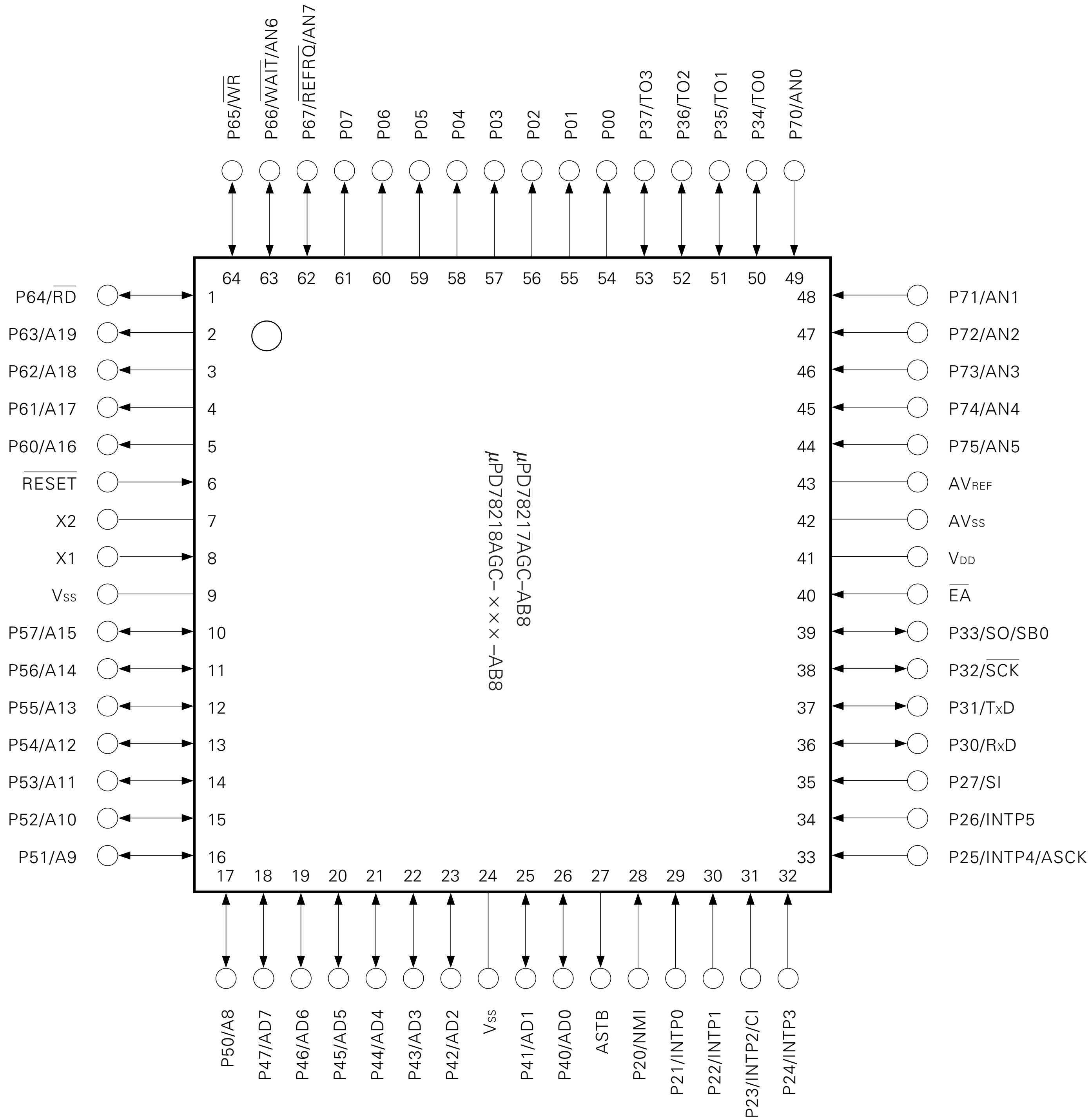
Note Additional function pins are included in I/O pins.

PIN CONFIGURATION (TOP VIEW)

64-pin plastic shrink DIP



64-pin plastic QFP

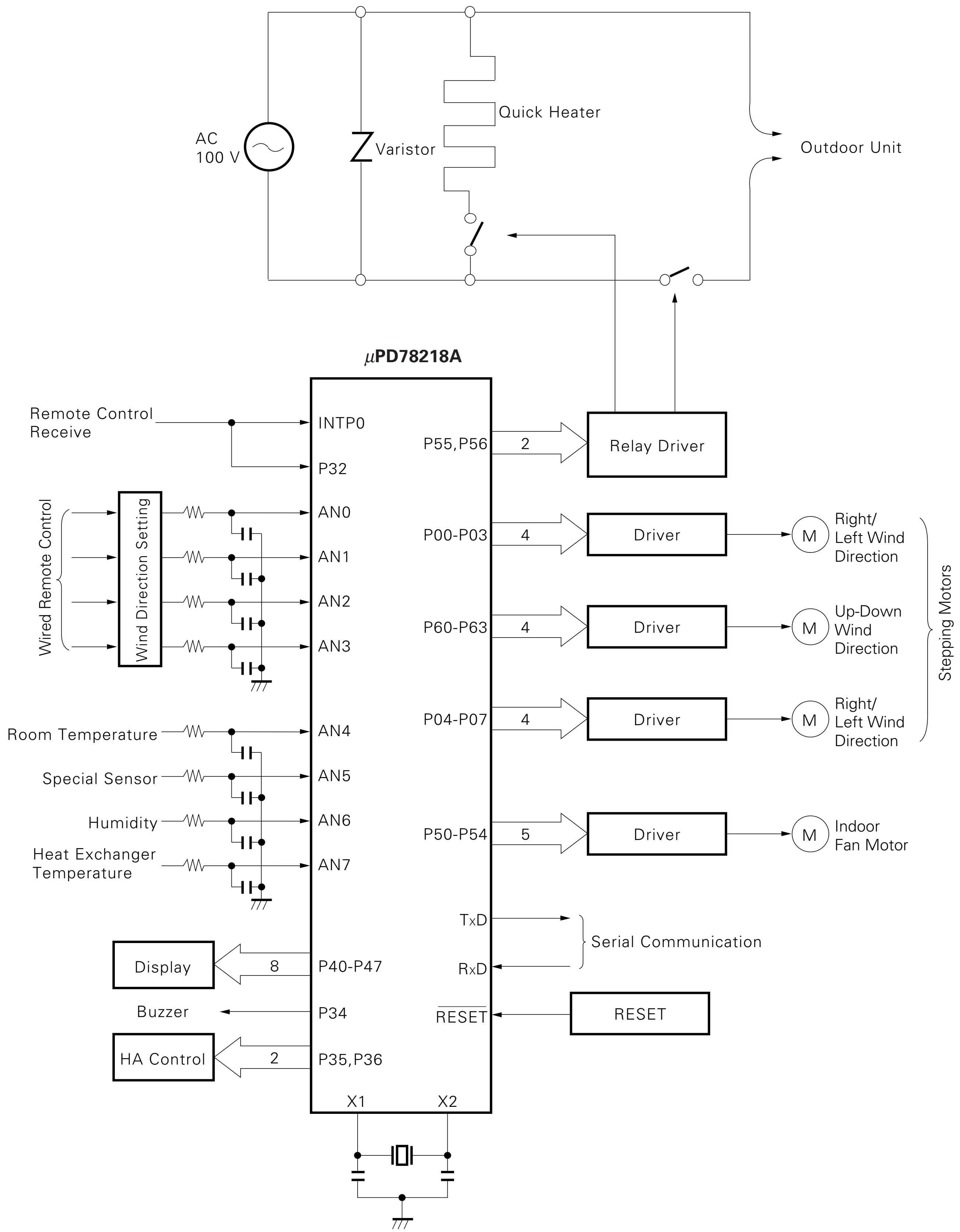


PIN IDENTIFICATION

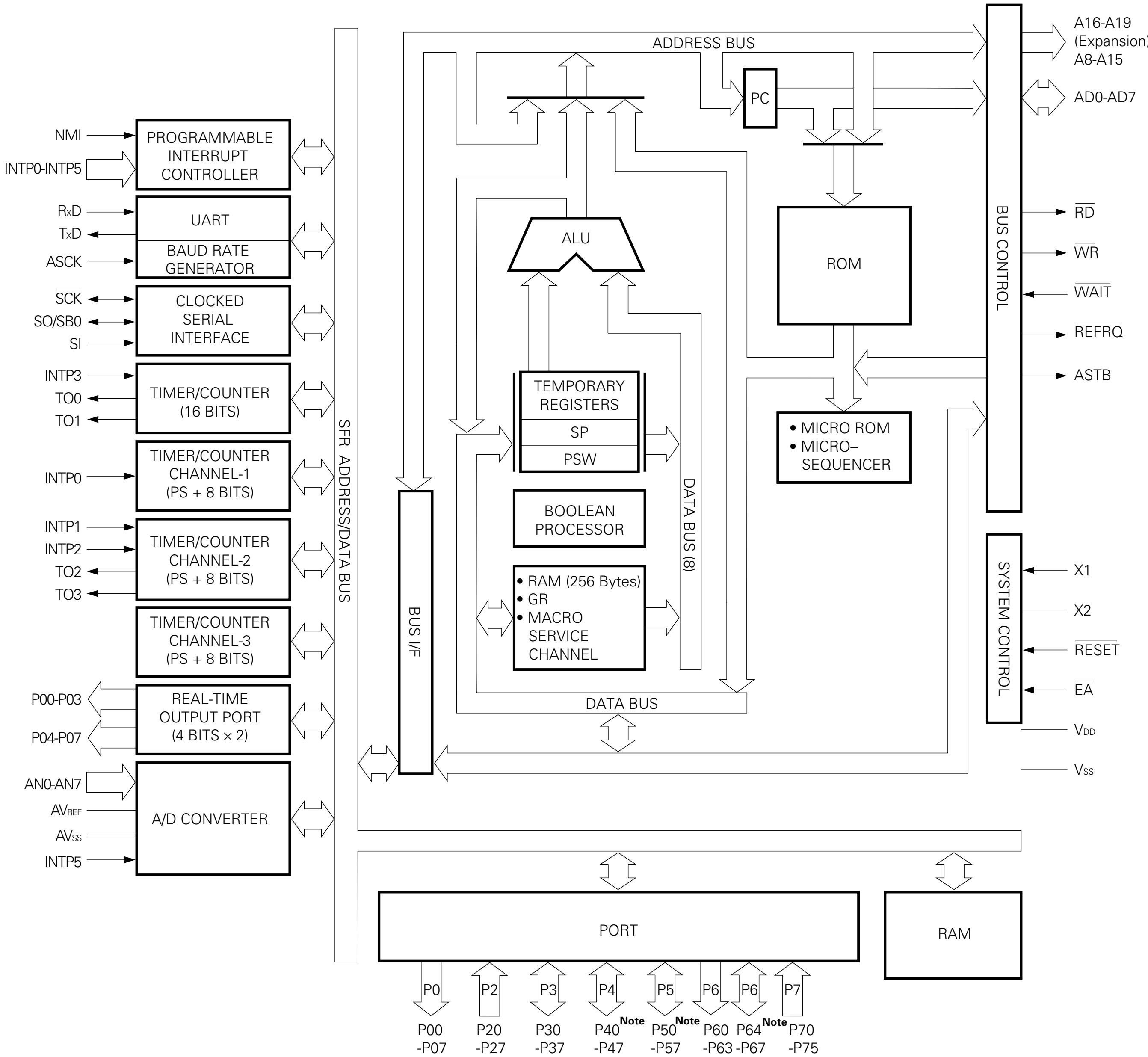
P00 to P07	: Port 0
P20 to P27	: Port 2
P30 to P37	: Port 3
P40 to P47	: Port 4
P50 to P57	: Port 5
P60 to P67	: Port 6
P70 to P75	: Port 7
TO0 to TO3	: Timer Output
CI	: Clock Input
RxD	: Receive Data
TxD	: Transmit Data
$\overline{SCK}$	: Serial Clock
ASCK	: Asynchronous Serial Clock
SB0	: Serial Bus
SI	: Serial Input
SO	: Serial Output
NMI	: Non-maskable Interrupt
INTP0 to INTP5	: Interrupt From Peripherals
AD0 to AD7	: Address/Data Bus
A8 to A19	: Address Bus

$\overline{RD}$	: Read Strobe
$\overline{WR}$	: Write Strobe
$\overline{WAIT}$	: Wait
ASTB	: Address Strobe
$\overline{REFRQ}$	: Refresh Request
$\overline{RESET}$	: Reset
X1, X2	: Crystal
$\overline{EA}$	: External Access
AN0 to AN7	: Analog Input
AV_{REF}	: Reference Voltage
AV_{SS}	: Analog Ground
V_{DD}	: Power Supply
V_{SS}	: Ground

EXAMPLE OF SYSTEM CONFIGURATION (INVERTER AIR-CONDITIONER IN-DOOR UNIT)



INTERNAL BLOCK DIAGRAM



Caution **Inernal ROM/RAM capacity varies depending on the product.**

Note In case of the μPD78217A, P40 to P47, P50 to P57, P64 and P65 cannot be used as ports.

CONTENTS

1. DIFFERENCES BETWEEN μPD78218A AND μPD78214 SUBSERIES

Series Name		μPD78218A Subseries			μPD78214 Subseries			
Part Number		**μPD78217A**	**μPD78218A**	μPD78P218A	μPD78212	μPD78213	μPD78214	μPD78P214
Minimum instruction execution time (at 12-MHz)		500 ns	333 ns		333 ns	500 ns	333 ns	
PUSH PSW instruction execution time (number of clocks)		When stack area is an internal dual port RAM : 6 Other than above : 8			When stack area is an internal dual port RAM : 5 or 7 Other than above : 7 or 9			
Power voltage range		V_{DD}=+5V±10%		V_{DD}=+5V±0.3V	V_{DD}=+5V±10%			
On-chip memory	ROM	ROM-less	32 Kbytes (mask ROM)	32 Kbytes (PROM)	8 Kbytes (mask ROM)	ROM-less	16 Kbytes (mask ROM)	16 Kbytes (PROM)
	RAM	1024 bytes			384 bytes	512 bytes		
I/O pins		36	54		54	36	54	
16-bit timer/counter one-shot pulse output		Available			Not available			
Macro service counter bit width		8/16 bits select capability (except type A)			Only 8 bits			
Macro service type C MPD, MPT increments		16-bit increment			Only low-order 8 bits increment (high-order 8 bits are unchanged)			
Macro service execution time		Macro service depends on mode. Compare with user's manual of products.						
Restrictions when data is transferred from macro service type A memory to SFR		Generated when transfer source buffer (memory) address is 0FED0H to 0FEDFH.			Generated when transfer data is in D0H to DFH.			
A/D converter	Input voltage restrictions	Only pins involved in A/D conversion			Pins involved in A/D conversion and pins selected by ADM register bits ANI0 to ANI2 only: 0V to AV_{REF} pin voltage			
	AV_{REF} voltage restrictions	3.6 V to V_{DD}			3.4 V to V_{DD}			
Stabilization time for oscillation in STOP mode release		Dedicated counter 15 bits or $\overline{NMI}$ active pulse width + dedicated counter 16 bits			$\overline{NMI}$ active pulse width + dedicated counter 16 bits			
Package		• 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QFP (14 x 14 mm) • 64-pin ceramic shrink DIP (CERDIP, with window, 750 mil): μPD78P218A only			• 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QUIP: Except μPD78212 • 68-pin plastic QFJ: Except μPD78212 • 64-pin plastic QFP (14 x 14 mm) • 74-pin plastic QFP (20 x 20 mm) • 64-pin ceramic shrink DIP (CERDIP, with window, 750 mil): μPD78P214 only			

2. PIN FUNCTIONS

2.1 PORTS

Pin Name	I/O	Alternate Function	Function
P00 to P07	Output	——	Port 0 (P0): Established as a real-time output port (4 bits × 2) Direct drive of transistors capability
P20	Input	NMI	Port 2 (P2): P20 cannot be used as a general-purpose port. (Non-maskable interrupt) However, the input level can be confirmed in the interrupt routine. The connection of the on-chip pull-up resistor can be specified as a 6-bit unit for P22 to P27 by software.
P21		INTP0	
P22		INTP1	
P23		INTP2/CI	
P24		INTP3	
P25		INTP4/ASCK	
P26		INTP5	
P27		SI	
P30	Input/ output	RxD	Port 3 (P3): The input/output specifiable bit-wise. Input mode pins specifiable for on-chip pull-up resistor connection as a batch by software.
P31		TxD	
P32		$\overline{\text{SCK}}$	
P33		SO/SB0	
P34 to P37		TO0 to TO3	
P40 to P47[Note]	Input/ output	AD0 to AD7	Port 4 (P4): The input/output specifiable as an 8-bit batch. The connection of the on-chip pull-up resistor specifiable as an 8-bit batch by software. LED direct drive capability.
P50 to P57[Note]	Input/ output	A8 to A15	Port 5 (P5): The input/output specifiable bit-wise. Input mode pins specifiable for on-chip pull-up resistor connection as a batch by software. LED direct drive capability.
P60 to P63	Output	A16 to A19	Port 6 (P6): P64 to P67 enables to specify the input/output bit-wise. The connection of the on-chip pull-up resistor to input mode pins can be specified as a batch for P64 to P67 by software.
P64[Note]	Input/ output	$\overline{\text{RD}}$	
P65[Note]		$\overline{\text{WR}}$	
P66		$\overline{\text{WAIT}}$/AN6	
P67		$\overline{\text{REFRQ}}$/AN7	
P70 to P75	Input	AN0 to AN5	Port 7 (P7)

Note In case of the μPD78217A, these cannot be used as ports.

2.2 NON-PORT PINS

Pin Name	I/O	Alternate Function	Function
TO0 to TO3	Output	P34 to P37	Timer output
CI	Input	P23 /INTP2	Count clock input to 8-bit timer/counter 2
R_XD	Input	P30	Serial data input (UART)
T_XD	Output	P31	Serial data output (UART)
ASCK	Input	P25/INTP4	Baud rate clock input (UART)
SB0	Input/output	P33/SO	Serial data input/output (SBI)
SI	Input	P27	Serial data input (3-wire serial I/O)
SO	Output	P33/SB0	Serial data output (3-wire serial I/O)
$\overline{\text{SCK}}$	Input/output	P32	Serial clock input/output (SBI, 3-wire serial I/O)
NMI	Input	P20	External interrupt request
INTP0		P21	
INTP1		P22	
INTP2		P23/CI	
INTP3		P24	
INTP4		P25/ASCK	
INTP5		P26	
AD0 to AD7	Input/output	P40 to P47 [Note]	Time multiplexing address/data bus (external memory connection)
A8 to A15	Output	P50 to P57 [Note]	Upper address bus (external memory connection)
A16 to A19	Output	P60 to P63	Upper address when extending address (external memory connection)
$\overline{\text{RD}}$	Output	P64 [Note]	Read strobe into external memory
$\overline{\text{WR}}$	Output	P65 [Note]	Write strobe into external memory
$\overline{\text{WAIT}}$	Input	P66/AN6	Wait insertion
ASTB	Output	—	Address (A0 to A7) latch timing output (during external memory access)
$\overline{\text{REFRQ}}$	Output	P67/AN7	Refresh pulse output into external pseudo-static memory
$\overline{\text{RESET}}$	Input	—	Chip reset
X1	Input	—	Crystal connection for system clock oscillation (external clock input to X1 enabled)
X2	—		
$\overline{\text{EA}}$	Input	—	ROM-less operating specification (external access of the same space as internal ROM). Used high for the μPD78218A and used low for the μPD78217A.
AN0 to AN5	Input	P70 to P75	Analog voltage input for A/D converter
AN6, AN7		P66/$\overline{\text{WAIT}}$, P67/$\overline{\text{REFRQ}}$	
AV_{REF}	—	—	Reference voltage apply for A/D converter
AV_{SS}			GND for A/D converter
V_{DD}			Positive power supply
V_{SS}			GND

Note In case of the μPD78217A, these cannot be used as ports.

2.3 PIN I/O CIRCUITS AND UNUSED PIN CONNECTION

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 2-1. For the input/output circuit configuration of each type, see Fig. 2-1.

Table 2-1 Input/Output Circuit Type of Each Pin

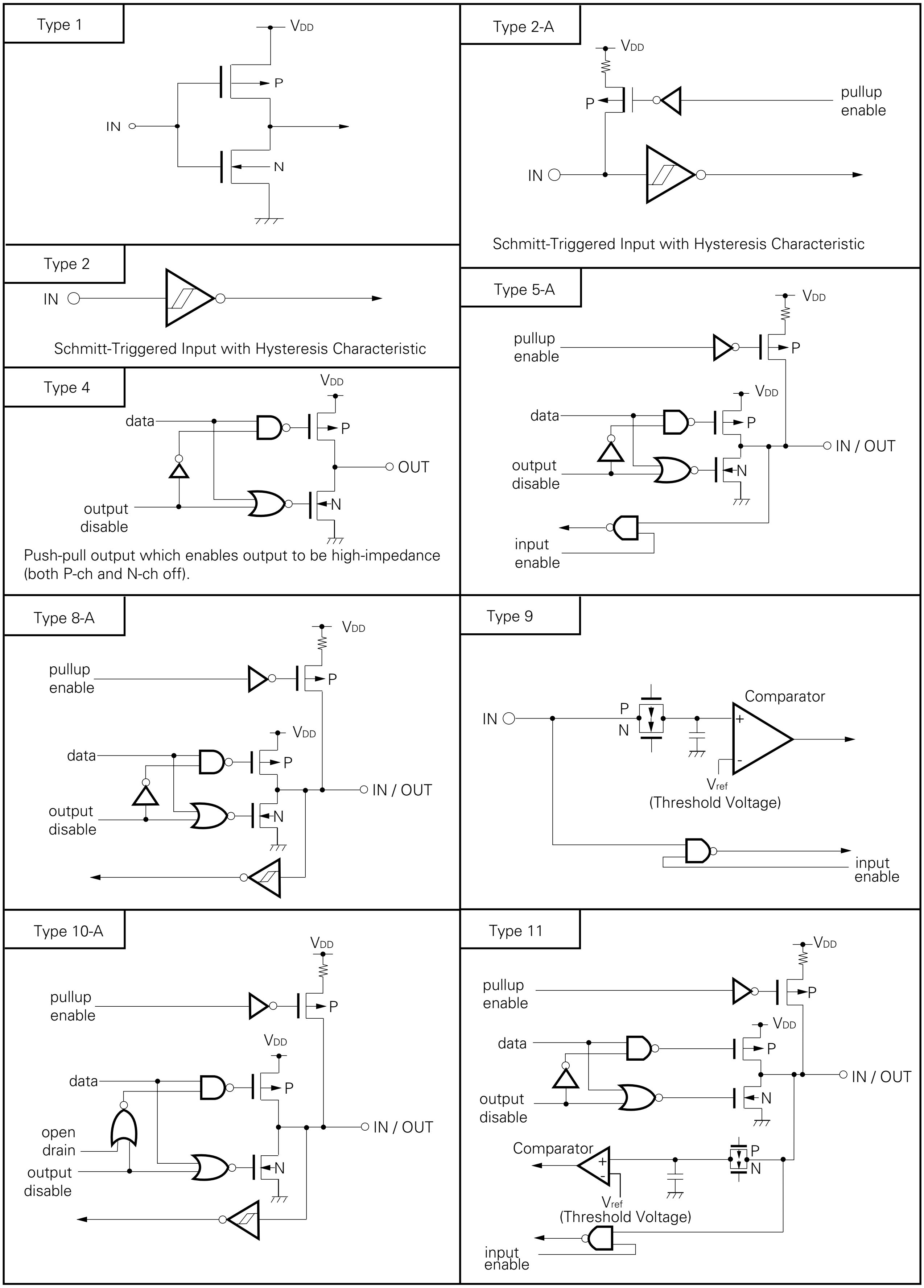
Pin Name	Input/Output Circuit Type	I/O	Unused Pin Connection
P00 to P07	4	Output	Leave open.
P20/NMI	2	Input	Connected to V_{DD} or V_{SS}.
P21/INTP0			
P22/INTP1	2-A		Connected to V_{DD}.
P23/INTP2/CI			
P24/INTP3			
P25/INTP4/ASCK			
P26/INTP5			
P27/SI			
P30/RxD	5-A	Input/output	Input : Connected to V_{DD}. Output : Leave open.
P31/TxD			
P32/$\overline{SCK}$	8-A		
P33/SB0/SO	10-A		
P34/TO0 to P37/TO3	5-A		
P40/AD0 to P47/AD7			
P50/A8 to P57/A15			
P60/A16 to P63/A19	4	Output	Leave open.
P64/$\overline{RD}$	5-A	Input/output	Input : Connected to V_{DD}. Output : Leave open.
P65/$\overline{WR}$			
P66/$\overline{WAIT}$/AN6	11		Input : Connected to V_{DD}.[Note] Output : Leave open.
P67/$\overline{REFRQ}$/AN7			
P70/AN0 to P75/AN5	9	Input	Connected to V_{SS}.
ASTB	4	Output	Leave open.
$\overline{RESET}$	2	Input	—
$\overline{EA}$	1		
AV_{REF}	—		Connected to V_{SS} or V_{DD}.[Note]
AV_{SS}			Connected to V_{SS}.

Note A voltage outside the range AV_{SS} to AV_{REF} should not be applied, as this may damage the μPD78217A/78218A.

Caution If the input/output mode is undefined for the input/output dual-function pins, connect these pins to V_{DD} via a resistor of several ten kΩ.
(Especially if the reset input pin exceeds the low-level input voltage at power-on or in case of input/output switching by software.)

Remark The type numbers are standardized for 78K series, therefore they are not always consecutive numbers for each product (some circuits are not incorporated).

Fig. 2-1 Pin Input/Output Circuits



3. INTERNAL BLOCK FUNCTIONS

3.1 MEMORY SPACE

A memory space of 1 Mbytes can be accessed. Fig. 3-1 shows that memory space. The program memory mapping differs depending on the $\overline{EA}$ pin status.

(1) μPD78217A ($\overline{EA}$ = L)

The program memory is mapped onto external memory (64256 bytes: 00000H to 0FAFFH). This area can also be used as data memory.

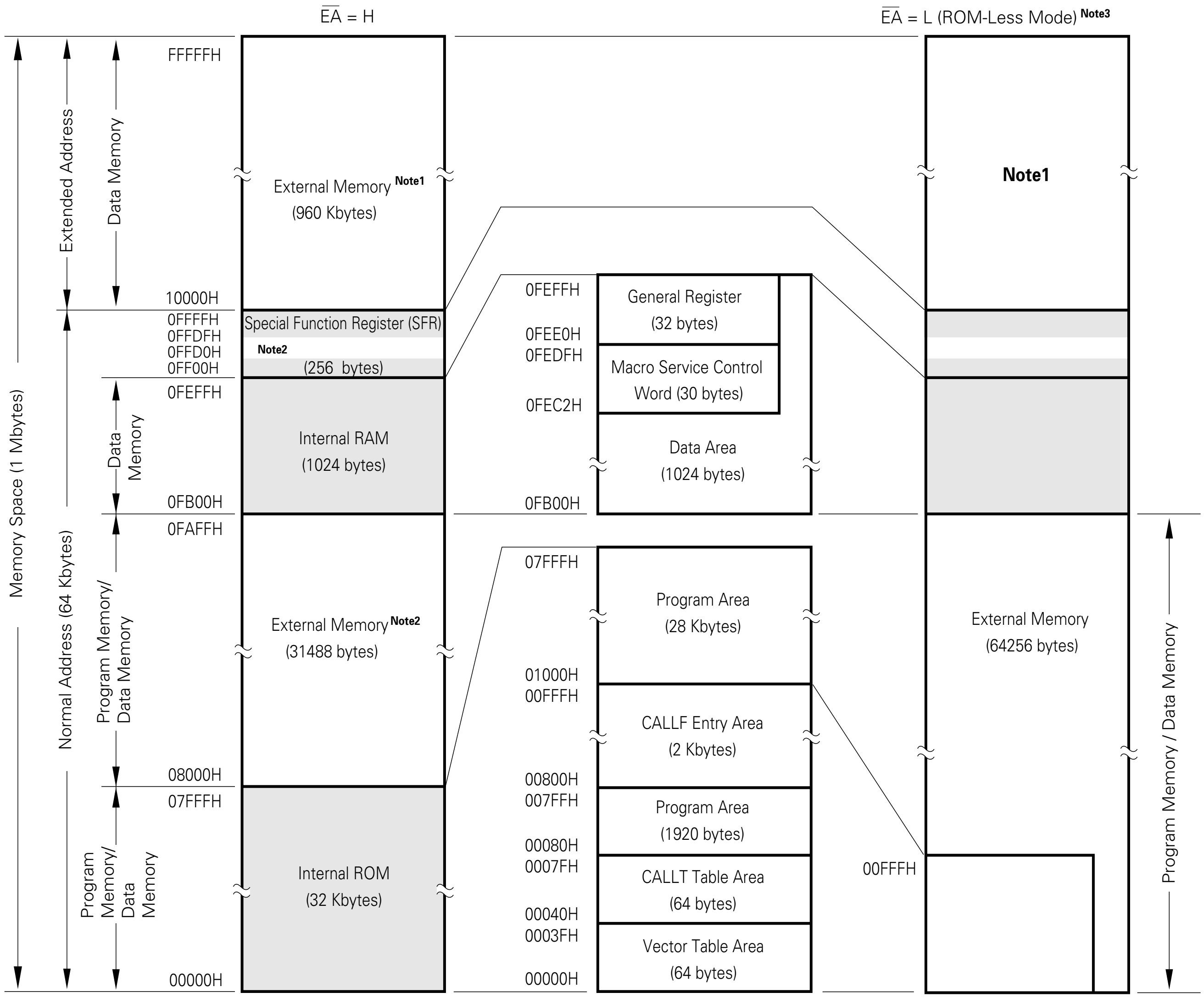
The data memory is mapped onto internal RAM (1024 bytes: 0FB00H to 0FEFFH). In the 1-Mbyte expansion mode, external memory (960 Kbytes: 10000H to FFFFFH) is mapped as expanded data memory.

(2) μPD78218A ($\overline{EA}$ = H)

The program memory is mapped onto internal ROM (32 Kbytes: 00000H to 07FFFH) and external memory (31488 bytes: 08000H to 0FAFFH). The external memory is accessed in the external memory expansion mode. The area mapped onto the external memory can also be used as data memory.

The data memory is mapped onto internal RAM (1024 bytes: 0FB00H to 0FEFFH). In the 1-Mbyte expansion mode, external memory (960 Kbytes: 10000H to FFFFFH) is mapped as expanded data memory.

Fig. 3-1 Memory Map

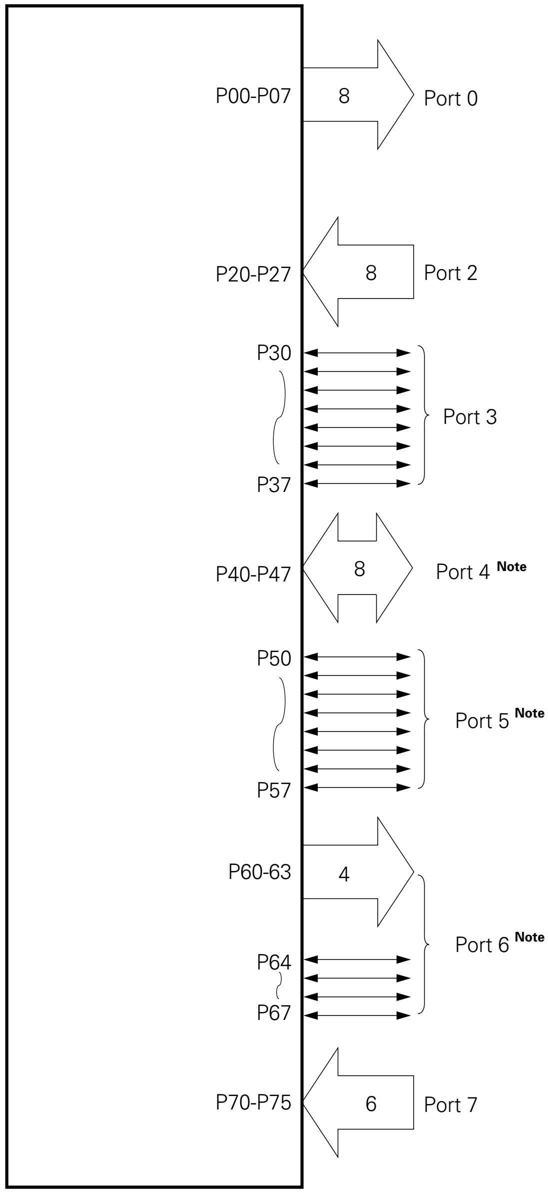


Notes
1. Accessed by 1-Mbyte expansion mode. Shaded areas denote internal memory.
2. Accessed by external memory expansion mode.
3. The μPD78217A applies only when $\overline{EA}$ = L.

3.2 PORTS

The μPD78217A/78218A has the ports shown in Fig. 3-2 which allow various kinds of control. The functions of each port are shown in Table 3-1. For ports 2 to 6, on-chip pull-up resistor can be specified by software at input.

Fig. 3-2 Port Configuration



Note In case of the μPD78217A, P40 to P47, P50 to P57, P64, and P65 cannot be used as ports.

Table 3-1 Port Function

Name	Pin Name	Function	Designation of Software Pull-Up
Port 0	P00 to P07	Output or high-impedance specifiable as an 8-bit batch. Can also operate as 4 bits real-time output (P00 to P03, P04 to P07). Transistor direct drive capability.	———
Port 2	P20 to P27	Input port	6-bit batch (P22 to P27)
Port 3	P30 to P37	Input or output specifiable bit-wise.	Input mode pins specifiable as a batch
Port 4 [Note]	P40 to P47	Input or output specifiable as an 8-bit batch. LED direct drive capability.	8-bit batch
Port 5 [Note]	P50 to P57	Input or output specifiable bit-wise. LED direct drive capability.	Input mode pins specifiable as a batch
Port 6 [Note]	P60 to P63	Output port	———
	P64 to P67	Input or output specifiable bit-wise.	Input mode pins specifiable as a batch
Port 7	P70 to P75	Input port	———

Note In case of the μPD78217A, P40 to P47, P50 to P57, P64, and P65 cannot be used as ports.

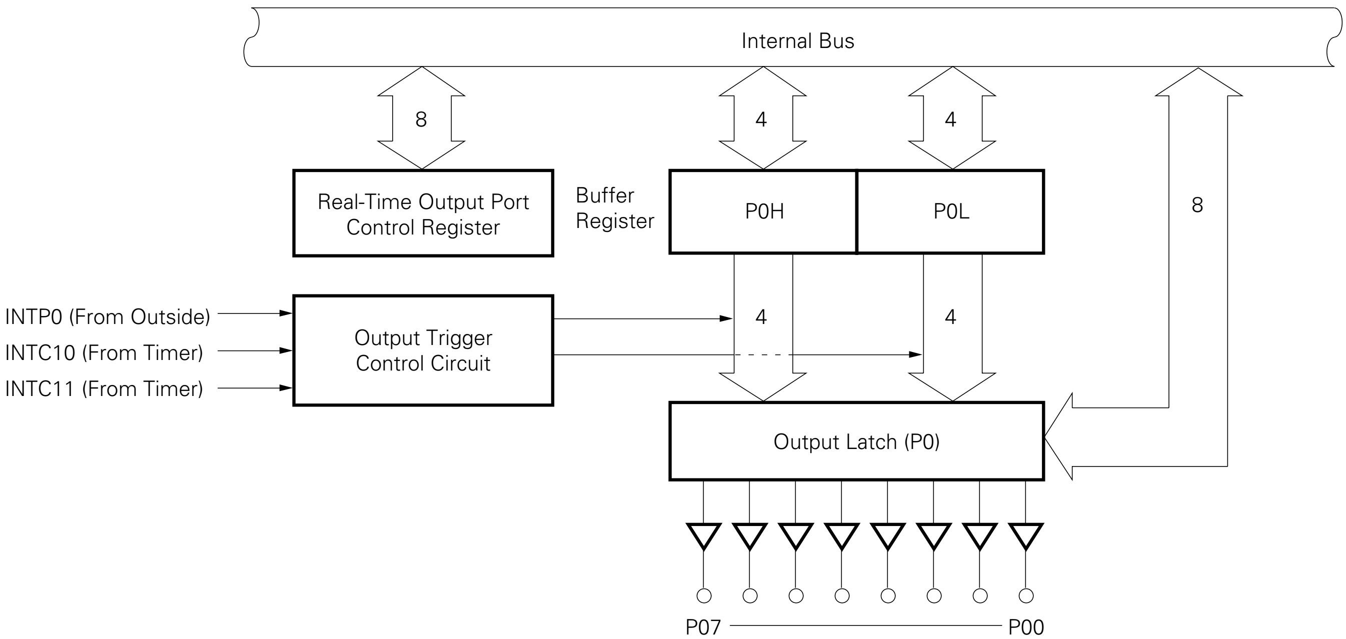
3.3 REAL-TIME OUTPUT PORT

The real-time output port outputs the data stored in the buffer in synchronization with timer match interrupts or external interrupts. A jitterless pulse output is obtained by means of this.

Therefore, it is most suitable for applications which output any pattern at any interval time. (Stepping motor open loop control, etc.)

Port 0 and the buffer register are the core elements of the configuration, as shown in Fig. 3-3.

Fig. 3-3 Real-Time Output Port Block Diagram



3.4 TIMER/COUNTER UNIT

The μPD78217A/78218A has a 16-bit timer/counter unit for 1 channel and 8-bit timer/counter units for 3 channels.

Table 3-2 Type and Function of Timer/Counter

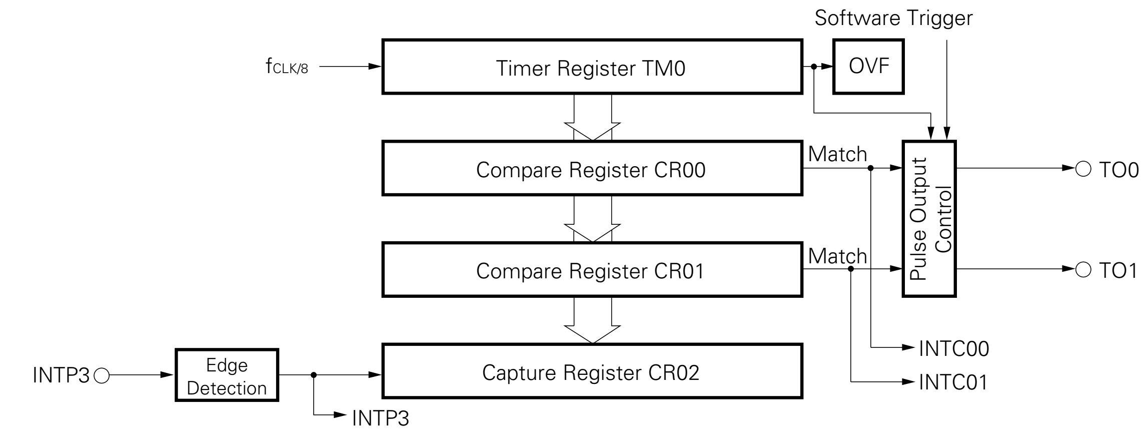
Type & Function \ Unit		16-Bit Timer/ Counter	8-Bit Timer/ Counter 1	8-Bit Timer/ Counter 2	8-Bit Timer/ Counter 3
Type	Interval timer	2 chs	2 chs	2 chs	1 ch
	External event counter	—	—	○	—
	One-shot timer	—	—	○	—
Function	Timer output	2 chs	—	2 chs	—
	Toggle output	○	—	○	—
	PWM/PPG output	○	—	○	—
	One-shot pulse output	○	—	—	—
	Real-time output	—	○	—	—
	Pulse amplitude measurement	○	○	○	—
	Number of interrupt requests	2	2	2	1
	Clock source of serial interface	—	—	—	○

Since 7 interrupt requests are supported in total, it can also function as timer for 7 channels.

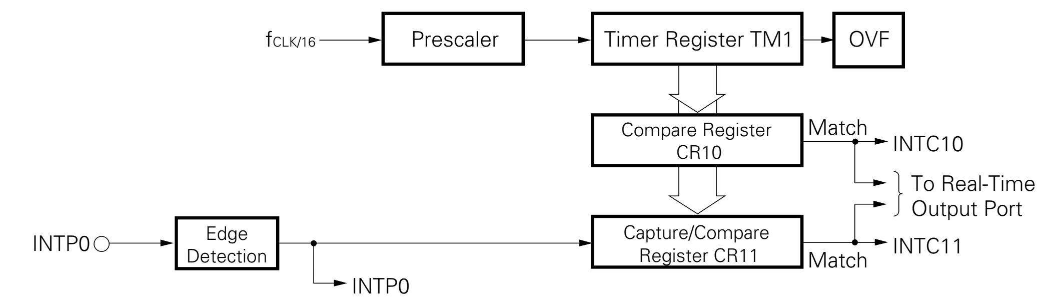
Remark The one-shot pulse output function activates the pulse output level by software, and inactivates it by hardware (interrupt request signal).
This function is different from the one-shot timer function of 8-bit timer/counter 2.

Fig. 3-4 Timer/Counter Unit Block Diagram

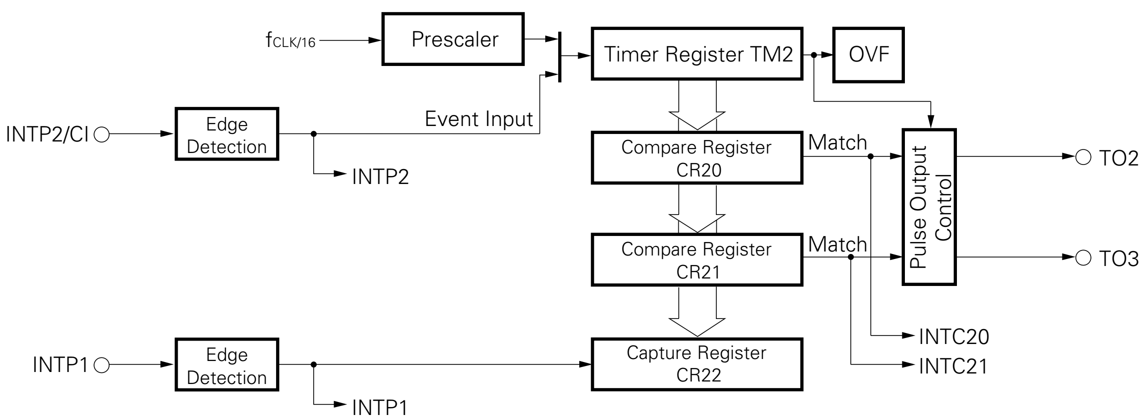
16-bit timer/counter unit



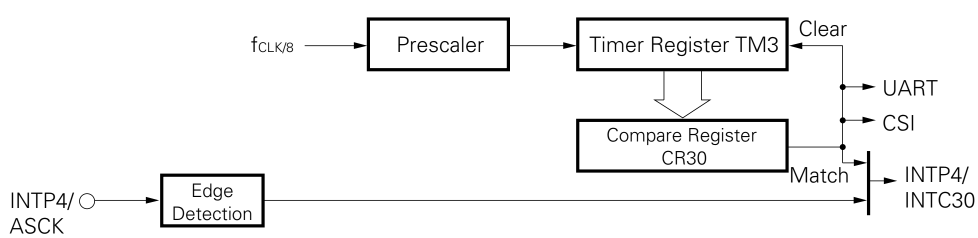
8-bit timer/counter unit 1



8-bit timer/counter unit 2



8-bit timer/counter unit 3



OVF: Overflow Flag

3.5 A/D CONVERTER

The μPD78217A/78218A incorporate the analog/digital (A/D) converter with 8-channel multiplexed analog input (AN0 to AN7).

The conversion method used is successive approximation. After the A/D conversion results are generated, they are held in the 8-bit A/D conversion result register (ADCR), which may allow high-speed and high-precision conversion (conversion time: Approx. 30 μs; at 12-MHz operation).

The following two modes are available for starting A/D conversion:

- Hardware start : Starts conversion by trigger input (INTP5)
- Software start : Starts conversion by the A/D converter mode register (ADM) bit setting

The following two modes of operation after starting are available:

- Scan mode : Multiple analog input are selected sequentially and conversion data is obtained from all pins.
- Select mode : The analog input is fixed at one pin and a continuous conversion value is obtained.

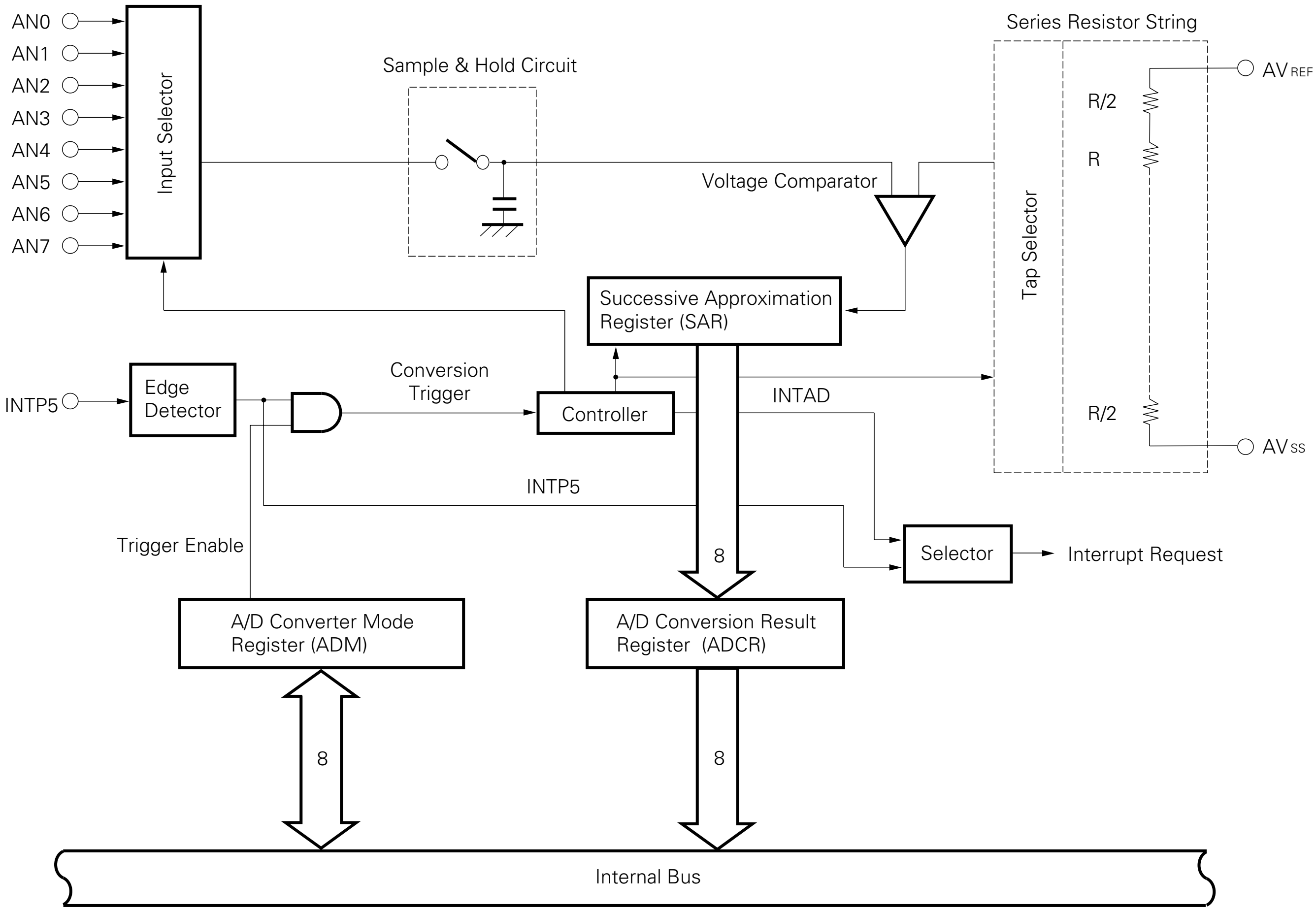
The above modes and the conversion operation are all stopped by ADM.

If the conversion result is transferred to the ADCR, an interrupt request INTAD is generated, (except in software start select mode). Therefore, the conversion value can be transferred to memory continuously using macro service (See section **4.1.3 "Macro Service"**).

Table 3-3 INTAD Generation Mode

	Scan Mode	Select Mode
Hardware start	○	○
Software start	○	—

Fig. 3-5 A/D Converter Block Diagram



3.6 SERIAL INTERFACE

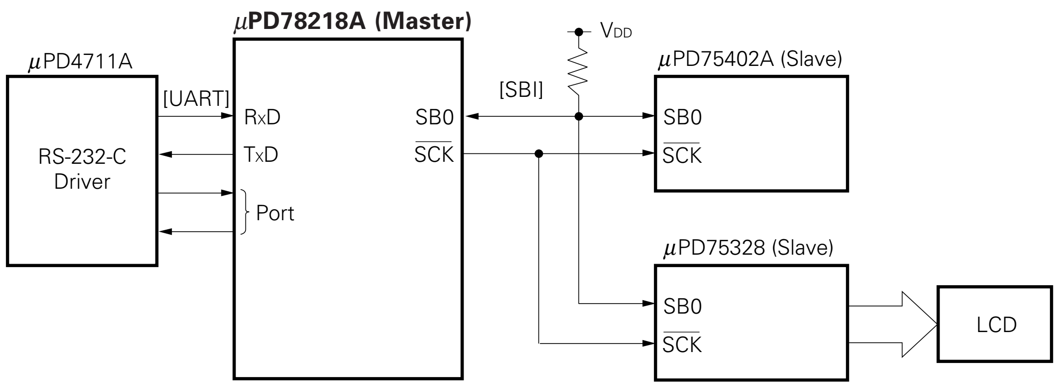
The μPD78217A/78218A has two independent serial interfaces.

- Asynchronous serial interface (UART)
- Clock synchronous serial interface (CSI)
  - 3-wire serial I/O
  - Serial bus interface (SBI)

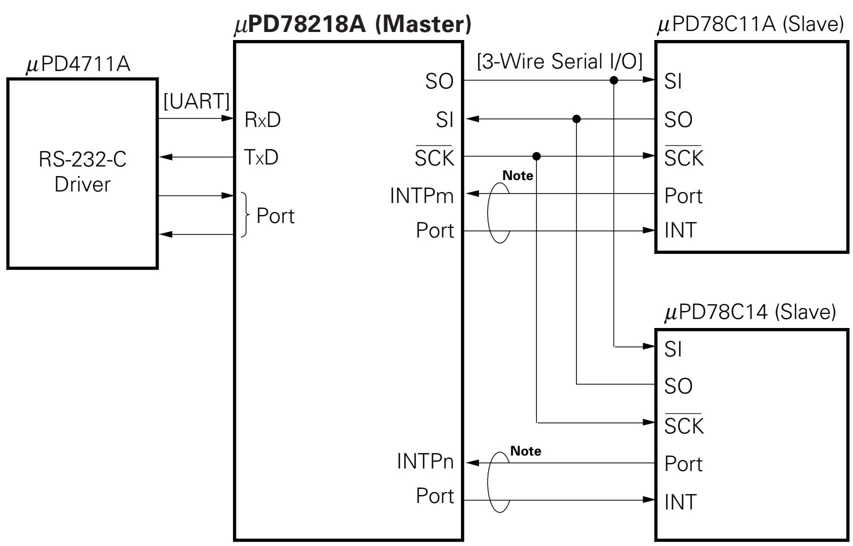
Therefore, communication with external devices and local communication inside the system can be performed simultaneously (See **Fig. 3-6**).

Fig. 3-6 Serial Interface Example

(a) UART + SBI



(b) UART + 3-wire serial I/O



Note Handshake Line

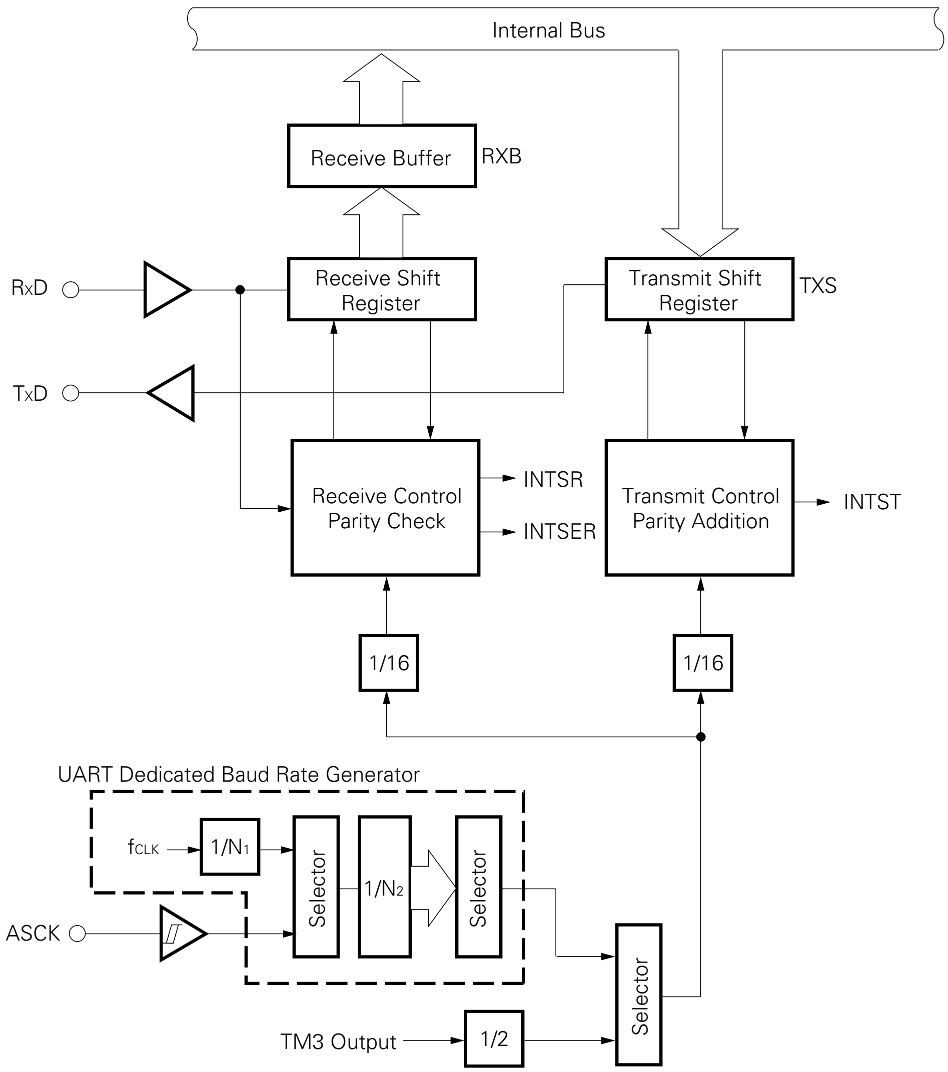
3.6.1 Asynchronous Serial Interface

The μPD78217A/78218A incorporates UART (Universal Asynchronous Receiver Transmitter) as the asynchronous serial interface. UART is used to send/receive one byte of data following a start bit.

The UART incorporates a dedicated baud rate generator which can generate a wide range of desired baud rates and also determine baud rates by scaling the ASCK pin input clocks or 8-bit timer/counter 3 output (TM3 output), allowing transmission/reception with a variety of baud rates.

If the UART dedicated baud rate generator is used, the MIDI standard baud rate (31.25 kbps) can also be obtained.

Fig. 3-7 Asynchronous Serial Interface (UART) Block Diagram

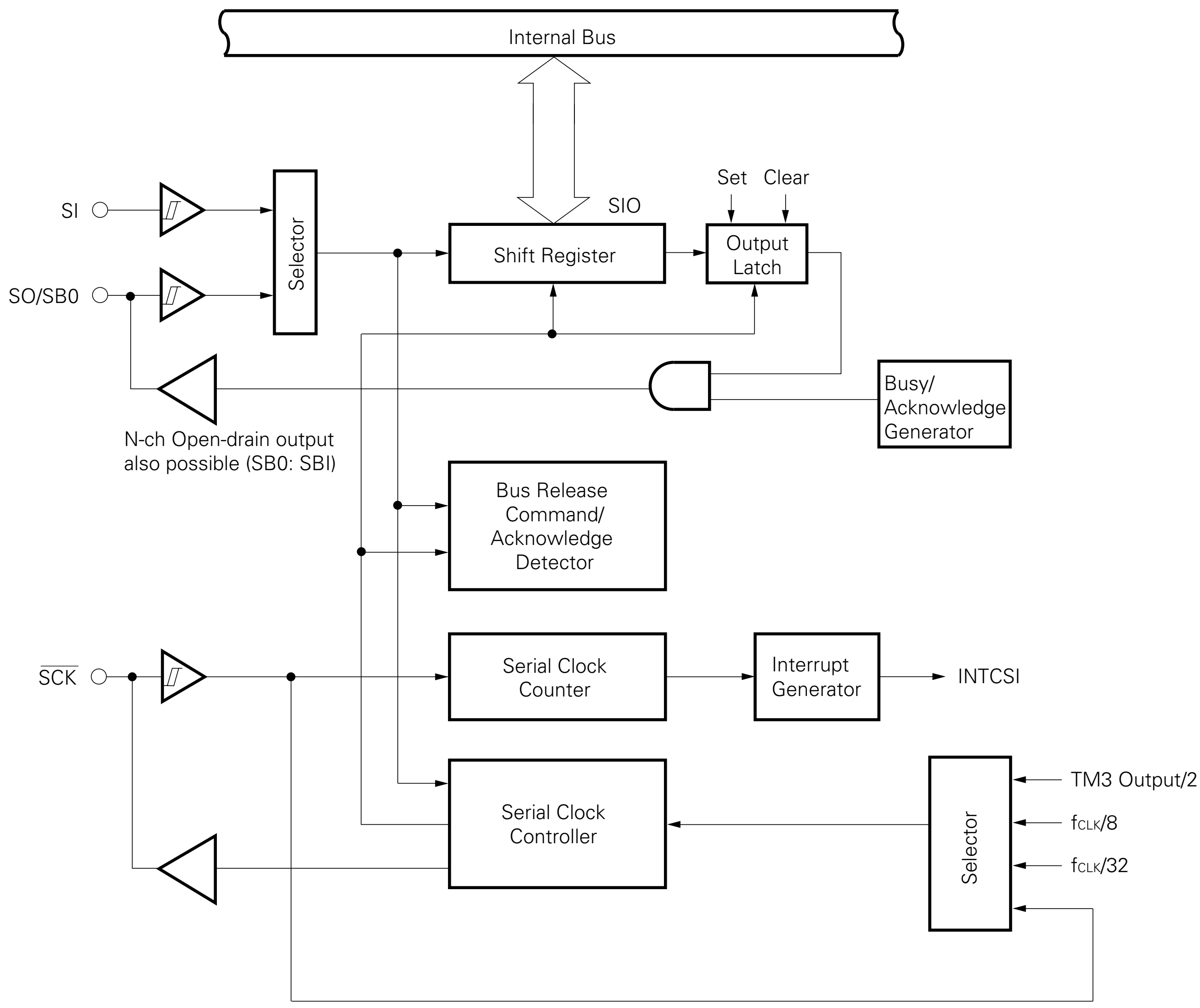


f_{CLK}: Internal system clock frequency (System Clock Frequency/2)

3.6.2 Clock Synchronous Serial Interface

The master device starts transmission by activating the serial clock and transfers one-byte data in synchronization with this clock.

Fig. 3-8 Clock Synchronous Serial Interface Block Diagram



f_{CLK}: Internal System Clock Frequency (System Clock Frequency/2)

(1) 3-wire serial I/O

This is an interface for communicating with devices incorporating a conventional clock synchronous serial interface.

Basically, communication is performed with three lines, one serial clock line ($\overline{SCK}$) and two serial data lines (SI, SO). When connecting to multiple devices, a handshake line is necessary.

(2) SBI

Communication with multiple devices is performed with one serial clock line ($\overline{SCK}$) and one serial bus line (SB0). This is NEC's standard serial interface.

The master device selects the slave device to be communicated with by outputting its "address" from the SB0 pin. Therefore, "commands" and "data" perform transfer and receive between the master and slave.

4. INTERNAL/EXTERNAL CONTROL FUNCTION

4.1 INTERRUPTS

Two interrupt request servicing methods can be selected, as shown in the following table.

Table 4-1 Interrupt Request Servicing

Service Mode	Servicing Subject	Service	PC, PSW Contents
Vectored interrupt	Software	Branches to service routine, and executes (any process contents)	With save and return
Macro service	Firmware	Data transfer, etc., between memory and I/O (fixed process contents)	Hold

4.1.1 Interrupt Sources

There are 19 types of interrupt sources and a BRK instruction execution, as shown in Table 4-2.

The priority of the interrupt servicing can be set to 2 levels (high and low priority levels). Therefore, the levels of nest control when the interrupt is in progress and when interrupt requests occur simultaneously (see **Fig. 4-1, Fig. 4-2**) can be separated. Nesting will always take place in the macro service (It won't be put on hold).

The default priority is the priority level (fixed) to service the interrupt requests which occur at the same level simultaneously (see **Fig. 4-2**).

Table 4-2 Interrupt Sources

Type	Default Priority	Source		Internal/ External	Macro Service
		Name	Trigger		
Software	—	BRK	Instruction execution	—	—
Non-maskable		NMI	Pin input edge detection	External	
Maskable	0 (highest)	INTP0	Pin input edge detection (TM1 capture trigger)		○
	1	INTP1	Pin input edge detection (TM2 capture trigger)		
	2	INTP2	Pin input edge detection (TM2 event counter input)		
	3	INTP3	Pin input edge detection (TM0 capture trigger)		
	4	INTC00	TM0 to CR00 match signal generation	Internal	
	5	INTC01	TM0 to CR01 match signal generation		
	6	INTC10	TM1 to CR10 match signal generation		
	7	INTC11	TM1 to CR11 match signal generation		
	8	INTC21	TM2 to CR21 match signal generation		
	9	INTP4	Pin input edge detection	External	
		INTC30	TM3 to CR30 match signal generation	Internal	
	10	INTP5	Pin input edge detection	External	
		INTAD	A/D converter conversion termination (transfer to ADCR)	Internal	
	11	INTC20	TM2 to CR20 match signal generation		
	12	INTSER	ASI receive error generation		—
	13	INTSR	ASI receive termination		○
	14	INTST	ASI transmit termination		
	15 (lowest)	INTCSI	CSI transfer termination		

TM0 : 16-bit timer
TM1 to TM3 : 8-bit timer
ASI : Asynchronous serial interface
CSI : Clock synchronous serial interface

Fig. 4-1 Servicing Example when an Interrupt Request Occurrence is Issued while an Interrupt is Serviced

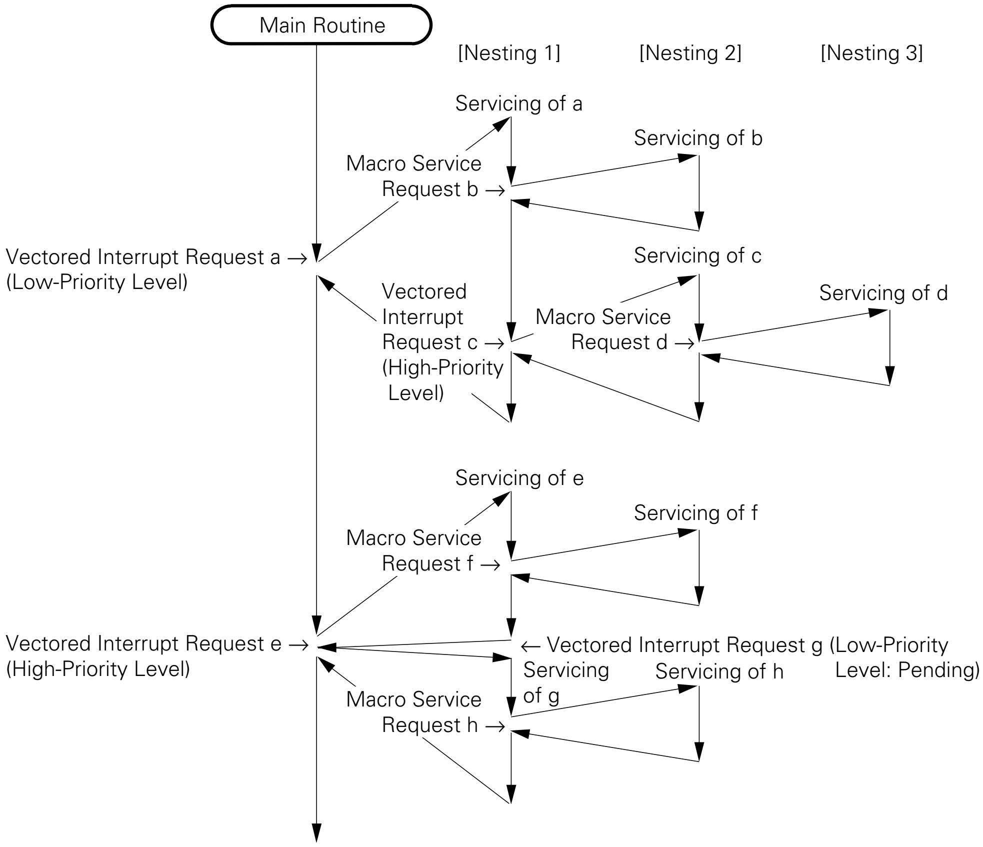
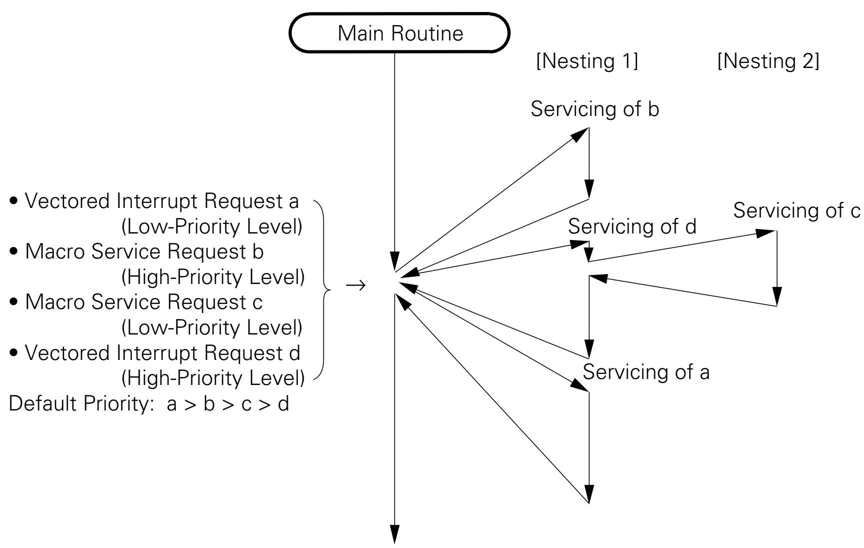


Fig. 4-2 Servicing Example of Simultaneous Interrupt Requests



4.1.2 Vectored Interrupt

The memory contents of the vector table address, which corresponds to the interrupt source, is branched into the service routine as a destination address.

As the CPU executes the interrupt servicing, the following operations occur.

- When branch : Saving the CPU status (PC, PSW contents) to the stack.
- When return : Returning the CPU status (PC, PSW contents) from the stack.

The RETI instruction executes returning to the main routine from the service routine.

Table 4-3 Vector Table Address

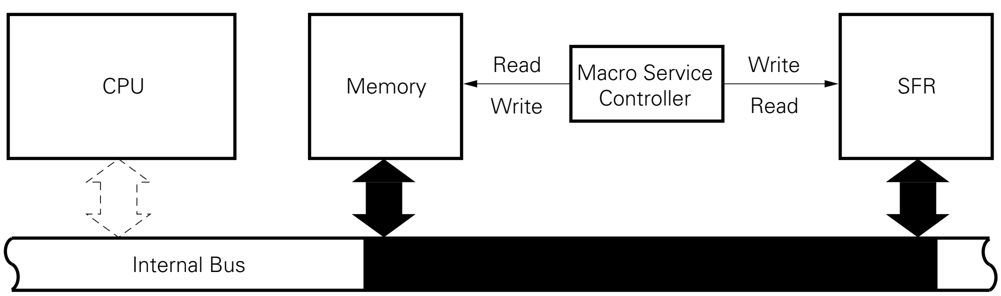
Interrupt Source	Vector Table Address	Interrupt Source	Vector Table Address
BRK	003EH	INTC21	001CH
NMI	0002H	INTP4	000EH
INTP0	0006H	INTC30	
INTP1	0008H	INTP5	0010H
INTP2	000AH	INTAD	
INTP3	000CH	INTC20	0012H
INTC00	0014H	INTSER	0020H
INTC01	0016H	INTSR	0022H
INTC10	0018H	INTST	0024H
INTC11	001AH	INTCSI	0026H

4.1.3 Macro Service

This is a function to transfer data between the memory and special function registers (SFR) without going through the CPU. The macro service controller accesses the memory and SFR, and transfers data directly without fetching it.

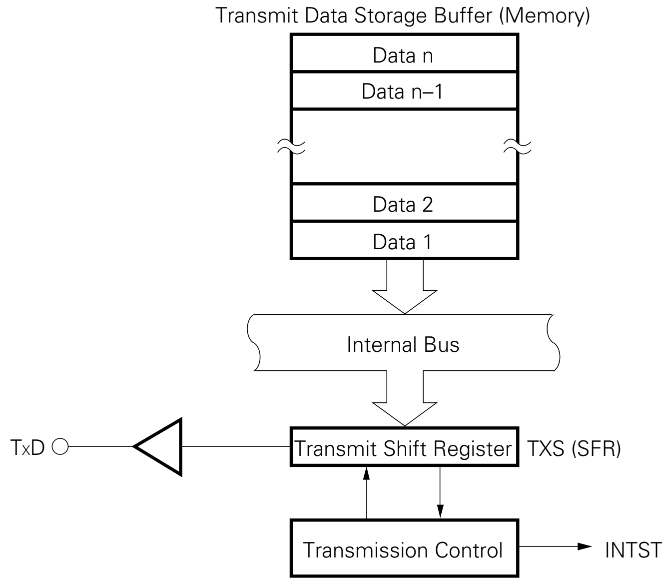
High-speed data transfer is enabled because no data is saved, restored or fetched.

Fig. 4-3 Macro Service



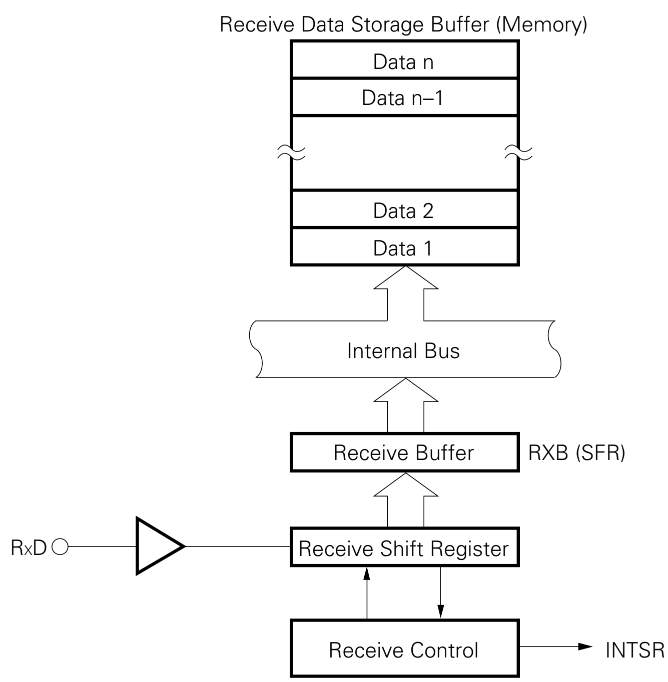
4.1.4 Macro Service Application Examples

(1) Transmit operation of serial interface



Whenever the macro service request INTST is generated, the next transmit data is transferred to TXS from the memory. When the data n (last byte) is transferred to TXS (the transmit data storage buffer becomes empty), a vectored interrupt request INTST is generated.

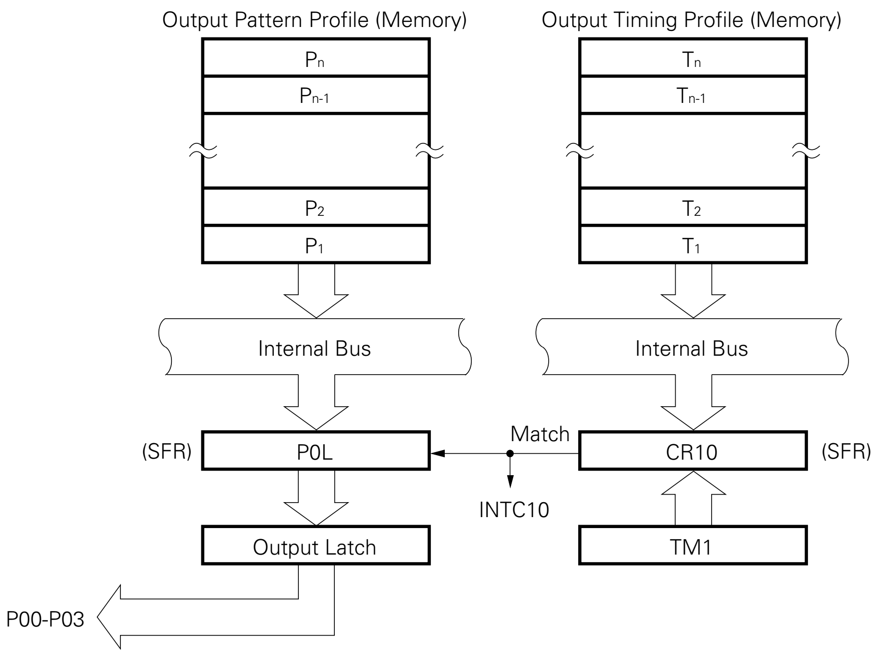
(2) Receive operation of serial interface



Whenever the macro service request INTSR is generated, the receive data is transferred to the memory from RXB. When the data n (last byte) is transferred to the memory (the receive data storage buffer becomes empty), the vectored interrupt request INTSR is generated.

(3) Real-time output port

The INTC10 and INTC11 become output triggers of the real-time output port. In the macro service for them, the next output pattern and interval can be set simultaneously. Therefore, the INTC10 and INTC11 can control 2 system stepping motor independently. Also, they can be applied to control a PWM or DC motor, etc.



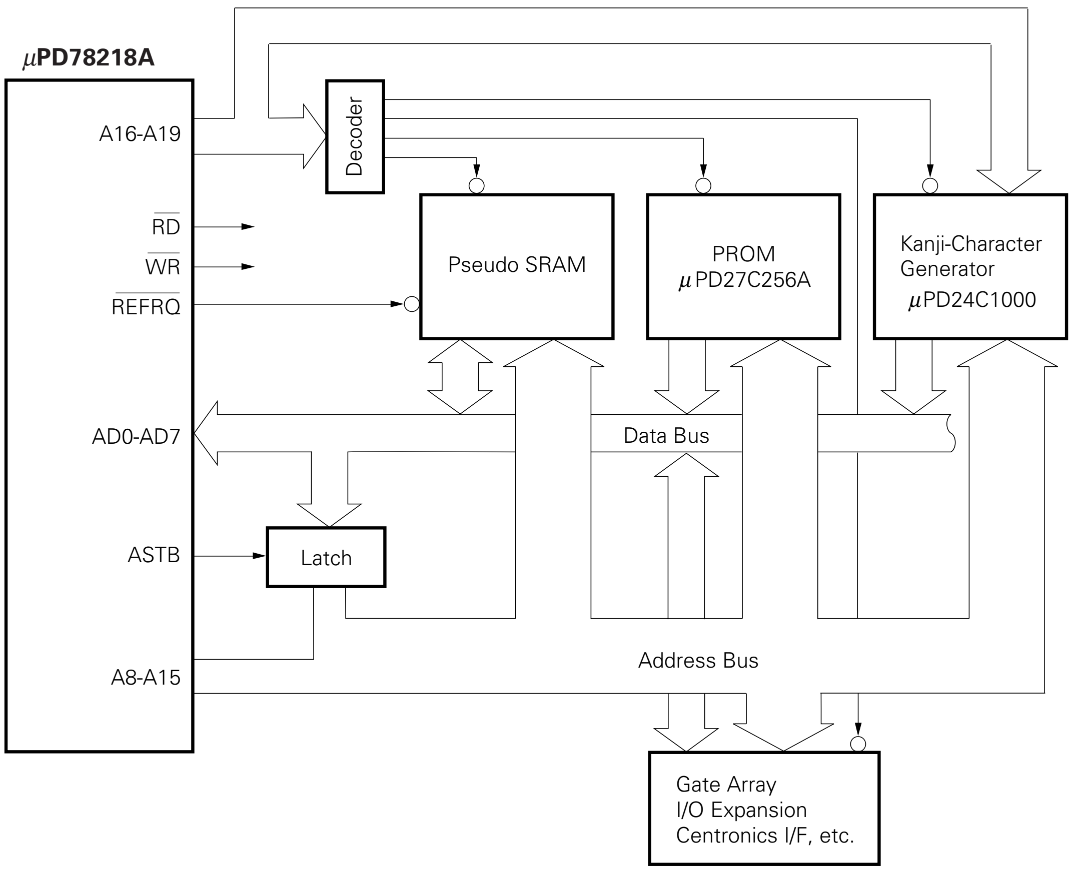
Whenever the macro service request INTC10 is generated, the pattern and timing are transferred to P0L and CR10, respectively. When the contents of the TM1 match with the contents of the CR10, the next INTC10 is generated and the contents of the P0L are sent to the output latch. If T_n (last byte) is sent to CR10, a vectored interrupt request INTC10 is generated.

The same operation is available for INTC11 (differences: CR10 → CR11, P0L → P0H, P00-P03 → P04-P07).

4.2 LOCAL BUS INTERFACE

The μPD78217A/78218A can be connected to an external memory and I/O (memory mapped I/O), and supports the 1M-byte memory space (see **Fig.3-1**).

Fig. 4-4 Local Bus Interface Example



4.2.1 Memory Expansion

The following modes have been prepared as a memory expansion function.

- External memory expansion mode : Expands the program memory and data memory to 31488 bytes (64256 bytes for the μPD78217A) externally. However, this area can be used unconditionally under the ROM-less mode ($\overline{EA}$ = L).
- 1-Mbyte expansion mode : Expands the data memory by 960 Kbytes and become a 1-Mbyte memory space.

4.2.2 Programmable Wait

A wait can be independently inserted to the memory mapped on both a normal address (00000H to 0FFFFH) and an expanded address (10000H to FFFFFH). Therefore, the efficiency of the entire system is not decreased.

4.2.3 Pseudo-Static RAM Refresh Function

The refresh operations are as follows.

- Pulse refresh : Outputs the refresh pulse to $\overline{REFRQ}$ pin in synchronization with a bus cycle.
- Power-down self refresh : Outputs a low-level to the $\overline{REFRQ}$ pin in the standby mode and holds the contents of the pseudo-static RAM.

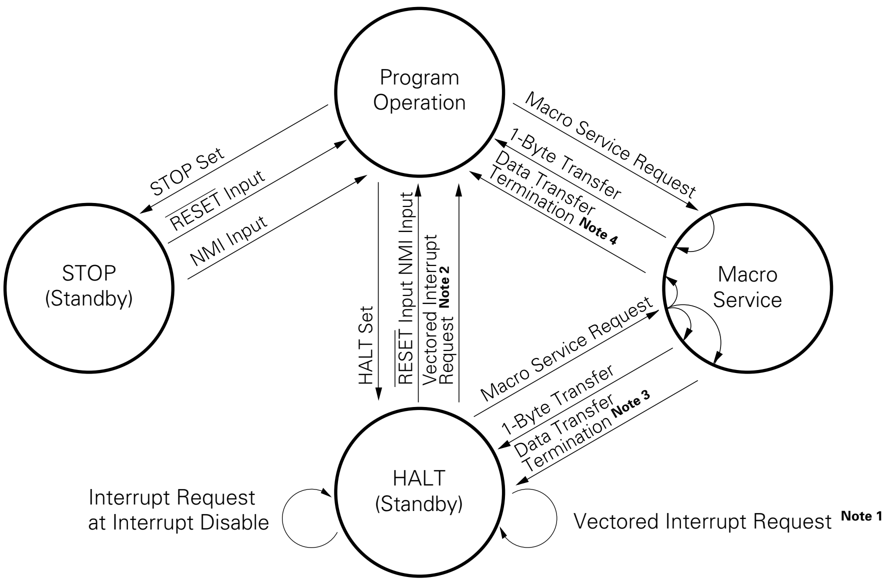
4.3 STANDBY

This is a function to reduce the power consumption of the chip. The following modes are available.

- HALT mode : Stops the operation clock of the CPU. The average power consumption is reduced by switching from normal mode to HALT mode and vice-versa.
- STOP mode : Stops the oscillator. This stops all operation in the chip and enables minute power consumption consisting only of leakage current.

These modes are programmable.
The macro service is started from the HALT mode.

Fig. 4-5 Standby Status Flow



Notes
1. In case a vectored interrupt request is a low-priority level (status to disable interrupt of a low-priority sequence under the HALT setting).
2. In case a vectored interrupt request is a high-priority level or in case of the status to enable interrupt of a low-priority sequence under the HALT setting.
3. In case a macro service is a high-priority level (status to disable interrupt of a low-priority sequence under the HALT setting).
4. In case a macro service is a high-priority level or in case of the status to enable interrupt of a low-priority sequence under the HALT setting.

4.4 RESET

When a low level is input to the RESET pin, the internal hardware is initialized (reset state).

When the RESET input changes from low level to high level, the following data is set in the program counter (PC).

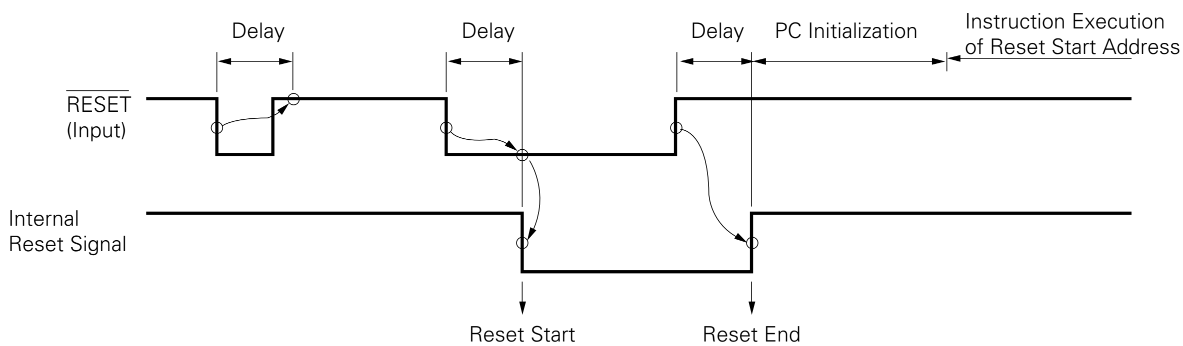
- Lower 8 bits of PC : Contents of 0000H address
- Upper 8 bits of PC : Contents of 0001H address

The contents of the PC set the destination address and the program starts to be executed from the address. Therefore, it can start from any address by reset start.

Please set the program for the contents of each register as required.

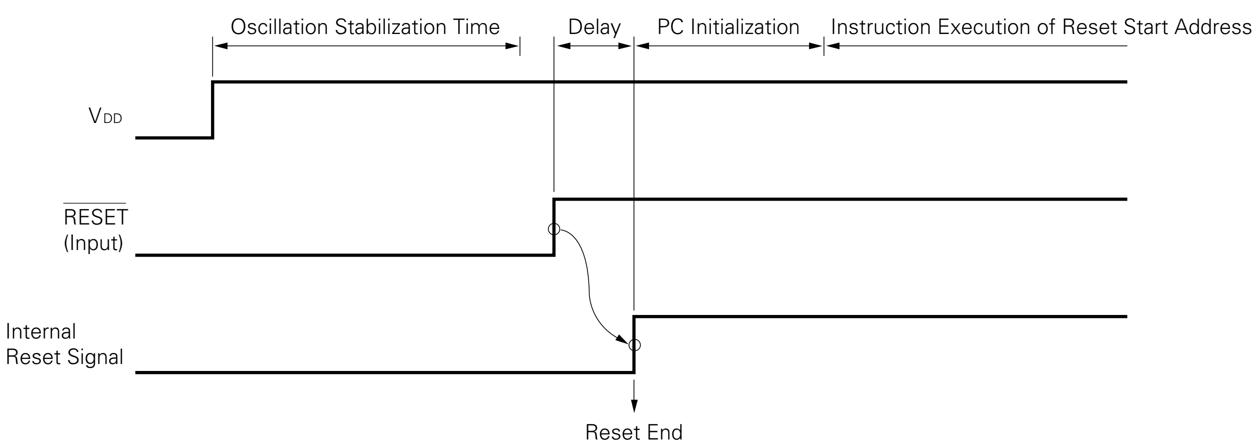
A noise eliminator has been incorporated in the RESET input circuit to prevent any error from noise. This noise eliminator is a sampling circuit based on analog delay.

Fig. 4-6 Reset Acknowledge



Set the RESET signal active in the reset operation at power-on until the oscillation stabilization time (approx. 40 ms) elapses.

Fig. 4-7 Reset Operation at Power-On



5. INSTRUCTION SET

(1) 8-bit instructions

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, SHR, SHL, ROR4, ROL4, DBNZ, PUSH, POP

Table 5-1 Instructions Classified by 8-Bit Addressing Mode

1st Operand \ 2nd Operand	#byte	A	r r'	saddr saddr'	sfr	mem	&mem	!addr16	&!addr16	PSW	n	None[Note2]
A	ADD[Note1]		MOV XCH	MOV XCH ADD[Note1]	MOV XCH ADD[Note1]	MOV XCH ADD[Note1]	MOV XCH ADD[Note1]	MOV	MOV	MOV		
r	MOV		MOV XCH ADD[Note1]								ROL ROLC ROR RORC SHR SHL	MULU DIVUW INC DEC
r1												DBNZ
saddr	MOV ADD[Note1]	MOV		MOV XCH ADD[Note1]								INC DBNZ DEC
sfr	MOV ADD[Note1]	MOV										PUSH POP
mem & mem		MOV										
mem1 &mem1												ROR4 ROL4
!addr16		MOV										
&!addr16		MOV										
PSW	MOV	MOV										PUSH POP
STBC	MOV											

Notes 1. ADDC, SUB, SUBC, AND, OR, XOR and CMP are the same as ADD.

2. There is no 2nd operand, or the 2nd operand is not an operand address.

(2) 16-bit instructions

MOVW, ADDW, SUBW, CMPW, INCW, DECW, SHRW, SHLW, PUSH, POP

Table 5-2 Instructions Classified by 16-Bit Addressing Mode

2nd Operand / 1st Operand	#word	AX	rp rp'	saddrp	sfrp	mem1	&mem1	SP	n	None
AX	ADDW SUBW CMPW		ADDW SUBW CMPW	MOVW ADDW SUBW CMPW	MOVW ADDW SUBW CMPW	MOVW	MOVW	MOVW		
rp	MOVW		MOVW						SHLW SHRW	INCW DECW PUSH POP
saddrp	MOVW	MOVW								
sfrp	MOVW	MOVW								
mem1 &mem1		MOVW								
SP	MOVW	MOVW								INCW DECW

(3) Bit manipulation instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

Table 5-3 Instructions Classified by Bit Manipulation Instruction Addressing Mode

1st Operand \ 2nd Operand	CY	A.bit	/A.bit	X.bit	/X.bit	saddr.bit	/saddr.bit	sfr.bit	/sfr.bit	PSW.bit	/PSW.bit	None[Note]
CY		MOV1 AND1 OR1 XOR1	AND1 OR1	MOV1 AND1 OR1 XOR1	AND1 OR1	MOV1 AND1 OR1 XOR1	AND1 OR1	MOV1 AND1 OR1 XOR1	AND1 OR1	MOV1 AND1 OR1 XOR1	AND1 OR1	SET1 CLR1 NOT1
A.bit	MOV1											SET1 CLR1 NOT1 BT BF BTCLR
X.bit	MOV1											SET1 CLR1 NOT1 BT BF BTCLR
saddr.bit	MOV1											SET1 CLR1 NOT1 BT BF BTCLR
sfr.bit	MOV1											SET1 CLR1 NOT1 BT BF BTCLR
PSW.bit	MOV1											SET1 CLR1 NOT1 BT BF BTCLR

Note There is no 2nd operand, or the 2nd operand is not an operand address.

(4) Call/branch instructions

CALL, CALLF, CALLT, BR, BC, BT, BF, BTCLR, DBNZ, BL, BNC, BNL, BZ, BE, BNZ, BNE

Table 5-4 Instructions Classified by Call/Branch Instruction Addressing Mode

Operands of Instruction Address	$addr16	!addr16	rp	!addr11	[addr5]
Basic instructions	BR BC[Note]	CALL BR	CALL BR	CALLF	CALLT
Compound instructions	BT BF BTCLR DBNZ				

Note BL, BNC, BNL, BZ, BE, BNZ and BNE are the same as BC.

(5) Other instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, NOP, EI, DI, SEL

6. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

PARAMETER	SYMBOL	TEST CONDITIONS	RATING	UNIT
Supply voltage	V_{DD}		–0.5 to +7.0	V
	AV_{REF}		–0.5 to V_{DD} +0.5	V
	AV_{SS}		–0.5 to +0.5	V
Input voltage	V_{I1}		–0.5 to V_{DD} +0.5	V
	V_{I2}	**Note**	–0.5 to AV_{REF} +0.5	V
Output voltage	V_O		–0.5 to V_{DD} +0.5	V
Output current, low	I_{OL}	Per pin	15	mA
		All output pins	100	mA
Output current, high	I_{OH}	Per pin	–10	mA
		All output pins	–50	mA
★ Operating ambient temperature	T_A		–40 to +85	°C
Storage temperature	T_{stg}		–65 to +150	°C

Note P70/AN0 to P75/AN5, P66/$\overline{\text{WAIT}}$/AN6, P67/$\overline{\text{REFRQ}}$/AN7 pins are used as A/D converter input pins. However, V_{I1} absolute maximum ratings should also be satisfied.

Caution Product quality may suffer if the absolute maximum rating is exceeded for even a single parameter even momentarily. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute maximum ratings are not exceeded.

OPERATING CONDITIONS

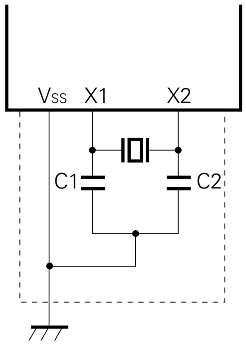
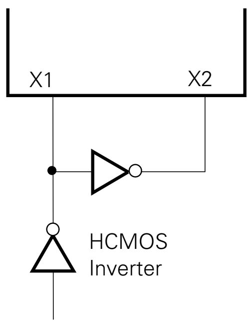
★

CLOCK FREQUENCY	OPERATING AMBIENT TEMPERATURE (T_A)	SUPPLY VOLTAGE (V_{DD})
4 MHz ≤ f_{XX} ≤ 12 MHz	–40 to +85 °C	+5 V ± 10 %

CAPACITANCE (T_A = 25 °C, V_{DD} = V_{SS} = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_I	f = 1 MHz unmeasured pins returned to 0 V.			20	pF
Output capacitance	C_O				20	pF
I/O capacitance	C_{IO}				20	pF

OSCILLATOR CHARACTERISTICS (T_A= –40 to +85 °C, V_{DD} = +5 V ±10 %, V_{SS} = 0 V)

RESONATOR	RECOMMENDED CIRCUIT	PARAMETER	MIN.	MAX.	UNIT
Ceramic resonator or crystal resonator		Oscillator frequency (f_{XX})	4	12	MHz
External clock		X1 input frequency (f_X)	4	12	MHz
		X1 input rising/falling time (t_{XR} , t_{XF})	0	30	ns
		X1 input high/low level width (t_{WXH} , t_{WXL})	30	130	ns

Caution When using the clock oscillator, wiring in the area enclosed with the dotted line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- **Wiring should be as short as possible.**
- **Wiring should not cross other signal lines.**
- **Wiring should not be placed close to a varying high current.**
- **The potential of the oscillator capacitor ground should be the same as V_{SS}. Do not ground it to a ground pattern in which a high current flows.**
- **Do not fetch a signal from the oscillator.**

RECOMMENDED OSCILLATOR CONSTANTS

CERAMIC RESONATOR

MANUFACTURER	FREQUENCY [MHz]	PART NUMBER	RECOMMENDED CONSTANTS	
			C1 [pF]	C2 [pF]
Murata Mfg.	12	CSA12.0MTZ	30	30
		CST12.0MTW	Capacitor on-chip type	
Matsushita Electronics Parts	12	EFOGC1205C4[Note]	Capacitor on-chip type	
		EFOEC1205C4		
★		EFOEN1205C4	33	33
★ TDK Co.	12	FCR12.0M2S	33	33
		FCR12.0MC	Capacitor on-chip type	

Note Production discontinued.

DC CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = +5 V ±10 %, V_{SS} = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input voltage, low	V_{IL}		0		0.8	V
Input voltage, high	V_{IH1}	Pins except for **Note 1** and **Note 2**	2.2		V_{DD}	V
	V_{IH2}	Pin of **Note 1**	2.2		AV_{REF}	V
	V_{IH3}	Pin of **Note 2**	0.8 V_{DD}		V_{DD}	V
Output voltage, low	V_{OL1}	I_{OL} = 2.0 mA			0.45	V
	V_{OL2}	I_{OL} = 8.0 mA Note3			1.0	V
Output voltage, high	V_{OH1}	I_{OH} = –1.0 mA	V_{DD}–1.0			V
	V_{OH2}	I_{OH} = –100 μA	V_{DD}–0.5			V
	V_{OH3}	I_{OH} = –5.0 mA Note4	2.0			V
X1 input current, low	I_{IL}	0 V ≤ V_I ≤ V_{IL}			–100	μA
X1 input current, high	I_{IH}	V_{IH3} ≤ V_I ≤ V_{DD}			100	μA
Input leakage current	I_{LI}	0 V ≤ V_I ≤ V_{DD}			±10	μA
Output leakage current	I_{LO}	0 V ≤ V_O ≤ V_{DD}			±10	μA
AV_{REF} current	AI_{REF}	Operating mode f_{XX} = 12 MHz		1.5	5.0	mA
V_{DD} supply current	I_{DD1}	Operating mode f_{XX} = 12 MHz		20	40	mA
	I_{DD2}	HALT mode f_{XX} = 12 MHz		7	20	mA
Data retention voltage	V_{DDDR}	STOP mode	2.5		5.5	V
Data retention current	I_{DDDR}	STOP mode, V_{DDDR} = 2.5 V		2	20	μA
		STOP mode, V_{DDDR} = 5 V ±10 %		5	50	μA
Pull-up resistor	R_L	V_I = 0 V	15	40	80	kΩ

Notes 1. P70/AN0 to P75/AN5, P66/$\overline{\text{WAIT}}$/AN6, P67/$\overline{\text{REFRQ}}$/AN7 pins are used as A/D converter input pins.
2. X1, X2, $\overline{\text{RESET}}$, P20/NMI, P21/INTP0, P22/INTP1, P23/INTP2/CI, P24/INTP3, P25/INTP4/ASCK, P26/INTP5, P27/SI, P32/$\overline{\text{SCK}}$, P33/SO/SB0, $\overline{\text{EA}}$ pins
3. P40/AD0 to P47/AD7, P50/A8 to P57/A15 pins
4. P00 to P07 pins

AC CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = +5 V ±10 %, V_{SS} = 0 V)

READ/WRITE OPERATION (1/2)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
X1 input clock cycle time	t_{CYX}		82	250	ns
Address setup time (to ASTB↓)	t_{SAST} •		52		ns
Address hold time (from ASTB↓)[Note]	t_{HSTA}		25		ns
Address hold time (from $\overline{\text{RD}}$↑)	t_{HRA}		30		ns
Address hold time (from $\overline{\text{WR}}$↑)	t_{HWA}		30		ns
$\overline{\text{RD}}$↓ delay time from address	t_{DAR} •		129		ns
Address float time (from $\overline{\text{RD}}$↓)	t_{FAR} •		11		ns
Data input time from address	t_{DAID} •	No. of waits = 0		228	ns
Data input time from ASTB↓	t_{DSTID} •	No. of waits = 0		181	ns
Data input time from $\overline{\text{RD}}$↓	t_{DRID} •	No. of waits = 0		100	ns
$\overline{\text{RD}}$↓ delay time from ASTB↓	t_{DSTR} •		52		ns
Data hold time (from $\overline{\text{RD}}$↑)	t_{HRID}		0		ns
Address active time from $\overline{\text{RD}}$↑	t_{DRA} •		124		ns
ASTB↑ delay time from $\overline{\text{RD}}$↑	t_{DRST} •		124		ns
$\overline{\text{RD}}$ low-level width	t_{WRL} •	No. of waits = 0	124		ns
ASTB high-level width	t_{WSTH} •		52		ns
$\overline{\text{WR}}$↓ delay time from address	t_{DAW} •		129		ns
Data output time from ASTB↓	t_{DSTOD} •			142	ns
Data output time from $\overline{\text{WR}}$↓	t_{DWOD}			60	ns
$\overline{\text{WR}}$↓ delay time from ASTB↓	t_{DSTW1} •	Refreshing disabled	52		ns
	t_{DSTW2} •	Refreshing enabled	129		ns
Data setup time (to $\overline{\text{WR}}$↑)	t_{SODWR} •	No. of waits = 0	146		ns
Data setup time (to $\overline{\text{WR}}$↓)	t_{SODWF} •	Refreshing enabled	22		ns
Data hold time (from $\overline{\text{WR}}$↑)[Note]	t_{HWOD}		20		ns
ASTB↑ delay time from $\overline{\text{WR}}$↑	t_{DWST} •		42		ns
$\overline{\text{WR}}$ low-level width	t_{WWL1} •	Refreshing disabled No. of waits = 0	196		ns
	t_{WWL2} •	Refreshing enabled No. of waits = 0	114		ns
$\overline{\text{WAIT}}$↓ input time from address	t_{DAWT} •			146	ns
$\overline{\text{WAIT}}$↓ input time from ASTB↓	t_{DSTWT} •			84	ns

Note The hold time includes the time to hold the V_{OH} and V_{OL} under the load conditions of C_L = 100 pF and R_L = 2 kΩ.

Remarks
1. The values in the above table are based on "f_{XX} = 12 MHz and C_L = 100 pF".
2. For a parameter with a dot (•) in the SYMBOL column, refer to "**t_{CYX} DEPENDENT BUS TIMING DEFINITION**" as well.

READ/WRITE OPERATION (2/2)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
$\overline{\text{WAIT}}$ hold time from ASTB↓		t_{HSTWT} •	No. of external waits = 1	174		ns
$\overline{\text{WAIT}}$↑ delay time from ASTB↓		t_{DSTWTH} •	No. of external waits = 1		273	ns
$\overline{\text{WAIT}}$↓ input time from $\overline{\text{RD}}$↓		t_{DRWTL} •			22	ns
$\overline{\text{WAIT}}$ hold time from $\overline{\text{RD}}$↓		t_{HRWT} •	No. of external waits = 1	87		ns
$\overline{\text{WAIT}}$↑ delay time from $\overline{\text{RD}}$↓		t_{DRWTH} •	No. of external waits = 1		186	ns
Data input time from $\overline{\text{WAIT}}$↑		t_{DWTID} •			62	ns
$\overline{\text{WR}}$↑ delay time from $\overline{\text{WAIT}}$↑		t_{DWTW} •		154		ns
$\overline{\text{RD}}$↑ delay time from $\overline{\text{WAIT}}$↑		t_{DWTR} •		72		ns
$\overline{\text{WAIT}}$ input time from $\overline{\text{WR}}$↓ (At refresh disabled)		t_{DWWTL} •			22	ns
$\overline{\text{WAIT}}$ hold time from $\overline{\text{WR}}$↓	Refresh disabled	t_{HWWT1} •	No. of external waits = 1	87		ns
	Refresh enabled	t_{HWWT2} •	No. of external waits = 1	5		ns
$\overline{\text{WAIT}}$↑ delay time from $\overline{\text{WR}}$↓	Refresh disabled	t_{DWWTH1} •	No. of external waits = 1		186	ns
	Refresh enabled	t_{DWWTH2} •	No. of external waits = 1		104	ns
$\overline{\text{REFRQ}}$↓ delay time from $\overline{\text{RD}}$↑		t_{DRRFQ} •		154		ns
$\overline{\text{REFRQ}}$↓ delay time from $\overline{\text{WR}}$↑		t_{DWRFQ} •		72		ns
$\overline{\text{REFRQ}}$ low-level width		t_{WRFQL} •		120		ns
ASTB↑ delay time from $\overline{\text{REFRQ}}$↑		t_{DRFQST} •		280		ns

Remarks 1. The values in the above table are based on "f_{XX} = 12 MHz and C_L = 100 pF".

2. For a parameter with a dot (•) in the SYMBOL column, refer to "**t_{CYX} DEPENDENT BUS TIMING DEFINITION**" as well.

SERIAL OPERATION

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	MAX.	UNIT
Serial clock cycle time	t_{CYSK}	Input	External clock	1.0		μs
		Output	Internal divided by 16	1.3		μs
			Internal divided by 64	5.3		μs
Serial clock low-level width	t_{WSKL}	Input	External clock	420		ns
		Output	Internal divided by 16	556		ns
			Internal divided by 64	2.5		μs
Serial clock high-level width	t_{WSKH}	Input	External clock	420		ns
		Output	Internal divided by 16	556		ns
			Internal divided by 64	2.5		μs
SI, SB0 setup time (to $\overline{SCK}$↑)	t_{SSSK}			150		ns
SI, SB0 hold time (from $\overline{SCK}$↑)	t_{HSSK}			400		ns
SO/SB0 output delay time (from $\overline{SCK}$↓)	t_{DSBSK1}	CMOS push-pull output (3-wire serial I/O mode)		0	300	ns
	t_{DSBSK2}	Open-drain output (SBI mode), R_L = 1 kΩ		0	800	ns
SB0 high hold time (from $\overline{SCK}$↑)	t_{HSBSK}	SBI mode		4		t_{CYX}
SB0 low setup time (to $\overline{SCK}$↓)	t_{SSBSK}			4		t_{CYX}
SB0 low-level width	t_{WSBL}			4		t_{CYX}
SB0 high-level width	t_{WSBH}			4		t_{CYX}

Remark The values in the above table are based on "f_{XX} = 12 MHz and C_L = 100 pF".

OTHER OPERATIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
NMI low-level width	t_{WNIL}		10		μs
NMI high-level width	t_{WNIH}		10		μs
INTP0 to INTP5 low-level width	t_{WITL}		24		t_{CYX}
INTP0 to INTP5 high-level width	t_{WITH}		24		t_{CYX}
$\overline{\text{RESET}}$ low-level width	t_{WRSL}		10		μs
$\overline{\text{RESET}}$ high-level width	t_{WRSH}		10		μs

EXTERNAL CLOCK TIMING

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
X1 input low-level width	t_{WXL}		30	130	ns
X1 input high-level width	t_{WXH}		30	130	ns
X1 input rise time	t_{XR}		0	30	ns
X1 input fall time	t_{XF}		0	30	ns
X1 input clock cycle time	t_{CYX}		82	250	ns

A/D CONVERTER CHRACTERISTICS (T_A = –40 to +85 °C, V_{DD} = +5 V ±10 %, V_{SS} = AV_{SS} = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Resolution			8			bit
Overall error[Note1]		4.0 V ≤ AV_{REF} ≤ V_{DD} T_A = –10 to +70°C			0.4	%
		3.6 V ≤ AV_{REF} ≤ V_{DD} T_A = –10 to +70°C			0.8	%
		4.0 V ≤ AV_{REF} ≤ V_{DD}			0.8	%
Quantization error					±1/2	LSB
Conversion time	t_{CONV}	82 ns ≤ t_{CYX} < 125 ns (The FR bit of ADM is to be "0")	360			t_{CYX}
		125 ns ≤ t_{CYX} < 250 ns (The FR bit of ADM is to be "1")	240			t_{CYX}
Sampling time	t_{SAMP}	82 ns ≤ t_{CYX} < 125 ns (The FR bit of ADM is to be "0")	72			t_{CYX}
		125 ns ≤ t_{CYX} < 250 ns (The FR bit of ADM is to be "1")	48			t_{CYX}
Analog input voltage	V_{IAN}		–0.3		AV_{REF} +0.3	V
Analog input impedance	R_{AN}			1000		MΩ
Reference voltage	AV_{REF}		3.6		V_{DD}	V
AV_{REF} current	AI_{REF}	f_{XX} = 12 MHz		1.5	5.0	mA
		Note 2		0.2	1.5	mA ★

Notes 1. Quantization error is not included. Represented by the ratio to full-scale value.
2. When ADM register's CS bit = 0, in STOP mode.

t_{CYX} DEPENDENT BUS TIMING DEFINITION (1/2)

PARAMETER	SYMBOL	FORMULA	MIN./MAX.	12 MHz	UNIT
X1 input clock cycle time	t_{CYX}		MIN.	82	ns
Address setup time (to ASTB↓)	t_{SAST}	t_{CYX} – 30	MIN.	52	ns
$\overline{\text{RD}}$↓ delay time from address	t_{DAR}	2t_{CYX} – 35	MIN.	129	ns
Address float time (from $\overline{\text{RD}}$↓)	t_{FAR}	t_{CYX}/2 – 30	MIN.	11	ns
Data input time from address	t_{DAID}	(4 + 2n) t_{CYX} – 100	MAX.	228 [Note]	ns
Data input time from ASTB↓	t_{DSTID}	(3 + 2n) t_{CYX} – 65	MAX.	181 [Note]	ns
Data input time from $\overline{\text{RD}}$↓	t_{DRID}	(2 + 2n) t_{CYX} – 64	MAX.	100 [Note]	ns
$\overline{\text{RD}}$↓ delay time from ASTB↓	t_{DSTR}	t_{CYX} – 30	MIN.	52	ns
Address active time from $\overline{\text{RD}}$↑	t_{DRA}	2t_{CYX} – 40	MIN.	124	ns
ASTB↑ delay time from $\overline{\text{RD}}$↑	t_{DRST}	2t_{CYX} – 40	MIN.	124	ns
$\overline{\text{RD}}$ low-level width	t_{WRL}	(2 + 2n) t_{CYX} – 40	MIN.	124 [Note]	ns
ASTB high-level width	t_{WSTH}	t_{CYX} – 30	MIN.	52	ns
$\overline{\text{WR}}$↓ delay time from address	t_{DAW}	2t_{CYX} – 35	MIN.	129	ns
Data output time from ASTB↓	t_{DSTOD}	t_{CYX} + 60	MAX.	142	ns
$\overline{\text{WR}}$↓ delay time from ASTB↓	t_{DSTW1}	t_{CYX} – 30 (Refreshing disabled)	MIN.	52	ns
	t_{DSTW2}	2t_{CYX} – 35 (Refreshing enabled)	MIN.	129	ns
Data setup time (to $\overline{\text{WR}}$↑)	t_{SODWR}	(3 + 2n) t_{CYX} – 100	MIN.	146 [Note]	ns
Data setup time (to $\overline{\text{WR}}$↓)	t_{SODWF}	t_{CYX} – 60 (Refreshing enabled)	MIN.	22	ns
ASTB↑ delay time from $\overline{\text{WR}}$↑	t_{DWST}	t_{CYX} – 40	MIN.	42	ns
$\overline{\text{WR}}$ low-level width	t_{WWL1}	(3 + 2n) t_{CYX} – 50 (Refreshing disabled)	MIN.	196 [Note]	ns
	t_{WWL2}	(2 + 2n) t_{CYX} – 50 (Refreshing enabled)	MIN.	114 [Note]	ns
$\overline{\text{WAIT}}$↓ input time from address	t_{DAWT}	3t_{CYX} – 100	MAX.	146	ns
$\overline{\text{WAIT}}$↓ input time from ASTB↓	t_{DSTWT}	2t_{CYX} – 80	MAX.	84	ns

Remark "n" indicates the number of waits.

Note When n = 0

t_{CYX} DEPENDENT BUS TIMING DEFINITION (2/2)

PARAMETER		SYMBOL	FORMULA	MIN./MAX.	12 MHz	UNIT
$\overline{\text{WAIT}}$ hold time from ASTB↓		t_{HSTWT}	$2Xt_{CYX} + 10$	MIN.	174 Note	ns
$\overline{\text{WAIT}}$↑ delay time from ASTB↓		t_{DSTWTH}	$2(1 + X)t_{CYX} - 55$	MAX.	273 Note	ns
$\overline{\text{WAIT}}$↓ input time from $\overline{\text{RD}}$↓		t_{DRWTL}	$t_{CYX} - 60$	MAX.	22	ns
$\overline{\text{WAIT}}$ hold time from $\overline{\text{RD}}$↓		t_{HRWT}	$(2X - 1)t_{CYX} + 5$	MIN.	87 Note	ns
$\overline{\text{WAIT}}$↑ delay time from $\overline{\text{RD}}$↓		t_{DRWTH}	$(2X + 1)t_{CYX} - 60$	MAX.	186 Note	ns
Data input time from $\overline{\text{WAIT}}$↑		t_{DWTID}	$t_{CYX} - 20$	MAX.	62	ns
$\overline{\text{WR}}$↑ delay time from $\overline{\text{WAIT}}$↑		t_{DWTW}	$2t_{CYX} - 10$	MIN.	154	ns
$\overline{\text{RD}}$↑ delay time from $\overline{\text{WAIT}}$↑		t_{DWTR}	$t_{CYX} - 10$	MIN.	72	ns
$\overline{\text{WAIT}}$ input time from $\overline{\text{WR}}$↓ (At refresh disabled)		t_{DWWTL}	$t_{CYX} - 60$	MAX.	22	ns
$\overline{\text{WAIT}}$ hold time from $\overline{\text{WR}}$↓	Refresh disabled	t_{HWWT1}	$(2X - 1)t_{CYX} + 5$	MIN.	87 Note	ns
	Refresh enabled	t_{HWWT2}	$2(X - 1)t_{CYX} + 5$	MIN.	5 Note	ns
$\overline{\text{WAIT}}$↑ delay time from $\overline{\text{WR}}$↓	Refresh disabled	t_{DWWTH1}	$(2X + 1)t_{CYX} - 60$	MAX.	186 Note	ns
	Refresh enabled	t_{DWWTH2}	$2Xt_{CYX} - 60$	MAX.	104 Note	ns
$\overline{\text{REFRQ}}$↓ delay time from $\overline{\text{RD}}$↑		t_{DRRFQ}	$2t_{CYX} - 10$	MIN.	154	ns
$\overline{\text{REFRQ}}$↓ delay time from $\overline{\text{WR}}$↑		t_{DWRFQ}	$t_{CYX} - 10$	MIN.	72	ns
$\overline{\text{REFRQ}}$ low-level width		t_{WRFQL}	$2t_{CYX} - 44$	MIN.	120	ns
ASTB↑ delay time from $\overline{\text{REFRQ}}$↑		t_{DRFQST}	$4t_{CYX} - 48$	MIN.	280	ns

Remarks
1. X: The number of the external waits (1, 2, ...)
2. $t_{CYX} \cong 82$ ns ($f_{XX} = 12$ MHz)
3. "n" indicates the number of waits.

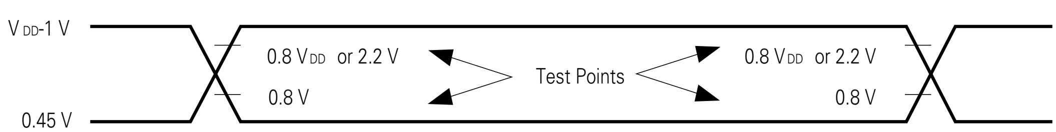
Note When X = 1

DATA RETENTION CHARACTERISTICS (T_A = −40 to +85 °C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data retention voltage	V_{DDDR}	STOP mode	2.5		5.5	V
Data retention current	I_{DDDR}	V_{DDDR} = 2.5 V		2	20	μA
		V_{DDDR} = 5 V ±10 %		5	50	μA
V_{DD} rise time	t_{RVD}		200			μs
V_{DD} fall time	t_{FVD}		200			μs
V_{DD} hold time (from STOP mode setting)	t_{HVD}		0			ms
STOP release signal input time	t_{DREL}		0			ms
Oscillation stabilization wait time	t_{WAIT}	Crystal resonator	30			ms
		Ceramic resonator	5			ms
Low-level input voltage	V_{IL}	Specified pin[Note]	0		0.1 V_{DDDR}	V
High-level input voltage	V_{IH}		0.9 V_{DDDR}		V_{DDDR}	V

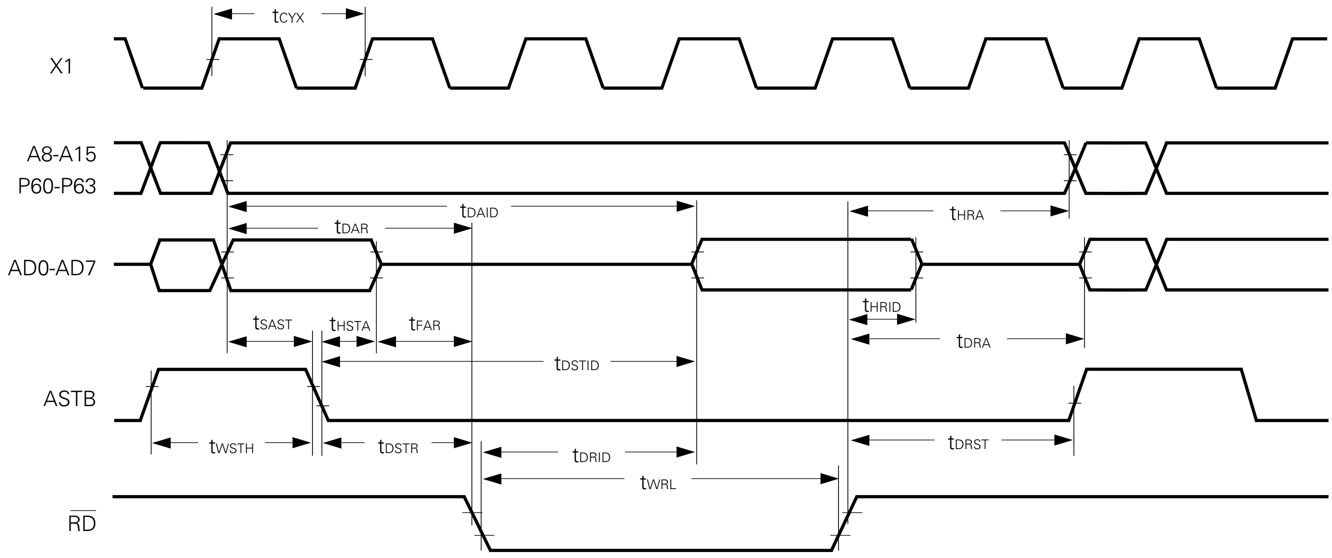
Note $\overline{RESET}$, P20/NMI, P21/INTP0, P22/INTP1, P23/INTP2/CI, P24/INTP3, P25/INTP4/ASCK, P26/INTP5, P27/SI, P32/$\overline{SCK}$, P33/SO/SB0 and $\overline{EA}$ pins.

AC Timing Test Point

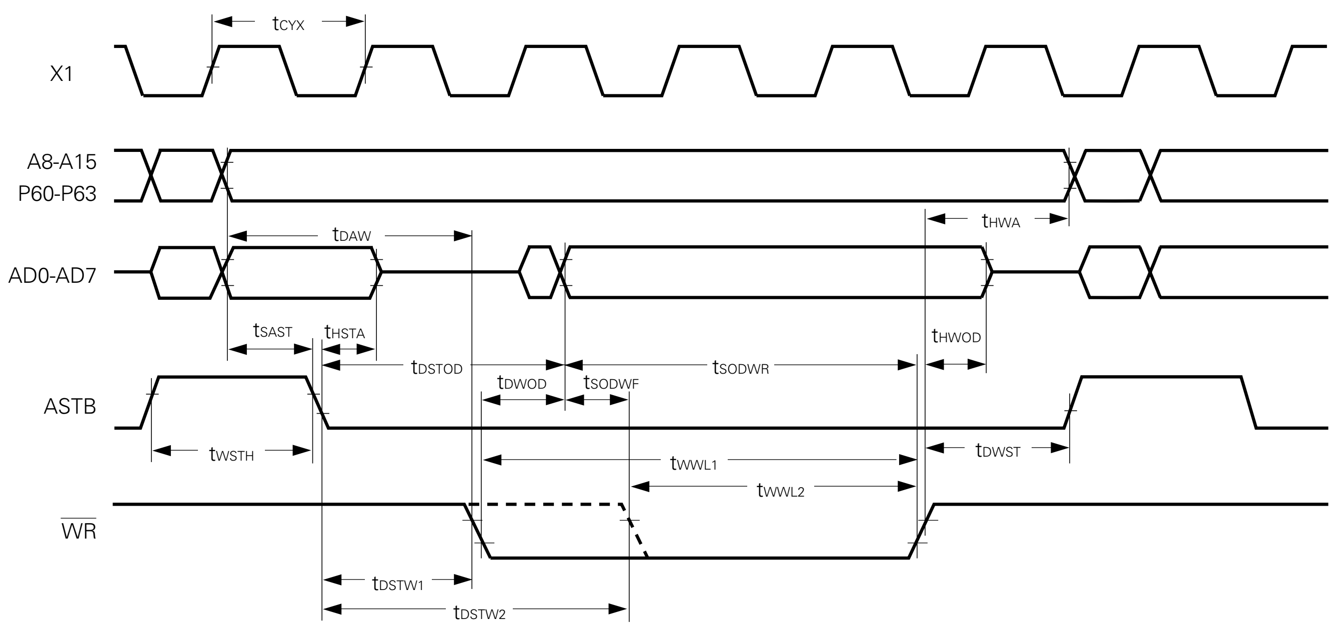


Timing Waveform

Read operation

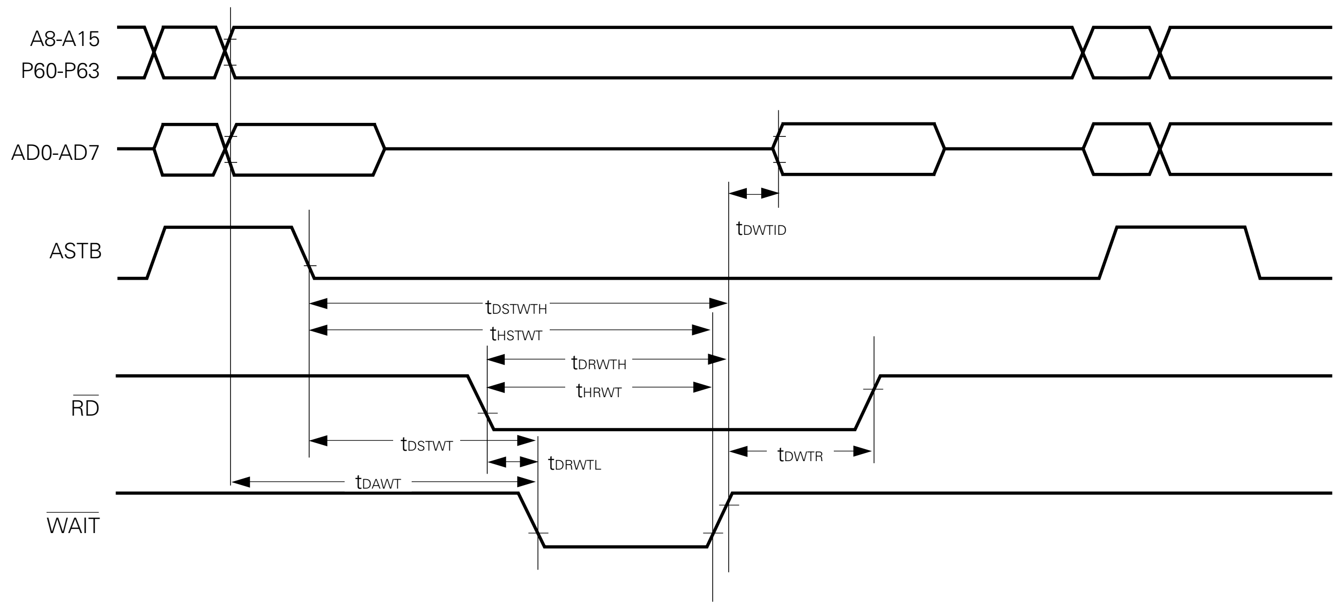


Write operation

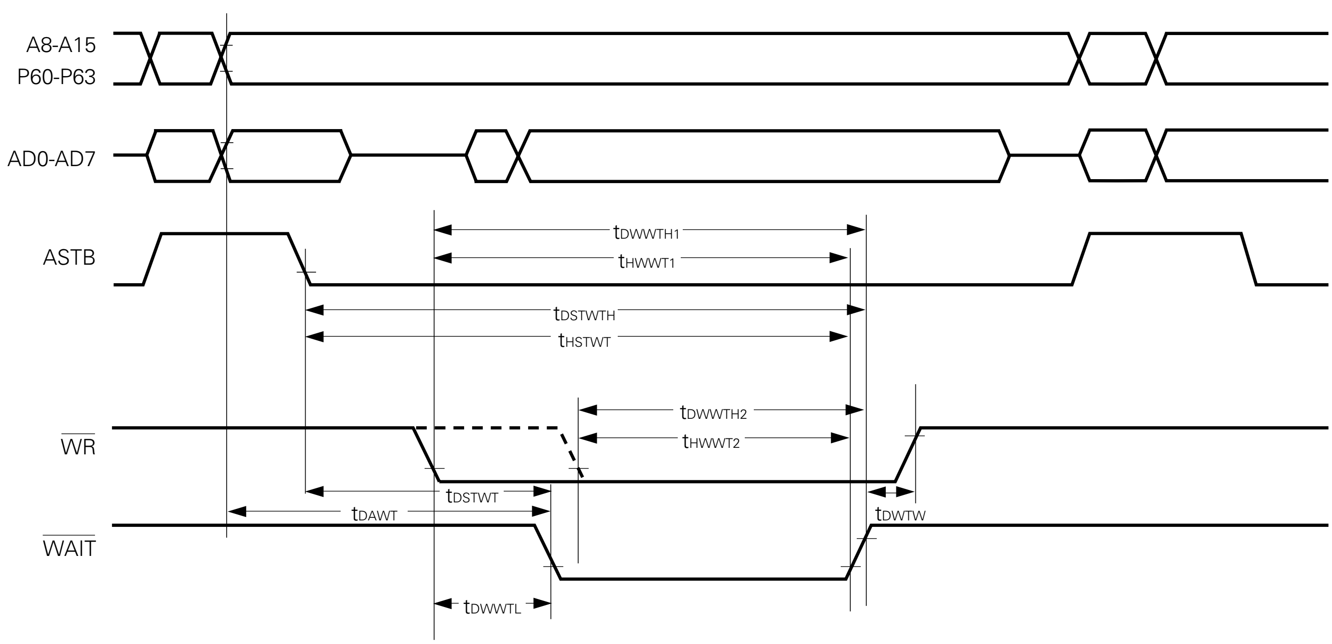


External WAIT Signal Input Timing

Read operation

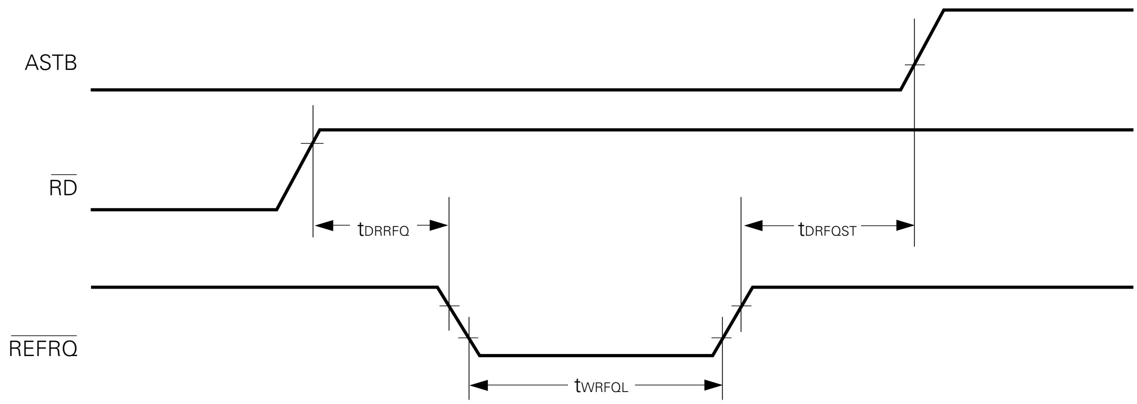


Write operation

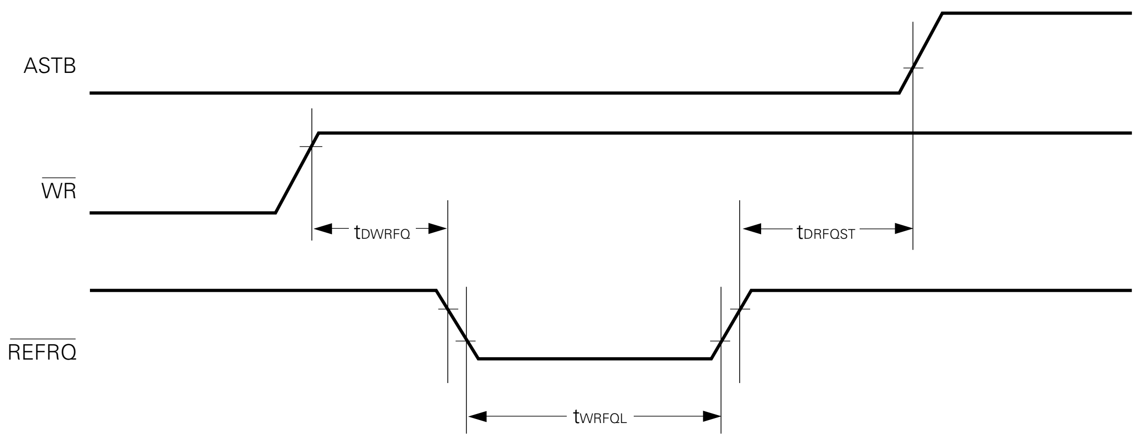


Refresh Timing Waveform

Refresh after read

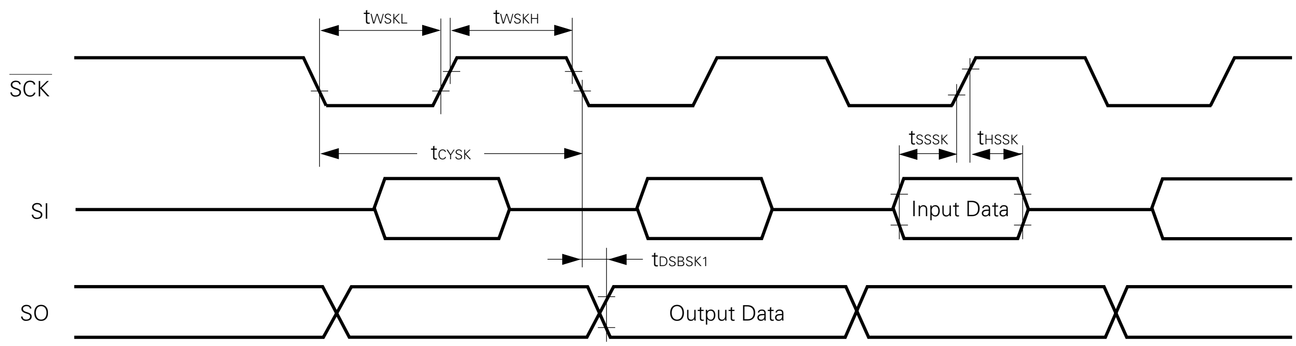


Refresh after write



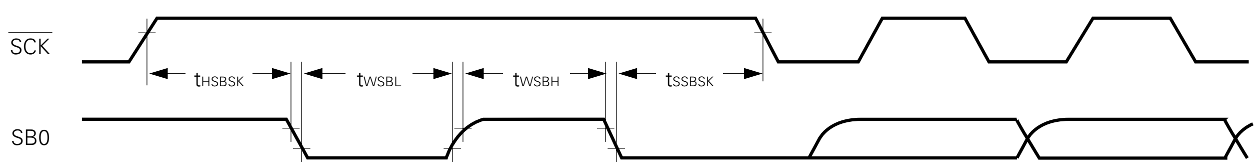
Serial Operation

3-wire serial I/O mode

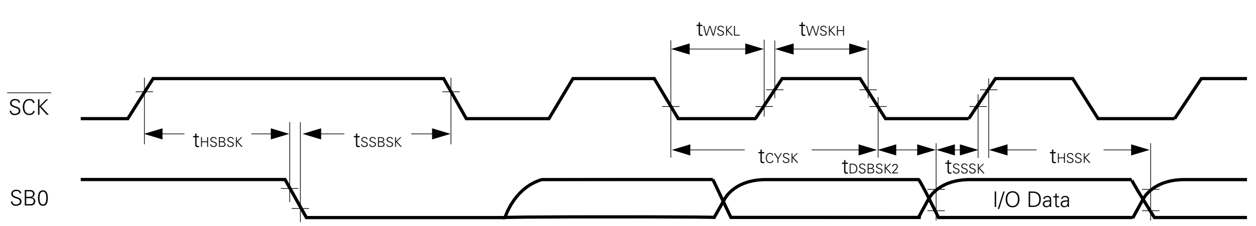


SBI Mode

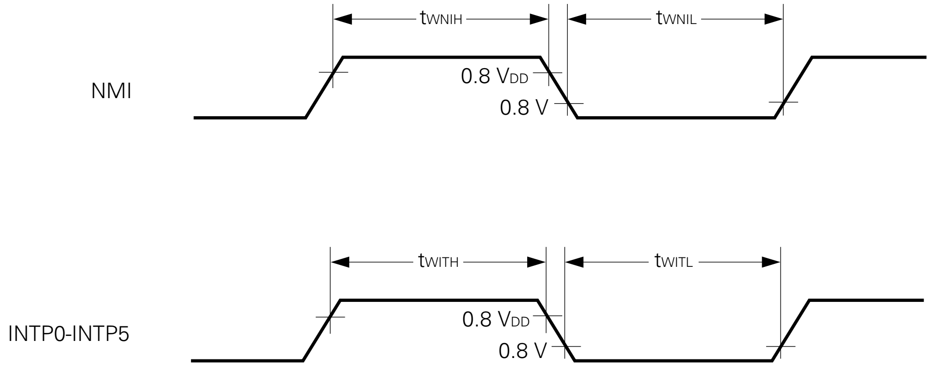
Bus release signal transfer



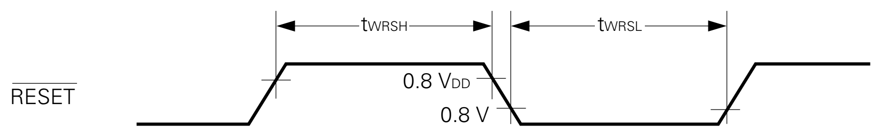
Command signal transfer



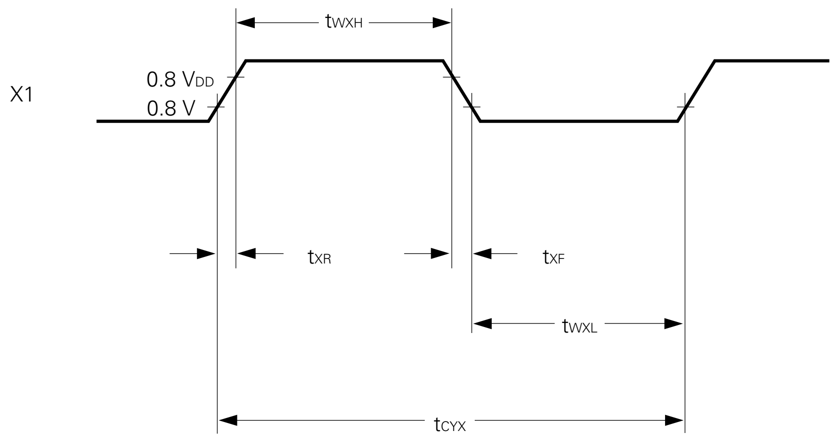
Interrupt Input Timing



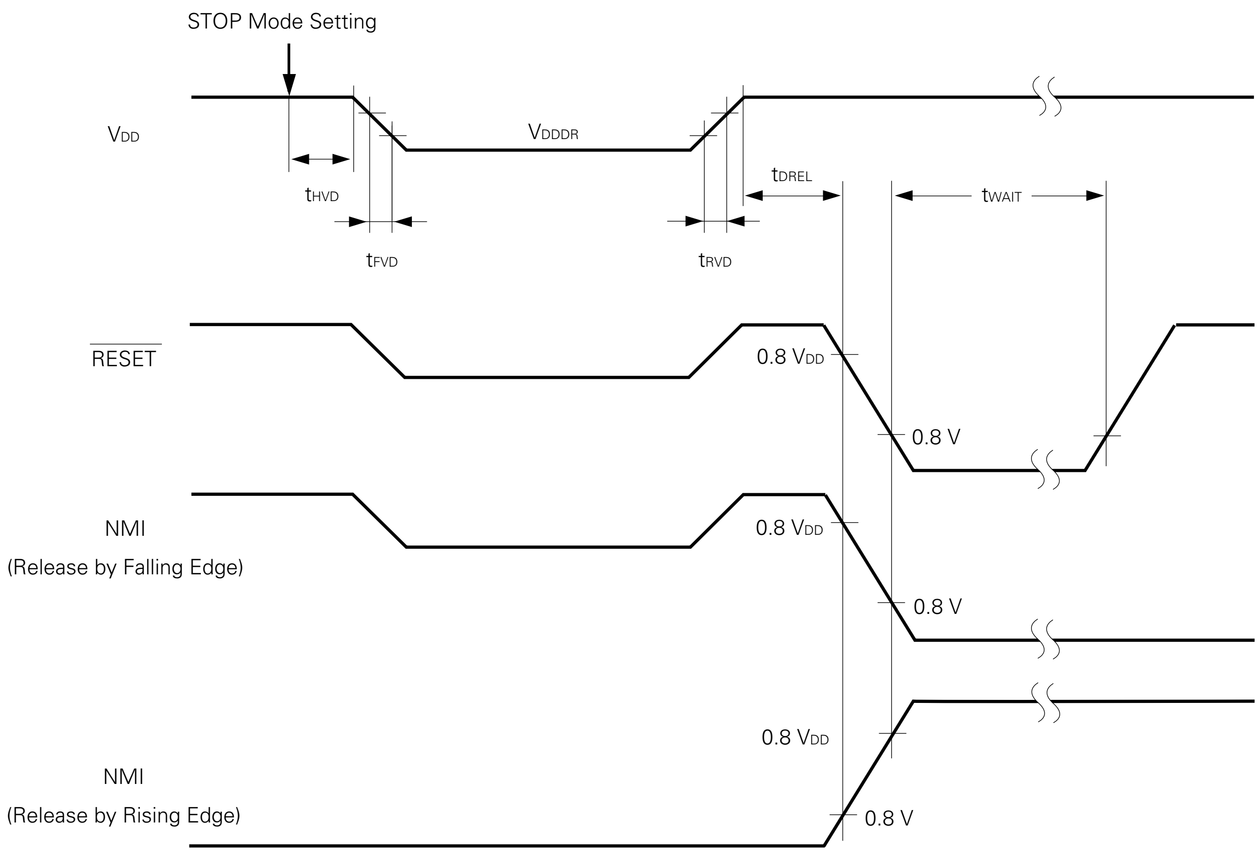
Reset Input Timing



External Clock Timing

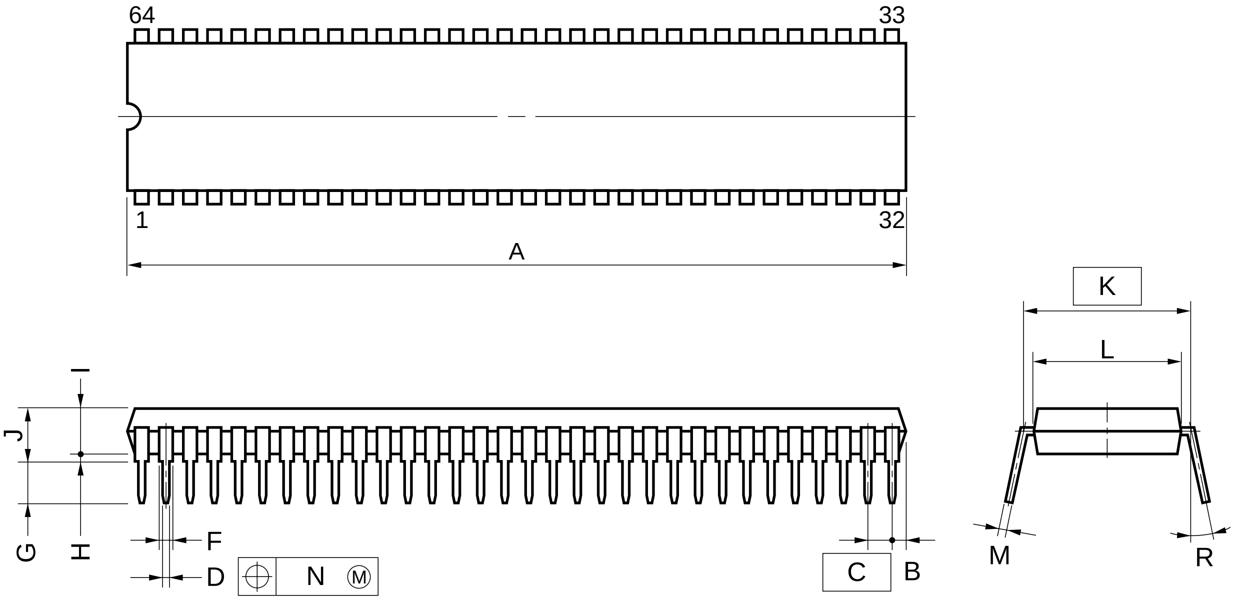


Data Retention Characteristics



7. PACKAGE DRAWINGS

64 PIN PLASTIC SHRINK DIP (750 mil)



NOTE

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

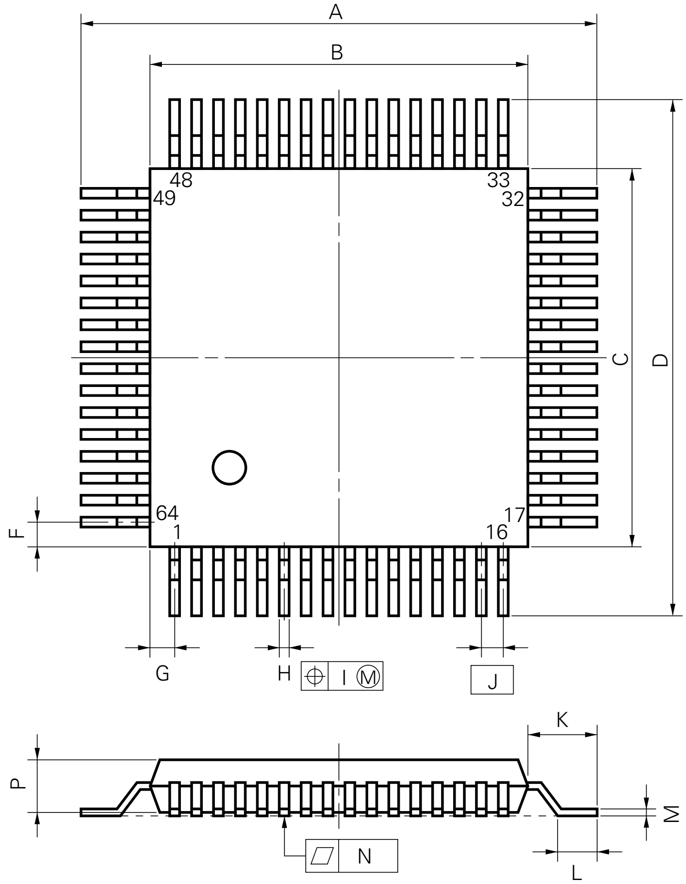
2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	58.68 MAX.	2.311 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50±0.10	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	3.2±0.3	0.126±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	17.0	0.669
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0~15°	0~15°

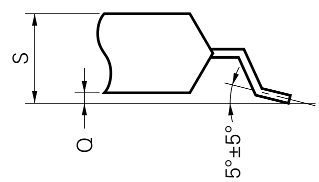
P64C-70-750A,C-1

Remark ES versions have the same package drawings and use the same materials as mass-produced versions.

64 PIN PLASTIC QFP (□14)



detail of lead end



NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

P64GC-80-AB8-3

ITEM	MILLIMETERS	INCHES
A	17.6±0.4	0.693±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	0.35±0.10	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	0.071±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.55	0.100
Q	0.1±0.1	0.004±0.004
S	2.85 MAX.	0.112 MAX.

Remark ES versions have the same package drawings and use the same materials as mass-produced versions.

8. RECOMMENDED SOLDERING CONDITIONS ★

The μPD78217A/78218A should be soldered and mounted under the conditions recommended in the table below.

For detail of recommended soldering conditions, refer to the information document **"Semiconductor Device Mounting Technology Manual" (IEI-1207)**.

For soldering methods and conditions other than those recommended below, contact an NEC sales representative.

Table 8-1 Surface Mounting Type Soldering Conditions

μPD78217AGC-AB8/78218AGC-××× -AB8 : 64-pin plastic QFP (14 x 14 mm)

Soldering Method	Soldering Conditions	Symbol
Infrared ray reflow	Package peak temperature: 235 °C, Reflow time: 30 seconds or less (at 210 °C or higher), Maximum number of reflow processes: 2 times <Cautions> (1) After the first reflow process, cool the package down to room temperature , then start the second reflow process. (2) After the first reflow process, do not use water to remove residual flux.	IR35-00-2
VPS	Package peak temperature: 215 °C, Reflow time: 40 seconds or less (at 200 °C or higher), Maximum number of reflow processes: 2 times <Cautions> (1) After the first reflow process, cool the package down to room temperature , then start the second reflow process. (2) After the first reflow process, do not use water to remove residual flux.	VP15-00-2
Partial heating	Pin temperature: 300 °C or below, Heat time: 3 seconds or less (per each side of the device)	—

Caution Apply only one kind of soldering method to a device, except for partial heating method.

Table 8-2 Insertion Type Soldering Conditions

μPD78217ACW/78218ACW-××× : 64-pin plastic shrink DIP (750 mil)

Soldering Method	Soldering Conditions
Wave soldering (pin only)	Solder temperature: 260 °C or below, Flow time: 10 seconds or less
Partial heating	Pin temperature: 300 °C or below, Heat time: 3 seconds or less (per pin)

Caution The wave soldering process must be applied only to pins, and make sure that the package body does not get jet soldered.

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD78217A/78218A.

Language Processing Software

RA78K/II [Notes1, 2, 3]	78K/II series common assembler package
CC78K/II [Notes1, 2, 3]	78K/II series common C compiler package
CC78K/II-L [Notes1, 2, 3]	78K/II series common C compiler library source file

PROM Writing Tools

PG-1500	PROM programmer
PA-78P214CW PA-78P214GC	Programmer adapters connected to PG-1500
PG-1500 controller [Notes1, 2]	PG-1500 control program

Debugging Tools

IE-78240-R-A IE-78240-R [Note4]	μPD78218A subseries common in-circuit emulators
IE-78200-R-BK	78K/II series common break board
IE-78240-R-EM IE-78200-R-EM [Note4]	μPD78218A subseries evaluation emulation boards
EP-78210CW [Note4] EP-78240CW-R EP-78210GC [Note4] EP-78240GC-R	μPD78218A subseries common emulation probes
EV-9200GC-64	Socket to be mounted on a user system board made for 64-pin plastic QFP
SD78K/II [Notes1, 2]	IE-78240-R-A screen debugger
DF78210 [Notes1, 2]	μPD78218A subseries device file

Fuzzy Inference Development Support System

FE9000 [Note1], FE9200 [Note5]	Fuzzy knowledge data creation tool
FT9080 [Note1], FT9085 [Note2]	Translator
FI78K/II [Notes1, 2]	Fuzzy inference module
FD78K/II [Notes1, 2]	Fuzzy inference debugger

Notes 1. PC-9800 series (MS-DOS™) based

2. IBM PC/AT™ (PC DOS™) based

3. HP9000 series 300™ (HP-UX™) based, SPARCstation™ (Sun OS™) based, EWS-4800 series (EWS-UX/V) based

4. No longer manufactured and not available for purchase

5. IBM PC/AT (PC DOS + Windows™) based

Remark For third-party development tools, see the **78K/II Series Development Tool Selection Guide (EF-231)**.

APPENDIX B. RELATED DOCUMENTS

Device Related Documents

Document Name		Document No. (Japanese)	Document No. (English)
μPD78218A Subseries User's Manual: Hardware		IEU-755	IEU-1313
78K/II Series User's Manual: Instruction		IEU-754	IEU-1311
78K/II Series Application Note	Fundamentals	IEA-607	IEA-1220
	Application	IEA-700	IEA-1282
	Floating Point Operation Program	IEA-686	IEA-1273
78K/II Series Selection Guide		IF-304	IF-1160
78K/II Series Instruction Table		IEM-5101	——
78K/II Series Instruction Set		IEM-5102	——
μPD78218A Series Special Function Register Table		IEM-5532	——

Development Tool Related Documents (User's Manuals)

Document Name		Document No. (Japanese)	Document No. (English)
RA78K Series Assembler Package	Operation	EEU-809	EEU-1399
	Language	EEU-815	EEU-1404
RA78K Series Structured Assembler Preprocessor		EEU-817	EEU-1402
CC78K Series C Compiler	Operation	EEU-656	EEU-1280
	Language	EEU-655	EEU-1284
CC78K Series Library Source File		EEU-777	——
PG-1500 PROM Programmer		EEU-651	EEU-1335
PG-1500 Controller		EEU-704	EEU-1291
IE-78240-R-A In-Circuit Emulator		EEU-796	EEU-1395
IE-78240-R In-Circuit Emulator	Hardware	EEU-705	EEU-1322
	Software	EEU-706	EEU-1331
SD78K/II Screen Debugger MS-DOS Based	Introduction	EEU-841	——
	Reference	EEU-813	——
SD78K/II Screen Debugger PC DOS Based	Introduction	——	——
	Reference	EEU-956	EEU-1447
78K/II Series Development Tool Selection Guide		EF-231	——

Caution The contents of the above related documents are subject to change without notice. The latest documents should be used for design, etc.

Embedded Software Related Documents (User's Manuals)

Document Name		Document No. (Japanese)	Document No. (English)
RX78K/II Real-Time OS	Basic	EEU-910	——
	Installation	EEU-884	——
	Debugger	EEU-895	——
	Technical	EEU-885	——
Fuzzy Knowledge Data Creation Tool		EEU-829	EEU-1438
78K/0, 78K/II, 87AD Series Fuzzy Inference Development Support System	Translator	EEU-862	EEU-1444
78K/II Series Fuzzy Inference Development Support System	Fuzzy Inference Module	EEU-860	EEU-1440
78K/II Series Fuzzy Inference Debugger		EEU-917	EEU-1459

Other Related Documents

Document Name	Document No. (Japanese)	Document No. (English)
QTOP Microcomputer Pamphlet	IB-5040	——
Semiconductor Device Package Manual	IEI-635	IEI-1213
Semiconductor Device Mounting Technology Manual	IEI-616	IEI-1207
Quality Grades on NEC Semiconductor Devices	IEI-620	IEI-1209
NEC Semiconductor Device Reliability & Quality Control System	IEM-5068	——
Electrostatic Discharge (ESD) Test	MEM-539	——
Guide to Quality Assurance for Semiconductor Devices	MEI-603	MEI-1202
Microcomputer-Related Products Guide – Third Party Products	MEI-604	——

Caution **The contents of the above related documents are subject to change without notice. The latest documents should be used for design, etc.**

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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