Integrated Circuit Systems, Inc.

ICS9147-01

Frequency Generator & Integrated Buffers for PENTIUM™

General Description

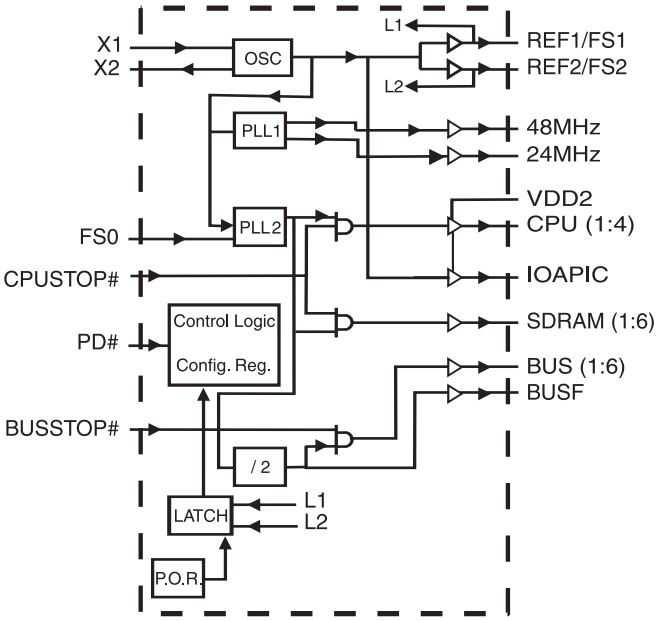
The **ICS9147-01** generates all clocks required for high speed RISC or CISC microprocessor systems such as Intel PentiumPro. Two bidirectional I/O pins (FS1,FS2) are latched at power-on to the functionality table, with FS0 selectable in real-time to toggle between conditions. The inputs provide for tristate and test mode conditions to aid in system level testing. These multiplying factors can be customized for specific applications. Glitch-free stop clockcontrols are provided for CPU clocks and BUS clocks.

High drive BUS and SDRAM outputs typically provide greater than 1 V/ns slew rate into 30 pF loads. CPU outputs typically provide better than 1V/ns slew rate into 20 pF loads while maintaining 50 ±5% duty cycle. The REF clock outputs typically provide better than 0.5V/ns slew rates. Seperate buffers supply pins VDD2 allow for 3.3V or reduced voltage swing (from 2.9 to 2.5V) for CPU (1:4) and IOAPIC outputs.

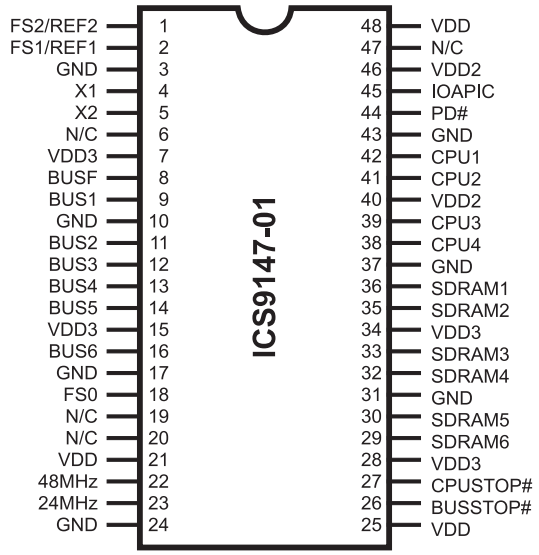
Features

- Four copies of CPU clock
- Six SDRAM (3.3 V TTL), usable as AGP clocks
- Seven copies of BUS clock (synchronous with CPU clock/2 or CPU/2.5 for 75 and 83.3 MHz CPU)
- CPU clocks to BUS clocks skew 1-4ns (CPU early)
- One IOAPIC clock @14.31818 MHz
- Two copies of Ref. clock @14.31818 MHz
- One each 48/24 MHz (3.3 V TTL)
- This device is configured into the ***Mobile*** mode for power management of Intel 430 TX
- Ref. 14.31818 MHz Xtal oscillator input
- Separate 66/60 MHz select pin (LSB of select pins)
- Separate V_{DD2} for four CPU and single IOAPIC output buffers to allow 2.5V output (or Std. Vdd)
- Power Management Control Input pins
- 3.0V – 3.7V supply range w/2.5V compatible outputs
- 48-pin SSOP package

Block Diagram



Pin Configuration



48-Pin SSOP

Pentium is a trademark of Intel Corporation

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	REF2	OUT	Reference clock output*
	FS2	IN	Logic input frequency select Bit 2*
2	REF1	OUT	Reference clock output*
	FS1	IN	Logic input frequency select Bit1*
3, 10, 17, 24, 31, 37, 43	GND	PWR	Ground.
4	X1	IN	Crystal input. Nominally 14.318 MHz. Has internal load cap. External crystal load of 30pF to GND recommended for VDD power on faster than 2.0ms.
5	X2	OUT	Crystal output. Has internal load cap and feedback resistor to X1. External crystal load of 10pF to GND recommended for VDD power on faster than 2.0ms.
7, 15, 28, 34	VDD3	PWR	3.3V I/O power supply, BUS and SDRAM buffer supply.
8,9,11,12,13,14,16	BUSF, BUS(1:6)	OUT	BUS clock outputs. see select table for frequency
18	FSO	IN	Select pin for enabling 66.6 MHz or 60 MHz, or other selections in frequency select table.
21, 25, 48	VDD	PWR	Core power supply, and fixed clock power.
22, 23	48, 24MHz	OUT	48, 24MHz clock outputs
26	BUSSTOP#	IN	Input pin to synchronously stop all BUS (1:6) clocks when pin is low.
27	CPUSTOP#	IN	Input pin to synchronously stop all CPU and SDRAM clocks when pin is low.
36, 35, 33, 32, 30, 29	SDRAM (1:6)	OUT	SDRAM clocks at CPU speed. See select table for frequency. Powered by VDD3.
40, 46	VDD2	PWR	2.5V Power Supply for CPU and IOAPIC buffers, can be tied to VDD3 for 3.3V operation
41, 42, 39,38	CPU (1:4)	OUT	CPU clock output clocks .See select table for frequency
44	PD#	IN	Power down logic control input. When low, powers off both PLL and all outputs forced to logic low.
45	IOAPIC	OUT	IOAPIC clock output (Freq=14.318 with nominal crystal) Powered by VDD2 supply
6, 19, 20, 47	N/C	—	Pins not internally connected.

* Bidirectional input/output pins, input logic levels are latched at internal power-on-reset. Use 10Kohm resistor to program logic Hi to VDD or GND for logic low.

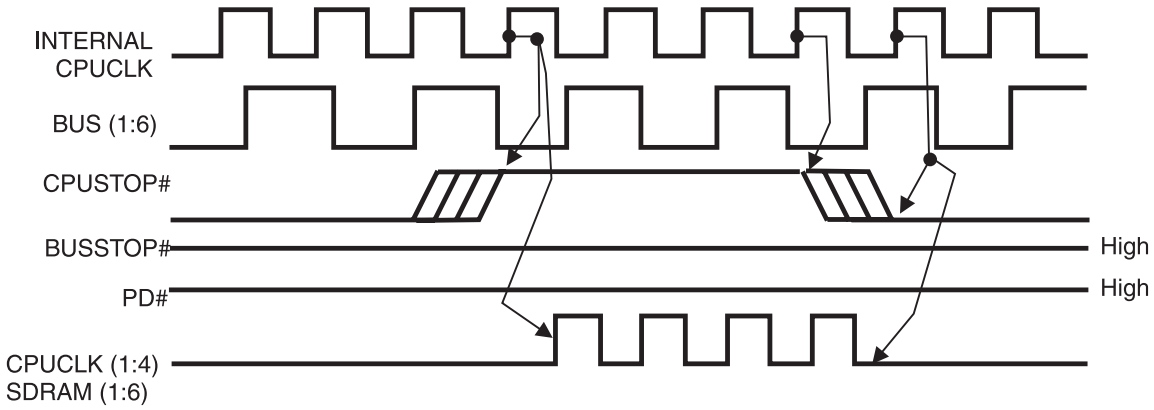
Functionality

PD#	CPU-STOP#	BUS-STOP#	FS2* (at REF2)	FS1* (at REF1)	FS0 (pin 18)	CPU (1:4), SDRM (1:6) (MHz)	BUS (1:6) BUSF (MHz)	48MHz (MHz)	24 MHz (MHz)	REF (1:2), IOAPIC (MHz)
1	1	1	0	0	0	60	30	48	24	14.318
1	1	1	0	0	1	66.6	33.3	48	24	14.318
1	1	1	0	1	0	50	25	48	24	14.318
1	1	1	0	1	1	55	27.5	48	24	14.318
1	1	1	1	0	0	75	30[a]	48	24	14.318
1	1	1	1	0	1	83.3	33.3[a]	48	24	14.318
1	1	1	1	1	0	REF/2	REF/4	REF/2	REF/4	REF
1	1	1	1	1	1	Tristate	Tristate	Tristate	Tristate	Tristate
0	1	1	X	X	X	LOW PLL off	LOW	LOW PLL off	LOW	LOW Osc Off
1	0	1	X	X	X	LOW	running	running	running	running
1	1	0	X	X	X	running	LOW	running	running	running

Note a: These frequency selections are at CPU/2.5 (internal VCO/5), not synchronous CPU/2

CPUSTOP# Timing Diagram

CPUSTOP# is an asychronous input to the clock synthesizer. It is used to turn off the CPU clocks for low power operation. CPUSTOP# is synchronized by the **ICS9147-01**. All other clocks will continue to run while the CPU and SDRAM clocks are disabled. The CPU and SDRAM clocks will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. CPU clock on latency is 0 to 1 CPU clocks and CPU clock off latency is 0 to 1 CPU clocks.



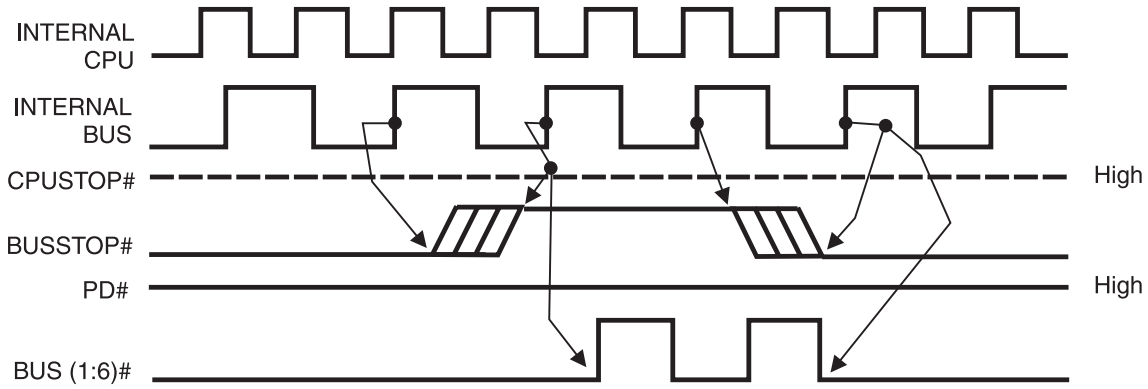
Notes:

1. All timing is referenced to the internal CPU clock.
2. CPUSTOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPU and SDRAM clocks inside the ICS9147-01.
3. All other clocks continue to run undisturbed.
4. PD# and BUSSTOP# are shown in a high (true) state.

BUSSTOP# Timing Diagram

BUSSTOP# is an asynchronous input to the ICS9147-01. It is used to turn off the BUS (1:6) clocks for low power operation. BUSSTOP# is synchronized by the ICS9147-01 internally. BUS (1:6) clocks are stopped in a low state and started with a full high pulse width guaranteed. BUS (1:6) clock on latency cycles are less than 4 CPU clocks and BUS (1:6) clock off latency is less than 4 clocks.

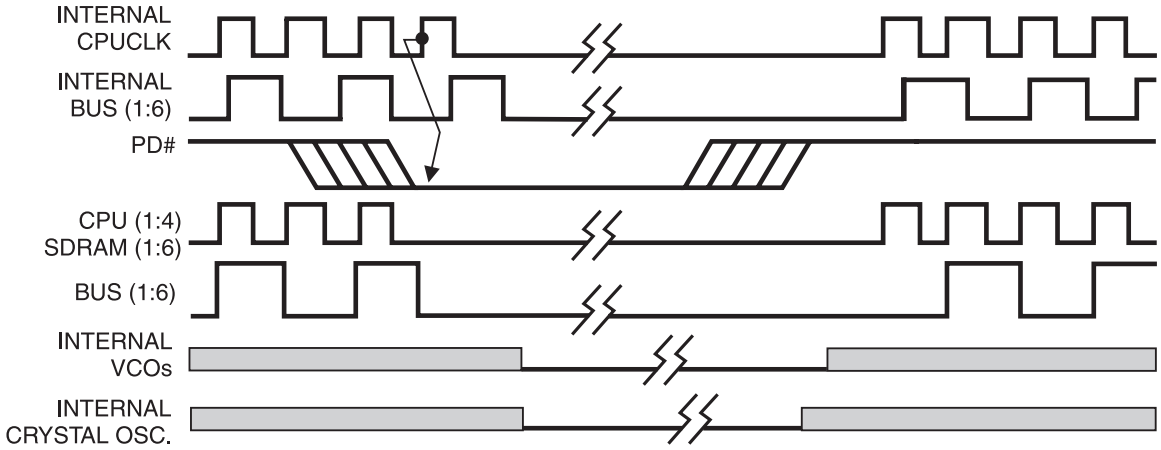
(Drawing shown on next page.)



Notes:
1. All timing is referenced to the Internal BUS clock (defined as inside the ICS9147 device.)
2. BUSSTOP# is an asynchronous input, and metastable conditions may exist. This signal is required to be synchronized inside the ICS9147.
3. All other clocks continue to run undisturbed.
4. PD# and CPUSTOP# are shown in a high (true) state.

PD# Timing Diagram

The power down selection is used to put the part into a very low power state without turning off the power to the part. PD# is an asynchronous active low input. This signal is synchronized internal by the **ICS9147-01** prior to its control action of powering down the clock synthesizer. PD# is an asynchronous function for powering up the system. Internal clocks will not be running after the device is put in power down state. When PD# is active (low) all clocks are driven to a low state and held prior to turning off the VCOs and the Crystal oscillator. The power on latency is guaranteed to be less than 3mS. The power down latency is less than three CPU clock cycles. BUSSTOP# and CPUSTOP# are don't care signals during the power down operations.



Notes:
1. All timing is referenced to the Internal CPU clock (defined as inside the ICS9147 device).
2. PD# is an asynchronous input and metastable conditions may exist. This signal is synchronized inside the ICS9147.
3. The shaded sections on the VCO and the Crystal signals indicate an active clock is being generated.

Absolute Maximum Ratings

Supply Voltage ..... 7.0 V

Logic Inputs ..... GND –0.5 V to V_{DD} +0.5 V

Ambient Operating Temperature ..... 0°C to +70°C

Storage Temperature ..... –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics at 3.3V

V_{DD} = 3.0 – 3.7 V, T_A = 0 – 70° C unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	VIL	Latched inputs and Fulltime inputs	-	-	0.2VDD	V
Input High Voltage	VIH	Latched inputs and Fulltime inputs	0.7VDD	-	-	V
Input Low Current	IIL	VIN = 0V (Fulltime inputs)	-28.0	-10.5	-	□A
Input High Current	IIH	VIN=VDD (Fulltime inputs)	-5.0	-	5.0	□A
Output Low Current	IOL1a	VOL = 0.8V; CPU, SDRAM; VDD2 = 3.3V	19.0	30.0	-	mA
	IOL1b	VOL = 0.8V; CPU; VDD2 = 2.5V	19.0	30.0		mA
Output High Current	IOH1a	VOH = 2.0V; CPU, SDRAM; VDD2 = 3.3V	-	-26.0	-16.0	mA
	IOH1b	VOH = 2.0V; CPU; VDD2 = 2.5V		-12.5	-9.5	mA
Output Low Current	IOL2	VOL = 0.8V; for fixed 24, 48, BUS, REF	16.0	25.0	-	mA
Output High Current	IOH2	VOH = 2.0V; for fixed 24, 48, BUS, REF	-	-22.0	-14.0	mA
Output Low Current	IOL3a	VOL = 0.8V; IOAPIC; VDD2 = 3.3V	19.0	33.0	-	mA
	IOL3b	VOL = 0.8V; IOAPIC; VDD2 = 2.5V	19.0	33.0		mA
Output High Current	IOH3a	VOH = 2.0V for IOAPIC at VDD2 = 3.3V	-	-45.0	-16.0	mA
	IOH3b	VOH = 2.0V; IOAPIC; VDD2 = 2.5V		-13.0	-10.0	mA
Output Low Voltage	VOL1a	IOL = 10mA; CPU, SDRAM;VDD2 = 3.3V	-	0.3	0.4	V
	VOL1b	IOL = 10mA; CPU; VDD2=2.5V		0.3	0.4	V
Output High Voltage	VOH1a	IOH = -10mA; CPU, SDRAM; VDD = 3.3V	2.4	2.8	-	V
	VOH1b	IOH = -10mA; CPU; VDD2=2.5V	1.95	2.1		V
Output Low Voltage	VOL2	IOL = 8mA; for fixed CLKs	-	0.3	0.4	V
Output High Voltage	VOH2	IOH = -8mA; for fixed CLKs	2.4	2.8	-	V
Output Low Voltage	VOL3a	IOL = 10mA; for IOAPIC at VDD2 = 3.3V	-	0.3	0.4	V
	VOL3b	IOL = 10mA; IOAPIC; VDD2 = 2.5V		0.3	0.4	V
Output High Voltage	VOH3a	IOH = -10mA; for IOAPIC at VDD2 = 3.3V	2.4	2.8	-	V
	VOH3b	IOH = -10mA; IOAPIC; VDD2 = 2.5V	2.0	2.2	-	V
Supply Current	IDD	@66.6 MHz; all outputs unloaded	-	120	180	mA
Supply Current	IDDPD	Power Down		300	500	□A

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.

Electrical Characteristics at 3.3V

V_{DD} = 3.0 – 3.7 V, T_A = 0 – 70° C unless otherwise stated

AC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Rise Time[1]	Tr1a	20pF load, 0.8 to 2.0V CPU; VDD = 3.3V	-	0.9	1.5	ns
Rise Time[1]	Tr1b	20pF load, 0.8 to 2.0V CPU; VDDL @ 2.5V	-	1.5	2.0	ns
Fall Time[1,3]	Tf1	20pF load, 2.0 to 0.8V CPU;	-	0.8	1.4	ns
Rise Time[1]	Tr2	30pF load SDRAM 0.8 to 2.0V	-	1.0	1.6	ns
Fall Time[1]	Tf2	30pF load SDRAM 2.0 to 0.8V	-	0.9	1.5	ns
Rise Time[1]	Tr3	30pF load BUS 0.8 to 2.0V	-	1.2	2.0	ns
Fall Time[1]	Tf3	30pF load BUS 2.0 to 0.8V	-	1.1	1.9	ns
Rise Time[1,3]	Tr4	20pF load, 0.8 to 2.0V 24, 48, REF2, & IOAPIC	-	0.83	1.4	ns
Rise Time[1]	Tr4a	45pF load, 0.8 to 2.0V , IOAPIC with VDDL = 2.5V	-	2.2	2.6	ns
Fall Time[1,3]	Tf4	20pF load, 2.0 to 0.8V 24, 48, REF2, & IOAPIC	-	0.81	1.3	ns
Rise Time[1]	Tr5	Load = 45pF 0.8 to 2.0V IOAPIC VDD = 3.3V		1.6	2.0	ns
Fall Time[1]	Tf5	Load = 45pF 2.0 to 0.8V, REF1 VDD = 3.3V		1.6	2.0	ns
Duty Cycle[1]	Dt	20pF load @ VOUT=1.4V	45	50	55	%
Jitter, Cycle to Cycle[1]	Tjc-c	CPU, VDD2 = 3.0 to 3.7V		150	250	ps
Jitter, One Sigma[1, 2]	Tj1s1	CPU; Load=20pF, SDRAM & BUS Clocks Load = 30pF	-	50	150	ps
Jitter, Absolute[1, 2]	Tjab1	CPU; Load=20pF, SDRAM & BUS Clocks Load = 30p	-250	-	250	ps
Jitter, One Sigma[1]	Tj1s2	REF2, 48/24MHz Load=20pF, REF1 CL = 47pF	-	1	3	%
Jitter, Absolute[1]	Tjab2	REF2, 48/24MHz Load=20pF, REF1 CL = 47pF	-5	2	5	%
Input Frequency[1]	Fi		12.0	14.318	16.0	MHz
Logic Input Capacitance[1]	CIN	Logic input pins	-	5	-	pF
Crystal Oscillator Capacitance[1]	CINX	X1, X2 pins	-	18	-	pF
Power-on Time[1]	ton	From VDD=1.6V to 1st crossing of 66.6 MHz VDD supply ramp < 40ms	-	2.5	4.5	ms
Clock Skew[1]	Tsk1	CPU to CPU; Load=20pF; @1.4V (Same VDD)	-	150	250	ps
Clock Skew[1]	Tsk2	BUS to BUS; Load=20pF; @1.4V	-	300	500	ps
Clock Skew[1,2]	Tsk3	CPU to BUS; Load=20pF; @1.4V (CPU is early)	1	2.6	4	ns
Clock Skew[1]	Tsk4	SDRAM (@3.3V) to CPU (@2.5V) (2.5V CPU is late)		250	400	ps

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.
Note 2: Includes VDD2 = 2.5V
Note 3: VDD3 = 3.3V

Shared Pin Operation - Input/Output Pins

Pins 1 and 2 on the **ICS9147-01** serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 4-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm(10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figs. 1 and 2 show the recommended means of implementing this function. In Fig. 1 either one of the resistors is loaded onto the board (selective stuffing) to configure the device's internal logic. Figs. 2a and b provide a single resistor loading option where either solder spot tabs or a physical jumper header may be used.

These figures illustrate the optimal PCB physical layout options. These configuration resistors are of such a large ohmic value that they do not effect the low impedance clock signals. The layouts have been optimized to provide as little impedance transition to the clock signal as possible, as it passes through the programming resistor pad(s).

Test Mode Operation

The **ICS9147-01** includes a production test verification mode of operation. This requires that the FSO and FS1 pins be programmed to a logic high and the FS2 pin be programmed to a logic low(see Shared Pin Operation section). In this mode the device will output the following frequencies.

Pin	Frequency
REF, IOAPIC	REF
48MHz	REF/2
24MHz	REF/4
CPU, SDRAM	REF/2
BUS (1:6)	REF/4

Note: REF is the frequency of either the crystal connected between the devices X1and X2 or, in the case of a device being driven by an external reference clock, the frequency of the reference (or test) clock on the device's X1 pin.

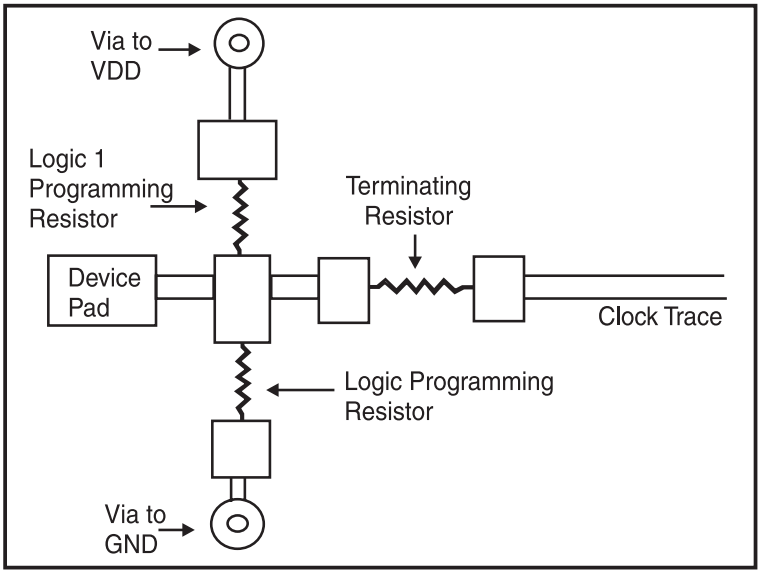


Fig. 1

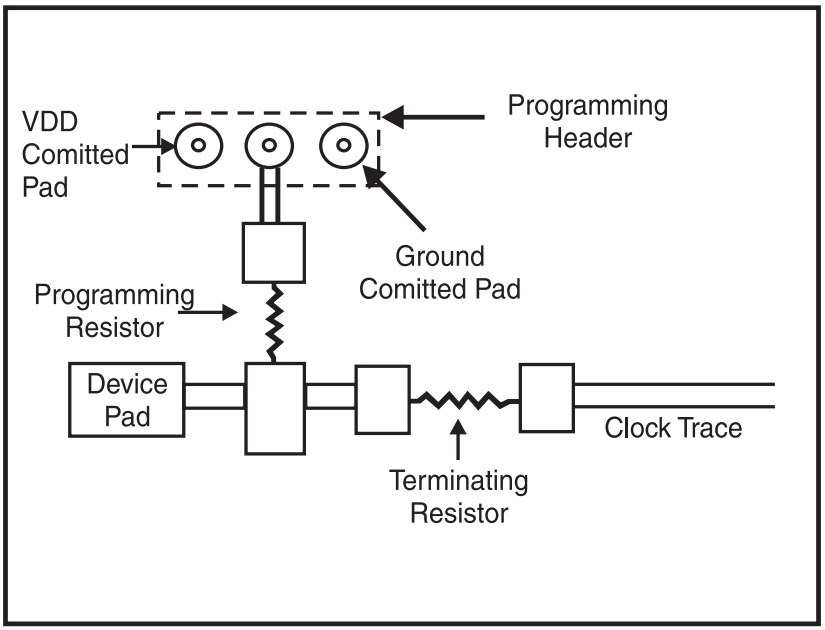

VDD
Comitted
Pad
Programming
Header
Ground
Comitted Pad
Programming
Resistor
Device
Pad
Clock Trace
Terminating
Resistor

Fig. 2a

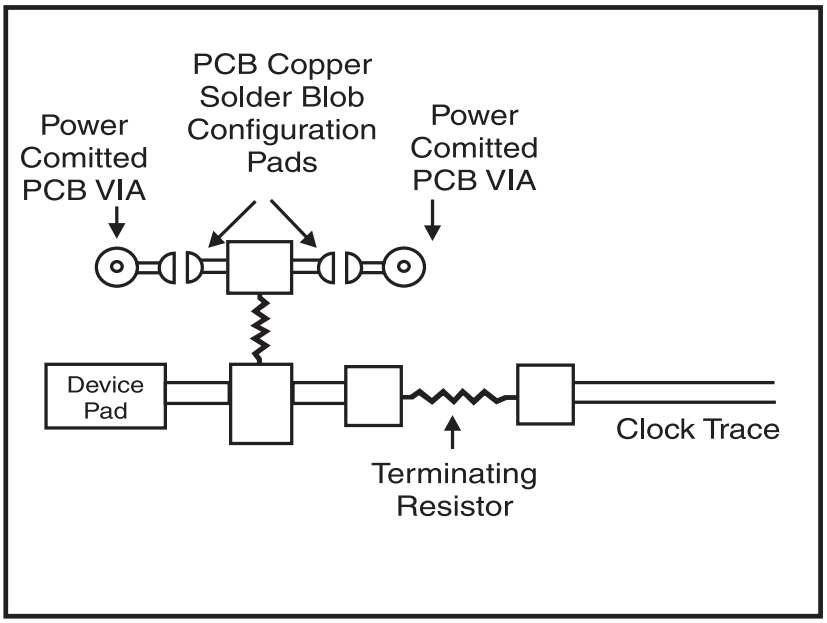
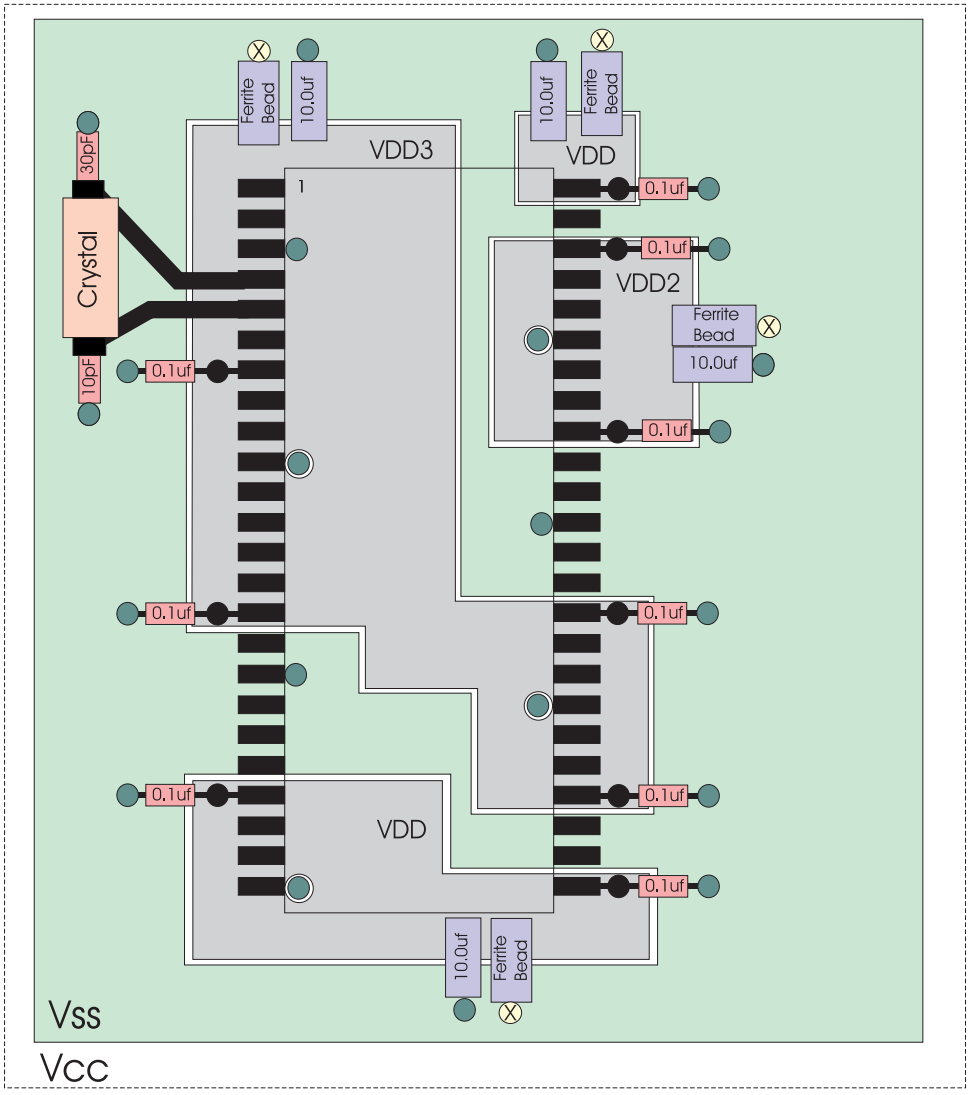

PCB Copper
Solder Blob
Configuration
Pads
Power
Comitted
PCB VIA
Power
Comitted
PCB VIA
Device
Pad
Clock Trace
Terminating
Resistor

Fig. 2b

Recommended PCB Layout for ICS9147-01



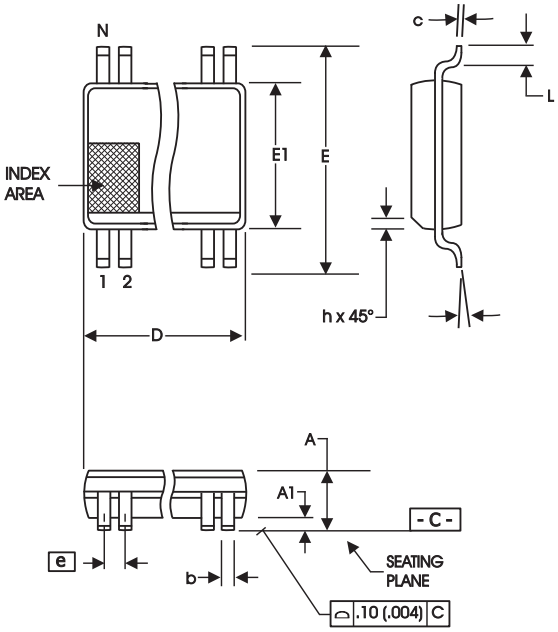
Connection to VDD plane.

Connection to VSS plane.

Connection to System VCC plane

Connection to Isolated VDD plane

NOTE:
This PCB Layout is based on a 4 layer board with an internal Ground (common) and Vcc plane. Placement of components will depend on routing of signal trace. The 0.1uf Capacitors should be placed as close as possible to the Power pins. Placement on the backside of the board is also possible. The Ferrite Beads can be replaced with 10-15ohm Resistors. For best results, use a Fixed Voltage Regulator between the main (board) Vcc and the different Vdd planes.



300 mil SSOP Package

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	15.75	16.00	.620	.630

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

Ordering Information

ICS9147F-01

Example:

ICS XXXX F - PPP

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Package Type
F=SSOP

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS = Standard Device