

# 9+2-Bit Parity Generator/Checker

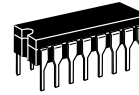
The MC10170 is a 11-bit parity circuit, which is segmented into 9 data bits and 2 control bits.

Output A generates odd parity on 9 bits; that is, Output A goes high for an odd number of high logic levels on the bit inputs in only 2 gate delays.

The Control Inputs can be used to expand parity to larger numbers of bits with minimal delay or can be used to generate even parity. To expand parity to larger words, the MC10170 can be used with the MC10160 or other MC10170's. The MC10170 can generate both even and odd parity.

$P_D = 300 \text{ mW typ/pkg (No Load)}$   
 $t_{pd} = 2.5 \text{ ns typ (Control Inputs to B Output)}$   
 $4.0 \text{ ns typ (Data Inputs to A Output)}$   
 $6.0 \text{ ns typ (Data Inputs to B Output)}$   
 $t_r, t_f = 2.0 \text{ ns typ (20\%–80\%)}$

## MC10170

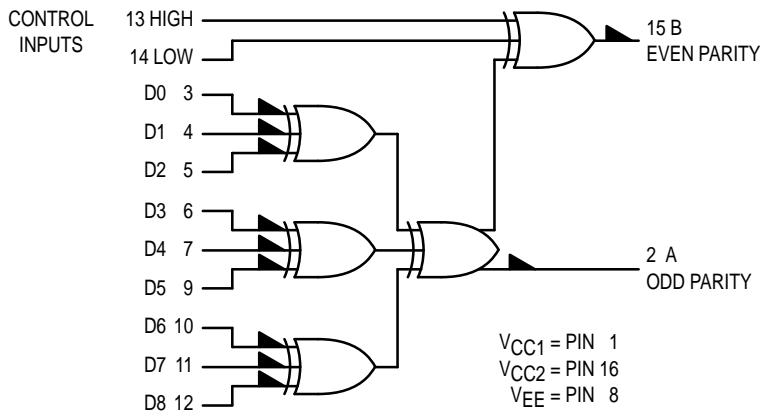


**L SUFFIX**  
CERAMIC PACKAGE  
CASE 620-10

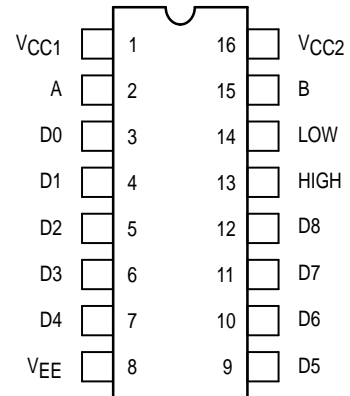


**P SUFFIX**  
PLASTIC PACKAGE  
CASE 648-08

### LOGIC DIAGRAM



### PIN ASSIGNMENT



INPUTS	OUTPUTS	
	Odd Parity Output A	Even Parity Output B
Sum of D Inputs at High Level		
Even	Low	High
Odd	High	Low



## ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			-30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I <sub>E</sub>	8		78		57	71		78	mAdc
Input Current	I <sub>inH</sub>	3		350			200		220	μAdc
		5		350			220		220	
	I <sub>inL</sub>	3	0.5		0.5			0.3		μAdc
Output Voltage Logic 1	V <sub>OH</sub>	2	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700	Vdc
		15	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700	
Output Voltage Logic 0	V <sub>OL</sub>	2	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	Vdc
		15	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	
Threshold Voltage Logic 1	V <sub>OHA</sub>	2	-1.080		-0.980			-0.910		Vdc
		15	-1.080		-0.980			-0.910		
Threshold Voltage Logic 0	V <sub>OLA</sub>	2		-1.655			-1.630		-1.595	Vdc
		15		-1.655			-1.630		-1.595	
Switching Times (50Ω Load)										ns
Propagation Delay	t <sub>13+15+</sub> t <sub>14-15-</sub> t <sub>3+2-</sub> t <sub>3-15+</sub>	15	1.5	4.2	1.5	2.5	4.0	1.5	4.4	
		15	1.5	4.2	1.5	2.5	4.0	1.5	4.4	
		2	2.0	6.6	2.0	4.0	6.0	2.0	6.6	
		15	4.0	9.5	4.0	6.0	8.8	4.0	9.5	
Rise Time (20 to 80%)	t <sub>2+</sub>	2	1.5	4.3	1.5	2.0	3.9	1.5	4.3	
Fall Time (20 to 80%)	t <sub>2-</sub>	2	1.5	4.3	1.5	2.0	3.9	1.5	4.3	

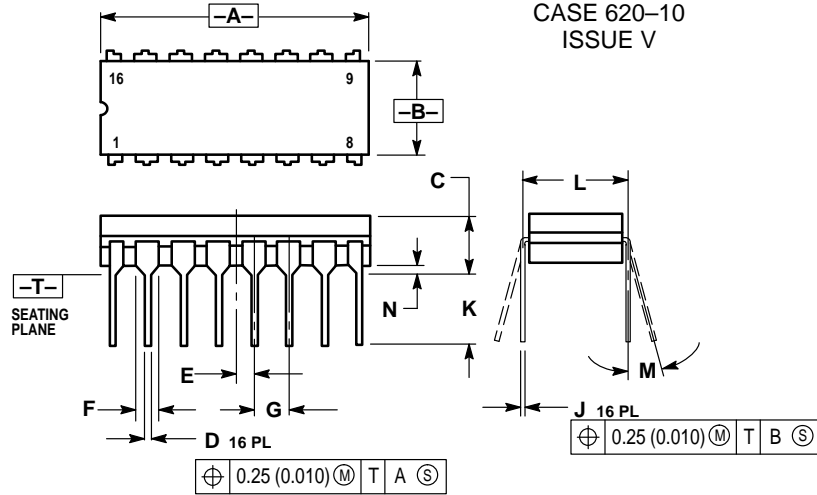
## ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature			TEST VOLTAGE VALUES (Volts)					(V <sub>CC</sub> ) Gnd	
			V <sub>IHmax</sub>	V <sub>ILmin</sub>	V <sub>IHAmin</sub>	V <sub>ILAmax</sub>	V <sub>EE</sub>		
-30°C			-0.890	-1.890	-1.205	-1.500	-5.2		
+25°C			-0.810	-1.850	-1.105	-1.475	-5.2		
+85°C			-0.700	-1.825	-1.035	-1.440	-5.2		
Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW						
			V <sub>IHmax</sub>	V <sub>ILmin</sub>	V <sub>IHAmin</sub>	V <sub>ILAmax</sub>	V <sub>EE</sub>		
Power Supply Drain Current	I <sub>E</sub>	8						1, 16	
Input Current	I <sub>inH</sub>	3	3				8	1, 16	
		5	5				8	1, 16	
Output Voltage	Logic 1	V <sub>OH</sub>	2 15	3, 4, 5 14			8 8	1, 16	
								1, 16	
Output Voltage	Logic 0	V <sub>OL</sub>	2 15	4, 5 13, 14			8 8	1, 16	
								1, 16	
Threshold Voltage	Logic 1	V <sub>OHA</sub>	2 15			5 13	8 8	1, 16	
								1, 16	
Threshold Voltage	Logic 0	V <sub>OLA</sub>	2 15			5 13	8 8	1, 16	
								1, 16	
Switching Times	(50Ω Load)					Pulse In	Pulse Out	-3.2 V	+2.0
Propagation Delay	t <sub>13+15+</sub> t <sub>14-15-</sub> t <sub>3+2-</sub> t <sub>3-15+</sub>	15 15 2 15						8 8 8 8	1, 16
									1, 16
									1, 16
									1, 16
Rise Time	(20 to 80%)	t <sub>2+</sub>	2			3	2	8	1, 16
Fall Time	(20 to 80%)	t <sub>2-</sub>	2			3	2	8	1, 16

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

OUTLINE DIMENSIONS

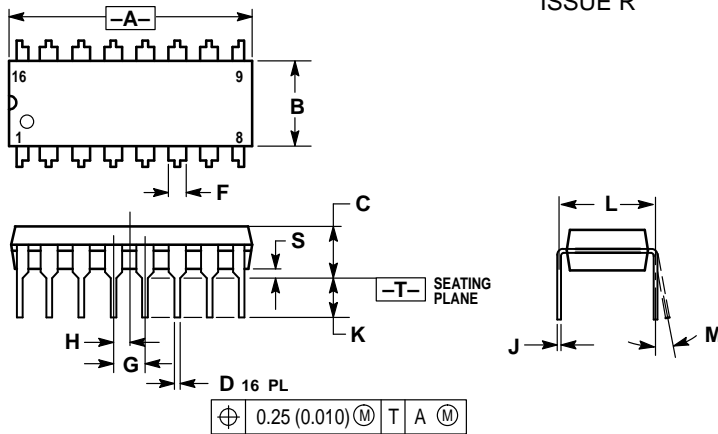
L SUFFIX  
CERAMIC DIP PACKAGE  
CASE 620-10  
ISSUE V



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
  4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

P SUFFIX  
PLASTIC DIP PACKAGE  
CASE 648-08  
ISSUE R



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
  4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
  5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

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