LXT335

Quad Short Haul PCM Analog Interface

General Description

The LXT335 is a quad, short-haul, PCM analog line interface for 2.048 Mhz transmission systems. It includes four independent data receivers and four independent line drivers in a single, 64-pin QFP package. Its low impedance transmit output drivers provide constant line impedance whether transmitting marks or spaces. The output pulse amplitudes are also constant, and are stabilized against supply voltage variations. The LXT335 is configurable for either balanced 120 Ω or unbalanced 75 Ω systems and exceeds latest ETSI return loss recommendations. .All transmitters incorporate a power down mode with output tri-stating.

The LXT335 features a differential receiver architecture with high noise interference margin. It uses peak detection with a variable threshold for reliable data recovery as low as 500 mV (up to 12 dB of cable attenuation). Each receiver incorporates an analog loss of signal (LOS) detector that meets latest ITU standards. The LXT335 features a driver failure monitoring circuit in parallel to TTIP and TRING that reports driver shorts.

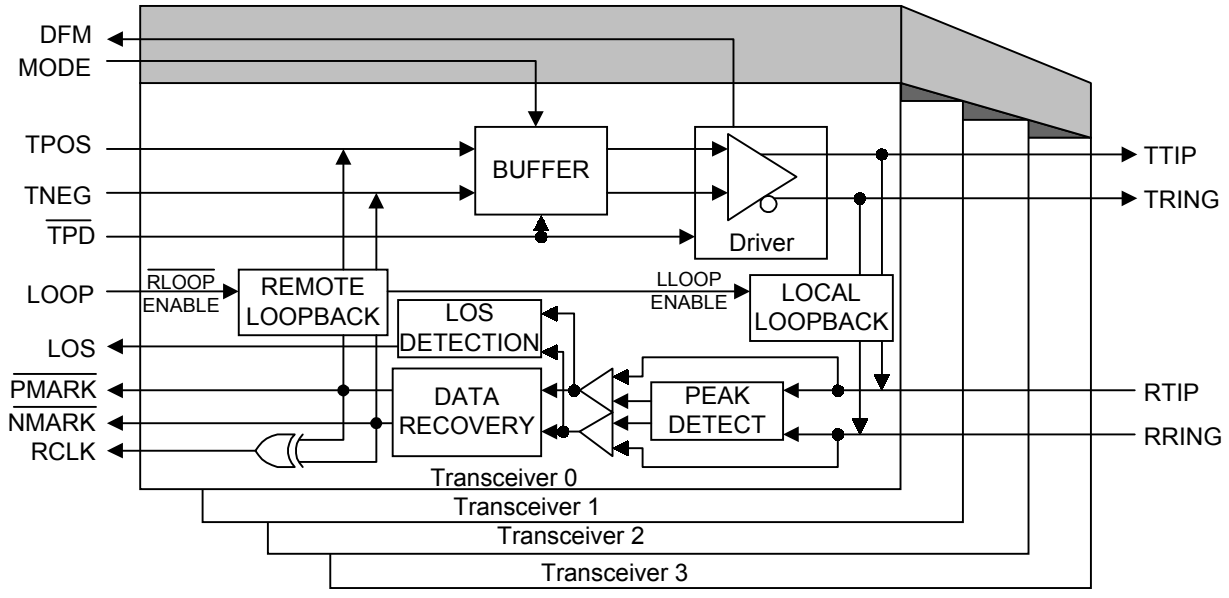
Applications

- High-density E1 line interface cards using digital backend ASICS
- Multiplexers, digital crossconnects, SDH systems

Features

- Quad E1 short haul PCM analog front-end per ITU G.703
- Single rail supply voltage of 5 V (typical)
- Low power consumption of 410 mW (typical)
- Four independent high-performance line drivers with constant low impedance for typical 20 db return loss
- Voltage stabilized output amplitudes
- Four high performance line receivers with 14 db, single tone interference margin
- Data recovery for cable attenuation of up to 12 db at 1024 khz
- On-chip driver short circuit monitoring function
- Local and remote loopback testing function
- Small footprint 64-pin QFP package

LXT335 Block Diagram



PIN ASSIGNMENTS AND SIGNAL DESCRIPTIONS

Figure 1: LXT335 (QE) Pinout Diagram

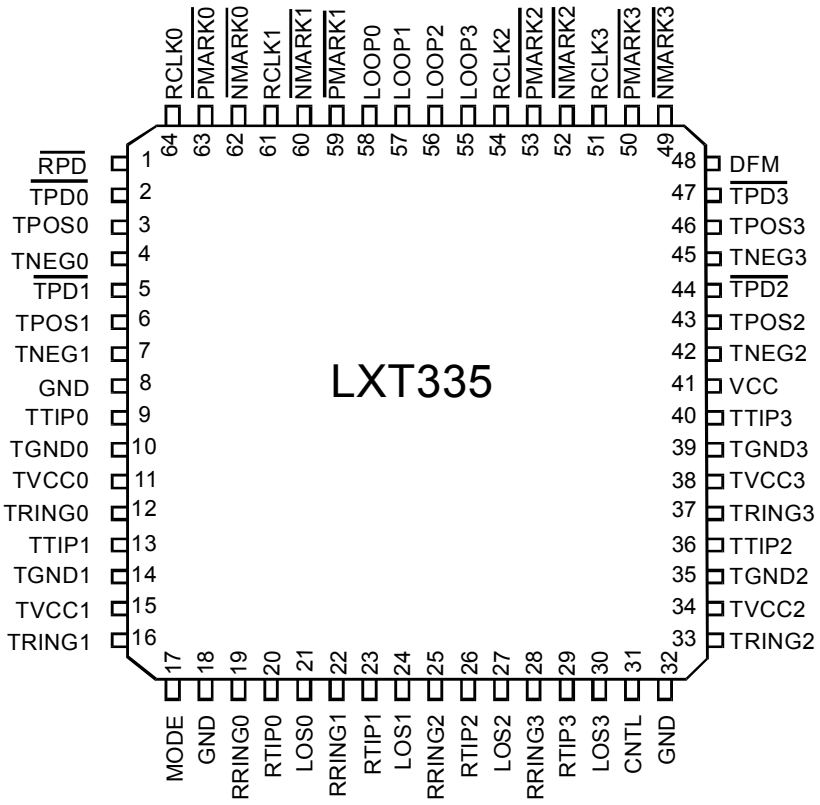


Table 1: Pin Descriptions

Pin #	Sym	I/O[1]	Description
1	$\overline{\text{RPD}}$	DI	**Receive Power Down.** When this pin is asserted Low, LXT335 powers down all four receivers and switches the receiver output pins $\overline{\text{PMARK}}$, $\overline{\text{NMARK}}$ and RCLK to tri-state mode.
2	$\overline{\text{TPD0}}$	DI	**Transmit Power Down Input–Port 0.** All TPD*x* pins are identical. With TPD asserted Low, the transmit drivers enter a low-power, High-Z mode with all analog and digital circuitry powered down. TPD — Operating Mode H — Normal Operation Mode L — Power Down Transmitter

1. Entries in I/O column are DI = Digital Input; DO = Digital Output; DIO = Digital Input Output; AI = Analog Input; AO = Analog Output; High Z = high impedance input/output; S = power/ground pins

Table 1: Pin Descriptions – continued

Pin #	Sym	I/O[1]	Description
3	TPOS0	DI	**Transmit Positive Data-Port 0.** **Transmit Negative Data-Port 0.** All TPOS*x*/TNEG*x* pins are identical. These pins act as active High RZ data inputs for the positive and negative pulse to be transmitted to the line. The transmit pulse width is determined by the duty cycle of TPOS and TNEG.
4	TNEG0	DI	
5	$\overline{\text{TPD1}}$	DI	**Transmit Power Down Input–Port 1.** See $\overline{\text{TPD0}}$, pin 2.
6	TPOS1	DI	**Transmit Positive Data–Port 1.** **Transmit Negative Data–Port 1.** See TPOS0/TNEG0, pins 3 and 4.
7	TNEG1	DI	
8	GND	S	**Ground.**
9	TTIP0	AO	**Transmit Tip Output–Port 0.** All TTIP*x* pins are identical. The TTIP0/TRING0 pins are the differential line driver outputs of transceiver 0.
10	TGND0	S	**Transmit Ground-Port 0.**
11	TVCC0	S	**Transmit Positive Supply–Port 0.**
12	TRING0	AO	**Transmit Ring Output–Port 0.** All TRING*x* are identical. The TTIP0/TRING0 pins are the differential line driver outputs of transceiver 0.
13	TTIP1	AO	**Transmit Tip Output–Port 1.** See TTIP0, pin 9.
14	TGND1	S	**Transmit Ground-Port 1.**
15	TVCC1	S	**Transmit Positive Supply–Port 1.**
16	TRING1	AO	**Transmit Ring Output–Port 1.** See TRING0, pin 12.
17	MODE	DI	**Mode Select Input.** If this pin is asserted Low all LXT335 drivers are configured for low power unmatched line drive mode. If this pin is asserted High all LXT335 line drivers are configured for matched line drive mode. MODE — Operating Mode L — Unmatched Line Drive Mode H — Matched Line Drive Mode
18	GND	S	**Ground.**

1. Entries in I/O column are DI = Digital Input; DO = Digital Output; DIO = Digital Input Output; AI = Analog Input; AO = Analog Output; High Z = high impedance input/output; S = power/ground pins

Table 1: Pin Descriptions – continued

Pin #	Sym	I/O[1]	Description
19 20	RRING0 RTIP0	AI AI	**Receive Ring Input–Port 0.** **Receive Tip Input–Port 0.** All RTIP*x*/RRING*x* pins are identical. These pins are the inputs of the fully differential line receiver.
21	LOS0	DO High Z	**Loss of Signal Output–Port 0.** All LOS*x* pins are identical. This output is asserted High when the incoming signal is more than 22 dB below the nominal 0 dB level. The LOS condition is cleared and the output is deasserted if the incoming signal is equal to or greater than 21 dB below the nominal 0 dB level. During a driver fail condition this pin acts as driver 0 fail monitor output.
22 23	RRING1/ RTIP1	AI AI	**Receive Ring Input–Port 1.** **Receive TIP Input–Port 1.** See RTIP0/RRING0, pins 19 and 20.
24	LOS1	DO	**Loss of Signal Output–Port 1.** See LOS0, pin 21.
25 26	RRING2/ RTIP2	AI AI	**Receive Ring Input–Port 2.** **Receive TIP Input–Port 2.** See RTIP0/RRING0, pins 19 and 20.
27	LOS2	DO	**Loss of Signal Output–Port 2.** See LOS0, pin 21.
28 29	RRING3/ RTIP3	AI AI	**Receive Ring Input–Port 3.** **Receive TIP Input–Port 3.** See RTIP0/RRING0, pins 19 and 20.
30	LOS3	DO	**Loss of Signal Output–Port 3.** See LOS0, pin 21.
31	CNTL	DI	**Pulse Amplitude Control Input.** If this pin is asserted High the transmitter operation mode is pin selectable via MODE between 75 and 120 Ohm without changing external components. If this pin is asserted Low the line driver operation modes may be selected via MODE. CNTL MODE Result L L Unmatched Line Driver Mode L H Matched Line Driver Mode H L Pin Selectable Driver Mode (120 Ω) H H Pin Selectable Driver Mode (75 Ω)
32	GND	S	**Ground.**

1. Entries in I/O column are DI = Digital Input; DO = Digital Output; DIO = Digital Input Output; AI = Analog Input; AO = Analog Output; High Z = high impedance input/output; S = power/ground pins

Table 1: Pin Descriptions – continued

Pin #	Sym	I/O[1]	Description
33	TRING2	AO	**Transmit Ring Output–Port 2.** See TRING0, pin 12.
34	TVCC2	S	**Transmit Power Supply-Port 2.**
35	TGND2	S	**Transmit Ground-Port 2.**
36	TTIP2	AO	**Transmit Tip Output–Port 2.** See TTIP0, pin 9.
37	TRING3	AO	**Transmit Ring Output–Port 3.** See TRING0, pin 12.
38	TVCC3	S	**Transmit Power Supply-Port 3.**
39	TGND3	S	**Transmit Ground-Port 3**
40	TTIP3	AO	**Transmit Tip Output–Port 3** See TTIP0, pin 9.
41	VCC	S	**Receiver Positive Supply.**
42	TNEG2	DI	**Transmit Negative Data Input–Port 2.** **Transmit Positive Data Input–Port 2.** See TPOS0/TNEG0, pins 3 and 4.
43	TPOS2	DI	
44	$\overline{\text{TPD2}}$	DI	**Transmit Power Down Input–Port 2.** See $\overline{\text{TPD0}}$, pin 2.
45	TNEG3	DI	**Transmit Negative Data Input–Port 3.** **Transmit Positive Data Input–Port 3**. See TPOS0/TNEG0, pins 3 and 4.
46	TPOS3	DI	
47	$\overline{\text{TPD3}}$	DI	**Transmit Power Down Input–Port 3.** See $\overline{\text{TPD0}}$, pin 2.
48	DFM	DO	**Driver Failure Monitor Output**. When this pin is High it indicates that a driver short has been detected in one of the four drivers. The transceiver LOS*x* output identifies the specific failing driver in this case.
49	$\overline{\text{NMARK3}}$	DO	**Receive Negative Data Output–Port 3.** **Receive Positive Data Output–Port 3.** All $\overline{\text{NMARKx}}$/$\overline{\text{PMARKx}}$ pins are identical. These pins act as active Low bipolar return-to-zero (RZ) receive data outputs. A Low on an $\overline{\text{NMARKx}}$ pin corresponds to a receipt of a positive pulse on RRING. A Low on a $\overline{\text{PMARKx}}$ pin corresponds to a receipt of a positive pulse on RTIP.
50	$\overline{\text{PMARK3}}$	DO	

1. Entries in I/O column are DI = Digital Input; DO = Digital Output; DIO = Digital Input Output; AI = Analog Input; AO = Analog Output; High Z = high impedance input/output; S = power/ground pins

Table 1: Pin Descriptions – continued

Pin #	Sym	I/O[1]	Description
51	RCLK3	DO	**Receive Clock Output–Port 3.** All RCLK*x* pins are identical. This pin provides a timing signal from the received data at RTIP and RRING. $\overline{\text{PMARK3}}$ and $\overline{\text{NMARK3}}$ are internally connected to an XOR gate. The output of this gate goes to the RCLK3 output for external clock recovery applications.
52	$\overline{\text{NMARK2}}$	DO	**Receive Negative Data Output–Port 2.** **Receive Positive Data–Port 2.** SEE $\overline{\text{NMARK3}}$/$\overline{\text{PMARK3}}$, pins 49, 50.
53	$\overline{\text{PMARK2}}$	DO	
54	RCLK2	DO	**Receive Clock Output–Port 2** See RCLK3, pin 51.
55	LOOP3	DI	**Loopback Mode Select Input–Port 3.** **Loopback Mode Select Input–Port 2.** **Loopback Mode Select Input–Port 1.** **Loopback Mode Select Input–Port 0.** All LOOP*x* pins are identical. If this pin is asserted High Local Analog Loopback is selected which causes LXT335 to ignore data received on RTIP and RRING and loop data internally from TTIP and TRING back to the receive inputs. If this pin is asserted Low Remote Loopback is selected which causes LXT335 to ignore data on $\overline{\text{NMARK}}$ and $\overline{\text{PMARK}}$ and to loop internally data received on RTIP and RRING to TTIP and TRING. If this pin is left open or unconnected normal operation mode is selected. LOOP*x* — Operating Mode L — Remote Loopback H — Local Loopback Open — Normal Operation Mode
56	LOOP2	DI	
57	LOOP1	DI	
58	LOOP0	DI	
59	$\overline{\text{NMARK1}}$	DO	**Receive Negative Data / Bipolar Violation Indication Output–Port 1** **Receive Positive Data/ Receive Data Output–Port 1** See $\overline{\text{NMARK3}}$/$\overline{\text{PMARK3}}$, pins 49, 50.
60	$\overline{\text{PMARK1}}$	DO	
61	RCLK1	DO	**Receive Clock Output–Port 1** See RCLK3, pin 51.
62	$\overline{\text{NMARK0}}$	DO	**Receive Negative Data Output–Port 0** **Receive Positive Data/ Receive Data Output–Port 0** See $\overline{\text{NMARK3}}$/$\overline{\text{PMARK3}}$, pins 49, 50.
63	$\overline{\text{PMARK0}}$	DO	
64	RCLK0	DO	**Receive Clock Output–Port 0** See RCLK3, pin 51.

1. Entries in I/O column are DI = Digital Input; DO = Digital Output; DIO = Digital Input Output; AI = Analog Input; AO = Analog Output; High Z = high impedance input/output; S = power/ground pins

FUNCTIONAL DESCRIPTION

Page 1 shows a simplified block diagram of the LXT335. The LXT335 is a quad line interface unit with four on-chip transmit drivers and four data receivers optimized for G.703 2.048 MHz applications. The front end of each line interface interfaces with four lines, one pair for transmit, one pair for receive. These two lines comprise a digital data loop for full duplex transmission. Each line interface also interfaces with back-end processors, through bipolar data I/O channels, and allows control by hardwired pins for stand-alone operation.

Receiver

The four LXT335 receivers are identical. The following paragraphs describe the operation of a single receiver. LXT335 receives the input signal via a 1:1 transformer. Recovered data is active low and output at $\overline{\text{PMARK}}$ and $\overline{\text{NMARK}}$. Timing information for external clock recovery is output at RCLK.

A peak detector and data slicers process the received signal. The peak detector samples the received signal and determines its maximum value. A percentage of the peak value is provided to the data slicers as a threshold level of 50% to ensure an optimum signal-to-noise ratio.

The receiver is capable of accurately recovering signals with up to 12 dB of cable attenuation (from 2.4 V), corresponding to a received signal level of approximately 500 mV. Regardless of received signal level, LXT335 holds its peak detectors above a minimum level of 0.225 V (typical) to provide immunity from impulsive noise.

After the data slicers process, the received signal goes to the data recovery and pulse stretcher section and then to the receive outputs $\overline{\text{PMARK}}$ and $\overline{\text{NMARK}}$.

Loss Of Signal Detector

The Loss of Signal Detector uses an analog detection scheme and complies with the ITU G.775 recommendation. During LOS conditions, received data is output on $\overline{\text{PMARK}}$/$\overline{\text{NMARK}}$. Any signal ~22 dB below the nominal 0 dB signal generates a loss of signal condition. LOS is deactivated again when the signal level rises to more than ~21 dB (typical) below the minimum 0 dB level. The $\overline{\text{PMARK}}$ and $\overline{\text{NMARK}}$ outputs stay active for external digital signal transition detection.

Transmitter

The four LXT335 low power transmitters are identical. The following paragraphs describe the operation of a single transmitter.

Bipolar transmit data from the digital backend processor is fed into the device at TPOS/TNEG and is passed through "as is". If $\overline{\text{TPD}}$ is asserted Low the transmitter remains powered down and the TTIP/TRNG outputs are held in a High-Z state. This feature allows use of the LXT335 in fully redundant applications.

Each output driver is supplied by a separate power supply (TVCC0 to TVCC3, TGND0 to TGND3). Current limiters on the output drivers provide short circuit protection and generate a driver failure monitoring signal in case the current limit is exceeded.

The transmitted pulse shape must be generated externally. Pulses are applied to the line drivers for transmission onto the line at TTIP and TRING. The line driver provides a constant low output impedance of < 3 Ω (typical) regardless of whether it is driving marks or spaces or during transitions. LXT335 provides programmable pulse amplitude output voltages.

If MODE is asserted High, the LXT335 is configured for matched line driver applications. In conjunction with external series resistors a well controlled driver output impedance provides excellent transmit return loss exceeding ETSI ETS300166 and Swiss PTT recommendations. If MODE is asserted Low, the LXT335 is configured for unmatched low power line driver applications where it drives a transformer without series resistors.

Asserting CNTL High and MODE Low, configures the LXT335 for 120 Ω loads. Asserting CNTL High and MODE High configures the LXT335 for 75 Ω loads. In transformer coupled applications the LXT335 produces 2.048 MHz pulses for both 75 Ω coaxial (2.37 V) and 120 Ω shielded twisted-pair (3.0 V) lines. Different transformer and resistor combinations are used for optimum transmit return loss performance. Internal circuitry stabilizes the output pulse amplitudes against supply variations and references them to an on-chip bandgap voltage reference.

Certain applications require common 1:2 transformers for the transmitter and receiver and software switchable 75/120 Ω operation while maintaining return loss in compliance with ETS300166. The LXT335 can be used with 25Ω transmit series resistors for both 75Ω and 120Ω operation (Figure 8).

Driver Failure Monitor

All transceiver incorporate internal Driver Failure Monitors (DFM) in parallel with TTIP and TRING. A capacitor, charged via a measure of the driver output current and discharged by a measure of the maximum allowable current, is used to detect driver failures. Shorted lines draw excess current, overcharging the cap. When the capacitor charge deviates outside the nominal charge window for one of the 4 drivers, the common DFM output pin reports a driver short circuit fail. The individual driver failure monitor output takes precedence and overwrites the transceiver specific LOS output. During a long string of spaces, a short-induced overcharge eventually bleeds off, clearing the DFM flag.

Diagnostic Mode Of Operation

Loopback

All LOOP*x* pins are identical. If this pin is asserted High, Local Analog Loopback is selected which causes LXT335 to ignore data received on RTIP and RRING and loop data internally from TTIP and TRING back to the receive inputs. If this pin is asserted Low, Remote Loopback is selected which causes LXT335 to ignore data on $\overline{\text{NMARK}}$ and $\overline{\text{PMARK}}$ and to loop internally data received on RTIP and RRING to TTIP and TRING.

If this pin is left open or unconnected normal operation mode is selected.

APPLICATION INFORMATION

Figure 2: Low Power Transmit Interface for Coax Cables

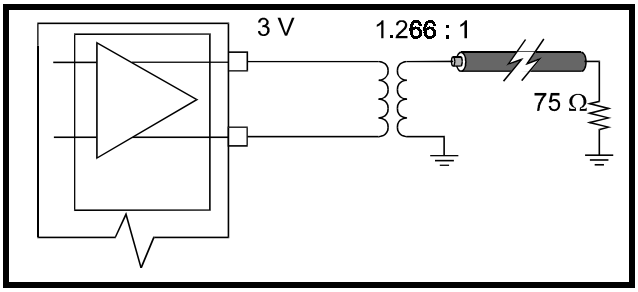


Figure 3: Transmit Interface for Coax Cables

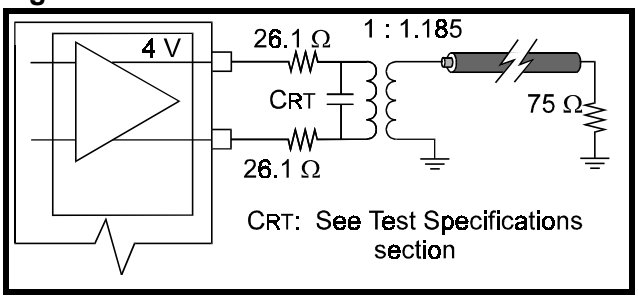


Figure 4: Low Power Transmit Interface for Twisted Pair Lines

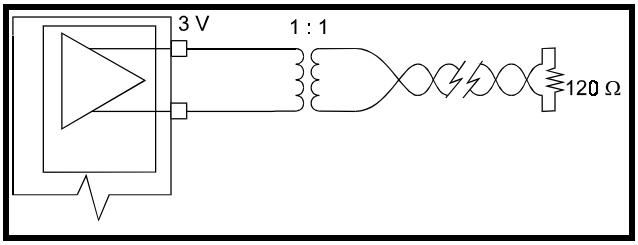


Figure 5: Transmit Interface for Twisted Pair Lines

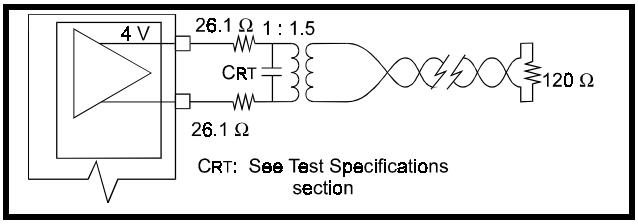


Figure 6: Receive Interface for Twisted Pair Lines

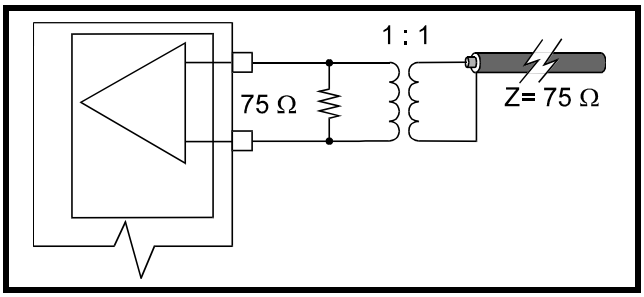


Figure 7: Receive Interface for Twisted-Pair Lines

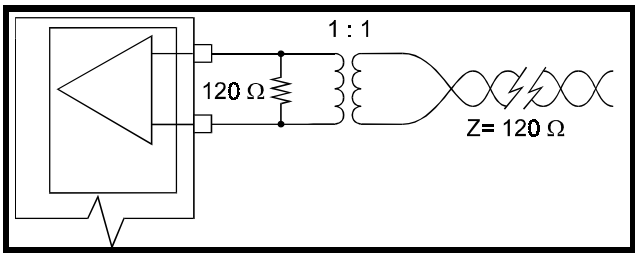


Table 2: Transformer Selection Guide[1]

Manufacturer	Transmit Side		Receive side (1:1 Ratio) (20 dB Return Loss)
	Part Number	Transformer Turns Ratio	Type
Pulse Engineering	PE-65586	1:1.36	Quad
	PE-65766	1:1.266	Dual
	PE-68789	1:1.5	Dual
	PE-65762	1:1.36	Dual
	PE-65861	1:2	Dual
	PE-65861	1:1	Dual
	PE-68789	1:1.185	Single
	PE-65389	1.266:1	Single
HALO	TG27-1505NX	1:1.36	Octal
	TD64-1205D	1:1.26	Dual
	TG29-1205NX	1:2	Octal
Bel-Fuse	0553-0013	1:1.36	Dual
	5006-1C	1:2	Dual
Schott Corp	67129300	1:2	Single

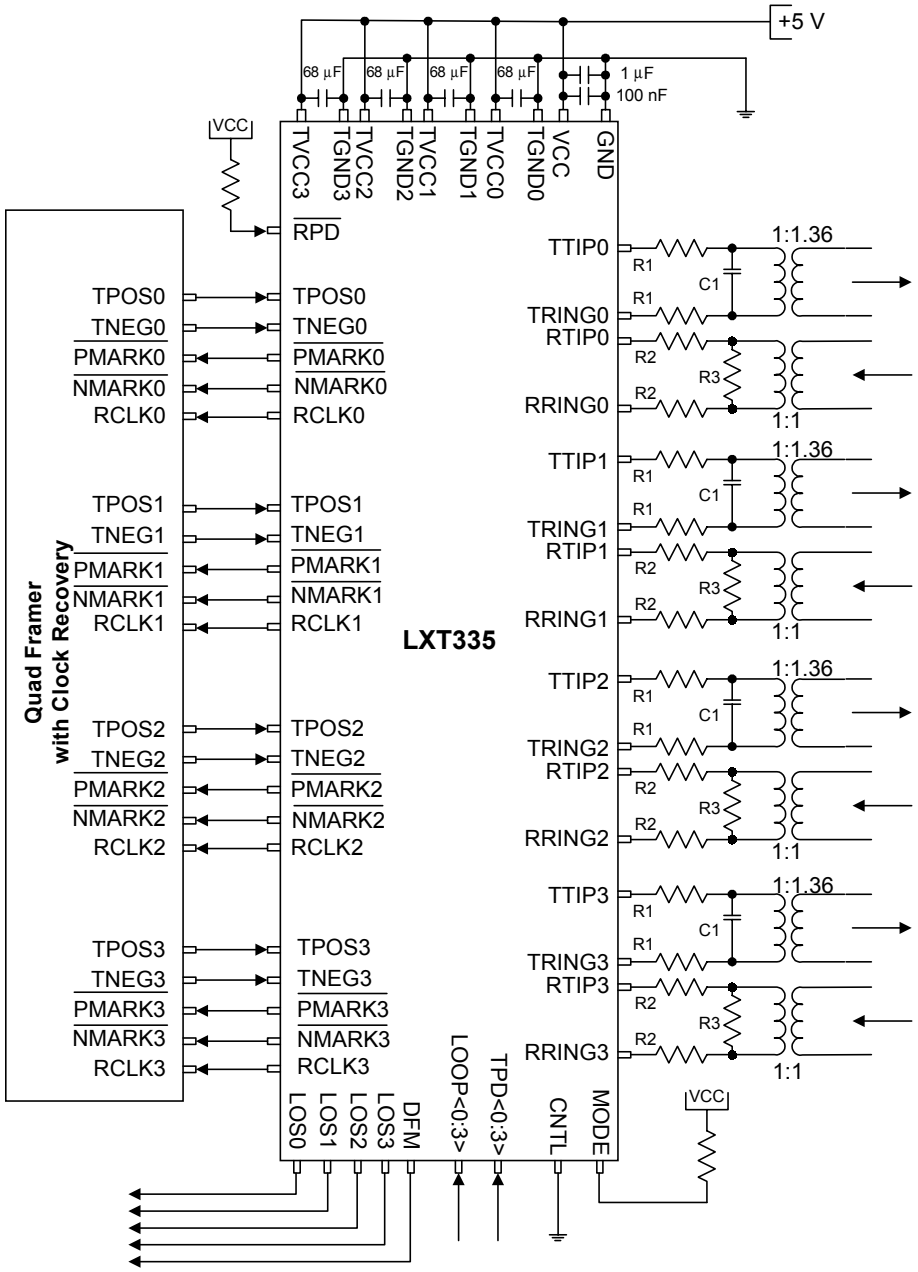
1. As of the publication date, Level One Communications, Inc., has tested the transformers listed in this table. However, part numbers and specifications change without notice. Design engineers should validate components before committing to their use.

Table 3: Transmit Transformer and Resistor Combinations

Transformer	Resistor	Return Loss[1]	CNTL1	MODE1	Impedance
1.266:1	0 Ω	< 1 dB	Low	Low	75 Ω
1:1	0 Ω	< 1 dB	Low	Low	120 Ω
1:1.185	26.1 Ω	20 dB	Low	High	75 Ω
1:1.5	26.1 Ω	20 dB	Low	High	120 Ω
1:1.36	25 Ω	18 dB	Low	High	75 Ω
1:1.36	25 Ω	18 dB	Low	High	120 Ω
1:2	15 Ω	≥ 8 dB	High	High	75 Ω
1:2	15 Ω	≥ 8 dB	High	Low	120 Ω

1. Typical values 51 kHz - 3.078 MHz

Figure 8: E1 120 Ω and 75 Ω Matched Line Applications



Component	Application	
	120 Ω	**75 Ω**
R1. Transmit resistor	25 Ω	25 Ω
R2. Receive resistor	1 kΩ	1 kΩ
R3. Receive terminating resistor	120 Ω	75 Ω
C1. Transmit capacitor (typical)	180 pF	180 pF

TEST SPECIFICATIONS

NOTE

The minimum and maximum values in Tables 4 through 9 and Figures 9 and 10 are performance specifications of the LXT335 and are guaranteed by test except, where noted, by design.

Table 4: Absolute Maximum Ratings

Parameter	Sym	Min.	Max.	Unit
DC supply voltage	V_{CC}, GND	-0.3	6.0	V
Input voltage on any pin [1]	V_{IN}	GND-0.3	RV_{CC} + 0.3	V
Input voltage on RTIP, RRING	V_{IN}	-6	RV_{CC} + 0.3	V
Transient latchup current on any pin[2]	I_{IN}	–	100	mA
Input current on any digital pin[3]	I_{IN}	-10	10	mA
DC input current on TTIP, TRING[3]	I_{IN}	–	±100	mA
DC input current on RTIP, RRING[3]	I_{IN}	–	±20	mA
Storage temperature	T_{STOR}	-65	+150	° C
Total package power dissipation	–	–	1	W

CAUTION

Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to absolute maximum ratings conditions for external periods may affect device reliability.

1. Reference to ground.
2. Exceeding these values will cause SCR latchup.
3. Constant input current.

Table 5: Recommended Operating Conditions

Parameter	Sym	Min	Typ	Max	Units	Test Condition
DC supply voltage [1]	V_{CC}	4.75	5.0	5.25	V	
Ambient operating temperature	T_A	-40	+25	+85	° C	

1. TV_{CC} must not exceed RV_{CC} BY 0.3 V

Table 6: DC Characteristics (over recommended range)

Parameter		Sym	Min	Typ[1]	Max	Unit	Test Condition
Digital I/O pins	High-level input voltage	VIH	2.0	–	–	V	
	Low-level input voltage	VIL	—	–	0.8	V	
	High-level output voltage[2]	VOH	3.5	–	–	V	IOUT= -400µA
	Low-level output voltage[2]	VOL	—	–	0.4	V	IOUT= 1.6 mA
Input leakage current (digital input pins)		IIL	-10	–	+10	µA	
Tristate leakage current[5]		IHZ	-10		+10	µA	
Driver short circuit current		–	–	–	50	mA	See Figures 3 and 5
MODE input pins	Low-level input voltage	VINL	–	–	1.5	V	pins 17, 55, 56, 57, 58
	High-level input voltage	VINH	3.5	–	–	V	
	Mid-range input voltage	VINM	2.3	2.5	2.7	V	
	Low-level input current	IINL	–	–	50	µA	
	High-level input current	IINH	–	–	50	µA	
Total power dissipation [3]	75 Ω system (MODE=H)	PD	–	660	750	mW	Figure 3
	120 Ω system (MODE=H)	PD	–	660	750	mW	Figure 5
Total power dissipation[4]	75 Ω system (MODE=L)	PD	–	410	470	mW	Figure 2
	120 Ω system (MODE=L)	PD	–	410	470	mW	Figure 4
Power down current		ICCO	–	–	10	mA	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Output Drivers will output CMOS logic levels into CMOS loads.
3. 100% 1s density. Power dissipation including device load while driving a matched line over the operating temperature range. Digital inputs are within 10% of the supply rails and digital outputs are driving a 50 pF load.
4. 50% 1s density. Power dissipation including device load while driving a line without matching resistors over the operating temperature range. Digital inputs are within 10% of the supply rails and digital outputs are driving a 50 pF load.
5. Applies to the following pins: 9, 12, 13, 16, 33, 36, 37, 40, 49-54, 59-64.

Table 7: Receive Characteristics

Parameter		Sym	Min	Typ	Max	Units	Test Condition
Permissible cable attenuation		–	500	–	–	mV	
		–	–	–	12	dB	@1024 kHz
Receiver dynamic range		DR	0.5	–	4.2	VP	
Signal to noise interference margin[1]		S/I	15	–	–	dB	per G.703, O.151
Signal to single tone interference margin		S/X	14	–	–	dB	O.151
$\overline{\text{PMARK}}$ / $\overline{\text{NMARK}}$ output Jitter		–	–	0.01	–	U.I.	peak to peak
Slicer ratio		SRE	43	50	57	%	rel. to peak input voltage
Analog loss of signal threshold		–	22	–	–	dB	
Loss of signal threshold		–	–	1	–	dB	
Receiver input impedance		–	–	40	–	kΩ	@ 1.024 kHz, RTIP to RRING
Input return loss[2]	51 kHz – 102 kHz	–	20	–	–	dB	measured against nominal impedance, Figures 6, 7.
	102 – 2048 kHz	–	20	–	–	dB	
	2048 kHz – 3072 kHz	–	20	–	–	dB	

1. No errors shall occur when the combined signal attenuated by the maximum specified interconnting cable loss is applied to the input port. See ITU O.151 recommendation for further details.
2. Guaranteed by design and other correlation factors.

Table 8: Transmit Timing Characteristics

Parameter	Sym	Min	Typ	Max	Unit	Test Condition
Transmit data rate	–	–	2.048	–	Mbps	
Transmit data tolerance	–	-50	–	50	ppm	
Output pulse width	tPW	–	244	–	ns	

Table 9: Receive Timing Characteristics (See Figure 9)

Parameter	Sym	Min	Typ	Max	Units	Test Condition
$\overline{\text{PMARK}}$/$\overline{\text{NMARK}}$ pulse width	tMPW	200	244	300	ns	
Receiver throughput delay	tRXD	–	65	–	ns	
Receive data rate tolerance	–	–	±80	–	ppm	
Receive data to receive clock delay time	–	–	5	–	ns	

Figure 9: Receive Timing Specifications

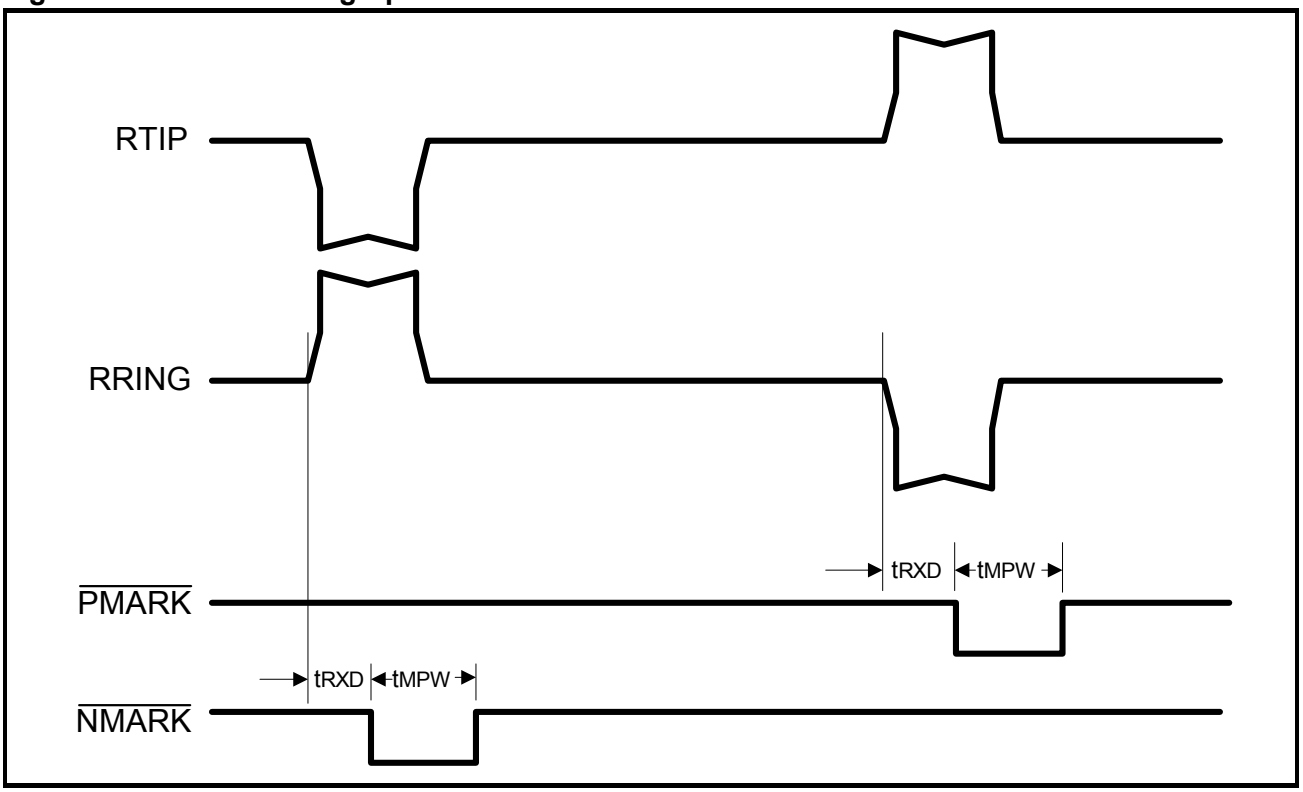
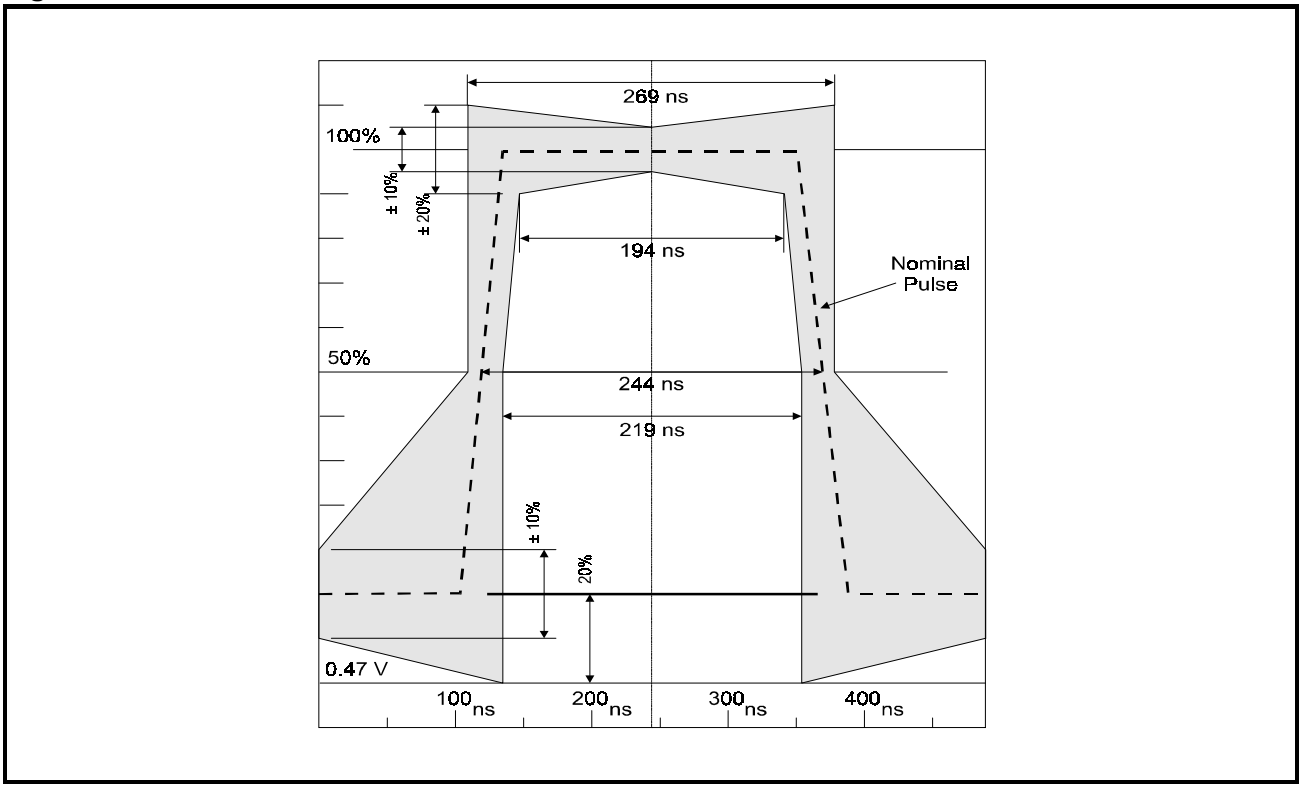


Figure 10: 2.048 MHz Pulse Mask G.703



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