500mA Power Op Amp with Adjustable Precision Current Limit

FEATURES

- **±500mA Minimum Output Current**
- **Independent Adjustment of Source and Sink Current Limits**
- **2% Current Limit Accuracy**
- Operates with Single or Split Supplies
- Shutdown/Enable Control Input
- Open Collector Status Flags:
  - Sink Current Limit
  - Source Current Limit
  - Thermal Shutdown
- Fail Safe Current Limit and Thermal Shutdown
- 1.6V/µs Slew Rate
- 3.6MHz Gain Bandwidth Product
- Fast Current Limit Response: 2MHz Bandwidth
- Specified Temperature Range: –40°C to 85°C

APPLICATIONS

- Automatic Test Equipment
- Laboratory Power Supplies
- Motor Drivers
- Thermoelectric Cooler Driver

DESCRIPTION

The LT®1970 is a ±500mA power op amp with precise externally controlled current limiting. Separate control voltages program the sourcing and sinking current limit sense thresholds with 2% accuracy. Output current may be boosted by adding external power transistors.

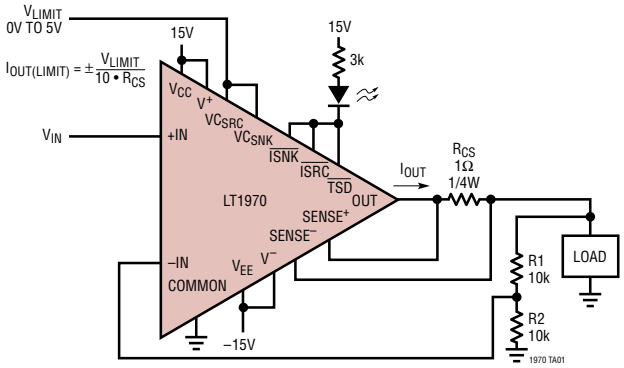
The circuit operates with single or split power supplies from 5V to 36V total supply voltage. In normal operation, the input stage supplies and the output stage supplies are connected (V_{CC} to V^+ and V_{EE} to $V^–$). To reduce power dissipation it is possible to power the output stage (V^+, $V^–$) from independent, lower voltage rails. The amplifier is unity-gain stable with a 3.6MHz gain bandwidth product and slews at 1.6V/µs. The current limit circuits operate with a 2MHz response between the VC_{SRC} or VC_{SNK} control inputs and the amplifier output.

Open collector status flags signal current limit circuit activation, as well as thermal shutdown of the amplifier. An enable logic input puts the amplifier into a low power, high impedance output state when pulled low. Thermal shutdown and a ±800mA fixed current limit protect the chip under fault conditions.

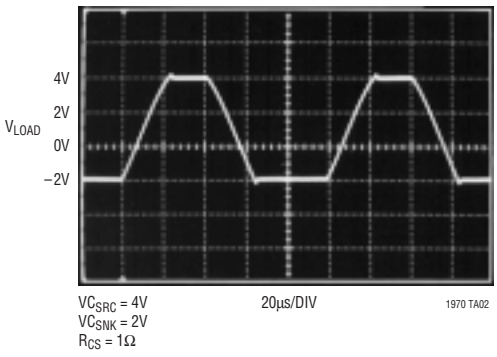
The LT1970 is packaged in a 20-lead TSSOP package with a thermally conductive copper bottom plate to facilitate heat sinking.

TYPICAL APPLICATION

A_V = 2 Amplifier with Adjustable ±500mA Full-Scale Current Limit and Fault indication



Current Limited Sinewave Into 10Ω Load

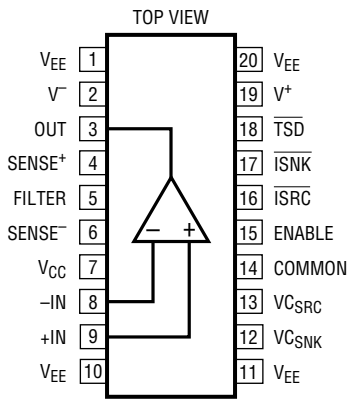


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC} to V_{EE}) 36V
Positive High Current Supply (V^+) ..... V^- to V_{CC}
Negative High Current Supply(V^-) ..... V_{EE} to V^+
Amplifier Output (OUT) ..... V^- to V^+
Current Sense Pins
($SENSE^+$, $SENSE^-$, FILTER) ..... V^- to V^+
Logic Outputs ($\overline{ISRC}$, $\overline{ISNK}$, $\overline{TSD}$) ..... COMMON to V_{CC}
Input Voltage (–IN, +IN) ..... V_{EE} – 0.3V to V_{EE} + 36V
Input Current 10mA
Current Control Inputs
(VC_{SRC}, VC_{SNK}) .....COMMON to COMMON + 7V
Enable Logic Input ..... COMMON to V_{CC}
COMMON ..... V_{EE} to V_{CC}
Output Short-Circuit Duration ..... Indefinite
Operating Temperature Range (Note 2) .. –40°C to 85°C
Specified Temperature Range (Note 3) ... –40°C to 85°C
Maximum Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec).....300°C

PACKAGE/ORDER INFORMATION



FE PACKAGE
20-LEAD PLASTIC TSSOP

T_{JMAX} = 150°C, θ_{JA} = 40°C/W (NOTE 6)

UNDERSIDE METAL CONNECTED TO V_{EE}

ORDER PART NUMBER
LT1970CFE

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. See Test Circuit for standard test conditions.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Op Amp Characteristics							
V_{OS}	Input Offset Voltage				200	600	µV
		0°C < T_A < 70°C	●			800	µV
		–40°C < T_A < 85°C	●			1000	µV
	Input Offset Voltage Drift (Note 4)		●	–10	–4	10	µV/°C
I_{OS}	Input Offset Current	V_{CM} = 0V	●	–100		100	nA
I_B	Input Bias Current	V_{CM} = 0V	●	–600	–160		nA
	Input Noise Voltage	0.1Hz to 10Hz			3		μV_{P-P}
e_n	Input Noise Voltage Density	1kHz			15		$nV/\sqrt{Hz}$
i_n	Input Noise Current Density	1kHz			3		$pA/\sqrt{Hz}$
R_{IN}	Input Resistance	Common Mode			500		kΩ
		Differential Mode			100		kΩ
C_{IN}	Input Capacitance	Pin 8 and Pin 9 to Ground			6		pF
V_{CM}	Input Voltage Range	Typical		–14.5		13.6	V
		Guaranteed by CMRR Test	●	–12.0		12.0	V
CMRR	Common Mode Rejection Ratio	–12V < V_{CM} < 12V	●	92	105		dB
PSRR	Power Supply Rejection Ratio	V_{EE} = V^- = –5V, V_{CC} = V^+ = 3V to 30V	●	90	100		dB
		V_{EE} = V^- = –5V, V_{CC} = 30V, V^+ = 2.5V to 30V	●	110	130		dB
		V_{EE} = V^- = –3V to –30V, V_{CC} = V^+ = 5V	●	90	100		dB
		V_{EE} = –30V, V^- = –2.5V to –30V, V_{CC} = V^+ = 5V	●	110	130		dB

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. See Test Circuit for standard test conditions.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
A_{VOL}	Large-Signal Voltage Gain	R_L = 1k, –12.5V < V_{OUT} < 12.5V	 ●	100 75	150		V/mV V/mV
		R_L = 100Ω, –12.5V < V_{OUT} < 12.5V	 ●	80 40	120		V/mV V/mV
		R_L = 10Ω, –5V < V_{OUT} < 5V, V^+ = –V^- = 8V	 ●	20 5	60		V/mV V/mV
V_{OL}	Output Sat Voltage Low	V_{OL} = V_{OUT} – V^- R_L = 100, V_{CC} = V^+ = 15V, V_{EE} = V^- = –15V R_L = 10, V_{CC} = –V_{EE} = 15V, V^+ = –V^- = 5V	 ● 		 1.9 0.8	 2.4 	 V V
V_{OH}	Output Sat Voltage High	V_{OH} = V^+ – V_{OUT} R_L = 100, V_{CC} = V^+ = 15V, V_{EE} = V^- = –15V R_L = 10, V_{CC} = –V_{EE} = 15V, V^+ = –V^- = 5V	 ● 		 1.7 1.0	 2.2 	 V V
I_{SC}	Output Short-Circuit Current	Output Low, R_{SENSE} = 0Ω Output High, R_{SENSE} = 0Ω		500 –1000	800 –800	1200 –500	mA mA
SR	Slew Rate	–10V < V_{OUT} < 10V, R_L = 1k		0.7	1.6		V/µs
FPBW	Full Power Bandwidth	V_{OUT} = 10V_{PEAK} (Note 5)		11			kHz
GBW	Gain Bandwidth Product	f = 10kHz			3.6		MHz
t_S	Settling Time	0.01%, V_{OUT} = 0V to 10V, A_V = –1, R_L = 1k			8		µs
Current Sense Characteristics							
$V_{SENSE(MIN)}$	Minimum Current Sense Voltage	VC_{SRC} = VC_{SNK} = 0V	 ●	0.1 0.1	4	7 10	mV mV
$V_{SENSE(4\%)}$	Current Sense Voltage 4% of Full Scale	VC_{SRC} = VC_{SNK} = 0.2V	●	15	20	25	mV
$V_{SENSE(10\%)}$	Current Sense Voltage 10% of Full Scale	VC_{SRC} = VC_{SNK} = 0.5V	●	45	50	55	mV
$V_{SENSE(FS)}$	Current Sense Voltage 100% of Full Scale	VC_{SRC} = VC_{SNK} = 5V	 ●	490 480	500 500	510 520	mV mV
I_{BI}	Current Limit Control Input Bias Current	VC_{SRC}, VC_{SNK} Pins	●	–1	–0.2	0.1	µA
I_{SENSE^-}	$SENSE^-$ Input Current	0V < (VC_{SRC}, VC_{SNK}) < 5V	●	–200		200	nA
I_{FILTER}	FILTER Input Current	0V < (VC_{SRC}, VC_{SNK}) < 5V	●	–200		200	nA
I_{SENSE^+}	$SENSE^+$ Input Current	VC_{SRC}= VC_{SNK} = 0V VC_{SRC} = 5V, VC_{SNK} = 0V VC_{SRC}= 0V, VC_{SNK} = 5V VC_{SRC} = VC_{SNK} = 5V	● ● ● ●	–500 200 –300 –25	 250 –250 	500 300 –200 25	nA µA µA µA
	Current Sense Change with Output Voltage	VC_{SRC} = VC_{SNK} = 5V, –12.5V < V_{OUT} < 12.5V	●	–0.1		0.1	%
	Current Sense Change with Supply Voltage	VC_{SRC} = VC_{SNK} = 5V, 6V < (V_{CC}, V^+) < 18V 2.5V < V^+ < 18V, V_{CC} = 18V –18V < (V_{EE}, V^-) < –2.5V –18V < V^- < –2.5V, V_{EE} = –18V			±0.05 ±0.01 ±0.05 ±0.01		% % % %
	Current Sense Bandwidth				2		MHz
R_{CSF}	Resistance FILTER to $SENSE^-$		●	750	1000	1250	Ω
Logic I/O Characteristics							
	Logic Output Leakage ISRC, ISNK, TSD	V = 15V	●			1	µA
	Logic Low Output Level	I = 5mA	●		0.2	0.4	V
	Logic Output Current Limit		●		25		mA
V_{ENABLE}	Enable Logic Threshold		●	0.8	1.6	2.4	V
I_{ENABLE}	Enable Pin Bias Current		●	–1		1	µA

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. See Test Circuit for standard test conditions.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{SUPPLY}	Total Supply Current	V_{CC}, V^+ and V^-, V_{EE} Connected	●		7	13	mA
I_{CC}	V_{CC} Supply Current	V_{CC}, V^+ and V^-, V_{EE} Separate	●		3	7	mA
$I_{CC(STBY)}$	Supply Current Disabled	V_{CC}, V^+ and V^-, V_{EE} Connected, $V_{ENABLE} \leq 0.8V$	●		0.6	1.5	mA
t_{ON}	Turn-On Delay	(Note 7)			10		µs
t_{OFF}	Turn-Off Delay	(Note 7)			10		µs

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The LT1970C is guaranteed functional over the operating temperature range of –40°C and 85°C.

Note 3: The LT1970C is guaranteed to meet specified performance from 0°C to 70°C. The LT1970C is designed, characterized and expected to meet specified performance from –40°C to 85°C but is not tested or QA sampled at these temperatures.

Note 4: This parameter is not 100% tested.

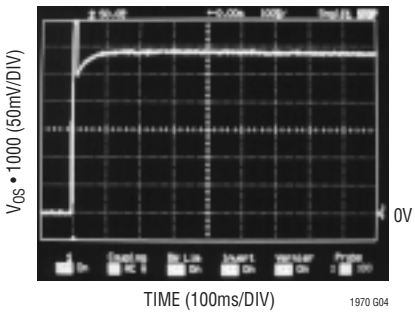
Note 5: Full power bandwidth is calculated from slew rate measurements: FPBW = SR/(2 • π • V_P)

Note 6: Thermal resistance varies depending upon the amount of PC board metal attached to the device. If the maximum dissipation of the package is exceeded, the device will go into thermal shutdown and be protected.

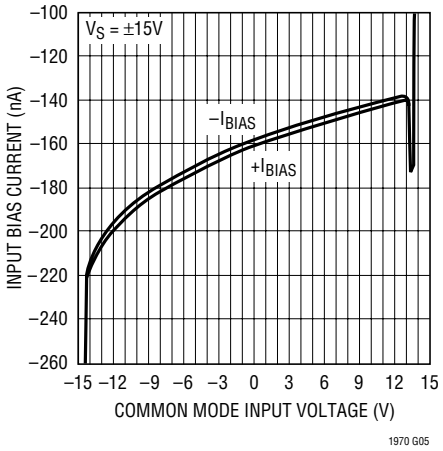
Note 7: Turn-on and turn-off delay are measured from V_{ENABLE} crossing 1.6V to the OUT pin at 90% of normal output voltage.

TYPICAL PERFORMANCE CHARACTERISTICS

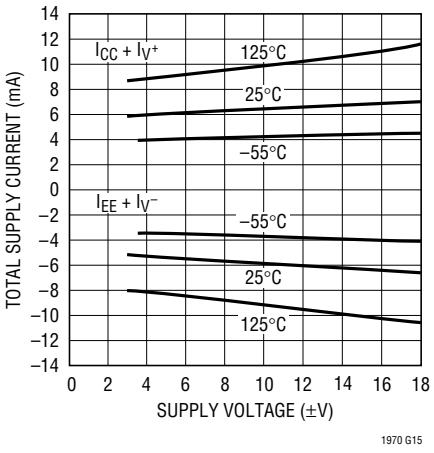
Warm-Up Drift V_{IO} vs Time



Input Bias Current vs V_{CM}

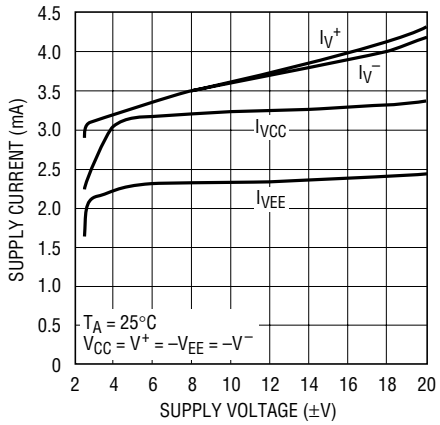


Total Supply Current vs Supply Voltage



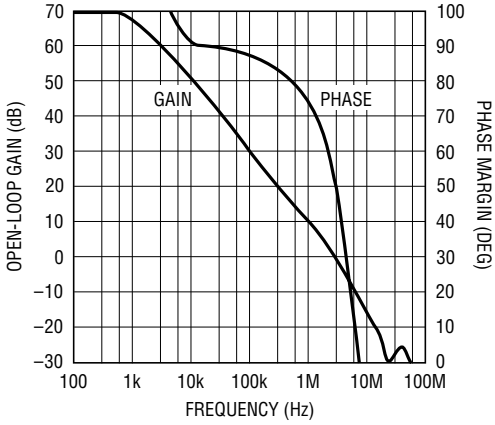
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Supply Voltage



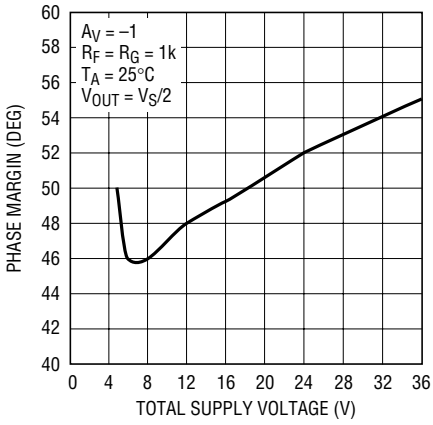
1870 G16

Open-Loop Gain and Phase vs Frequency



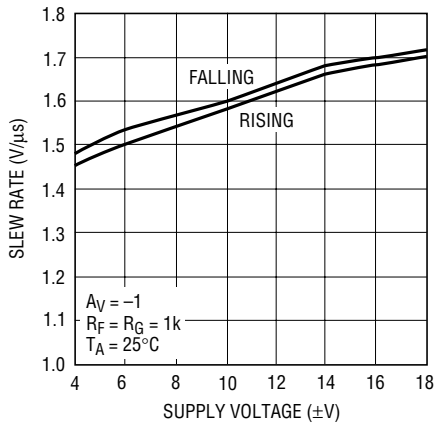
1970 G18

Phase Margin vs Supply Voltage



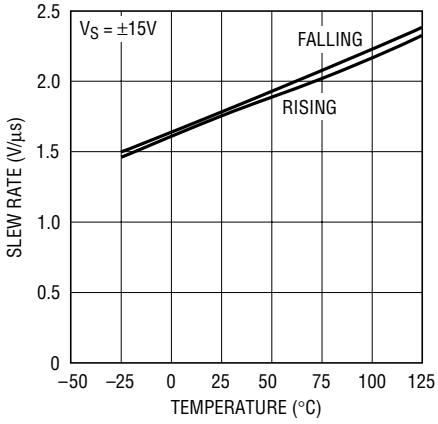
1970 G21

Slew Rate vs Supply Voltage



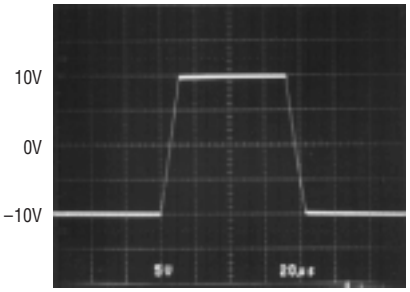
1970 G23

Slew Rate vs Temperature



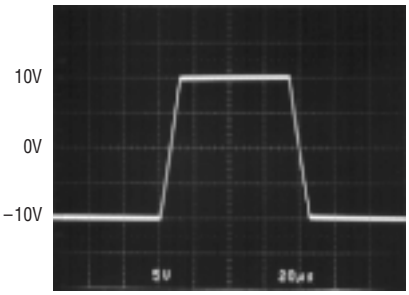
1970 G24

Large-Signal Response, A_V = 1



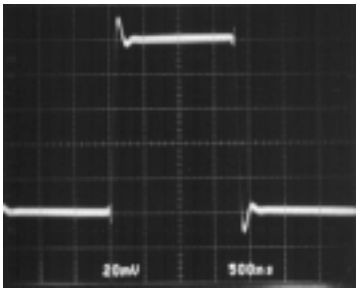
R_L = 1k 20µs/DIV 1970 G39

Large-Signal Response, A_V = –1



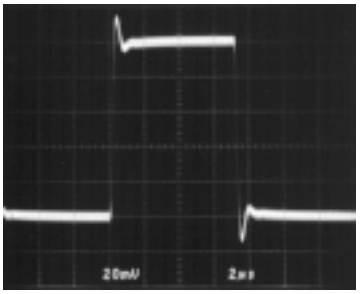
R_L = 1k 20µs/DIV 1970 G40
C_L = 1000pF

Small-Signal Response, A_V = 1



R_L = 1k 500ns/DIV 1970 G41

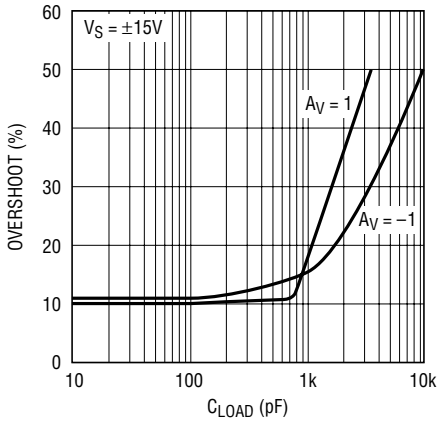
Small-Signal Response, A_V = –1



R_L = 1k 2µs/DIV 1970 G42
C_L = 1000pF

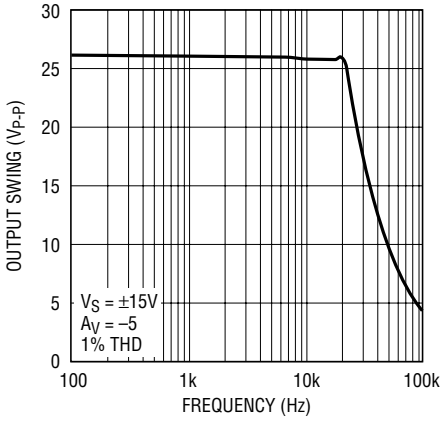
TYPICAL PERFORMANCE CHARACTERISTICS

% Overshoot vs C_{LOAD}



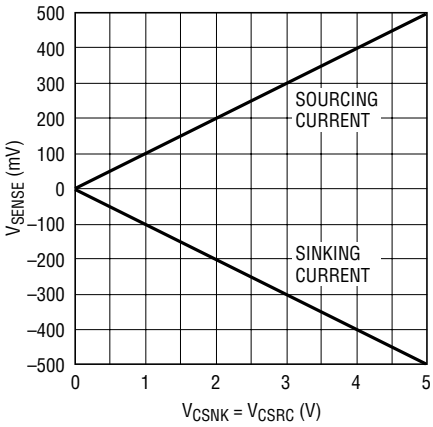
1970 G44

Undistorted Output Swing vs Frequency



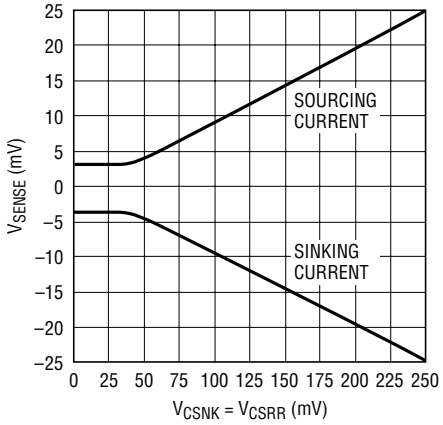
1970 G47

Full Range Current Sense Transfer Curve



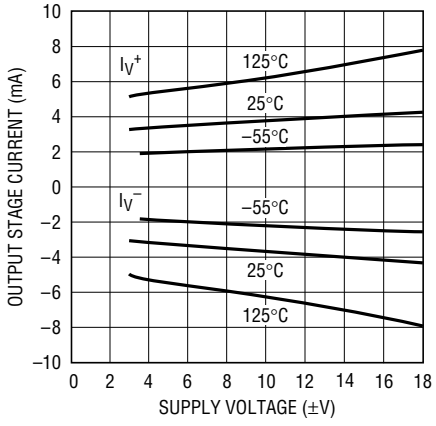
1970 G50

Low Level Current Sense Transfer Curve



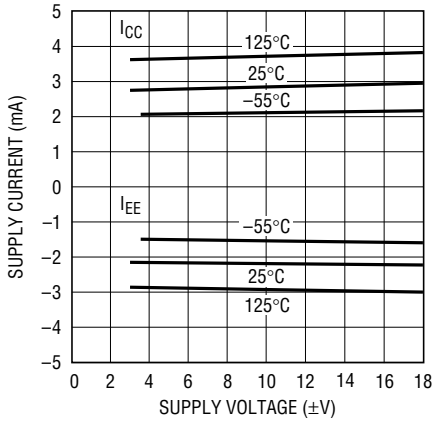
1970 G51

Output Stage Quiescent Current vs Supply Voltage



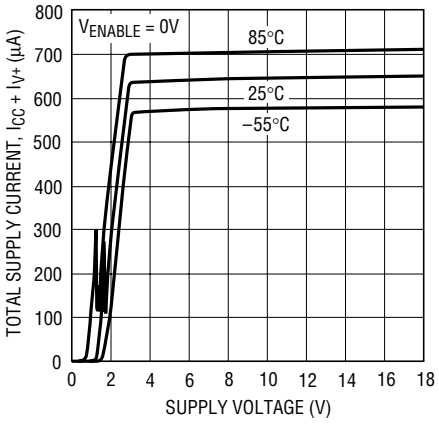
1970 G80

Control Stage Quiescent Current vs Supply Voltage



1970 G81

Supply Current vs Supply Voltage in Shutdown



1970 G82

PIN FUNCTIONS

V_{EE} (Pins 1, 10, 11, 20, Package Base): Minus Supply Voltage. V_{EE} connects to the substrate of the integrated circuit die, and therefore must always be the most negative voltage applied to the part. Decouple V_{EE} to ground with a low ESR capacitor. V_{EE} may be a negative voltage or it may equal ground potential. Any or all of the V_{EE} pins may be used. Unused V_{EE} pins must remain open.

V^- (Pin 2): Output Stage Negative Supply. V^- may equal V_{EE} or may be smaller in magnitude. Only output stage current flows out of V^-, all other current flows out of V_{EE}. V^- may be used to drive the base/gate of an external power device to boost the amplifier's output current to levels above the rated 500mA of the on-chip output devices. Unless used to drive boost transistors, V^- should be decoupled to ground with a low ESR capacitor.

OUT (Pin 3): Amplifier Output. The OUT pin provides the force function as part of a Kelvin sensed load connection. OUT is normally connected directly to an external load current sense resistor and the $SENSE^+$ pin. Amplifier feedback is directly connected to the load and the other end of the current sense resistor. The load connection is also wired directly to the $SENSE^-$ pin to monitor the load current.

The OUT pin is current limited to ±800mA typical. This current limit protects the output transistor in the event that connections to the external sense resistor are opened or shorted which disables the precision current limit function.

$SENSE^+$ (Pin 4): Positive Current Sense Pin. This lead is normally connected to the driven end of the external sense resistor. Positive current limit operation is activated when the voltage V_{SENSE} ($V_{SENSE}+ - V_{SENSE}-$) equals 1/10 of the programming control voltage at VC_{SRC} (Pin 13). Negative current limit operation is activated when the voltage V_{SENSE} equals –1/10 of the programming control voltage at VC_{SNK} (Pin 12).

FILTER (Pin 5): Current Sense Filter Pin. This pin is normally not used and should be left open in most applications. When very large capacitive loads are driven, a filter capacitor connected between FILTER and $SENSE^+$ will reduce overshoot as the amplifier enters current limiting mode. The filter time constant is set by an internal 1k resistor and the external filter capacitor. Capacitor values of 1nF to 100nF are most effective at reducing overshoot.

$SENSE^-$ (Pin 6): Negative Current Sense Pin. This pin is normally connected to the load end of the external sense resistor. Positive current limit operation is activated when the voltage V_{SENSE} ($V_{SENSE}+ - V_{SENSE}-$) equals 1/10 of the programming control voltage at VC_{SRC} (Pin 13). Negative current limit operation is activated when the voltage V_{SENSE} equals –1/10 of the programming control voltage at VC_{SNK} (Pin 12).

V_{CC} (Pin 7): Positive Supply Voltage. All circuitry except the output transistors draw power from V_{CC}. Total supply voltage from V_{CC} to V_{EE} must be between 3.5V and 36V. V_{CC} must always be greater than or equal to V^+. V_{CC} should always be decoupled to ground with a low ESR capacitor.

–IN (Pin 8): Inverting Input of Amplifier. –IN may be any voltage from V_{EE} – 0.3V to V_{EE} + 36V. –IN and +IN remain high impedance at all times to prevent current flow into the inputs when current limit mode is active. Care must be taken to insure that –IN or +IN can never go to a voltage below V_{EE} – 0.3V even during transient conditions or damage to the circuit may result. A Schottky diode from V_{EE} to –IN can provide clamping if other elements in the circuit can allow –IN to go below V_{EE}.

+IN (Pin 9): Noninverting Input of Amplifier. +IN may be any voltage from V_{EE} – 0.3V to V_{EE} + 36V. –IN and +IN remain high impedance at all times to prevent current flow into the inputs when current limit mode is active. Care must be taken to insure that –IN or +IN can never go to a voltage below V_{EE} – 0.3V even during transient conditions or damage to the circuit may result. A Schottky diode from V_{EE} to +IN can provide clamping if other elements in the circuit can allow +IN to go below V_{EE}.

PIN FUNCTIONS

VC_{SNK} (Pin 12): Sink Current Limit Control Voltage Input. The current sink limit amplifier will activate when the sense voltage between $SENSE^+$ and $SENSE^-$ equals $-1.0 \bullet V_{VCSNK}/10$. VC_{SNK} may be set between V_{COMMON} and $V_{COMMON} + 6V$. The transfer function between VC_{SNK} and V_{SENSE} is linear except for very small input voltages at $VC_{SNK} < 60mV$. V_{SENSE} limits at a minimum set point of 4mV typical to insure that the sink and source limit amplifiers do not try to operate simultaneously. To force zero output current, the ENABLE pin can be taken low.

VC_{SRC} (Pin 13): Source Current Limit Control Voltage Input. The current source limit amplifier will activate when the sense voltage between $SENSE^+$ and $SENSE^-$ equals $V_{VCSRC}/10$. VC_{SRC} may be set between V_{COMMON} and $V_{COMMON} + 6V$. The transfer function between VC_{SRC} and V_{SENSE} is linear except for very small input voltages at $VC_{SRC} < 60mV$. V_{SENSE} limits at a minimum set point of 4mV typical to insure that the sink and source limit amplifiers do not try to operate simultaneously. To force zero output current, the ENABLE pin can be taken low.

COMMON (Pin 14): Control and ENABLE inputs and flag outputs are referenced to the COMMON pin. COMMON may be at any potential between V_{EE} and $V_{CC} - 3V$. In typical applications, COMMON is connected to ground.

ENABLE (Pin 15): ENABLE Digital Input Control. When taken low this TTL-level digital input turns off the amplifier output and drops supply current to less than 1mA. Use the ENABLE pin to force zero output current. Setting $VC_{SNK} = VC_{SRC} = 0V$ allows $I_{OUT} = \pm 4mV/R_{SENSE}$ to flow in or out of V_{OUT}.

$\overline{ISRC}$ (Pin 16): Sourcing Current Limit Digital Output Flag. $\overline{ISRC}$ is an open collector digital output. $\overline{ISRC}$ pulls low whenever the sourcing current limit amplifier assumes control of the output. This pin can sink up to 10mA of current. The current limit flag is off when the source current limit is not active. $\overline{ISRC}$, $\overline{ISNK}$ and $\overline{TSD}$ may be wired "OR" together if desired. $\overline{ISRC}$ may be left open if this function is not monitored.

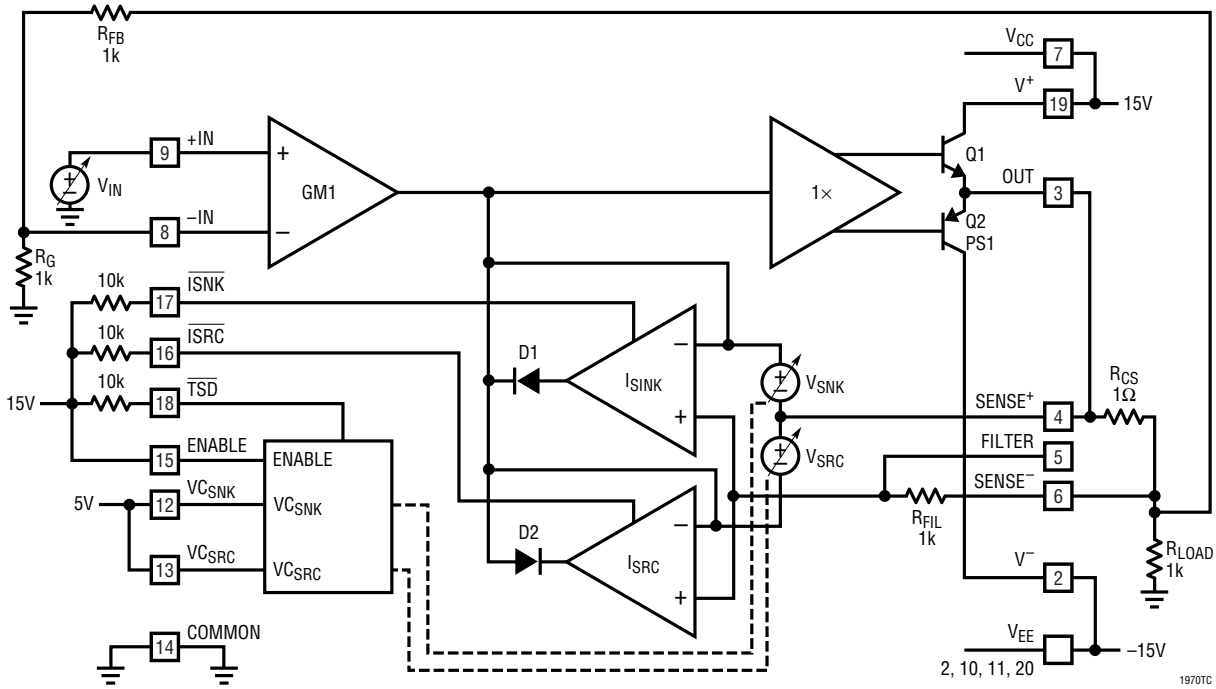
$\overline{ISNK}$ (Pin 17): Sinking Current Limit Digital Output Flag. $\overline{ISNK}$ is an open collector digital output. $\overline{ISNK}$ pulls low whenever the sinking current limit amplifier assumes control of the output. This pin can sink up to 10mA of current. The current limit flag is off when the source current limit is not active. $\overline{ISRC}$, $\overline{ISNK}$ and $\overline{TSD}$ may be wired "OR" together if desired. $\overline{ISNK}$ may be left open if this function is not monitored.

$\overline{TSD}$ (Pin 18): Thermal Shutdown Digital Output Flag. $\overline{TSD}$ is an open collector digital output. $\overline{TSD}$ pulls low whenever the internal thermal shutdown circuit activates, typically at a die temperature of 160°C. This pin can sink up to 10mA of output current. The $\overline{TSD}$ flag is off when the die temperature is within normal operating temperatures. $\overline{ISRC}$, $\overline{ISNK}$ and $\overline{TSD}$ may be wired "OR" together if desired. $\overline{ISNK}$ may be left open if this function is not monitored. Thermal shutdown activation should prompt the user to evaluate electrical loading or thermal environmental conditions.

V^+ (Pin 19): Output Stage Positive Supply. V^+ may equal V_{CC} or may be smaller in magnitude. Only output stage current flows through V^+, all other current flows into V_{CC}. V^+ may be used to drive the base/gate of an external power device to boost the amplifier's output current to levels above the rated 500mA of the on-chip output devices. Unless used to drive boost transistors, V^+ should be decoupled to ground with a low ESR capacitor.

Package Base: The exposed backside of the package is electrically connected to the V_{EE} pins on the IC die. The package base should be soldered to a heat spreading pad on the PC board that is electrically connected to V_{EE}.

BLOCK DIAGRAM AND TEST CIRCUIT



APPLICATIONS INFORMATION

The LT1970 power op amp with precision controllable current limit is a flexible voltage and current source module. The drawing on the front page of this data sheet is representative of the basic application of the circuit, however many alternate uses are possible with proper understanding of the subcircuit capabilities.

CIRCUIT DESCRIPTION

Main Operational Amplifier

Subcircuit block GM1, the 1X unity-gain current buffer and output transistors Q1 and Q2 form a standard operational amplifier. This amplifier has ±500mA current output capability and a 3.6MHz gain bandwidth product. Most applications of the LT1970 will use this op amp in the main signal path. All conventional op amp circuit configurations are supported. Inverting, noninverting, filter, summation or nonlinear circuits may be implemented in a conventional manner. The output stage includes current limiting at ±800mA to protect against fault conditions. The input stage has high differential breakdown of 36V minimum between –IN and +IN. No current will flow at the inputs when differential input voltage is present. This feature is important when the precision current sense amplifiers "I_{SINK}" and "I_{SRC}" become active.

Current Limit Amplifiers

Amplifier stages "I_{SINK}" and "I_{SRC}" are very high transconductance amplifier stages with independently controlled offset voltages. These amplifiers monitor the voltage between input pins $SENSE^+$ and $SENSE^–$ which usually sense the voltage across a small external current sense resistor. The transconductance amplifiers outputs connect to the same high impedance node as the main input stage GM1 amplifier. Small voltage differences between $SENSE^+$ and $SENSE^–$, smaller than the user set $VC_{SNK}/10$ and $VC_{SRC}/10$ in magnitude, cause the current limit amplifiers to decouple from the signal path. This is functionally indicated by diodes D1 and D2 in the Block Diagram. When the voltage V_{SENSE} increases in magnitude sufficient to equal or overcome one of the offset voltages $VC_{SNK}/10$ or $VC_{SRC}/10$, the appropriate current limit amplifier becomes

APPLICATIONS INFORMATION

active and because of its very high transconductance, takes control from the input stage, GM1. The output current is regulated to a value of $I_{OUT} = V_{SENSE}/R_{SENSE} = (VC_{SRC}$ or $VC_{SNK})/(10 \bullet R_{SENSE})$.

Most applications will connect pins $SENSE^+$ and OUT together, with the load on the opposite side of the external sense resistor and pin $SENSE^-$. Feedback to the inverting input of GM1 should be connected from $SENSE^-$ to –IN. The common mode range of stages "I_{SINK}" and "I_{SRC}" allow other connections. Ground side sensing of load current may be employed by connecting the load between pins OUT and $SENSE^+$. Pin $SENSE^-$ would be connected to ground in this instance. Load current would be regulated in exactly the same way as the conventional connection. However, voltage mode accuracy would be degraded in this case due to the voltage across R_{SENSE}.

Creative applications are possible where pins $SENSE^+$ and $SENSE^-$ monitor a parameter other than load current. The operating principle that at most one of the current limit stages may be active at one time, and that when active, the current limit stages take control of the output from GM1, can be used for many different signals.

Current Limit Threshold Control Buffers

Input pins VC_{SNK} and VC_{SRC} are used to set the response thresholds of current limit amplifiers "I_{SINK}" and "I_{SRC}". Each of these inputs may be independently driven by a voltage of 0V to 5V above the COMMON reference pin. The 0V to 5V input voltage is attenuated by a factor of 10 and applied as an offset to the appropriate current limit amplifier. AC signals may be applied to these pins. The AC bandwidth from a V_C pin to the output is typically 2MHz.

The transfer function from V_C to the associated V_{OS} is linear from about 0.1V to 5V in, or 10mV to 500mV at the current limit amplifier inputs. An intentional nonlinearity is built into the transfer functions at low levels. This nonlinearity insures that both the sink and source limit amplifiers cannot become active simultaneously. Simultaneous activation of the limit amplifiers could result in uncontrolled outputs. As shown in the Typical Performance Characteristics curves, the control inputs have a "hockey stick" shape, to keep the minimum limit threshold at 4mV for each limit amplifier.

ENABLE Control

The ENABLE input pin puts the LT1970 into a low supply current, high impedance output state. The ENABLE pin responds to TTL threshold levels with respect to the COMMON pin. Pulling the ENABLE pin low is the best way to force zero current at the output. Setting $VC_{SNK} = VC_{SRC}$ = 0V allows the output current to remain as high as $\pm 4mV/R_{SENSE}$.

Operating Status Flags

The LT1970 has three digital output indicators; $\overline{TSD}$, $\overline{ISRC}$ and $\overline{ISNK}$. These outputs are open collector drivers referred to the COMMON pin. The outputs have 36V capabilities and can sink in excess of 10mA. $\overline{ISRC}$ and $\overline{ISNK}$ indicate activation of the associated current limit amplifier. The $\overline{TSD}$ output indicates excessive die temperature has caused the circuit to enter thermal shutdown. The three digital outputs may be wire "OR'd" together, monitored individually or left open. These outputs do not affect circuit operation, but provide an indication of the present operational status of the chip.

THERMAL MANAGEMENT

Minimizing Power Dissipation

The LT1970 can operate with up to 36V total supply voltage with output currents up to ±500mA. The amount of power dissipated in the chip could approach 18W under worst-case conditions. This amount of power will cause die temperature to rise until the circuit enters thermal shutdown. While the thermal shutdown feature prevents damage to the circuit, normal operation is impaired. Thermal design of the LT1970 operating environment is essential to getting maximum utility from the circuit.

The first concern for thermal management is minimizing the heat which must be dissipated. The separate power pins V^+ and V^- can be a great aid in minimizing on-chip power. The output pin can swing to within 1.0V of V^+ or V^- even under maximum output current conditions. Using separate power supplies, or off chip dissipative elements, to set V^+ and V^- to their minimum values for the required output swing will minimize power dissipation. The supplies V_{CC} and V_{EE} may also be reduced to a minimal value,

APPLICATIONS INFORMATION

but these supply pins do not carry high currents, and the power saving is much less. V_{CC} and V_{EE} must be greater than the maximum output swing by 2V or more.

When V^- and V^+ are provided separately from V_{CC} and V_{EE}, care must be taken to insure that V^- and V^+ are always less than or equal to the main supplies in magnitude. Protection Schottky diodes may be required to insure this in all cases, including power on/off transients.

Operation with reduced V^+ and V^- supplies does not affect any performance parameters except maximum output swing. All DC accuracy and AC performance specifications guaranteed with $V_{CC} = V^+$ and $V_{EE} = V^-$ are still valid within the reduced signal swing range.

Heat Sinking

The power dissipated in the LT1970 die must have a path to the environment. With 100°C/W thermal resistance in free air with no heat sink, the package power dissipation is limited to only 1W. The 20-pin TSSOP package with exposed copper underside is an efficient heat conductor if it is effectively mounted on a PC board. Thermal resistances as low as 40°C/W can be obtained by soldering the bottom of the package to a large copper pattern on the PC board. For operation at 85°C, this allows up to 1.625W of power to be dissipated on the LT1970. At 25°C operation, up to 3.125W of power dissipation can be achieved. The PC board heat spreading copper area must be connected to V_{EE}.

DRIVING REACTIVE LOADS

Capacitive Loads

The LT1970 is much more tolerant of capacitive loading than most operational amplifiers. In a worst-case configuration as a voltage follower, the circuit is stable for capacitive loads less than 2.5nF. Higher gain configurations improve the C_{LOAD} handling. If very large capacitive loads are to be driven, a resistive decoupling of the amplifier from the capacitive load is effective in maintaining stability and reducing peaking. The current sense resistor, usually connected between the output pin and the load can serve as a part of the decoupling resistance.

Very large capacitive loads above 1µF can also cause transient overshoots when the current limiting circuits activate. The FILTER pin is provided to assist in controlling this problem. Should load capacitance cause transient overshoot, a 1nF to 100nF capacitor between the FILTER and $SENSE^-$ pins will minimize the overshoot. The best value of capacitor to use in this situation will likely require some empirical evaluation, as the optimum is a complex function of output current, load resistance, sense resistor and load capacitance.

Inductive Loads

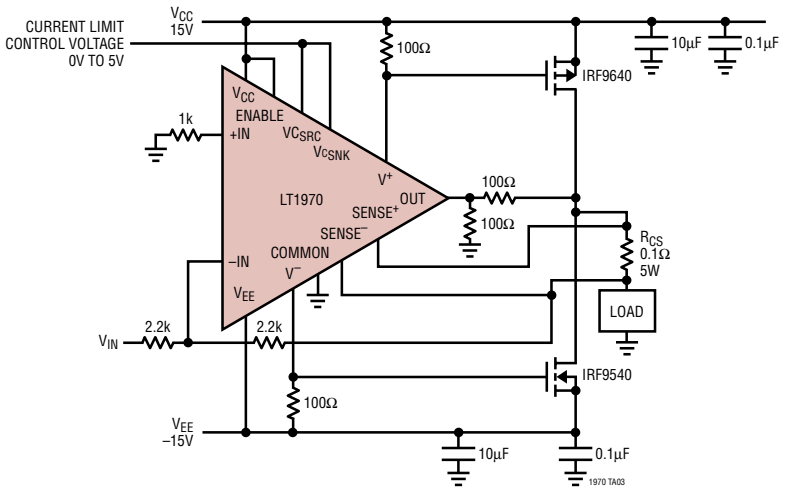
Load inductance is usually not a problem at the outputs of operational amplifiers, but the LT1970 can be used as a high output impedance current source. This condition may be the main operating mode, or when the circuit enters a protective current limit mode. Just as load capacitance degrades the phase margin of normal op amps, load inductance causes a peaking in the loop response of the feedback controlled current source. The inductive load may be caused by long lead lengths at the amplifier output. If the amplifier will be driving inductive loads or long lead lengths (greater than 4 inches) a 500pF capacitor from the $SENSE^-$ pin to the ground plane will cancel the inductive load and insure stability.

Supply Bypassing

The LT1970 can supply large currents from the power supplies to a load at frequencies up to 4MHz. Power supply impedance must be kept low enough to deliver these currents without causing supply rails to droop. Low ESR capacitors, such as 0.1µF or 1µF ceramics, located close to the pins are essential in all applications. When large, high speed transient currents are present additional capacitance may be needed near the chip. Check supply rails with a scope and if signal related ripple is seen on the supply rail, increase the decoupling capacitor as needed.

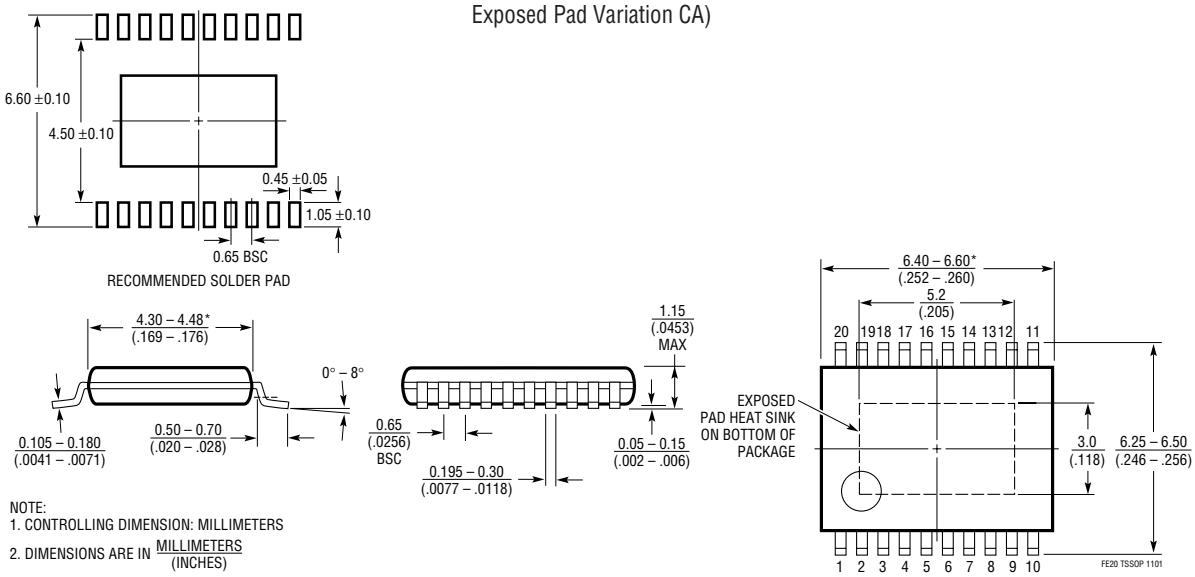
TYPICAL APPLICATION

A_V = –1 Amplifier with Discrete Power Devices to Boost Output Current to 5A



PACKAGE DESCRIPTION

FE Package
20-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663,
Exposed Pad Variation CA)



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN MILLIMETERS (INCHES)
3. DRAWING NOT TO SCALE
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .150mm (.006") PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1010	Fast ±150mA Power Buffer	
LT1206	250mA/60MHz Current Feedback Amplifier	Shutdown Mode, Adjustable Supply Current
LT1210	1.1A/35MHz Current Feedback Amplifier	Stable with C_L = 10,000pF

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