HSP50214A

December 1999

OBSOLETE PRODUCT
POSSIBLE SUBSTITUTE PRODUCT
HSP50214B

Programmable Downconverter

Features

- Up to 65 MSPS Front-End Processing Rates (CLKIN) and 55 MSPS (41 MSPS Using the Discriminator) Back-End Processing Rates (PROCCLK)
  Clocks May Be Asynchronous
- Processing Capable of >100dB SFDR
- Up to 255-Tap Programmable FIR
- Overall Decimation Factor Ranging from 4 to 16384
- Output Samples Rates to ≅12.94 MSPS with Output Bandwidths to ≅ 982kHz Lowpass
- 32-Bit Programmable NCO for Channel Selection and Carrier Tracking
- Digital Resampling Filter for Symbol Tracking Loops and Incommensurate Sample-to-Output Clock Ratios
- Digital AGC with Programmable Limits and Slew Rate to Optimize Output Signal Resolution; Fixed or Auto Gain Adjust
- Serial, Parallel, and FIFO 16-Bit Output Modes
- Cartesian to Polar Converter and Frequency Discriminator for AFC Loops and Demodulation of AM, FM, FSK, and DPSK
- Input Level Detector for External I.F. AGC Support

Applications

- Single Channel Digital Software Radio Receivers
- Base Station Rx's: AMPS, NA TDMA, GSM, and CDMA
- Compatible with HSP50210 Digital Costas Loop for PSK Reception
- Evaluation Platform Available

Description

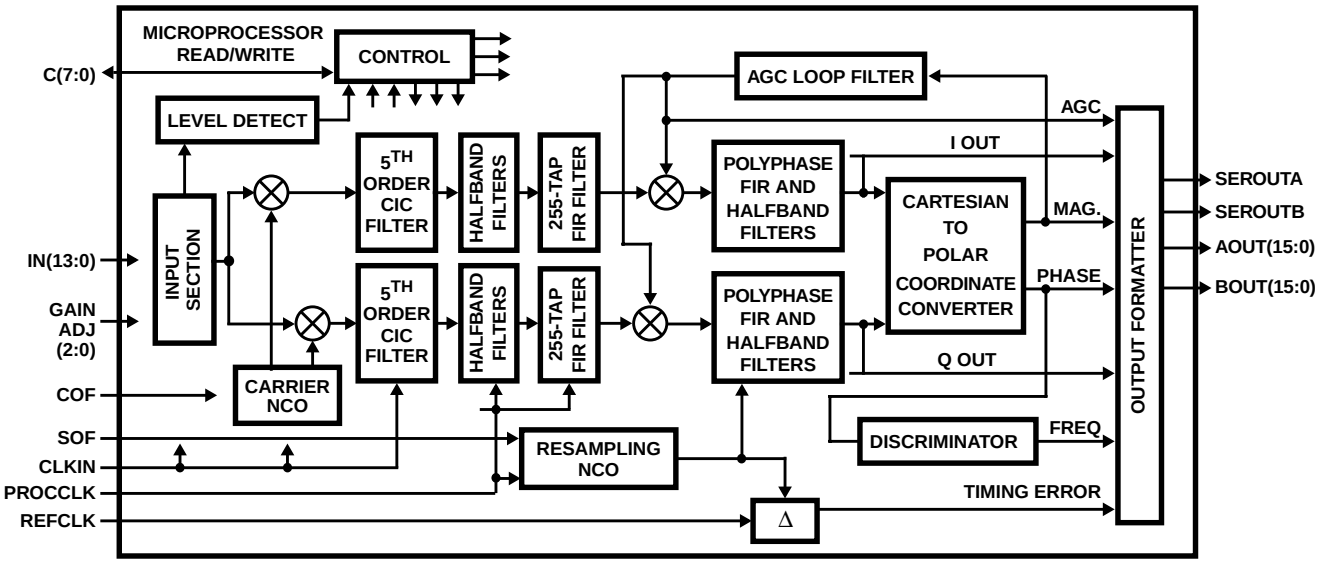
The HSP50214A Programmable Downconverter converts digitized IF data into filtered baseband data which can be processed by a standard DSP microprocessor. The Programmable Downconverter (PDC) performs down conversion, decimation, narrowband low pass filtering, gain scaling, resampling, and Cartesian to Polar coordinate conversion.

The 14-bit sampled IF input is down converted to baseband by digital mixers and a quadrature NCO, as shown in the Block Diagram. A decimating (4 to 32) fifth order Cascaded Integrator-Comb (CIC) filter can be applied to the data before it is processed by up to 5 decimate-by-2 halfband filters. The halfband filters are followed by a 255-tap programmable FIR filter. The output data from the programmable FIR filter is scaled by a digital AGC before being re-sampled in a polyphase FIR filter. The output section can provide seven types of data: Cartesian (I, Q), polar (R, q), filtered frequency (dq/dt), Timing Error (TE), and AGC level in either parallel or serial format.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HSP50214AVC	0 to 70	120 Ld MQFP	Q120.28x28
HSP50214AVI	-40 to 85	120 Ld MQFP	Q120.28x28

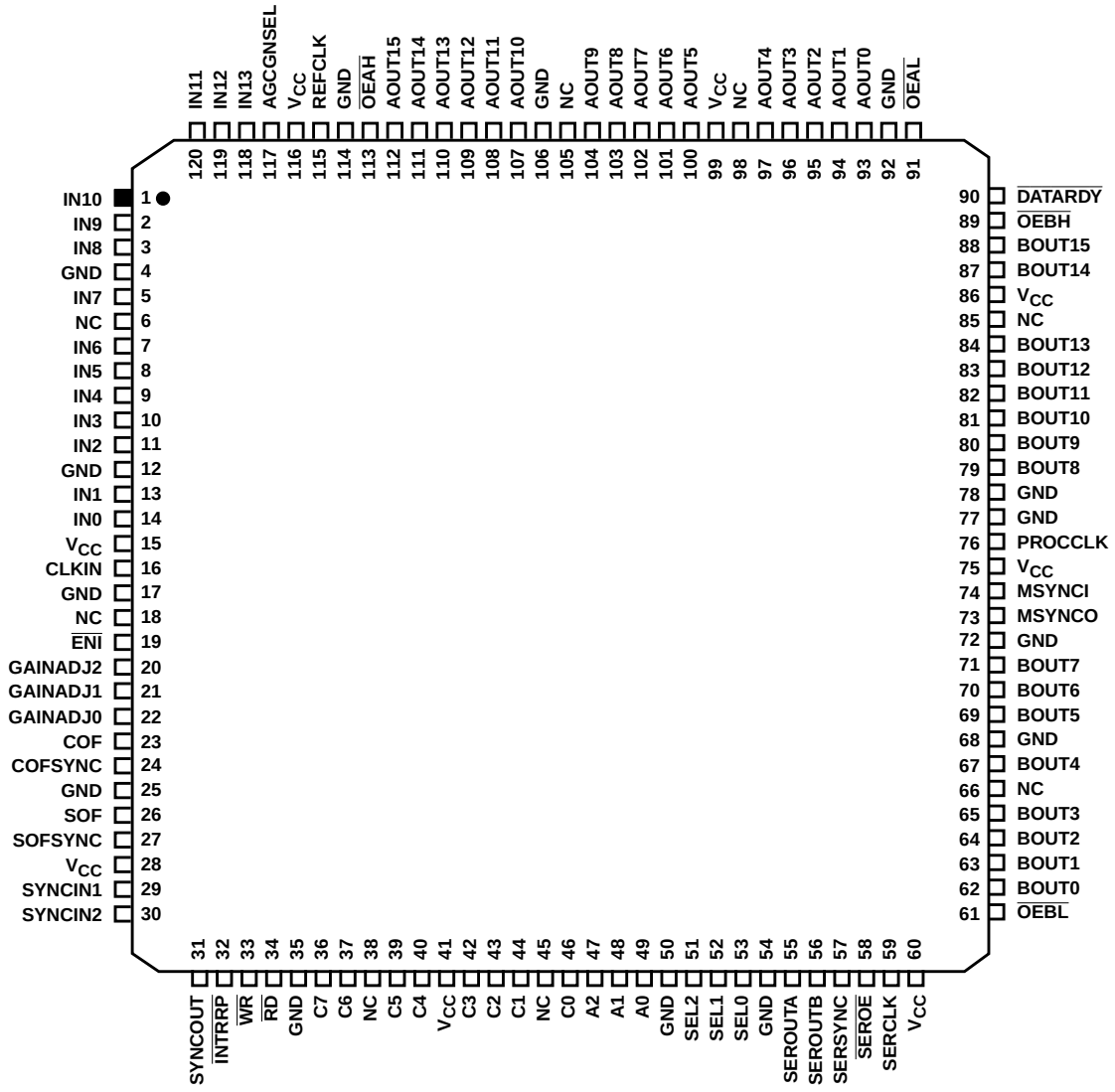
Block Diagram



File Number **4449.1**

Pinout

120 LEAD MQFP
TOP VIEW



Pin Descriptions

NAME	TYPE	DESCRIPTION
V_{CC}	-	Positive Power Supply Voltage.
GND	-	Ground.
CLKIN	I	Input Clock. This clock should be a multiple of the input sample rate. All input section processing occurs on the rising edge of CLKIN. The frequency of CLKIN is designated f_{CLKIN}.
IN(13:0)	I	Input Data. The format of the input data may be set to offset binary or 2's complement. IN13 is the MSB (see Control Word 0).
$\overline{ENI}$	I	Input Enable. Active Low. This pin enables the input to the part in one of two modes, gated or interpolated (see Control Word 0). In gated mode, one sample is taken per CLKIN when $\overline{ENI}$ is asserted. The input sample rate is designated f_S, which can be different from f_{CLKIN} When $\overline{ENI}$ is used.
GAINADJ(2:0)	I	GAINADJ Input. Adds an offset to the gain via the shifter following the mixer. GAINADJ value is added to the shift code from the microprocessor (µP) interface. The shift code is saturated to a maximum code of F. The gain is offset by (6dB)(GAINADJ); (000 = 0dB gain adjust; 111 = 42dB gain adjust) GAINADJ2 is the MSB. See "Using the Input Gain Adjust Control Signals" Section.
PROCCLK	I	Processing Clock. PROCCLK is the clock for all processing functions following the CIC Section. Processing is performed on PROCCLK's rising edge. All output timing is derived from this clock. ***NOTE: This clock may be asynchronous to CLKIN.***
AGCGNSEL	I	AGC Gain Select. This pin selects between two AGC loop gains. This input is setup and held relative to PROCCLK. Gain setting 1 is selected when AGCGNSEL = 1.
COF	I	Carrier Offset Frequency Input. This serial input pin is used to load the carrier offset frequency into the Carrier NCO (see Serial Interface Section). The offset may be 8, 16, 24, or 32 bits. The setup and hold times are relative to CLKIN. This input is compatible with the output of the HSP50210 Costas loop [1].
COFSYNC	I	Carrier Offset Frequency Sync. This signal is asserted one CLK before the most significant bit (MSB) of the offset frequency word (see Serial Interface Section). The setup and hold times are relative to CLKIN. This input is compatible with the output of the HSP50210 Costas loop [1].
SOF	I	Re-Sampler Offset Frequency Input. This serial input pin is used to load the offset frequency into the Re-Sampler NCO (see Serial Interface Section). The offset may be 8, 16, 24, or 32 bits. The setup and hold times are relative to PROCCLK. This input is compatible with the output of the HSP50210 Costas loop [1].
SOFSYNC	I	Re-Sampler Offset Frequency Sync. This signal is asserted one CLK before the MSB of the offset frequency word (see Serial Interface Section). The setup and hold times are relative to PROCCLK. This input is compatible with the output of the HSP50210 Costas loop [1].
AOUT(15:0)	O	Parallel Output Bus A. Two parallel output modes are available on the HSP50214A. The first is called the Direct Output Port, where the source is selected through Control Word 20 (see the Microprocessor Write Section) and comes directly from the Output MUX Section (see Output Control Section). The most significant byte of AOUT always outputs the most significant byte of the Parallel Direct Output Port whose data type is selected via µP interface. AOUT15 is the MSB. In this mode, the AOUT(15:0) bus is updated as soon as data is available. $\overline{DATARDY}$ is asserted to indicate new data. The second mode for parallel data is called the Buffer RAM Output Port. The Buffer RAM Output Port acts like a FIFO for blocks of information called data sets. Within a data set is I, Q, magnitude, phase, and frequency information; a data type is selected using SEL(2:0). Up to 7 data sets are stored in the Buffer RAM Output Port. The LSBytes of the AOUT and BOUT busses form the 16 bits for the buffered output mode and can be used for buffered mode while the MSBytes are outputting data in the direct output mode.
BOUT(15:0)	O	Parallel Output Bus B. Two parallel output modes are available on the HSP50214A. The first is called the Direct Output Port, where the source is selected through Control Word 20 (see the Microprocessor Write Section) and comes directly from the Output MUX Section (see Output Control Section). The most significant byte of BOUT always outputs the most significant byte of the Parallel Direct Output Port whose data type is selected via µP interface. BOUT15 is the MSB. In this mode, the BOUT(15:0) bus is updated as soon as data is available. $\overline{DATARDY}$ is asserted to indicate new data. The second mode for parallel data is called the Buffer RAM Output Port. The Buffer RAM Output Port acts like a FIFO for blocks of information called data sets. Within a data set is I, Q, magnitude, phase, and frequency information; a particular information is selected using SEL(2:0). Up to 7 data sets is stored in the Buffer RAM Output Port. The least significant byte of BOUT can be used to either output the least significant byte of the B Parallel Direct Output Port or the least significant byte of the Buffer RAM Output Port. See Output Section.

Pin Descriptions (Continued)

NAME	TYPE	DESCRIPTION
$\overline{\text{DATARDY}}$	O	Output Strobe Signal. Active Low. Indicates when new data from the Direct Output Port Section is available. DATARDY is asserted for one PROCCLK cycle during the first clock cycle that data is available on the parallel out busses. See Output Section.
$\overline{\text{OEAH}}$	I	Output enable for the MSByte of the AOUT bus. Active Low.
$\overline{\text{OEAL}}$	I	Output enable for the LSByte of the AOUT bus. Active Low.
$\overline{\text{OEBH}}$	I	Output enable for the MSByte of the BOUT bus. Active Low.
$\overline{\text{OEBL}}$	I	Output enable for the LSByte of the BOUT bus. Active Low.
SEL(2:0)	I	Select Address is used to choose which information in a data set from the Buffer RAM Output Port is sent to the least significant bytes of AOUT and BOUT. SEL2 is the MSB.
$\overline{\text{INTRRP}}$	O	Interrupt Output. Active Low. This output is asserted for 8 PROCCLK cycles when the Buffer RAM Output Port is ready for reading.
SEROUTA	O	Serial Output Bus A Data. I, Q, magnitude, phase, frequency, timing error and AGC information can be sequenced in programmable order. See Output Section and Microprocessor Write Section.
SEROUTB	O	Serial Output Bus B Data. Contents may be related to SEROUTA. I, Q, magnitude, phase, frequency, timing error and AGC information can be sequenced in programmable order. See Output Section and Microprocessor Write Section.
SERCLK	O	Output Clock for Serial Data Out. Derived from PROCCLK as given by Control Word 20 in the Microprocessor Write Section.
SERSYNC	O	Serial Output Sync Signal. Serves as serial data strobes. See Output Section and Microprocessor Write Section.
$\overline{\text{SEROE}}$	I	Serial Output Enable. When high, the SEROUTA, SEROUTB, SERCLK, and SERSYNC signals are set to a high impedance.
C(7:0)	I/O	Processor Interface Data Bus. See Microprocessor Write Section. C7 is the MSB.
A(2:0)	I	Processor Interface Address Bus. See Microprocessor Write Section. A2 is the MSB.
$\overline{\text{WR}}$	I	Processor Interface Write Strobe. C(7:0) is written to Control Words selected by A(2:0) in the Programmable Down Converter on the rising edge of this signal. See Microprocessor Write Section.
$\overline{\text{RD}}$	I	Processor Interface Read Strobe. C(7:0) is read from output or status locations selected by A(2:0) in the Programmable Down Converter on the falling edge of this signal. See Microprocessor Read Section.
REFCLK	I	Reference Clock. Used as an input clock for the timing error detector. The timing error is computed relative to REFCLK. REFCLK frequency must be less than or equal to PROCCLK/2.
MSYNCO	O	Multiple Chip Sync Output. Provided for synchronizing multiple parts when CLKIN and PROCCLK are asynchronous. MSYNCO is the synchronization signal between the input section operating under CLKIN and the back end processing operating under PROCCLK. This output sync signal from one part is connected to the MSYNCI signal of all the HSP50214As.
MSYNCI	I	Multiple Chip Sync Input. The MSYNCI pin of all the parts should be tied to the MSYNCO of one part. ***NOTE: MSYNCI must be connected to an MSYNCO signal for operation.***
SYNCIN1	I	CIC Decimation/Carrier NCO Update Sync. Can be used to synchronize the CIC Section, carrier NCO update, or both. See the Multiple Chip Synchronization Section and Control Word 0 in the Microprocessor Write Section. Active High.
SYNCIN2	I	FIR/Timing NCO Update/AGC Gain Update Sync. Can be used to synchronize the FIR, Timing NCO update, AGC gain update, or any combination of the above. See the Multiple Chip Synchronization Section and Control Words 7, 8, and 10 in the Microprocessor Write Section. Active High.
SYNCOUT	O	Strobe Output. This synchronization signal is generated by the µP interface for synchronizing multiple parts. Can be generated by PROCLK or CLKIN (see Control Word 0 and Control Word 24 in the Microprocessor Write Section). Active High.

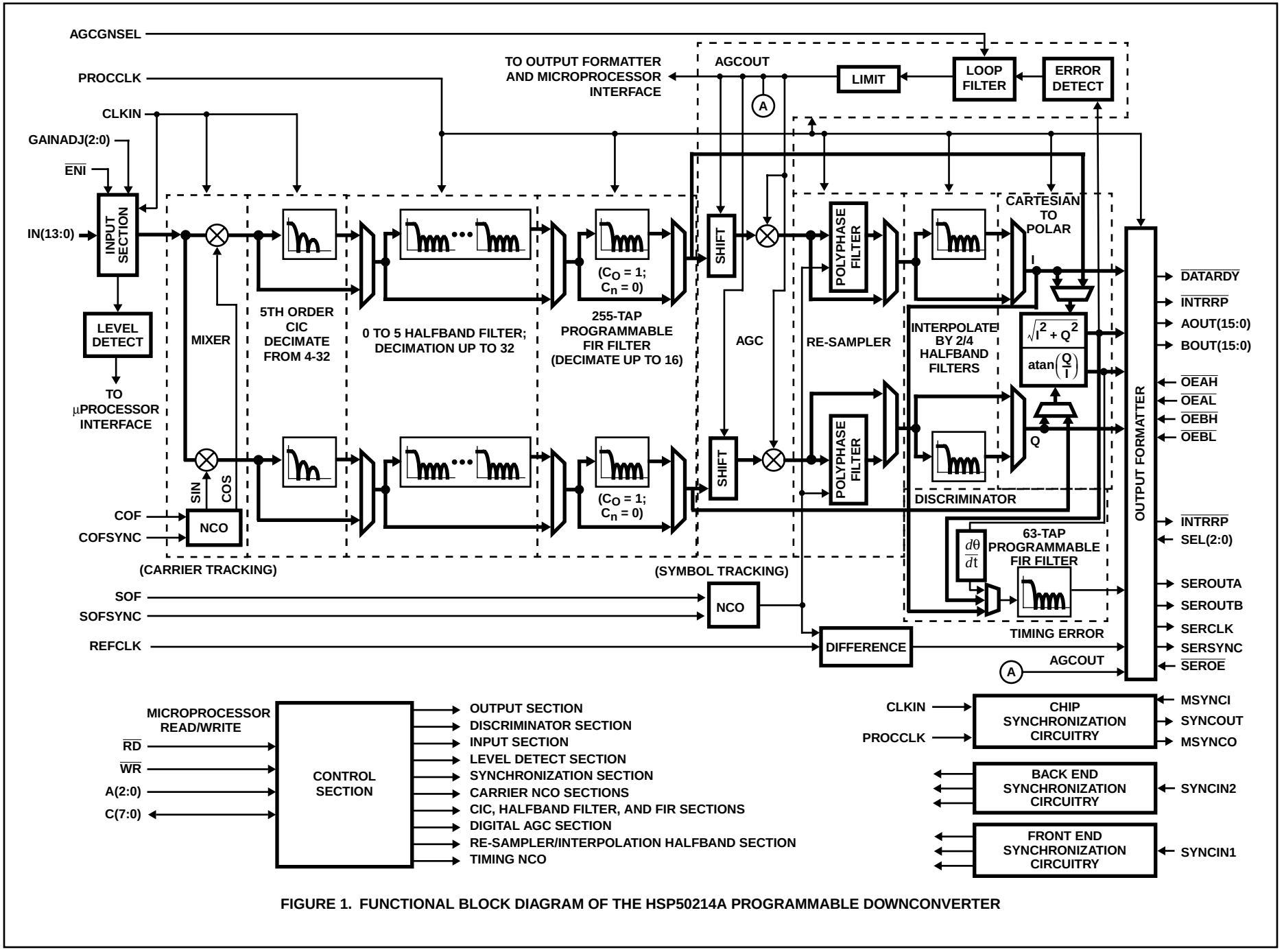


FIGURE 1. FUNCTIONAL BLOCK DIAGRAM OF THE HSP50214A PROGRAMMABLE DOWNCONVERTER

Functional Description

The HSP50214A Programmable Downconverter (PDC) is an agile digital tuner designed to meet the requirements of a wide variety of communications industry standards. The PDC contains the processing functions needed to convert sampled IF signals to baseband digital samples. These functions include LO generation/mixing, decimation filtering, programmable FIR shaping/bandlimiting filtering, resampling, Automatic Gain Control (AGC), frequency discrimination and detection as well as multi-chip synchronization. The HSP50214A interfaces directly with a DSP microprocessor to pass baseband and status data.

A top level functional block diagram of the HSP50214A is shown in Figure 1. The diagram shows the major blocks and multiplexers used to reconfigure the data path for various architectures. The HSP50214A can be broken into 13 sections: Synchronization, Input, Input Level Detector, Carrier Mixer/Numerically Control Oscillator (NCO), CIC Decimating Filter, Halfband Decimating Filter, 255-Tap Programmable FIR Filter, Automatic Gain Control (AGC), Re-sampler/Halfband Filter, Timing NCO, Cartesian to Polar Converter, Discriminator, and Output Sections. All of these sections are configured through a microprocessor interface.

The HSP50214A has three clock inputs; two are required and one is optional. The input level detector, carrier NCO, and CIC decimating filter sections operate on the rising edge of the input clock, CLKIN. The halfband filter, programmable FIR filter, AGC, Re-Sampler/Halfband filters, timing NCO, discriminator, and output sections operate on the rising edge of PROCCLK. The third clock, REFCLK, is used to generate timing error information.

NOTE: All of the clocks may be asynchronous.

PDC Applications Overview

This section highlights the motivation behind the key programmable features from a communications system level perspective. These motivations will be defined in terms of ability to provide DSP processing capability for specific modulation formats and communication applications. The versatility of the Programmable Downconverter can be intimidating because of the many Control Words required for chip configuration. This section provides system level insight to help allay reservations about this versatile DSP product. It should help the designer capitalize on the greatest feature of the PDC - ***VERSATILITY THROUGH PROGRAMMABILITY***. It is this feature, when fully understood, that brings the greatest return on design investment by offering a single receiver design that can process the many waveforms required in the communications marketplace.

FDM Based Standards and Applications

Table 1 provides an overview of some common frequency division multiplex (FDM) base station applications to which the PDC can be applied. The PDC provides excellent selectivity for frequency division multiple access (FDMA) signals. This high selectivity is achieved with 0.012Hz resolution frequency control of the NCO and the sharp filter responses capable with a 255-tap, 22-bit coefficient FIR filter. The 16-bit resolution out of the Cartesian to Polar Coordinate Converter are routed to the frequency detector, which is followed by a 63-tap, 22-bit coefficient FIR filter structure for facilitating FM and FSK detection. The 14-bit input resolution is the smallest bit resolution found throughout the conversion and filtering sections, providing excellent dynamic range in the DSP processing. A unique input gain scaler adds an additional 42dB of range to the input level variation, to compensate for changes in the analog RF front end receive equipment. Synchronization circuitry allows precise timing control of the base station reconfiguration for all receive channels simultaneously. Portions of this table were corroborated with reference [2].

TABLE 1. CELLULAR PHONE BASE STATION APPLICATIONS USING FDMA

STANDARD	AMPS (IS-91)	MCS-L1 MCS-L2	NMT-400 NMT-900	C450	ETACS NTACS
RX BAND (MHz)	824-849	925-940	453-458 890-915	451-456	871-904 915-925
CHANNEL BW (kHz)	30	25.0 12.5	25 12.5	20.0 10.0	25.0 12.5
# TRAFFIC CHANNELS	832	600 1200	200 1999	222 444	1240 800
VOICE MODULATION	FM	FM	FM	FM	FM
PEAK DEVIATION (kHz)	12	5	5	4	9.5
CONTROL MODULATION	FSK	FSK	FSK	FSK	FSK
PEAK DEVIATION (kHz)	8	4.5	3.5	2.5	6.4
CONTROL CHANNEL RATE (Kbps)	10	0.3	1.2	5.3	8

TDM Based Standards and Applications

Table 2 provides an overview of some common Time Division Multiplexed (TDM) base station applications to which the PDC can be applied. For time division multiple access (TDMA) applications, such as North American TDMA (IS136), where 30kHz is the received band of interest for the PCS basestation, the PDC offers 0.012Hz frequency resolution in downconversion in addition to $\alpha = 0.35$ matched (programmable) filtering capability. The $\pi/4$ DPSK modulation can be processed using the PDC Cartesian to Polar coordinate converter and $d\phi/dt$ detector circuitry or by processing the I/Q samples in the DSP μP. The PDC provides the ability to change the received signal gain and frequency, synchronous with burst timing. The synchronous gain adjustment allows the user to measure the power of the signal at the A/D at the end of a burst, and synchronously reload that same gain value at the arrival of the next user burst.

For applications other than cellular phones (where the preambles are not changed), the PDC frequency discriminator output can be used to obtain correlation on the preamble pattern to aid in burst acquisition.

TABLE 2. CELLULAR BASESTATION APPLICATIONS USING TDMA

STANDARD	GSM	PCN	IS-54
TYPE	Cellular	Cellular	Cellular
BASESTATION RX BAND (MHz)	935-960	1805-1880	824-849
CHANNEL BW (kHz)	200	200	30
# TRAFFIC CHANNELS	8	16	3
VOICE MODULATION	GMSK	GMSK	π/4 DQPSK
CHANNEL RATE (Kbps)	270.8	270.8	48.6
CONTROL MODULATION	GMSK	GMSK	π/4 DQPSK
CHANNEL RATE (Kbps)	270.8	270.8	48.6

Several applications are combinations of frequency and time domain multiple access schemes. For example, GSM is a TDMA signal that is frequency hopped. The individual channels contain Gaussian MSK modulated signals. The PDC again offers the 0.012Hz tuning resolution for de-hopping the received signal. The combination of halfband and 256-tap programmable, 22-bit coefficient FIR filters readily performs the necessary matched filtering for demodulation and optimum detection of the GMSK signals.

CDMA Based Standards and Applications

For Code Division Multiple Access (CDMA) type signals, the PDC offers the ability to have a single wideband RF front end, from which it can select a single spread channel of interest. The synchronization circuitry provides for easy control of multiple PDC for applications where multiple received signals are required, such as base-stations.

In IS-95 CDMA, the receive signal bandwidth is approximately 1.2288MHz wide with many spread spectrum channel in the band. The PDC supplies the downconversion and filtering required to receive a single RF channel in the presence of strong adjacent interference. Multiple PDC's would be sourced from a single receive RF chain, each processing a different receive frequency channel. The despreader would usually follow the PDC. In some very specific applications, with short, fixed codes, the filtering and despreading may be possible with innovative use of the programmable, 22-bit coefficient FIR filter. The PDC offers 0.012Hz resolution on tuning to the desired receive channel and excellent rejection of the portions of the band not being processed, via the halfband and 255-tap programmable, 22-bit coefficient FIR filter.

Traditional Modulation Formats

AM, ASK, FM and FSK

The PDC has the capability to fully demodulate AM and FM modulated waveforms. The PDC outputs 15 bits of amplitude or 16 bits of frequency for these modulation formats. The FM discriminator has a 63-tap programmable, 22-bit coefficient FIR filter for additional signal conditioning of the FM signal. Digital versions of these formats, ASK and FSK are also readily processed using the PDC. Just as in the AM modulated case, ASK signals will use 15-bit magnitude output of the Cartesian to Polar Coordinate converter. Multi-tone FSK can be processed several ways. The frequency information out of the discriminator can be used to identify the received tone, or the filter can be used to identify and power detect a specific tone of the received signal. AMPS is an example of an FM application.

PM and PSK

The PDC provides the downconversion, demodulation, matched filtering and coordinate conversion required for demodulation of PM and PSK modulated waveforms. These modulation formats will require external carrier and symbol timing recovery loop filters to complete the receiver design. The PDC was designed to interface with the HSP50210 Digital Costas Loop to implement the carrier phase and symbol timing recovery loop filters (for continuous PSK signals - not burst).

Digital modulation formats that combine amplitude and phase for symbol mapping, such as m-ary QAM, can also be downconverted, demodulated, and matched filtered. The received symbol information is provided with 16 bits of resolution in either Cartesian or Polar coordinates to facilitate remapping into bits and to recover the carrier phase. External Symbol mapping and Carrier Recovery Loop Filtering is required for this waveform.

Resampling and Interpolation Filters

Two key features of the resampling FIR filter are that the resampler filter allows the output sample rate to be programmed with millihertz resolution and that the output sample rate can be phase locked to an independent separate clock. The resampler frees the front end sampling clocks from having to be synchronous or integrally related in rate to the baseband output. The asynchronous relationship between front end and back end clocks is critical in applications where ISDN interfaces drive the baseband interfaces, but the channel sample rates are not related in any way. The interpolation halfband filters can increase the rate of the output when narrow frequency bands are being processed. The increase in output rate allows maximum use of the programmable FIR while preserving time resolution in the baseband data.

14-Bit Input and Processing Resolution

The PDC maintains a minimum of 14 bits of processing resolution through to the output, providing over 84dB of dynamic range. The 18 bits of resolution on the internal references provide a spurious floor that is better than 98dBc. Furthermore, the PDC provides up to 42dB of gain scaling to compensate for any change in gain in the RF front end as well as up to 96dB of gain in the internal PDC AGC. This gain maximizes the output resolution for small signals and compensates for changes in the RF front end gain, to handle changes in the incoming signal.

Summary

The greatest feature of the PDC is its ability to be reconfigured to process many common standards in the communications industry. Thus, a single hardware element can receive and process a wide variety of signals from PCS to traditional cellular, from wireless local loop to SATCOM. The high resolution frequency tuning and narrowband filtering are instrumental in almost all of the applications.

Multiple Chip Synchronization

Multiple PDCs are synchronized using a MASTER/SLAVE configuration. One part is responsible for synchronizing the front end internal circuitry using CLKIN while another part is responsible for synchronizing the backend internal circuitry using PROCCLK.

The PDC is synchronized with other PDCs using five control lines: SYNCOUT, SYNCIN1, SYNCIN2, MSYNCO, and MSYNCI. Figure 2 shows the interconnection of these five signals for multiple chip synchronization where different sources are used for CLKIN and PPOCCLK.

PDC A is the Master sync through MSO.

PDC B configures the CLKIN sync through SYNCIN1.

PDC A configures the PROCCLK sync through SYNCIN2.

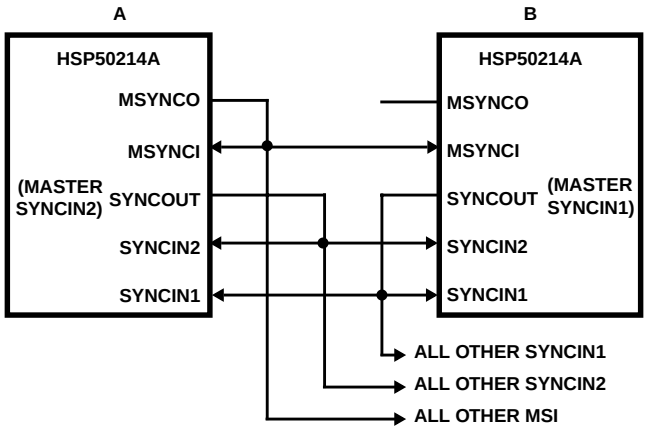


FIGURE 2. SYNCHRONIZATION CIRCUIT

SYNCOUT for PDC B should be set to be synchronous with CLKIN (Control Word 0, Bit 3 = 0. See the Microprocessor Write Section). SYNCOUT for PDC B is tied to the SYNCIN1 of all the PDCs. The SYNCIN1 can be programmed so that the carrier NCO and/or the 5th order CIC filter of all PDCs can be synchronously loaded/updated using SYNCIN1. See Control Word 0, Bits 19 and 20 in the Microprocessor Write Section for details.

SYNCOUT for one of the PDC's other than PDC B, should be set for PROCCLK (bit 3 = 1 in Control Word 0). This output signal is tied to the SYNCIN2 of all PDCs. The SYNCIN2 can be programmed so that the AGC updates its accumulator with the contents in the master registers (Control Word 8, Bit 29 in the Microprocessor Write Section). SYNCIN2 is also used to load or reset the timing NCO using bit 5, Control Word 11. The halfband and FIR filters can be reset on SYNCIN2 using Control Word 7, Bit 21. The MSYNCO of one of the PDCs is then used to drive the MSYNCI of all the PDCs (including its own).

For application configurations where CLKIN and PROCCLK have the same source, SYNCIN1 and SYNCIN2 can be tied together. However, if different enabling is desired for the front end and backend processing of the PDC's, these signals can still be controlled independently.

In the HSP50214A, the Control Word 25 reset signal has been extended so that the front end reset is 10 CLKIN periods wide and the back end reset is 10 PROCCLK periods wide. This guarantees that no enables will be caught in the pipelines. In addition, the SYNCIN1 internal reset signal, which is enabled by setting Control Word 7, Bit 21 = 1, has been extended to 10 cycles.

In summary, SYNCIN1 is used to update carrier phase offset, update carrier center frequency, reset CIC decimation counters and reset the carrier NCO (clear the feedback in the NCO). SYNCIN2 is used to reset the HB filter, FIR filter, re-sampler/HB state machines and the output FIFO, load a new gain into the AGC and load a new re-sampler NCO center frequency and phase offset.

Input Section

The block diagram of the input controller is provided in Figure 3. The input can support offset binary or two's complement data and can be operated in gated or interpolated mode (see Control Word 0 from the Microprocessor Write Section). The gated mode takes one sample per clock when the input enable (ENI) is asserted. The gated mode allows the user to synchronize a low speed sampling clock to a high speed CLKIN.

The interpolated mode allows the user to input data at a low sample rate and to zero-stuff the data prior to filtering. This zero stuffing effectively interpolates the input signal up to the rate of the input clock (CLKIN). This interpolated mode allows the part to be used at rates where the sampling frequency is above the maximum input rate range of the halfband filter section, and where the desired output bandwidth is too wide to use a Cascaded Integrator Comb (CIC) filter without significantly reducing the dynamic range. See Figures 4-7 for an interpolated input example, detailing the associated spectral results.

Interpolation Example:

The specifications for the interpolated input example are:

Input Sample Rate = 5 MSPS
PROCCLK = 28MHz
Interpolate by 8, Decimate by 10
Desired 85dB dynamic range output bandwidth = 500kHz

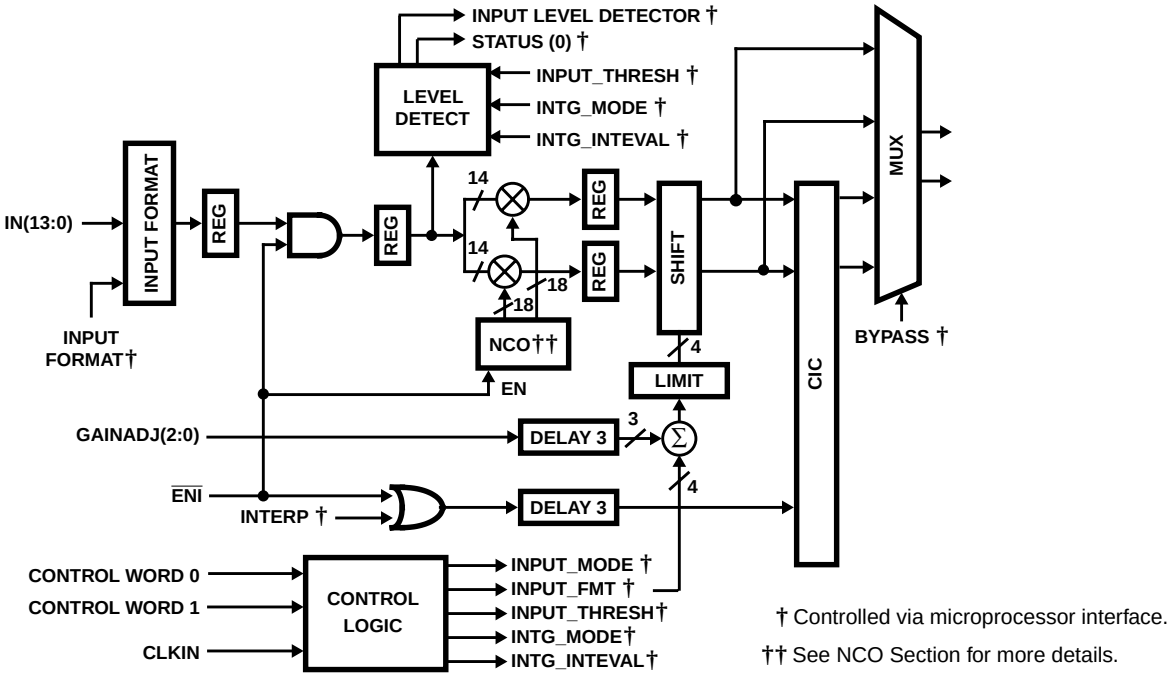
Input Level Detector

The Input Level Detector Section measures the average magnitude error at the PDC input for the microprocessor by comparing the input level against a programmable threshold and then integrating the result. It is intended to provide

a gain error for use in an AGC loop with either the RF/IF or A/D converter stages (see Figure 8). The AGC loop includes Input Level Detector, the microprocessor and an external gain control amplifier (or attenuator). The input samples are rectified and added to a threshold programmed via the microprocessor interface, as shown in Figure 9. The bit weighting of the data path through the input threshold detector is shown in Figure 10. The threshold is a signed number, so it should be set to the inverse of the desired input level. The threshold can be set to zero if the average input level is desired instead of the error. The sum of the threshold and the absolute value of the input is accumulated in a 32-bit accumulator. The accumulator can handle up to 2^{18} samples without overflow. The integration time is controlled by an 18-bit counter. The integration counter preload (ICPrel) is programmed via the microprocessor interface through Control Word 1. Only the upper 16 bits are programmable. The 2 LSBs are always zero. Control Word 1, Bits 29-14 are programmed to:

$$ICPrel = (N)/4 + 1 \quad \text{(EQ. 1)}$$

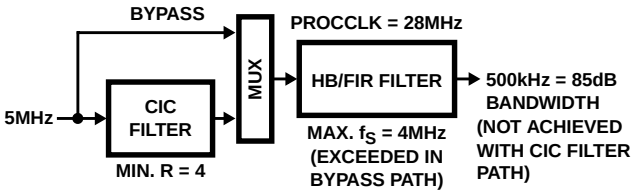
where N is the desired integration period, defined as the number of input samples to be integrated. N must be a multiple of 4: [0, 4, 8, 12, 16 .... , 2^{18}].



† Controlled via microprocessor interface.

†† See NCO Section for more details.

FIGURE 3. BLOCK DIAGRAM OF THE INPUT SECTION



Without Interpolation, the CIC bypass path exceeds the HB/FIR filter input sample rate and the CIC filter path will not yield the desired 85dB dynamic range band width of 500kHz.

FIGURE 4. STATEMENT OF THE PROBLEM

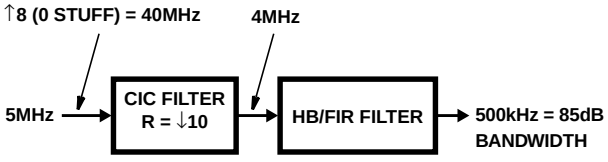


FIGURE 5. BLOCK DIAGRAM OF THE INTERPOLATION APPROACH

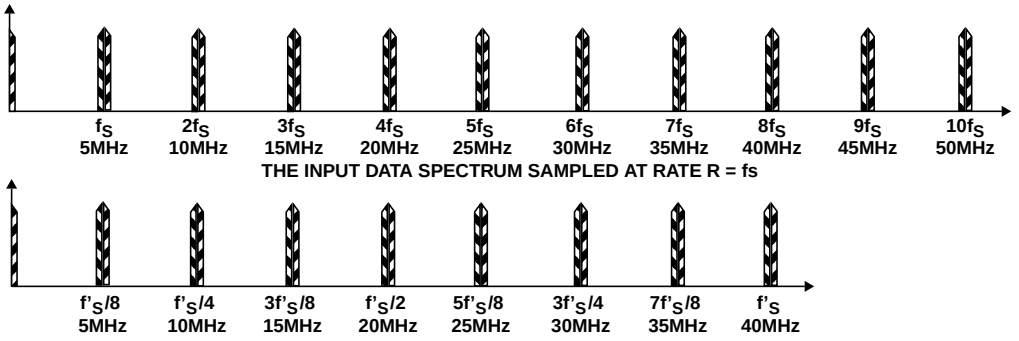


FIGURE 6. INTERPOLATION SPECTRUM: INTERPOLATE BY 8 THE INPUT DATA WITH ZERO STUFFING; SAMPLE AT RATE R = f'_S

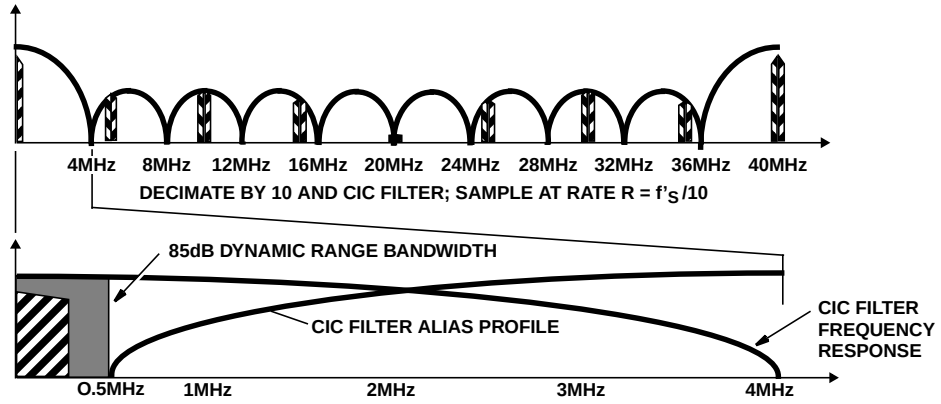


FIGURE 7. ALIAS PROFILE AND THE 85dB DYNAMIC RANGE BANDWIDTH

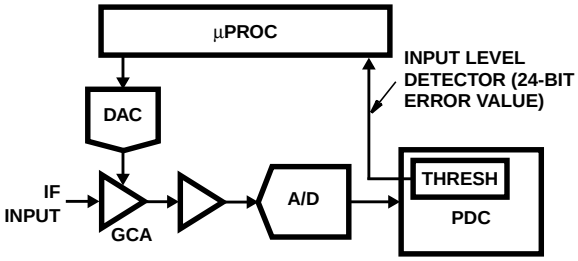
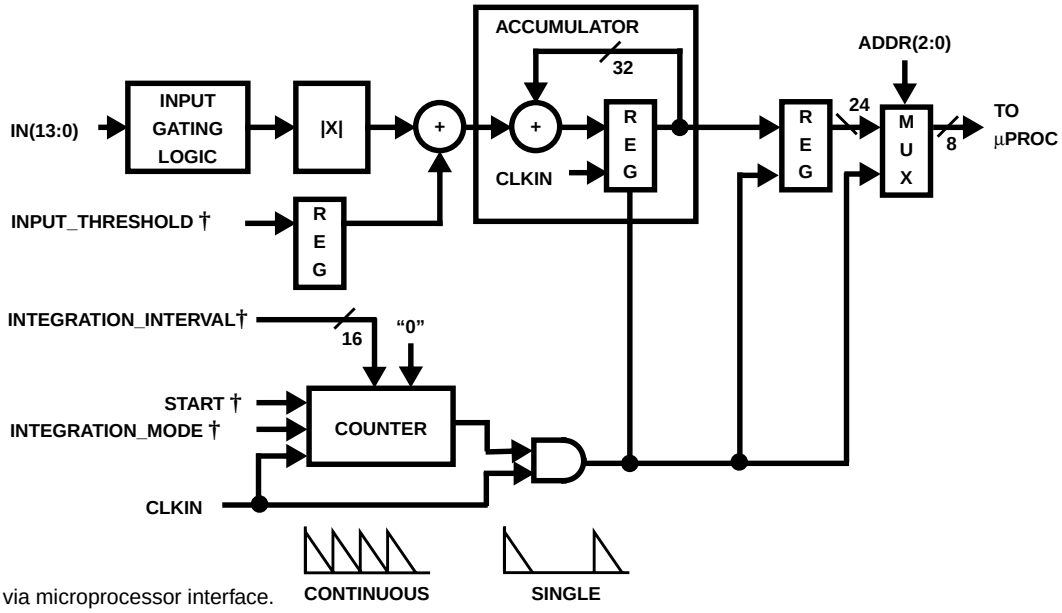


FIGURE 8. PROCESSOR BASED EXTERNAL IF AGC



† Controlled via microprocessor interface.

FIGURE 9.

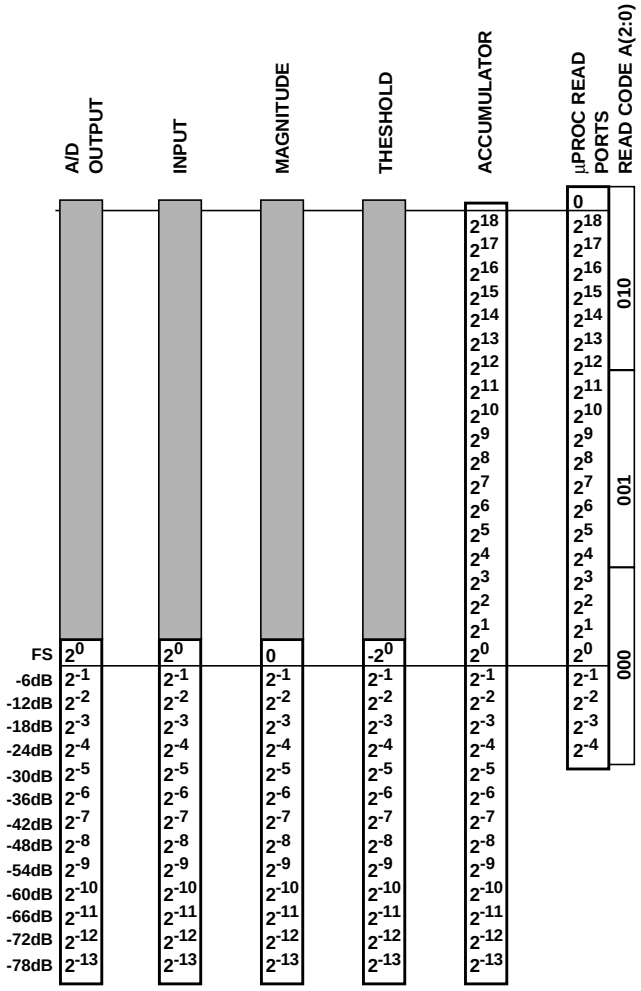


FIGURE 10. INPUT THRESHOLD DETECTOR BIT WEIGHTING

The integration period counter can be set up to run continuously or to count down and stop. Continuous integration counter operation lets the counter run, with sampling occurring every time the counter reaches zero. Because the processor samples the detector read port asynchronous to the CLKIN, data can be missed unless the status bit is monitored by the processor to ensure that a sample is taken for every integration count down sequence.

Additionally, in the HSP50214A, the ability to align the start/restart of the input level detector integration period with an external event is provided. This allows the sync signals, which are synchronized to external events, to be used to align all of the gain adjustments or measurements. If Control Word 27, Bit 17 is set to a logic one, the SYNCIN1 signal will cause the input level detector to start/restart its integration period. If Control Word 27, Bit 17 is set to a logic zero, control of the start/restart of the input level detector integration period does not respond to SYNCIN1.

In the count down and stop mode, the microprocessor read commands can be synchronized to system events, such as the start of a burst for a TDMA application. The integration counter can be started at any time by writing to Control Word 2. At the end of the integration period (counter = 0000), the upper 23 bits of the accumulator are transferred to a holding register for reading by the microprocessor. Note that it is not the restarting of the counter (by writing to Control Word 2) that latches the current value, but the end of the integration count. When the accumulator results are latched, a bit is set in the Status Register to notify the processor. Reading the most significant byte of the 23 bits clears the status bit. See the Microprocessor Read Section. Figure 10 illustrates a typical AGC detection process.

Typically, the average input error is read from the Input Level Detector port for use in AGC Applications. By setting the threshold to 0, however, the average value of the input signal can be read directly. The calculation is:

$$dBFS_{RMS} = (20)\log[(1.111)(level)/((N)(16))] \quad \text{(EQ. 2)}$$

where “level” is the 24-bit value read from the 3 level Detector Registers and “N” is the number of samples to be integrated. Note that to get the RMS value of a sinusoid, multiply the average value of the rectified sinusoid by 1.111. For a full scale input sinusoid, this yields an RMS value of approximately 3 dBFS.

NOTE: 1.111 scales the rectified sinusoid average (2/π) to 1/√2

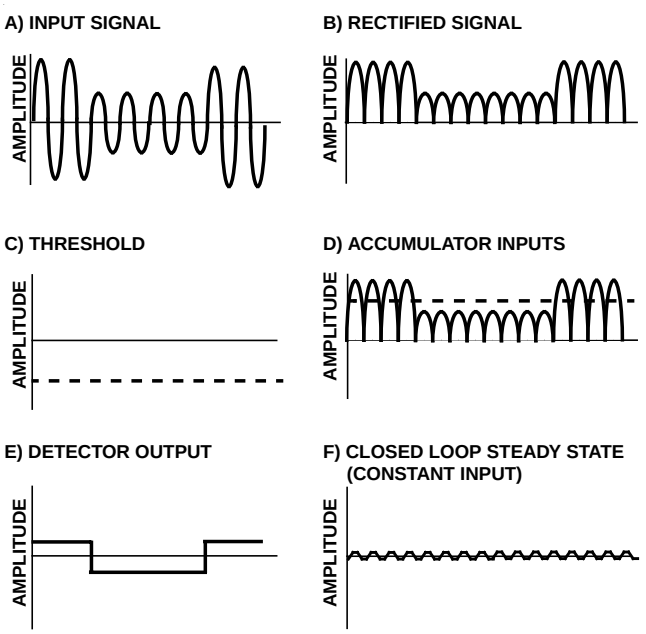


FIGURE 11. SIGNAL PROCESSING WITHIN LEVEL DETECTOR

In the HSP50214A, the polarity of the two LSB’s of the integration period pre-load is selectable. If Control Word 27, Bit 23 is set to a logic one, the two LSB’s of the integration period preload are set to logic ones. This allows a power of two to be set for the integration period, for easy normalization in the processor. If Control Word 27, Bit 23 is set to a logic zero, then the two LSB’s of the integration period preload are set to zeros as in the HSP50214.

Carrier Synthesizer/Mixer

The Carrier Synthesizer/Mixer Section of the HSP50214A is shown in Figure 12. The NCO has a 32-bit phase accumulator, a 10-bit phase offset adder, and a sine/cosine ROM.

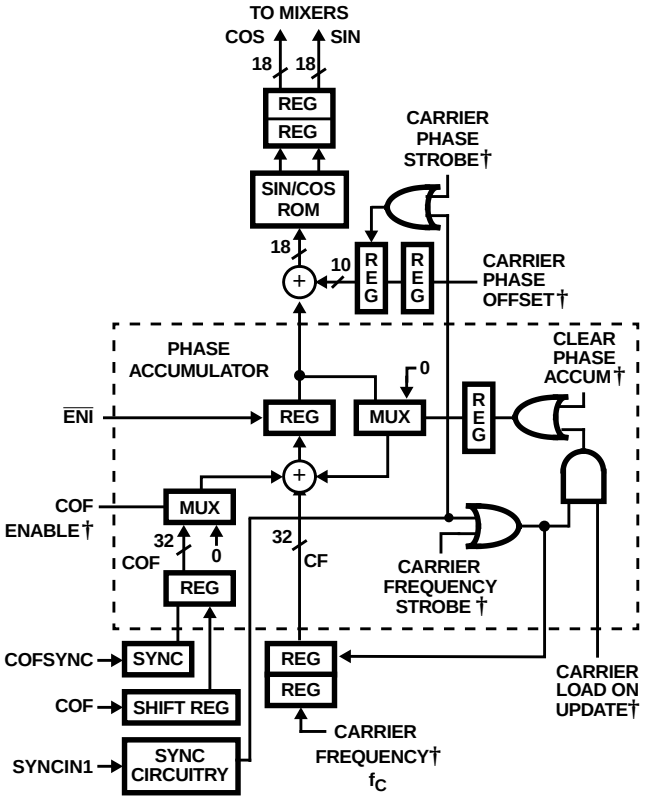
The frequency of the NCO is the sum of a center frequency Control Word, loaded via the microprocessor interface (Control Word 3, Bits 0 to 31), and an offset frequency, loaded serially via the COF and COFSYNC pins. The offset frequency can be zeroed in Control Word 0, Bit 1. Both frequency control terms are 32 bits and the addition is modulo 232. The output frequency of the NCO is computed as:

$$f_C = f_S * N/(2^{32}), \quad \text{(EQ. 3)}$$

or in terms of the programmed value:

$$N = INT[f_C \times 2^{32}/f_S]_{HEX}, \quad \text{(EQ. 3A)}$$

where N is the 32-bit sum of the center and offset frequency terms, fC is the frequency of the carrier NCO sinusoids, f_S is the input sampling frequency, and INT is the integer of the computation. See the Microprocessor Write Section on instructions for writing Control Word 3.



† Controlled via microprocessor interface.

FIGURE 12. BLOCK DIAGRAM OF NCO SECTION

For example, if N is 3267 (decimal), and f_S is 65MHz, then fC is 49.44Hz. If received data is modulated at a carrier frequency of 10MHz, then the synthesizer/mixer should be programmed for N = 27627627 (hex) or D89D89B9 (hex).

Because the input enable, ENI, controls the operation of the phase accumulator, the NCO output frequency is computed relative to the input sample rate, f_S, not to f_{CLKIN}. The frequency control, N, is interpreted as two's complement because the output of the NCO is quadrature. Negative frequency L.O.s select the upper sideband; positive frequency L.O.s select the lower sideband. The range of the NCO is -fS/2 to + fS/2. The frequency resolution of the NCO is fS/(232) or approximately 0.015Hz when CLKIN is 65 MSPS and ENI is tied low.

The phase of the Carrier NCO can be shifted by adding a 10-bit phase offset to the MSB's (modulo 360o) of the output of the phase accumulator. This phase offset control has a resolution of 0.35o and can be interpreted as two's complement from -180o to 180o (-p to p) or as binary from 0 to 360o (0 to 2p). The phase offset is given by:

$$\phi_{OFF} = 2\pi \times (PO/2^{10}); (-(2^9 - 1) < PO < (2^9 - 1)) \quad \text{(EQ. 4)}$$

or, in terms of the parameter to be programmed:

$$PO = INT[(2^{10}\phi_{OFF})/2\pi]_{HEX}; (-\pi < \phi_{OFF} < \pi) \quad \text{(EQ. 4A)}$$

where PO is the 10-bit two's complement value loaded into the Phase Offset Register (Control Word 4, Bits 9-0). For example, a value of 32 (decimal) loaded into the Phase Offset Register would produce a phase offset of 11.25o and a value of -512 would produce an offset of 180o. The phase offset is loaded via the microprocessor interface. See the Microprocessor Write Section on instructions for writing Control Word 4.

The most significant 18 bits from the phase adder are used as the address a sin/cos lookup table. This lookup table maps phase into sinusoidal amplitude. The sine and cosine values have 18 bits of amplitude resolution. The spurious components in the sine/cosine generation are at least -98dBc. The sine and cosine samples are routed to the mixer section where they are multiplied with the input samples to translate the signal of interest to baseband.

The mixer multiplies the 14-bit input by the 18-bit quadrature sinusoids. The mixer equations are:

$$I_{OUT} = I_{IN} \times \cos(\omega_c) \quad \text{(EQ. 5)}$$

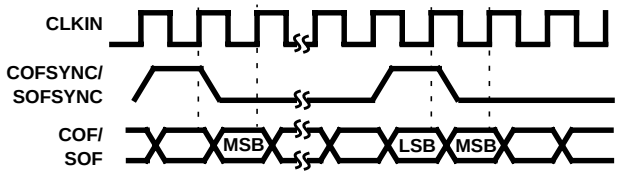
$$Q_{OUT} = I_{IN} \times \sin(\omega_c) \quad \text{(EQ. 5A)}$$

The mixer output is rounded symmetrically to 15 bits.

To allow the frequency and phase of multiple parts to be updated synchronously, two sets of registers are used for latching the center frequency and phase offset words. The offset phase and center frequency Control Words are first loaded into holding registers. The contents of the holding registers are transferred to active registers in one of two ways. The first technique involves writing to a specific Control Word Address. A processor write to Control Word 5, transfers the center frequency value to the active register while a processor write to Control Word 6 transfers the phase offset value to the active register.

The second technique, designed for synchronizing updates to multiple parts, uses the SYNCIN1 pin to update the active registers. When Control Word 1, Bit 20 is set to 1, the SYNCIN1 pin causes both the center frequency and Phase Offset Holding Registers to be transferred to active registers. Additionally, when Control Word 0, Bit 0 is set to 1, the feedback in the phase accumulator is zeroed when the transfer from the holding to active register occurs. This feature provides synchronization of the phase accumulator starting phase of multiple parts. It can also be used to reset the phase of the NCO synchronous with a specific event.

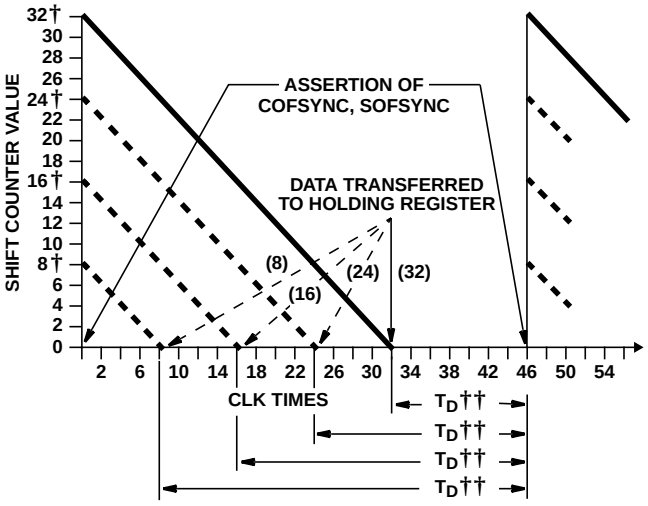
The carrier offset frequency is loaded using the COF and COFSYNC pins. Figure 13 details the timing relationship between COF, COFSYNC and CLKIN. The offset frequency word can be zeroed if it is not needed. Similarly, the Sample Offset Frequency Register controlling the Re-Sampler NCO is loaded via the SOF and SOFSYNC pins. The procedure for loading data through the two pin NCO interfaces is identical except that the timing of SOF and SOFSYNC is relative to PROCCLK.



OTE: Data must be loaded MSB first.

IGURE 13. SERIAL INPUT TIMING FOR COF AND SOF INPUTS

Each serial word has a programmable word width of either 8, 16, 24, or 32 bits (See Control Word 0, Bits 4 and 5, for the Carrier NCO programming and Control Word 11, Bits 3 and 4, for Timing NCO programming). On the rising edge of the clock, data on COF or SOF is clocked into an input shift register. The beginning of a serial word is designated by asserting either COFSYNC or SOFSYNC "high" one CLK period prior to the first data bit.



†Serial word width can be: 8, 16, 24, 32 bits wide.

†T_D is determined by the COFSYNC, COFSYNC rate.

FIGURE 14. HOLDING REGISTERS LOAD SEQUENCE FOR COF AND SOF SERIAL OFFSET FREQUENCY DATA

NOTE: Serial Data must be loaded MSB first, and COFSYNC or SOFSYNC should not be asserted for more than one CLK cycle.

NOTE: COF loading and timing is relative to CLKIN while SOF loading and timing is relative to PROCCLK.

NOTE: T_D can be 0, and the fastest rate is with 8-bit word width.

The assertion of the COFSYNC (or SOFSYNC) starts a count down from the programmed word width. On following CLKs, data is shifted into the register until the specified number of bits have been input. At this point the contents of the register are transferred from the Shift Register to the respective 32-bit Holding Register. The Shift Register can accept new data on the following CLK. If the serial input word is defined to be less than 32 bits, it will be transferred to the MSBs of the 32-bit Holding Register and the LSBs of the Holding Register will be zeroed. See Figure 14 for details.

CIC Decimation Filter

The mixer output may be filtered with the CIC filter or it may be routed directly to the halfband filters. The CIC filter is used to reduce the sample rate of a wideband signal to a rate that the halfbands and programmable filters can process, given the maximum computation speed of PROCCLK. (See Halfband and FIR Filter Sections for techniques to calculate this value).

Prior to the CIC filter, the output of the mixer goes through a barrel shifter. The shifter is used to adjust the gain in 6dB steps to compensate for the variation in CIC filter gain with decimation. (See Equation 6). Fine gain adjustments must be done in the AGC Section. The shifter is controlled by the sum of a 4-bit CIC Shift Gain word from the microprocessor and a 3-bit gain word from the GAINADJ(2:0) pins. The three bit value is pipelined to match the delay of the input samples. The sum of the 3 and 4-bit shift gain words saturates at a value of 15. Table 1 details the permissible values for the GAINADJ(2:0) barrel shifter control, while Figure 15 shows the permissible CIC Shift Gain values.

The CIC filter structure for the HSP50214A is fifth order; that is it has five integrator/comb pairs. A fifth order CIC has 84dB of alias attenuation for output frequencies below 1/8 the CIC output sample rate.

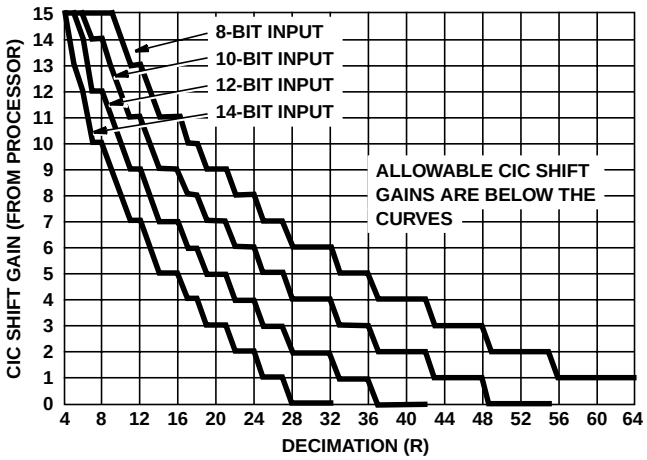


FIGURE 15. CIC SHIFT GAIN VALUES

The decimation factor of the CIC filter is programmed in Control Word 0, Bits 12 - 7. The CIC Shift Gain is programmed in Control Word 0, Bits 16-13. The CIC Bypass is set in Control Word 0, Bit 6. When bypassing the CIC filter, the $\overline{ENI}$ signal must be deasserted between samples, i.e., the C_{LKIN} note must be $\geq 2\ f_S$.

TABLE 3. GAIN ADJUST CONTROL AND CIC DECIMATION

ΔGAIN VALUE (dB)	GAIN ADJ(2:0)	MAX. CIC DECIMATION
0	000	32
6	001	27
12	010	24
18	011	21
24	100	18
30	101	16
36	110	12
42	111	10

CIC Gain Calculations

The gain through the CIC filter increases with increased decimation. The programmable barrel shifter that precedes the first integrator in the CIC is used to offset this variation. Gain variations due to decimation should be offset using the 4-bit CIC Shift Gain word. This allows the input signal level to be adjusted in 6dB steps to control the CIC output level.

The gain at each stage of the CIC is:

$$k = R^N, \quad \text{(EQ. 6)}$$

where R is the decimation factor and N is the number of stages. The input to the CIC from the mixer is 15 bits, and the bit widths of the accumulators for the five stages in the HSP50214A are 40, 36, 32, 32, and 32, as shown in Figure 16. This limits the maximum decimation in the CIC to 32 for a full scale input.

If R is 32, the gain through all five integrator stages is $32^5 = 2^{25}$. (The gain through the last four CIC stages is 2^{20}, through the last 3 it is 2^{15}, etc.). The sum of the input bits and the growth bits cannot exceed the accumulator size. This means that for a decimation of 32 and 15 input bits, the first accumulator must be 15 + 25 = 40 bits.

Thus, the value of the CIC Shift Gain word can be calculated:

$$SG = FLOOR\,[39 - (IIN) - \log_2(R)^5 \text{ for } 4<R<32 \quad = 15 \text{ for } R = 4 \quad \text{(EQ. 7)}$$

NOTE: The number of input bits is IIN. (If the number of bits into the CIC filter is used, the value 40 replaces 39).

For 14 bits, Equation 7 becomes:

$$SG = FLOOR[25 - \log_2(R)^5] \text{ for } 4 < R < 32 \quad = 15 \text{ for } R = 4 \quad \text{(EQ. 8A)}$$

For 12 bits, Equation 7 becomes:

$$SG = FLOOR[27 - \log_2(R)^5] \text{ for } 5 < R < 40 \quad = 15 \text{ for } 4 \le R \le 5 \quad \text{(EQ. 8B)}$$

For 10 bits, Equation 7 becomes:

$$SG = FLOOR[29 - \log_2(R)^5] \text{ for } 6 < R < 52 \quad = 15 \text{ for } 4 \le R \le 6 \quad \text{(EQ. 8C)}$$

For 8 bits, Equation 7 becomes:

$$SG = FLOOR[31 - \log_2(R)^5] \text{ for } 9 < R < 64 \quad = 15 \text{ for } 4 \le R \le 9 \quad \text{(EQ. 8D)}$$

Figure 15 is a plot of Equations 8A through 8D. The 4-bit CIC Shift Gain word has a range from 0 to 15. The 6-bit CIC Decimation Factor Counter Preload field, (R-1), has a range from 0 to 63, limited by the input resolution as cited above.

Using the Input Gain Adjust Control Signals

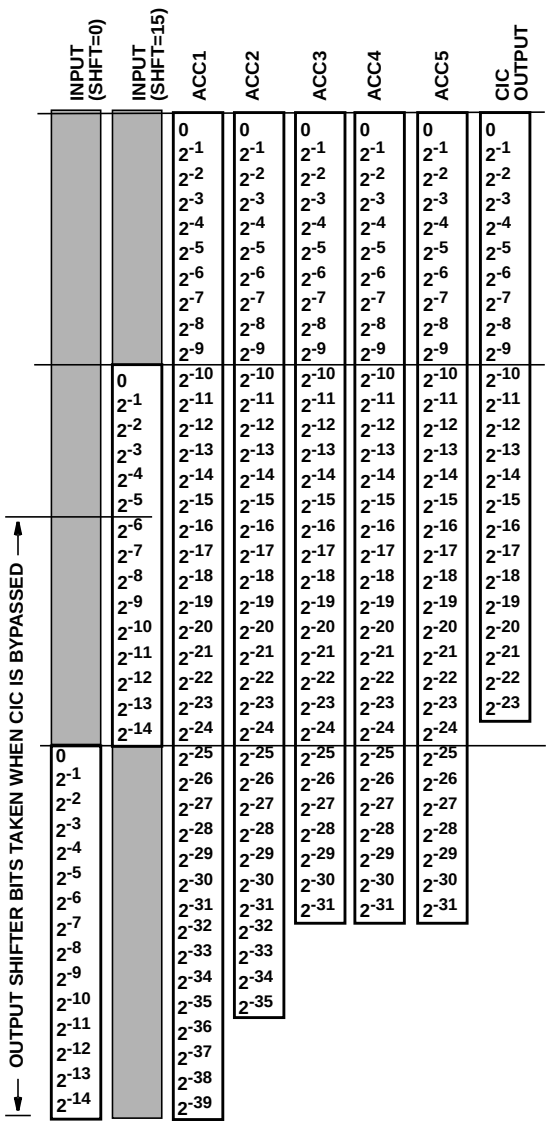
The input gain offset control GAINADJ(2:0)) is provided to offset the signal gain through the part, i.e., to keep the CIC filter output level constant as the analog front end attenuation is changed. The gain adjust offset is 6dB per code, so the gain adjust range is 0 to 42dB. For example, if 12dB of attenuation is switched in at the receiver RF front end, a code of 2 would increase the gain at the input to the CIC filter up 12dB so that the CIC filter output would not drop by 12dB. This fixed gain adjust eliminates the need for the software to continually normalize.

One must exercise care when using this function as it can cause overflow in the CIC filter. Each gain adjust in the shifter from the gain adjust control signals is the equivalent of an extra bit of input. The maximum decimation in the CIC is reduced accordingly. With a decimation of 32, all 40 bits of the CIC are needed, so no input offset gain is allowed. As the decimation is reduced, the allowable offset gain increases. Table 3 shows the decimation range versus desired offset gain range. Table 3 assumes that the CIC Shift Gain has been programmed per Equation 7 or 8A.

The CIC filter decimation counter can be loaded synchronous with other PDC chips, using the SYNCIN1 signal and the CIC External Sync Enable bit. The CIC external Sync Enable is set via Control Word 0, Bit 19.

Halfband Decimating Filters

The Programmable Down Converter has five halfband filter stages, as shown in Figure 17. Each stage decimates by 2 and filters out half of the available bandwidth. The first halfband, or HB1, has 7 taps. The remaining halfbands; HB2, HB3, HB4, and HB5; have 11, 15, 19, and 23 taps respectively. The coefficients for these halfbands are given in Table 4. Figure 18 shows the frequency response of each of the halfband filters with respect to normalized frequency, F_N. Frequency normalization is with respect to the input sampling frequency of each filter section. Each stage is activated by their respective bit location (15-20) in Control Word 7. Any combination of halfband filters may be used, or all may be bypassed.



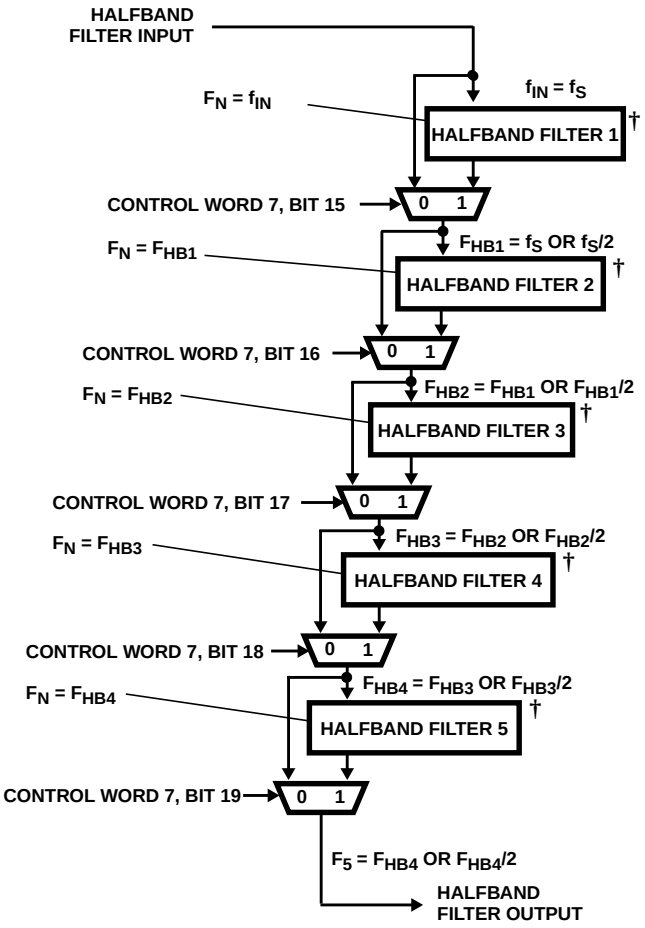
NOTE: If 14 input bits are not needed, the gain adjust can be increased by one for each bit that the input is shifted down at the input. For example, if only 12 bits are needed, an offset range of 24dB is possible for a decimation of 24.

FIGURE 16. CIC FILTER BIT WEIGHTING

Since each halfband filter section decimates by 2, the total decimation through the halfband filter is given by:

$$DEC_{HB} = 2^{N} \quad \text{(EQ. 9)}$$

where N = Number of Halfband Filters Selected (1 - 5).



† Each halfband section decimates by 2.

FIGURE 17. BLOCK DIAGRAM OF HALFBAND FILTER SECTION

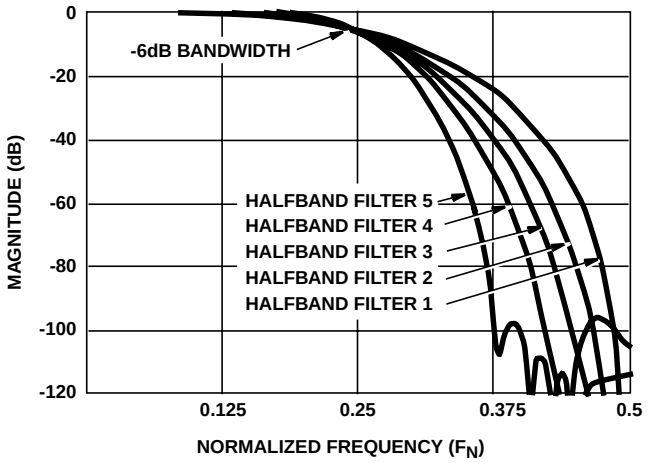


FIGURE 18. HALFBAND FILTER FREQUENCY RESPONSE

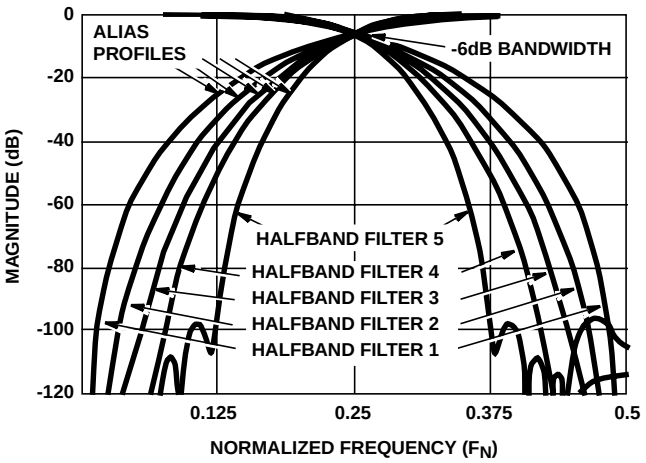


FIGURE 19. HALFBAND FILTER ALIAS CONSIDERATIONS

TABLE 4. HALFBAND FILTER COEFFICIENTS

COEFFICIENTS	HALFBAND #1	HALFBAND #2	HALFBAND #3	HALFBAND #4	HALFBAND #5
C0	- 0.031303406	0.005929947	-0.00130558	0.000378609	-0.000347137
C1	0.000000000	0.000000000	0.000000000	0.000000000	0.000000000
C2	0.281280518	-0.049036026	0.012379646	-0.003810883	0.00251317
C3	0.499954224	0.000000000	0.000000000	0.000000000	0.000000000
C4	0.281280518	0.29309082	-0.06055069	0.019245148	-0.010158539
C5	0.000000000	0.499969482	0.000000000	0.000000000	0.000000000
C6	- 0.031303406	0.29309082	0.299453735	-0.069904327	0.03055191
C7		0.000000000	0.499954224	0.000000000	0.000000000
C8		-0.049036026	0.299453735	0.304092407	-0.081981659
C9		0.000000000	0.000000000	0.500000000	0.000000000
C10		0.005929947	-0.06055069	0.304092407	0.309417725
C11			0.000000000	0.000000000	0.500000000
C12			0.012379646	-0.069904327	0.309417725
C13			0.000000000	0.000000000	0.000000000
C14			-0.00130558	0.019245148	-0.081981659
C15				0.000000000	0.000000000
C16				-0.003810883	0.03055191
C17				0.000000000	0.000000000
C18				0.000378609	-0.010158539
C19					0.000000000
C20					0.00251317
C21					0.000000000
C22					-0.000347137

***NOTE:** While Halfband filters are typically selected starting with the last stage in the filter chain to give the maximum alias free bandwidth, a higher throughput rate may be obtained using other filter combinations. See Application Note 9720, "Calculating Maximum Processing Rates of the PDC".*

Depending on the number of halfbands used, PROCCLK must operate at a minimum rate above the input sample rate, F_S, to the halfband. This relationship depends on the number of multiplies for each of the halfband filter stages. The filter calculations take 3, 4, 5, 6, and 7 multiplies per input for HB1, HB2, HB3, HB4, and HB5 respectively. If we keep the assumption that f_S is the input sampling frequency, then Equation 10 shows the minimum ratio needed.

$$f_{PROCCLK}/f_S \geq ([(7)(HB5)(2^{HB5})+ (6)(HB4)(2^{(HB4 + HB5)})+ (5)(HB3)(2^{(HB3+HB4+HB5)})+ (4)(HB2)(2^{(HB2+HB3+ HB4+HB5)})+ (3)(HB1)(2^{(HB1+HB2+HB3+HB4+HB5)})]/2^T \quad \text{(EQ. 10))}$$

where

HB1 = 1 if this section is selected and 0 if it is bypassed;
HB2 = 1 if this section is selected and 0 if it is bypassed;
HB3 = 1 if this section is selected and 0 if it is bypassed;
HB4 = 1 if this section is selected and 0 if it is bypassed;
HB5 = 1 if this section is selected and 0 if it is bypassed;
T = number of Halfband Filters Selected. The range for T is from 0 to 5.

Examples of PROCCLK Rate Calculations

Suppose we enable HB1, HB3, and HB5. Using Figure 16, HB1= 1, HB3 = 1, and HB5 = 1. Since stage 2 and stage 4 are not used, HB2 and HB4 = 0. PROCCLK must operate faster than (7x2+5x4+3x8)/8 = 7.25 times faster than F_S.

If all five halfbands are used, then PROCCLK must operate at (7x2+6x4+5x8+4x16+3x32)/32 = 7.4375 times faster than F_S.

255-Tap Programmable FIR Filter

The Programmable FIR filter can be used to implement real filters with even or odd symmetry, using up to 255 filter taps, or complex filters with up to 64 taps. The FIR filter takes advantage of symmetry in coefficients by summing data samples that share a common coefficient, prior to multiplication. In this manner, two filter taps are calculated per multiply accumulate cycle. Asymmetric filters cannot share common coefficients, so only one tap per multiply accumulate cycle is calculated. The filter can be effectively bypassed by setting the coefficient $C_0 = 1$ and all other coefficients, $C_N = 0$.

Additionally, the Programmable FIR filter provides for decimation factors, R, from 1 to 16. The processing rate of the Filter Compute Engine is PROCCLK. As a result, the frequency of PROCCLK must exceed a minimum value to ensure that a filter calculation is complete before the result is required for output. In configurations which do not use decimation, one input sample period is available for filter calculation before an output is required. For configurations which employ decimation, up to 16 input sample periods may be available for filter calculation.

For real filter configurations, use Equation 11 to calculate the number of taps available at a given input filter sample rate.

$$TAPS = (floor[PROCCLK/(F_{SAMP}/R) - R])(1 + SYM) - [(SYM)(ODD\#)] \quad \text{(EQ. 11A)}$$

for real filters, and

$$TAPS = floor[(PROCCLK/(F_{SAMP}/R) - R)/2] \quad \text{(EQ. 11B)}$$

for complex filters, where floor is defined as the integer portion of a number; PROCCLK is the compute clock; F_{SAMP} = the FIR input sample rate; R = Decimation Factor; SYM = 1 for symmetrical filter, 0 for asymmetrical filter; ODD# = 1 for an odd number of filter taps, 0 = an even number of taps.

Use Equation 12 to calculate the maximum input rate.

$$F_{SAMP} = (PROCCLK)(R)/[R + [floor[(Taps) + (SYM)(ODD\#)]/(1 + SYM)]] \quad \text{(EQ. 12A)}$$

for real filters, and

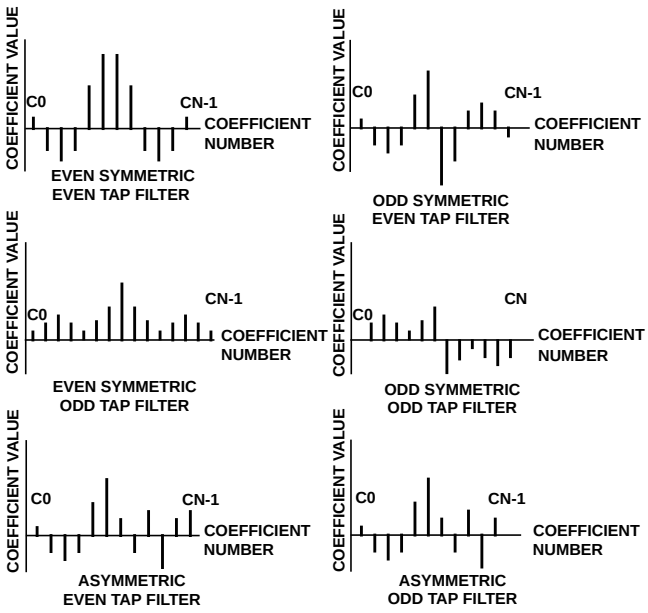
$$F_{SAMP} = [(PROCCLK)(R)]/[R + floor[(Taps)(2)]] \quad \text{(EQ. 12B)}$$

for complex filters, where floor[x], PROCCLK, F_{SAMP}, R = Decimation Factor, SYM, and ODD# are defined as in Equation 11.

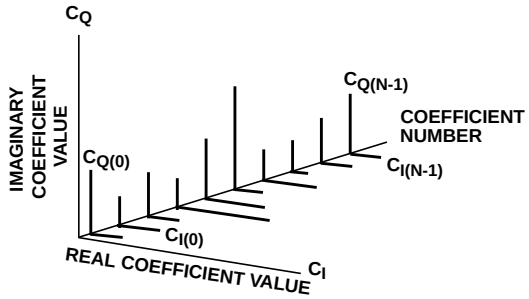
Use Equation 13 to calculate the maximum output sample rate for both real and complex filters.

$$F_{FIROUT} = (F_{SAMP})/R \quad \text{(EQ. 13)}$$

The coefficients are 22 bits and are loaded using writes to Control Words 128 through 255 (see Microprocessor Write Section). For real filters, the same coefficients are used by I and Q paths. If the filter is configured as a symmetric filter using Control Word 17, Bit 9, then coefficients are loaded starting with the center coefficient in Control Word 128 and proceeding to last coefficient in Control Word 128+n. The filter symmetry type can be set to even or odd symmetric, and the number of filter coefficients can be even or odd, as illustrated in Figure 20. Note that complex filters can also be realized but are only allowed to be asymmetric. Only the coefficients that are used need to be loaded.



REAL FILTERS



COMPLEX FILTERS

Definitions:

Even Symmetric: h(n) = h(N-n-1) for n = 0 to N-1

Odd Symmetric: h(n) = -h(N-n-1) for n = 0 to N-1

Asymmetric: A filter with no coefficient symmetry.

Even Tap filter: A filter where N is an even number.

Odd Tap filter: A filter where N is an odd number.

Real Filter: A filter implemented with real coefficients.

Complex Filters: A filter with quadrature coefficients.

FIGURE 20. DEMONSTRATION OF DIFFERENT TYPES OF DIGITAL FIR FILTERS CONFIGURED IN THE PROGRAMMABLE DOWNCONVERTER

Automatic Gain Control (AGC)

The AGC Section provides gain to small signals, after the large signals and out-of-band noise have been filtered out, to ensure that small signals have sufficient bit resolution in the Resampling/Interpolating Halfband filters and the Output Formatter. The AGC can also be used to manually set the gain. The AGC optimizes the bit resolution for a variety of input amplitude signal levels. The AGC loop automatically adds gain to bring small signals from the lower bits of the 26-bit programmable FIR filter output into the 16-bit range of the output section. Without gain control, a signal at -72dBf$_S$ = 20log$_{10}$(2^{-12}) at the input would have only 4 bits of resolution at the output (12 bits less than the full scale 16 bits). The potential increase in the bit resolution due to processing gain of the filters can be lost without the use of the AGC.

Figure 23 shows the Block Diagram for the AGC Section. The FIR filter data output is routed to the Resampling and Halfband filters after passing through the AGC multipliers and Shift Registers. The outputs of the Interpolating Halfband filters are routed to the Cartesian to Polar coordinate converter. The magnitude output of the coordinate converter is routed through the AGC error detector, the AGC error scaler and into the AGC loop filter. This filtered error term is used to drive the AGC multiplier and shifters, completing the AGC control loop.

The AGC Multiplier/Shifter portion of the AGC is identified in Figure 23. The gain control from the AGC loop filter is sampled when new data enters the Multiplier/Shifter. The limit detector detects overflow in the shifter or the multiplier and saturates the output of I and Q data paths independently. The shifter has a gain from 0 to 90.31dB in 6.021dB steps, where 90.31dB = 20log$_{10}$(2^N), when N = 15. The mantissa provides an additional 6dB of gain in 0.0338dB steps where 6.0204dB = 20log$_{10}$[1+(X)2^{-15}], where X = 2^{15}-1. Thus, the AGC multiplier/shifter transfer function is expressed as:

$$\text{AGC Mult/Shift Gain} = 2^N[1 + (X)2^{-15}], \quad \text{(EQ. 14)}$$

where N, the shifter exponent, has a range of 0>N>15 and X, the mantissa, has a range of 0>X>(2^{15}-1).

Equation 14 can be expressed in dB,

$$(\text{AGC Mult/Shift Gain})\text{dB} = 20\log_{10}(2^N[1 + (X)2^{-15}]) \quad \text{(EQ. 14A)}$$

The full AGC range of the Multiplier/Shifter is from 0 to 96.331dB (20log$_{10}$[1+(2^{15}-1)2^{-15}] + 20log$_{10}$[2^{15}] = 96.331). Figure 21 illustrates the transfer function of the AGC multiplier versus mantissa control for N = 0. Figure 22 illustrates the complete AGC Multiplier/Shifter Transfer function for all values of exponent and mantissa control.

The resolution of the mantissa was increased to 16 bits in the A Version, to provide a theoretical AM modulation level of -96dBc (depending on loop gain, settling mode and SNR). This effectively eliminates AM spurious caused by the AGC resolution.

For fixed gain, either set the upper and lower AGC limits to the same value, or set the limits to minimum and maximum gains and set the AGC gain to zero.

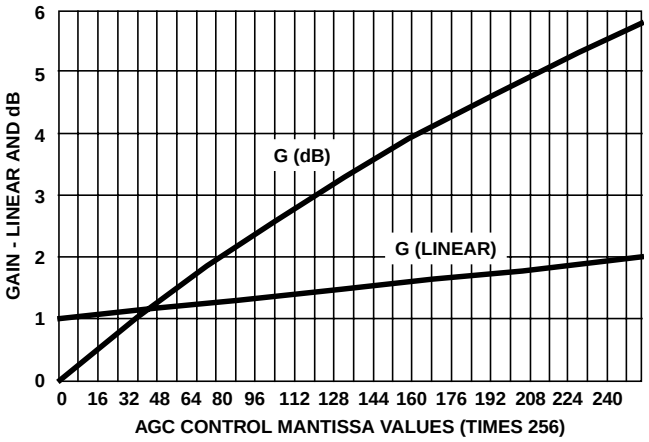


FIGURE 21. AGC MULTIPLIER LINEAR AND dB TRANSFER FUNCTION

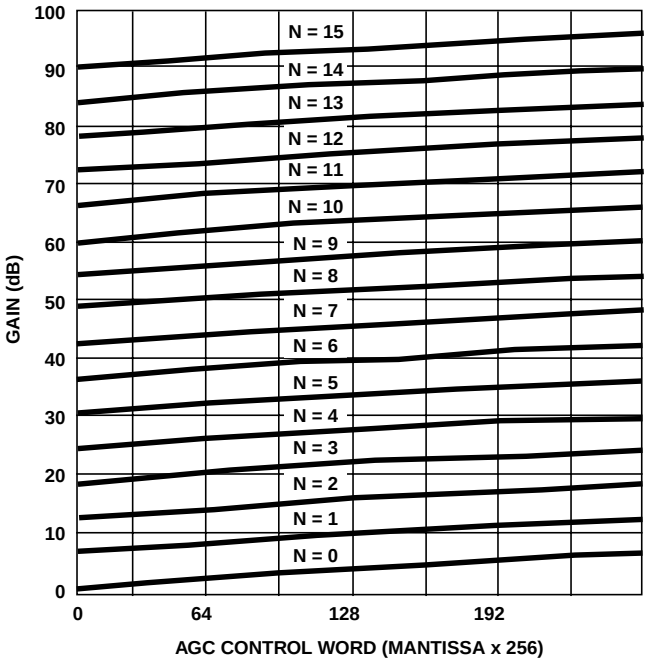


FIGURE 22. AGC GAIN CONTROL TRANSFER FUNCTION

The Cartesian to Polar Coordinate converter accepts I and Q data and generates magnitude and phase data. The magnitude output is determined by the equation:

$$|r| = 1.64676\sqrt{I^2 + Q^2}. \quad \text{(EQ. 15)}$$

where the magnitude limits are determined by the maximum I and Q signal levels into the Cartesian to Polar converter. Taking fractional 2's complement representation, magnitude ranges from 0 to 2.329, where the maximum output is

$$|r| = 1.64676\sqrt{(1.0)^2 + (1.0)^2} = 1.64676 \times 1.414 = 2.329.$$

The AGC loop feedback path consists of an error detector, error scaling, and an AGC loop filter. The error detector subtracts the magnitude output of the coordinate converter from the programmable AGC THRESHOLD value. The bit weighting of the AGC THRESHOLD value (Control Word 8, Bits 16-28) is shown in Table 5. Note that the MSB is always zero. The range of the AGC THRESHOLD value is 0 to 7.9995. The AGC Error Detector output has the identical range.

TABLE 5. AGC THRESHOLD (CONTROL WORD 8) BIT WEIGHTING

28	27	26	25	24	23	22	21	20	19	18	17	16
2^2	2^1	2^0.	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}

The loop gain is set in the AGC Error Scaling circuitry, using the two programmable mantissas and exponents. The mantissa, M, is a 4-bit value which weights the loop filter input from 0.0 to 0.9375. The exponent, E, defines a shift factor that provides additional weighting from 2^0 to 2^{-15}. Together the mantissa and exponent define the loop gain as given by,

$$\text{AGC Loop Gain} = M_{LG}2^{-4}\ 2^{-(15 - E_{LG})} \quad \text{(EQ. 16)}$$

where M_{LG} is a 4-bit binary value ranging from 0 to 15, and E_{LG} is a 4-bit binary value ranging from 0 to 15. Table 7 and 8 detail the binary values and the resulting scaling effects of the AGC scaling mantissa and exponent. The composite (shifter and multiplier) AGC scaling Gain range is from 0.0000 to $2.329(0.9375)2^0 = 0.0000$ to 2.18344. The scaled gain error can range (depending on threshold) from 0 to 2.18344, which maps to a "gain change per sample" range of 0 to 3.275dB/sample.

The AGC Gain mantissa and exponent values are programmed into Control Word 8, Bits 0-15. The PDC provides for the storing of two values of AGC Scaling Gain (both exponent and mantissa). This allows for quick adjustment of the loop gain by simply asserting the external control line AGCGNSEL. When AGCGNSEL = 0, then AGC GAIN 0 is selected, and when AGCGNSEL = 1, AGC Loop Gain 1 is selected. Possible applications include acquisition/tracking, no burst present/burst present, strong signal/weak signal, track/hold, or fast/slow AGC values.

The AGC loop filter consists of an accumulator with a built in limiting function. The maximum and minimum AGC gain limits are provided to keep the gain within a specified range and are programed by 12-bit Control Words using the following the equation:

$$\text{AGC Gain Limit} = (1 + m_{AGC}2^{-9})2^e \quad \text{(EQ. 17)}$$

$$(\text{AGC Gain Limit})\text{dB} = (6.02)(\text{eeee}) + 20\log(1.0 + 0.\text{eeeeeeee}) \quad \text{(EQ. 17A)}$$

where m is an 8-bit mantissa value between 0 and 511, and e is the 4-bit exponent ranging from 0 to 15. Control Word 9, Bits 16-27 are used for programming the upper limit, while bits 0-11 are used to program the lower threshold. The ranges and format for these limit values are shown in Tables 6A - C. The bit weightings for the AGC Loop Feedback elements are detailed in Table 9.

TABLE 6A. AGC LIMIT EXPONENT vs GAIN

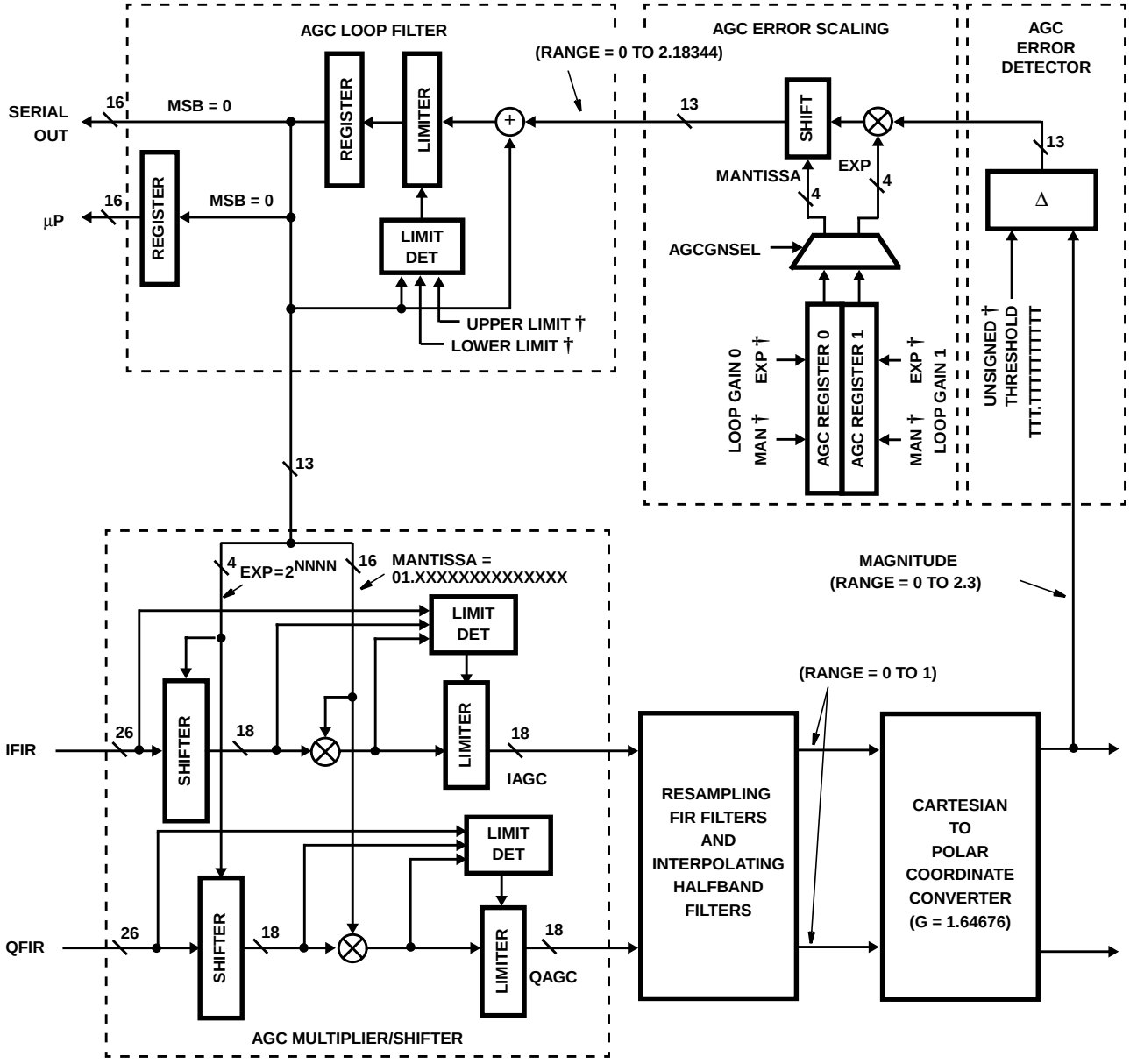
GAIN(dB)	EXPONENT	MANTISSA
96.330	15	511
90.309	15	0
84.288	14	0
78.268	13	0
72.247	12	0
66.227	11	0
60.206	10	0
54.185	9	0
48.165	8	0
42.144	7	0
36.124	6	0
30.103	5	0
24.082	4	0
18.062	3	0
12.041	2	0
6.021	1	0
0.000	0	0

TABLE 6B. AGC LIMIT MANTISSA vs GAIN

GAIN(dB)	EXPONENT	MANTISSA
6.000	0	509
5.750	0	480
5.500	0	452
5.250	0	425
5.000	0	398
4.750	0	372
4.500	0	347
4.250	0	323
4.000	0	299
3.750	0	276
3.500	0	254
3.250	0	232
3.000	0	211
2.750	0	190
2.500	0	170
2.250	0	151
2.000	0	132
1.750	0	114
1.500	0	96
1.250	0	79
1.000	0	62
0.750	0	46
0.500	0	30
0.250	0	14
0.020	0	1

TABLE 6C. AGC LIMIT DATA FORMAT

CONTROL WORD 9 BIT:	27	26	25	24	23	22	21	20	19	18	17	16
FORMAT	e	e	e	e	m	m	m	m	m	m	m	m



† Controlled via microprocessor interface.

FIGURE 23. AGC BLOCK DIAGRAM

Using AGC loop gain, the AGC range, and expected error detector output, the gain adjustments per output sample for the Loop Filter Section of the Digital AGC can be given by

$$\text{AGC Slew Rate} = 1.5\text{dB}(\text{THRESH} - (\text{MAG}*1.64676)) \times (M_{LG})(2^{-4})\left(2^{-(15-E_{LG})}\right) \quad \text{(EQ. 18)}$$

The loop gain determines the growth rate of the sum in the loop accumulator which, in turn, determines how quickly the AGC gain traces the transfer function given in Figures 21 and 22. Since the log of the gain response is roughly linear, the loop response can be approximated by multiplying the maximum AGC gain error by the loop gain. The expected range for the AGC rate is ~ 0.00004 to 1.23dB/symbol time for a threshold of 1/2 scale. See the notes at the bottom of Table 9 for calculation of the AGC response times. The maximum AGC Response is given by:

$$\text{AGC Response}_{Max} = \text{Input(Cart/Polar Gain)(Error Det Gain)(AGC Loop Gain)(AGC Output Weighting)} \quad \text{(EQ. 19)}$$

Since the AGC error is scaled to adjust the gain, the loop settles asymptotically to its final value. The loop settles to the mean of the signal.

TABLE 7. AGC LOOP GAIN BINARY MANTISSA TO GAIN SCALE FACTOR MAPPING

BINARY CODE (MMMM)	SCALE FACTOR	BINARY CODE (MMMM)	SCALE FACTOR
0000	0.0000	1000	0.5000
0001	0.0625	1001	0.5625
0010	0.1250	1010	0.6250
0011	0.1875	1011	0.6875
0100	0.2500	1100	0.7500
0101	0.3125	1101	0.8125
0110	0.3750	1110	0.8750
0111	0.4375	1111	0.9375

TABLE 8. AGC LOOP GAIN BINARY EXPONENT TO GAIN SCALE FACTOR MAPPING

BINARY CODE (EEEE)	SCALE FACTOR	BINARY CODE (EEEE)	SCALE FACTOR
0000	2^{15}	1000	2^{7}
0001	2^{14}	1001	2^{6}
0010	2^{13}	1010	2^{5}
0011	2^{12}	1011	2^{4}
0100	2^{11}	1100	2^{3}
0101	2^{10-}	1101	2^{2}
0110	2^{9}	1110	2^{1}
0111	2^{8}	1111	2^{0}

For example, if M_{LG} = 0101 and E_{LG} = 1100, the AGC Loop Gain = $0.3125*2^{-7}$. The loop gain mantissas and exponents are set in the AGC Loop Parameter Control Register (Control Word 8, Bits 0-15).

Two AGC loop gains are provided in the Programmable Down Converter, for quick adjustment of the AGC loop. The AGC Gain select is a control input to the device, selecting Gain 0 when AGCGNSEL = 0, and selecting Gain 1 when AGCGNSEL = 1.

In the HSP50214, a reset event (caused by SYNCIN2 or CW25) would clear the AGC loop filter accumulator. In the HSP50214A, if Control Word 27, Bit 15 is set to zero, the AGC loop filter accumulator will clear as in the original HSP50214. If Control Word 27, Bit 15 is set to a one, the backend reset (from CW25) will not clear the AGC loop filter accumulator.

In the HSP50214, the settling mode of the AGC forces the mean of the signal magnitude error to zero. The gain error is scaled and used to adjust the gain up or down. This proportional scaling mode causes the AGC to settle to the final gain value asymptotically. This AGC settling mode is preferred in many applications because the loop gain adjustments get smaller and smaller as the loop settles, reducing any AM distortion caused by the AGC.

With this AGC settling mode, the proportional gain error causes the loop to settle more slowly if the threshold is small. This is because the maximum value of the threshold minus the magnitude is smaller. Also, the settling can be asymmetric, where the loop may settle faster for “over range” signals than for “under range” signals (or vice versa).

In some applications, such as burst signals or TDMA signals, a very fast settling time and/or a more predictable settling time is desired. The AGC may be turned off or slowed down after an initial AGC settling period.

To minimize the settling time, a median AGC settling mode has been added to the HSP50214A. This mode uses a fixed gain adjustment with only the direction of the adjustment controlled by the gain error. This makes the settling time independent of the signal level.

For example, if the loop is set to adjust 0.5dB per output sample, the loop gain can slew up or down by 16dB in 16 symbol times, assuming a 2 samples per symbol output sample rate. This is called a median settling mode because the loop settles to where there is an equal number of magnitude samples above and below the threshold. The disadvantage of this mode is that the loop will have a wander (dither) equal to the programmed step size. For this reason, it is advisable to set one loop gain for fast settling at the beginning of the burst and the second loop gain for small adjustments during tracking.

The median settling mode is enabled by setting Control Word 27, Bit 16 to a logic one. If Control Word 27, Bit 16 is zero, the mean loop settling mode is selected and the loop works identically to the HSP50214.

In the median mode, the loop works as follows:

The sign of the true gain error selects a fixed gain error of 0010000000000_b or 1110000000000_b.

These gain error values are scaled by the programmable AGC loop gains to adjust the data path gain.

The maximum slew rate is ~1.5dB per output sample. See Equation 18.

In order to fully evaluate the dynamic range of the PDC, Table 9B is provided, which details the bit weighting from the input to the AGC Multiplier.

Re-Sampler/Halfband Filter

The re-sampler is an NCO controlled polyphase filter that allows the output sample rate to have a non-integer relationship to the input sample rate. The filter engine can be viewed conceptually as a fixed interpolation filter, followed by an NCO controlled decimator.

The prototype polyphase filter has 192 taps designed at 32 times the input sample rate. Each of the 32 phases has 6 filter taps (6)(32) = 192. The stopband attenuation of the prototype filter is greater than 60dB, as shown in Figure 24. The signal to total image power ratio is approximately 55dB, due to the aliasing of the interpolation images. The filter is capable of decimation factors from 1 to 4. If the output is at least 2x the baud rate, the 32 interpolation phases yield an effective sample rate of 64x the baud rate or approximately 1.5%, (1/64), maximum timing error.

Following the Re-sampler are two interpolation halfband filters. The halfband filters allow the user to up-sample by 2 or 4 to recover time resolution lost by decimating. Interpolating by 2 or 4 gives 1/4 or 1/8 baud time resolution (assuming 2x baud at the re-sampler output). The halfband filters use the same coefficients as HB3 and HB5 from the Halfband Filters Section. If one halfband is used, the 23-tap filter is chosen. If two are used, the 23-tap filter runs first followed by the 15-tap filter operating at twice the first halfband's rate. The 23-tap filter requires 7 multiplies, and the 15-tap filter requires 5 multiplies to complete a filter calculation.

Using the interpolation halfband filters allows for reduction in the FIR filter sample rate. This optimizes the use of the programmable FIR filter by allowing the FIR output sample rate to be closer to the Nyquist rate of the desired bandwidth. Optimizing the FIR filter performance provides better use of the programmable FIR taps. Table 10 details the maximum clocking rates for the possible resampling and interpolation halfband filter configurations of this section of the PDC. Control Word 16, Bits 2-0 identify the filter configuration. Control Word 16, Bit 3 is used to bypass the polyphase re-sampler filter.

For proper data output from the interpolation filters, the data ready signal must account for the interpolation process. Figure 25 illustrates the insertion of additional data ready pulses to provide sufficient pulses for the new output sample rate. The Re-sampler Output Pulse Delay parameter is set in Control Word 16, Bits 4-11. These bits set the delay between the output samples when interpolation is utilized. Program this distance between pulses using

$$N = [(f_{PROCCLK}/f_{OUT}) - 1] \quad \text{(EQ. 20)}$$

A value of at least 5 is required to have sufficient time to update the Output Buffer Register. (Writing 5 samples requires 5 clock cycles) A value of at least 16 is required for proper serial output from the part. (Conversion from 16-bit parallel to serial). The value is programmed in numbers of PROCCLK's.

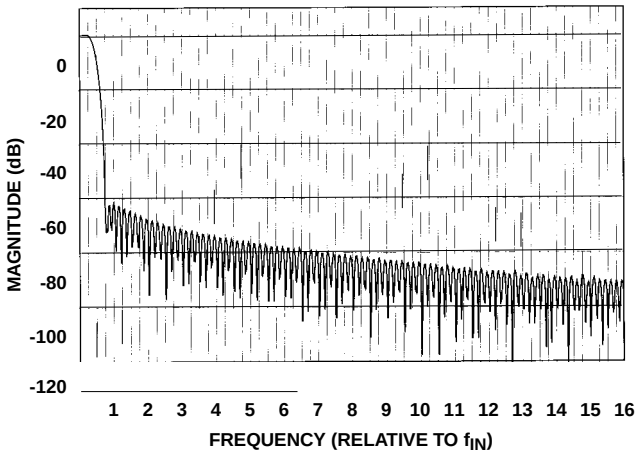


FIGURE 24A. POLYPHASE RESAMPLER FILTER BROADBAND FREQUENCY RESPONSE

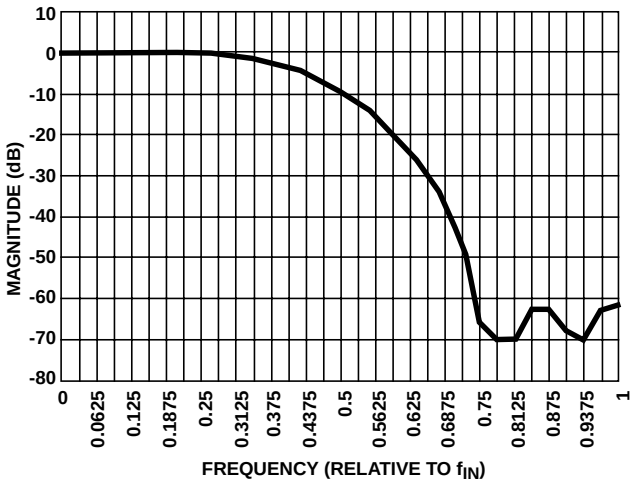


FIGURE 24B. POLYPHASE RESAMPLER FILTER PASS BAND FREQUENCY RESPONSE

TABLE 9A. BIT WEIGHTING FOR AGC LOOP FEEDBACK PATH

AGC ACCUM BIT POSITION	GAIN ERROR INPUT	GAIN ERROR BIT WEIGHT	AGC LOOP FILTER GAIN (MANTISSA)	AGC LOOP FILTER GAIN MULTIPLIER (OUTPUT)	SHIFT = 0	SHIFT = 4	SHIFT = 8	SHIFT = 15	AGC OUTPUT AND AGC LIMITS BIT WEIGHT		AGC GAIN RESOLUTION (dB)
31					2	2	2	2	0		
30					2	2	2	2	E	3	48
29					2	2	2	2	E	2	24
28					2	2	2	2	E	1	12
27	12	= 2		2	2	2	2	2	E	0	6
26	11	= 1		1	2	2	2	1	M	-1	3
25	10	= 0•	0•	0•	2	2	2	0•	M	-2	1.5
24	9	= 1	x	1	2	2	2	1	M	-3	0.75
23	8	= 2	x	2	2	2	2	2	M	-4	0.375
22	7	= 3	x	3	2	2	2	3	M	-5	0.1875
21	6	= 4	x	4	2	2	2	4	M	-6	0.09375
20	5	= 5		5	2	2	2	5	M	-7	0.04688
19	4	= 6		6	2	2	1	6	X	-8	0.02344
18	3	= 7		7	2	2	0•	7		-9	0.01172
17	2	= 8		8	2	2	1	8		-10	0.00586
16	1	= 9		9	2	2	2	9		-11	0.00293
15	0	= 10		10	2	1	3	10		-12	0.00146
14				11	2	0•	4	11		-13	0.000732
13				12	2	1	5	12		-14	0.000366
12				13	2	2	6	13		-15	0.000183
11				14	1	3	7	14		-16	0.0000916
10					0•	4	8	G		-17	0.0000458
9					1	5	9	G		-18	0.0000229
8					2	6	10	G		-19	0.0000114
7					3	7	11	G		-20	0.00000572
6					4	8	12	G		-21	0.00000286
5					5	9	13	G			
4					6	10	14	G			
3					7	11	G	G			
2					8	12	G	G			
1					9	13	G	G			
0					10	14	G	G			

$AGC\ Response_{Max}$ = Input(Cart/PolarGain)(Error Det Gain)(AGC Loop $Gain_{Max}$)(AGC Output Weighting). G = Ground = 0.

$AGC\ Response_{Max} = (1)(1.64676)(2^{-0})(1)(0.75dB) \sim 1.23dB/symbol\ time.$

$AGC\ Response_{Min} = (1)(1.64676)(2^{-15})(1)(0.75dB) \sim 0.00004dB/symbol\ time.$

Thus, the expected range for the AGC rate is ~ 0.00004 to 1.23dB/symbol time.

TABLE 9B. PDC BIT WEIGHTING

BIT WEIGHT	INPUT	SIN/COS	MIX OUT	CIC IN SHIFT = 0	CIC IN SHIFT = 15	CIC BIT WEIGHTS IIIIICCCCC	CIC OUT	HB DATA IN	HB DATA OUT/FIR IN	FIR COEF	FIR MULTI/ ACC	FIR OUT
0	0	0	0	S	S	xxxxxxxxxx	0	0	0	0	1	
1	1	1	1	S	S	xxxxxxxxxx	1	1	1	1	0	0
2	2	2	2	S	S	xxxxxxxxxx	2	2	2	2	1	1
3	3	3	3	S	S	xxxxxxxxxx	3	3	3	3	2	2
4	4	4	4	S	S	xxxxxxxxxx	4	4	4	4	3	3
5	5	5	5	S	S	xxxxxxxxxx	5	5	5	5	4	4
6	6	6	6	S	S	xxxxxxxxxx	6	6	6	6	5	5
7	7	7	7	S	S	xxxxxxxxxx	7	7	7	7	6	6
8	8	8	8	S	S	xxxxxxxxxx	8	8	8	8	7	7
9	9	9	9	S	S	xxxxxxxxxx	9	9	9	9	8	8
10	10	10	10	S	10(S)	xxxxxxxxxx	10	10	10	10	9	9
11	11	11	11	S	11	xxxxxxxxxx	11	11	11	11	10	10
12	12	12	12	S	12	xxxxxxxxxx	12	12	12	12	11	11
13	13	13	13	S	13	xxxxxxxxxx	13	13	13	13	12	12
14		14	14	S	14	xxxxxxxxxx	14	14	14	14	13	13
15		15	SRnd	S	15	xxxxxxxxxx	15	15	15	15	14	14
16		16		S	16	xxxxxxxxxx	16	16	16	16	15	15
17		17		S	17	xxxxxxxxxx	17	17	17	17	16	16
18				S	18	xxxxxxxxxx	18	18	18	18	17	17
19				S	19	xxxxxxxxxx	19	19	19	19	18	18
20				S	20	xxxxxxxxxx	20	20	20	20	19	19
21				S	21	xxxxxxxxxx	21	21	21	21	20	20
22				S	22	xxxxxxxxxx	22	22	22		21	21
23				S	23	xxxxxxxxxx	23	23	23		22	22
24				S	24	xxxxx	Rnd	Rnd	Rnd		23	23
25				25(S)	25	xxxxx	SAT	SAT	SAT		24	24
26				26	26	xxxxx					25	Rnd
27				27	27	xxxxx					26	SAT
28				28	28	xxxxx					27	
29				29	29	xxxxx					28	
30				30	30	xxxxx					29	
31				31	31	xxxxx					30	
32				32	32	xx					31	
33				33	33	xx					32	
34				34	34	xx					(Rnd Out of Mult.)	
35				35	35	xx						
36				36	36	x						
37				37	37	x						
38				38	38	x						
39				39	39	x						

NOTES:

1. SRnd = Symmetric Round; Rnd = Round; SAT = Saturation.
2. The NBW out of the CIC filter is 0.5 x F_{SOUT}. If the $NBW_{IN} = F_S/4$ and $NBWOUT = F_{SOUT}/2$, then the processing gain for a decimation x 16 CIC should be ~ 8 (9dB or 1.5 bits) versus A/D noise, the processing gain should be 10log (BW_{IN}/BW_{OUT}).

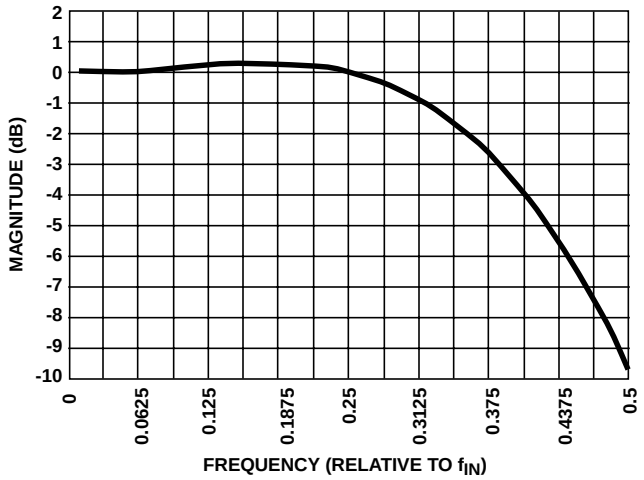


FIGURE 24C. POLYPHASE RESAMPLER FILTER EXPANDED RESOLUTION PASSBAND FREQUENCY RESPONSE

TABLE 10. POLYPHASE AND INTERPOLATING HALFBAND FILTER MAXIMUM CLOCKING RATES

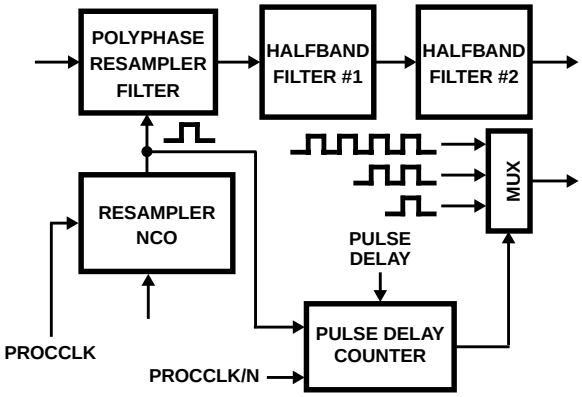
MODE	CLOCK CYCLES	RE-SAMPLER INPUT RATE (MHz)	INTER-POLATION RATE	OUTPUT RATE (MHz)
Bypass	0	55.00	-	55.0
Polyphase Filter	6	55/6 = 9.17	-	9.17 (Note 3)
Polyphase and 1 Halfband Filter	13	55/13 = 4.23	2	8.46 (Note 3)
Polyphase and 2 Halfband Filters	23	55/23 = 2.39	4	9.56 (Note 3)
1 Halfband Filter	7	55/7 = 7.86	2	15.71
2 Halfband Filters	17	55/17 = 3.24	4	12.94

NOTE:

3. This frequency is set by the Resampler NCO.

In burst systems (such as TDMA), time resolution is needed for quickly identifying the optimum sample point. The timing is adjusted by shifting the decimation in the DSP µP to the closest sample. Use of timing error in this way may yield a faster acquisition than a phase-locked loop coherent bit synchronization. Finding the optimum sample point minimizes intersymbol interference.

Fine time resolution is needed in CDMA systems to resolve different multipath rays. In CDMA systems, the demands on the programmable FIR can only be relieved by the re-sampler/interpolation halfband filters. Assume the chip rate for a baseband CDMA system is 1.2288MHz and PROCCLK is limited to 55MHz. Using the symmetric filter pre-sum approach, PROCCLK limits the programmable FIR to 110MIPS (millions of instructions per second) effective due to symmetry. If the CDMA filter (loaded into the programmable FIR Section) requires an impulse response with a span of 12 chips, the filter at 2x the chip-rate would need 24 taps. The 24 taps would translate into 59MIPS = (1.2288MHz)(2)(24). To get the same filtering at 8x the chip rate would require 944MIPS = (1.2288MHz)(8)(96). Direct 8x filtering can not be accomplished with the programmable filter alone because 944MIPS are much greater that the 60MIPs effective limit set by PROCCLK. It is necessary to decimate down to 2x the chip rate to get a realistic number of filter taps. Both interpolation halfband filters are then used to obtain the 8x CDMA output. 944 MIPS is a lot of MIPS. The HSP50214A gets the equivalent processing by decimating down and interpolating back up.



THIS BLOCK GENERATES EXTRA DATA READY PULSES FOR THE NEW OUTPUTS FROM THE INTERPOLATION PROCESS.

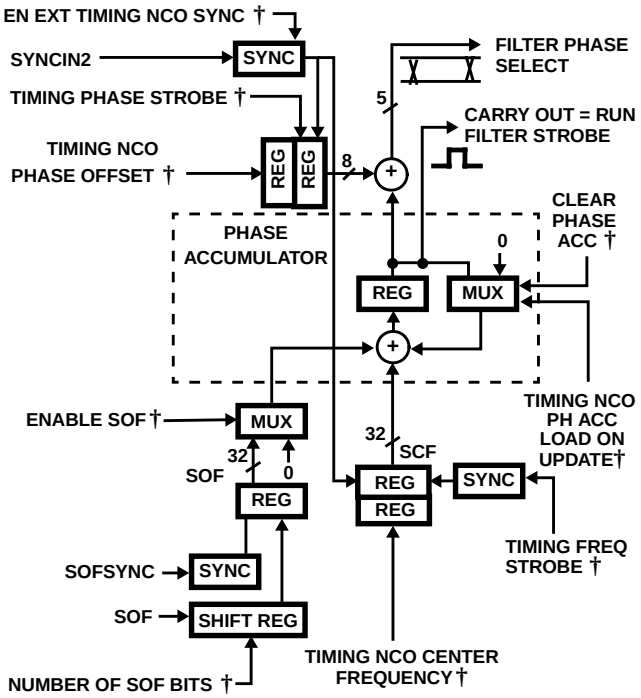
HB2	HB1	RSMPLR	# EXTRA PULSES
0	0	0	0 BYPASS
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	3 (NV)
1	0	1	3 (NV)
1	1	0	3
1	1	1	3

NV = INVALID MODE

FIGURE 25. GENERATING DATA READY PULSES FOR OUTPUT DATA

Timing NCO

The Timing NCO is very similar to the carrier NCO Phase Accumulator Section. It provides the NCO driven sample pulse and associated phase information to the resampling filter process described in the Re-sampler Filter Section. The Timing NCO does not include the SIN/COS Section found in the Carrier NCO. The top level block diagram is shown in Figure 26.

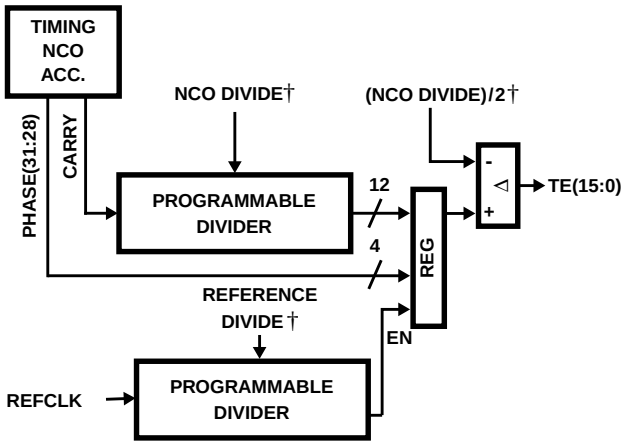


† Controlled via microprocessor interface.

FIGURE 26. TIMING NCO BLOCK DIAGRAM

The programmable parameters for the Timing NCO include an Enable External Timing NCO Sync (Control Word 11, Bit 5), the serial word width, Number of Offset Frequency Bits (Control Word 11, Bits 3-4), an Enable Offset Frequency control (Control Word 11, Bit 2), a Clear NCO Accumulator control (Control Word 11, Bit 1), a Timing NCO Phase Accumulator Load On Update control (Control Word 11, Bit 0), the Timing NCO Center Frequency (Control Word 12), a Timing Phase Offset (Control Word 13, Bits 0-7), a Timing Frequency Strobe (Control Word 14) and a Timing Phase Strobe (Control Word 15). Refer to the Carrier Synthesizer Mixer Section for a detailed discussion of the serial interface for the Timing NCO offset frequency word.

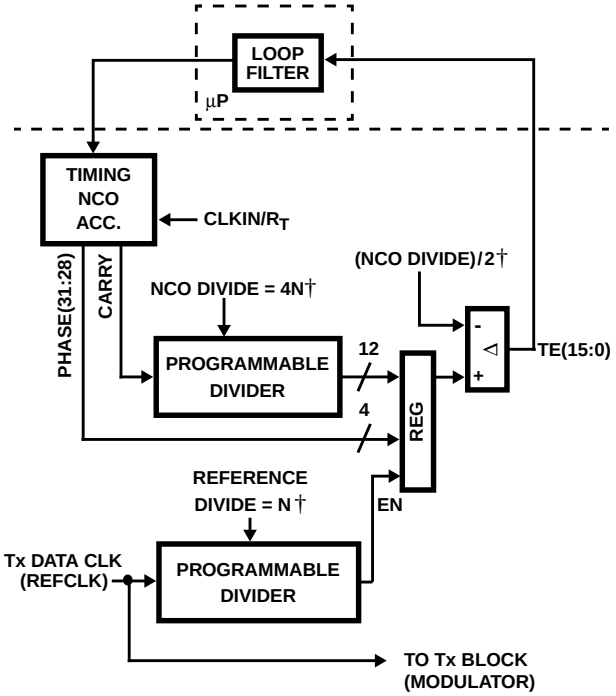
A timing error detector is provided for measuring the phase difference between the timing NCO and a external clock input, REFCLK. Timing Error is generated by comparing the values of two programmable counters. One counter is clocked with the Timing NCO carry out and the other is clocked by the REFCLK. The 12-bit NCO Divide parameter is set in Control Word 18, Bits 16-27. The NCO Divide parameter is the preload to the counter that is clocked by the Timing NCO carry out. The 12-bit Reference Divide parameter is set in Control Word 18, Bits 0-11, and is the preload for the counter that is clocked by the Reference clock. Figure 26 details the block diagram of the timing error generation circuit. The 16 bits of timing error are available both as a PDC serial output and as a processor read parameter. See the Processor Read Section for more details on accessing this value.



† Controlled via microprocessor interface.

FIGURE 27. TIMING ERROR GENERATION

Figure 27A illustrates an application where the Timing Error Generator is used to lock the receiver samples with a transmit data rate. In this example, the receive samples are at four times the transmit data rate. An external loop filter is required, whose frequency error output is fed into the Timing NCO. This allows the loop to track out the long term drift between the receive sample rate and the transmit data clock.



R_T = TOTAL DECIMATION (CIC, HB FILTERS AND FIR)

† Controlled via microprocessor interface.

FIGURE 27A. TIMING ERROR APPLICATION

Cartesian to Polar Converter

The Cartesian to Polar converter computes the magnitude and phase of the I/Q vector. The I and Q inputs are 18 bits. The converter phase output is 16 bits (truncated) with the 16 MSB's routed to the output formatter and all 18 bits routed to the frequency discriminator. The 16-bit output phase can be interpreted either as two's complement (-0.5 to approximately 0.5) or unsigned (0.0 to approximately 1.0), as shown in Figure 28. The phase conversion gain is $1/2\pi$. The phase resolution is 16 bits. The 16-bit magnitude is unsigned binary format with a range from 0 to 2.32. The magnitude conversion gain is 1.64676. The magnitude resolution is 16 bits. The MSB is always zero.

Table 11 details the phase and magnitude weighting for the 16 bits output from the PDC.

TABLE 11. MAG/PHASE BIT WEIGHTING

BIT	MAGNITUDE	PHASE (^{O})
15 (MSB)	2^2 (Always 0)	180
14	2^1	90
13	2^0	45
12	2^{-1}	22.5
11	2^{-2}	11.25
10	2^{-3}	5.625
9	2^{-4}	2.8125
8	2^{-5}	1.40625
7	2^{-6}	0.703125
6	2^{-7}	0.3515625
5	2^{-8}	0.17578125
4	2^{-9}	0.087890625
3	2^{-10}	0.043945312
2	2^{-11}	0.021972656
1	2^{-12}	0.010986328
0 (LSB)	2^{-13}	0.005483164

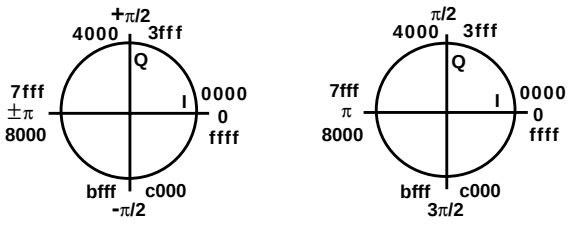


FIGURE 28. PHASE BIT MAPPING OF COORDINATE CONVERTER OUTPUT

The magnitude and phase computation requires 17 clocks for full precision. At the end of the 17 clocks, the magnitude and phase are latched into a register to be held for the next stage, either the output formatter or frequency discriminator. If a new input sample arrives before the end of the 17 cycles, the results of the computations up until that time, are latched. This latching means that an increase in speed causes only a decrease in resolution. Table 12 details the exact resolution that can be obtained with a fixed number of clock cycles up to the required 17. The input magnitude and phase errors induced by normal SNR values will almost always be worse than the Cartesian to Polar conversion.

TABLE 12. MAG/PHASE ACCURACY vs CLOCK CYCLES

CLOCKS	MAGNITUDE ERROR (% F_S)	PHASE ERROR (DEG.)†	PHASE ERROR (% FS)
6	0.065	3.5	2
7	0.016	1.8	1
8	0.004	0.9	0.5
9	<0.004	0.45	0.25
10	<0.004	0.22	0.12
11	<0.004	0.11	0.062
12	<0.004	0.056	0.03
13	<0.004	0.028	0.016
14	<0.004	0.014	0.008
15	<0.004	0.007	0.004
16	<0.004	0.0035	0.002
17	<0.004	0.00175	0.001

† Assumes $\pm 180^O$ = FS.

In the HSP50214, the input to the coordinate converter I/Q to |r|/θ) block is 18 bits. If the signal range is large and the AGC is not used, the quantization noise can become a contributing factor in the phase and frequency computations. For example, if the signal range is 84dB and the maximum signal is set at full scale, the minimum signal would have only 4 bits each for I and Q.

In the HSP50214A, an additional data path option was added that allows the output of the 255 tap programmable FIR filter to be routed directly to the coordinate converter. Rather than having to select only 18 bits out of the available 26 bit output, all 26 bits of the FIR output are routed to the coordinate converter. This change eliminates quantization effects to give more accuracy in the phase and frequency discriminator outputs. The AGC settling time is not a factor because the AGC is effectively bypassed for the magnitude, phase, and frequency computations.

NOTE: The most significant 18 bits of the computed phase are still routed to the discriminator.

One caveat to selecting the FIR outputs to be routed directly to the coordinate converter is that because the I/Q samples for the coordinate conversion are chosen from before the resampler, the magnitude and phase samples will not align with the I/Q samples, if the resampler or interpolation halfband filters are used.

This optional signal routing mode was intended for FM or for burst PSK where a fixed decimation can be used. It is also applicable when resampling or timing adjustments on the demodulated samples are done in a processor following PDC.

The magnitude resolution may suffer because there is no gain adjustment before computing the magnitude. If the signal is < - 90dBFS, it will be below the LSB of the magnitude output.

The enable signal for gating data into the coordinate converter is either the AGC data ready signal or the resampler data ready signal. If the resampler is bypassed, the AGC data ready signal is used and there is a delay of 6 clock cycles between the FIR data being ready and the coordinate converter block sampling it. If the resampler is enabled, its data ready signal will be delayed by 6 clocks (for the AGC) plus the compute delay of the resampler block. This may cause the I/Q to |r|/θ output sample alignment to shift with decimation. For this reason, it is recommended that the resampler/halfband filter block be bypassed when using this new data path.

To select the output of the 255 tap programmable FIR filter to be routed to the coordinate converter, set Control Word 27, Bit 13 to a logic one. For routing as in the HSP50214, set Control Word 27, Bit 13 to a logic zero.

Frequency Discriminator

The discriminator block delays phase from the Cartesian to Polar Section and subtracts it from the latest sample. This delay and subtract can be modeled as a programmable delay comb filter. The output of the filter is dθ/dt, or frequency. The transfer function of the discriminator is set by

$$H(z) = 1 - Z^{-D} \quad \text{(EQ. 21)}$$

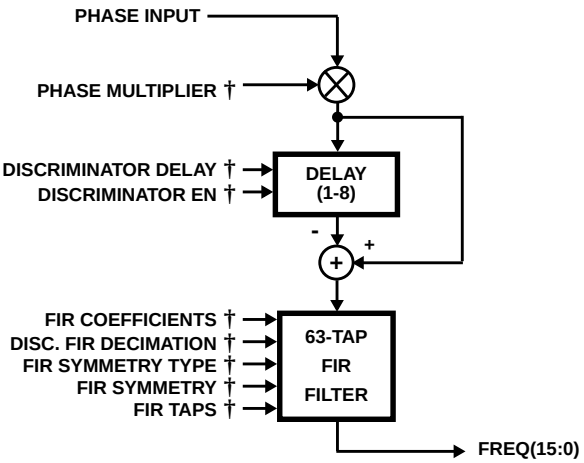
where D is the programmable discriminator delay expressed in number of sample clock delays. The discriminator output frequency is then filtered with a programmable FIR filter. The Block Diagram of the Frequency Discriminator is shown in Figure 29.

The range of delay in the discriminator is from 1 to 8 samples. Modulo 2π subtraction eliminates rollover problems in the subtraction at 2π. The alias free discriminator frequency range is given by:

$$\text{Range}_{FREQDISC} = CW \pm F_{SAMPOUT}/(D+1); \quad \text{(EQ. 22)}$$

where D is the discriminator delay defined in Equation 21 (1 < D < 8), $F_{SAMPOUT}$ is the Discriminator FIR filter output sample rate and CW is the desired center frequency. When the phase multiplier is set to a value other than 2^0, the discriminator range is reduced proportionally. The phase multiplier can be 1, 2, 4 or 8 (2^0 to 2^3). Thus, a multiply of 2^1 reduces the range by 2, a multiply of 2^2 reduces the range by 4, and a multiply of 2^3 reduces the range by 8.

The FIR filter can be configured with up to 63 symmetric taps and up to 32 asymmetric taps. In the symmetric mode, the FIR can be configured for even or odd symmetry, as well as with an even or odd number of filter taps. Decimation is provided to allow more processing time for longer (i.e., more taps) filter structures.



† Controlled via microprocessor interface.

FIGURE 29. FREQUENCY DISCRIMINATOR BLOCK DIAGRAM

The HSP50214A offers an expanded choice of signals to be filtered by the discriminator FIR. The choices are:

1) 18 bits of delayed, and subtracted (and optionally shifted) phase. This is the Discriminator FIR filter input found in the HSP50214.

2) 18 bits of magnitude from the coordinate converter block. This was added to provide for post-detection filtering of AM signals.

3) 18 bits from the I output of the resampler/interpolation halfband filter block. This was added to provide for processing of SSB signals.

The shift, delay, and subtract functions are bypassed for items (2) and (3).

In addition to the FIR input selections, the Q input to the coordinate converter block can be zeroed so that the magnitude output is the magnitude of I only. Again this was added to provide for processing SSB signals.

The Discriminator FIR filter input selections are made in Control Word 27, Bits 18 and 19. The bit definitions are:

- 00 Item (1) described above.
- 01 Item (2) described above.
- 1X Item (3) described above.

Control Word 27, Bit 14 is used to control the Q input to the coordinate converter. The bit definitions is:

- 0 I and Q enabled to the I/Q to R/Theta block.
- 1 The Q input to the I/Q to R/Theta block is zeroed.

The enable signals associated with the various input selections to the Discriminator FIR filter are:

- 1 The data ready strobe from the coordinate converter block.
- 2 The data ready strobe from the coordinate converter block.

The enable signals associated with the various input selections to the coordinate converter are:

3a The data ready signal to the coordinate converter block when the resampler is bypassed. This is the AGC output data ready signal.

3b The data ready to the coordinate converter block when the resampler/halfband filters are enabled. This is the resampler halfband filter block output data ready signal.

The discriminator input is 18 bits, and the output is rounded asymmetrically to 16 bits. The phase into the discriminator can be multiplied by 2^0, 2^1, 2^2, or 2^3 (modulo 2π) to remove PSK data modulation. All programmable parameters for the Frequency Discriminator are set in Control Word 17. Bits 15 and 16 are the phase multiplier which represents the shift applied to the input phase. For CW, the multiply should equal 2^0, (00). For BPSK, QPSK, and 8PSK, the multiply should equal 2^1, (01); 2^2, (10); or 2^3, (11); respectively. Bit 14 is used to enable or disable the discriminator. Bits 11-13 set the decimation in the programmable FIR filter. Bit 10 sets the filter symmetry type as either odd or even, bit 9 sets whether the filter is asymmetric or symmetric, and bits 3-8 set the number of FIR filter taps. Bits 0-2 set the number of delays in the frequency discriminator.

Output Section

The Output Section routes the 7 types of processed signals to output pins in three basic modes. These basic modes are: Parallel Direct Output, Serial Direct Output, and the Buffer RAM Output. The Serial and Parallel Direct Output modes were designed to output data strobes and “real time” continuous streams of data. The Buffer RAM Output mode outputs data upon receipt of an asynchronous request from an external DSP processor or other baseband processing engine. The use of the interrupt signal from the Programmable Down Converter in conjunction with the request strobes from the controller ensures that data is transferred only when both the controller and the Programmable Down Converter are ready. The Buffer RAM output can be operated in a First In First Out (FIFO) or SNAPSHOT mode with the data output either via the 8-bit processor interface or a 16-bit processor interface.

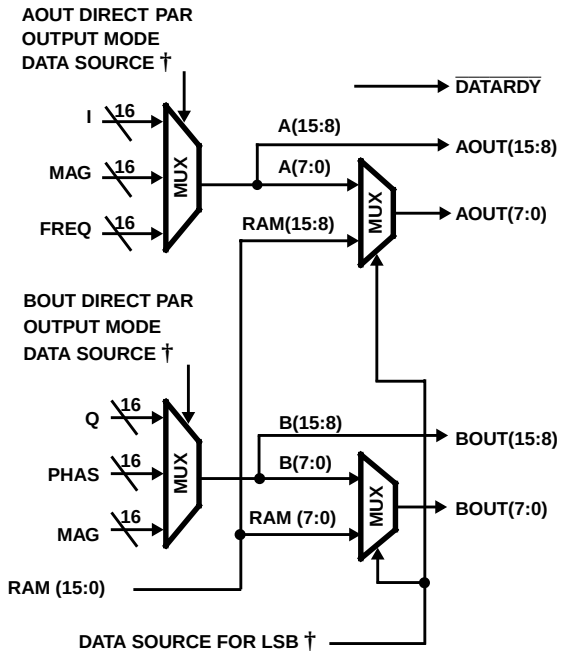
Parallel Direct Output Port Mode

The Parallel Direct Output Port Mode outputs two 16-bit words, AOUT and BOUT, of “real time” data. Figure 30 details the parallel output circuitry. Selection of the data source for the AOUT and BOUT parallel outputs is done via Control Word 20, Bits 22-23, and 20-21, respectively. The AOUT port can output I, Magnitude, or Frequency data. The BOUT port can output Q, Phase or Magnitude data. The upper bytes of AOUT and BOUT are always in the parallel direct mode. The 16-bit parallel direct mode is selected by setting Control Word 20, Bit 25, to zero.

The $\overline{\text{DATARDY}}$ output is asserted during the first clock cycle of the new data on the AOUT bus. The rate at which the data out of the HSP50214 transitions and the rate at which $\overline{\text{DATARDY}}$ is asserted can be different.

Data Transitions:

The transition rate of the parallel output data is dependent on which of the three types of data is selected for the AOUT Output channel: I (real symbols), |r| (magnitude), or f (frequency). Q (quadrature symbols), ø (phase), or |r| (magnitude) are available on the BOUT output. When selected as an output, the I Q, |r|, and ø outputs transition at the symbol rate. The f (frequency) output transitions at the discriminator FIR filter output rate.



† Controlled via microprocessor interface.

FIGURE 30. PARALLEL OUTPUT BLOCK DIAGRAM

Data Ready Signal Assertion Rate:

The assertion rate of the $\overline{\text{DATARDY}}$ signal Is the data transition rate of the A_{OUT} output data either [I, |r| or f]. The time alignment of parallel data words available for output are as follows:

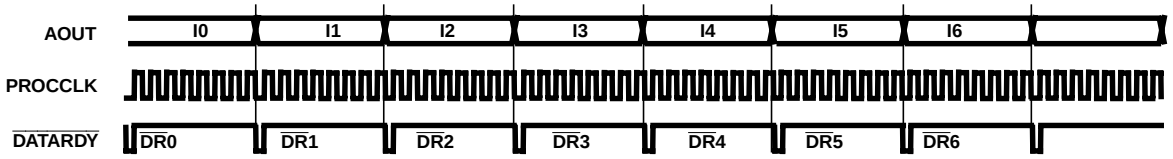
I and Q are aligned in time,

|r| and ø are time aligned, but one sample clock delayed from the associated I and Q samples.

DATARDY Is asserted time aligned with and at the same rate as the data type selected for the AOUT output. Figure 31 details the timing of the AOUT and $\overline{\text{DATARDY}}$ for an AOUT = I data selection.

Note that the BOUT data word may be at a different rate and skewed in time with respect to DATARDY, depending on the type of data selected for output. This is because of the timing relationships defined above, and because the DATARDY is driven by the AOUT signal. Figure 32 details such a configuration.

When the f (frequency) word is selected for output on AOUT, the DATARDY signal is asserted at the discriminator FIR filter output rate, which will be a reduced rate when decimation is engaged in the filter. The f (frequency) output is delayed from the associated I and Q samples one sample time plus, the discriminator FIR filter impulse response time. Figure 33 details the timing of this configuration for a FIR filter that decimates by 4.



NOTE: The number of PROCCLKS per output symbol is not representative, but shown to be small for clarity of establishing timing with respect to the DATARDY signal. For each application, the relationship of the output symbol rate to PROCCLK must be properly illustrated to determine the exact nature of the timing.

FIGURE 31. $\overline{\text{DATARDY}}$ WAVEFORMS WHEN I (READ DATA) IS SELECTED AS AOUT

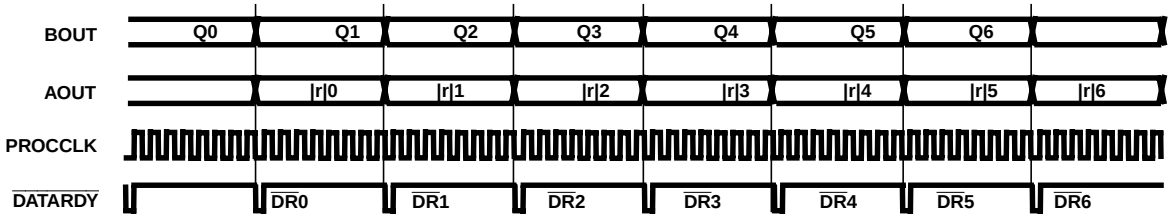
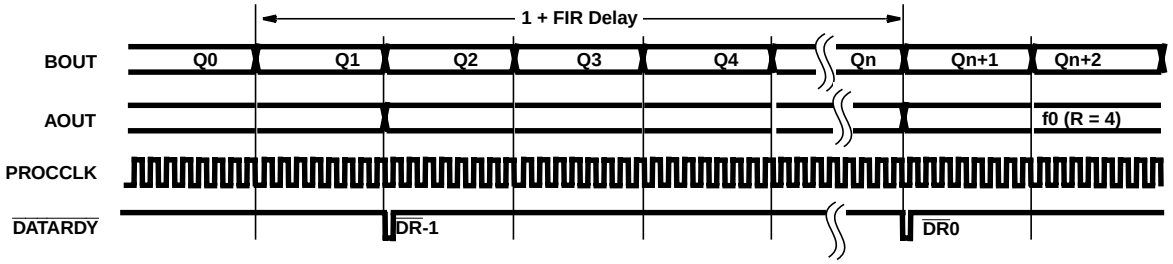


FIGURE 32. DATARDY WAVEFORMS WHEN |r| (MAGNITUDE) IS SELECTED AS AOUT



***NOTE:** I and Q are sample aligned in time. |r| and ϕ are sample aligned in time, but one sample delayed from I or Q. The frequency sample is delayed in time from I or Q by 1 sample time + 63 tap FIR impulse response. If the FIR is set to decimate and frequency is selected for AOUT, the DATARDY signal will be at the discriminator FIR output (decimated) rate.*

FIGURE 33. DATARDY WAVEFORMS WHEN f (FREQUENCY) IS SELECTED AS AOUT

Serial Direct Output Port Mode

The Serial Direct Output Port Mode offers the ability to construct two serial output data streams, SEROUTA AND SEROUTB, from 16-bit I, Q, magnitude, phase, frequency, timing error, and AGC level data words. The total number of data words (1 to 8) for serial output, and the sequential order of these data word components of the serial output are programmable. Each data word may be used once in either the SEROUTA or SEROUTB data streams. Figure 31 illustrates the conceptual implementation of the Serial Direct Output Port Mode.

In the Serial Direct Mode, the output data is loaded into Serial Shift Registers and routed to two serial output pins, SEROUTA and SEROUTB. The serial output shift clock, SERCLK, is PROCCLK divided by 1, 2, 4, 8, or 16. The divide down ratio is programmed using Control Word 20, Bits 14-16. The data is shifted out on the rising edge of the internal SERCLK. The external clock polarity of SERCLK is programmable via Control Word 20, Bit 18. A sync signal is provided for detection of the start or end of each word in the serial sequence. Control Word 20, Bit 17, sets the SERSYNC signal location as either preceding the MSB (typical for interfacing with microprocessors) or following the LSB (typical for interfacing to D/A converters). Control Word 20, Bit 19, sets the SERSYNC polarity as active low or high. The LSB of each data word can be configured as either the true LSB data, or set at a fixed logic “1” or “0” for use as a tag bit. Control Word 20, Bits 0-13 set the LSB of each of the 7 types of data words that can be configured in the serial output stream. Control Word 19, Bits 21-24 set the number of serial data words that will be linked to form the serial outputs. Up to 7 data words can be linked to form the serial output. SEROUTA and SEROUTB will have an identical number of words in the serial output streams.

The 16-bit I, Q, magnitude, phase, frequency, timing error, AGC level, and “zeros” data words are loaded into their respective shift registers. The Magnitude and AGC Level data word are unsigned binary format with a leading zero, while the remaining signals are 2’s complement format.

Any of the eight data sources can be selected as the first serial word for SEROUTA or SEROUTB. Control Word 19, Bits 25-30 set the data type for the first serial word for SEROUTA and SEROUTB. The three bit data type identifier is shown both in Table 13 and in Figure 34, to the right of the controls for the cross matrix switch. Serial output data word sequences are formed by linking data words by programming the data source for each shift requester’s shift input signal. This programming links the Shift Registers together in one or two serial chains. Thus, the Control Word 19 term “Link follows X data”, where X is one of the seven data types. Once the data source data word is selected (by programming a three bit word representing one of the data types into Control Word 19, Bits 25-27 (SEROUTA), and 28-30 (SEROUTB)), the process for identifying the next word is to select a three bit data type identifier which represents the data type to follow the source data type. Program these bits into the Control Word 19 field representing the “Link following X data”, where X = the source data type, defines the second word in the sequence. Likewise, the third data word is linked by selecting the Control Word 19 bits that identify the “Link following X data”, where X = the data type of the second word in the serial chain. The process continues until all the desired data words have been linked.

NOTE: ***I and Q are sample aligned in time. |r| and ϕ are sample aligned in time, but one sample delayed from I or Q. The frequency sample is delayed in time from I or Q by 1 sample time + 63 tap FIR impulse response. If the FIR is set to decimate, the FIR output will be repeated every sample time until a new value appears at the filter output. (i.e., the frequency samples are clocked out at the I, Q sample rate regardless of decimation.)***

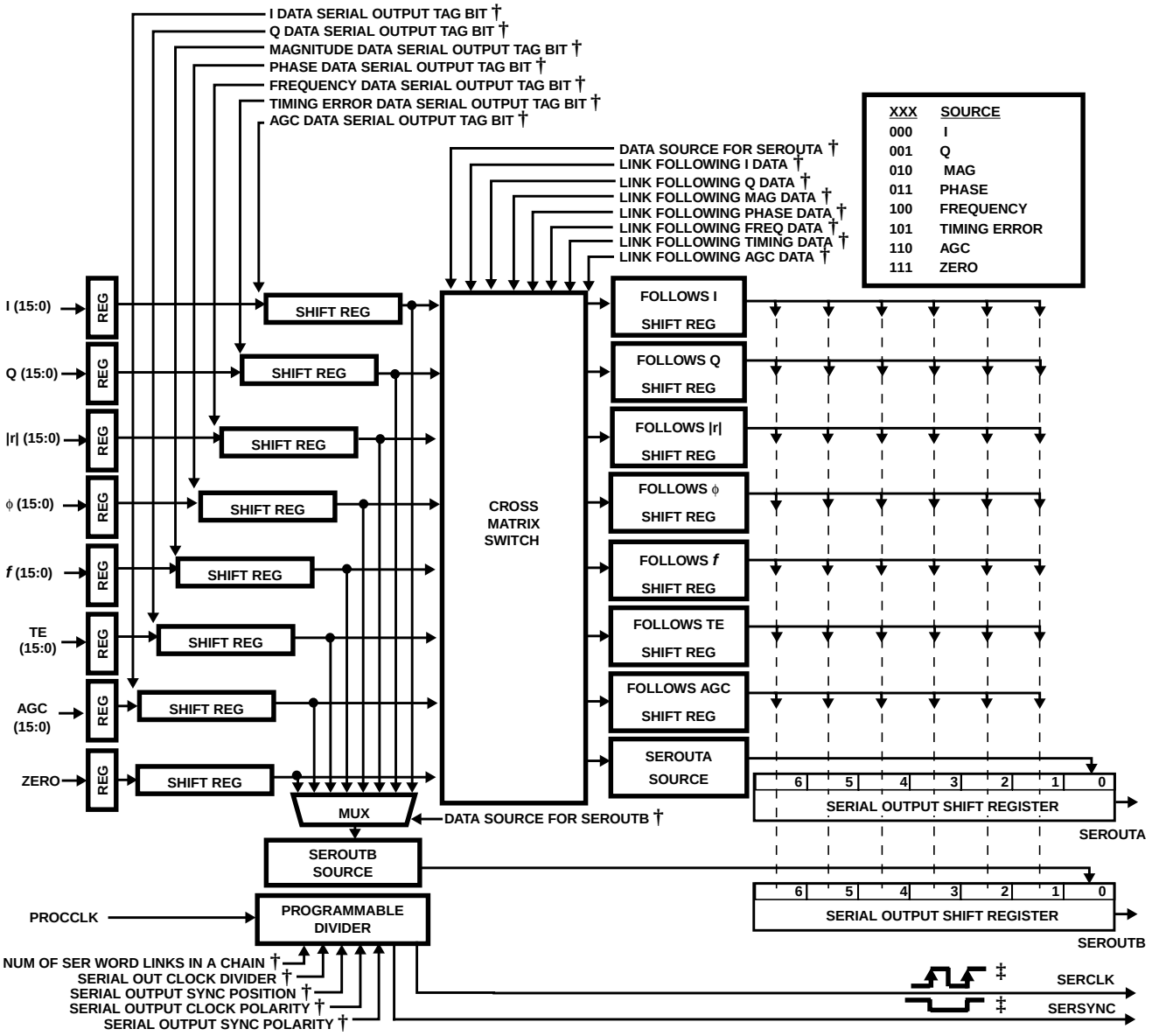
TABLE 13. LINKING CONTROL WORDS FOR SERIAL OUTPUT

DATA TYPE IDENTIFIER	DATA TYPE
000	I Data
001	Q Data
010	Magnitude (MAG) Data
011	Phase (PHAS) Data
100	Frequency (FREQ) Data
101	Timing Error (TIMER) Data
110	AGC Gain
111	Zeros

Two examples will illustrate the process of configuring a serial output using the Serial Output mode.

The serial data stream looks like:

SEROUTA:	CONTROL WORD 19 FIELD	SEROUTB:	CONTROL WORD 19 FIELD
start		start	
I data word >	SEROUTA source data = 000	|r| data word >	SEROUTB source data = 010
Q data word >	Link following I data = 001	*f* data word >	Link following |r| data = 100
ϕ data word >	Link following Q data = 011	TE data word>	Link following *f* data = 101
Zero data word >	Link following ϕ data = 111	AGC data word >	Link following TE data = 110
end >		end >	



† Controlled via microprocessor interface

‡ Polarity is programmable

FIGURE 34. SERIAL OUTPUT FORMATTER BLOCK DIAGRAM

Serial Output Configuration Example 1:

It is desired to output the I data word, followed by the Q data word, followed by the Phase data word on the SEROUTA output. Similarly, it is desired to output the Magnitude data word followed by the Frequency data word, followed by the Timing Error data word, followed by the AGC Level data word on the SEROUTB output. Table 14 illustrates how Control Word 19 should be programmed.

TABLE 14. EXAMPLE 1 SERIAL OUTPUT CONTROL SETTINGS

CONTROL WORD 19 BIT POSITION	FUNCTION	BIT VALUE	RESULT
30-28	SEROUTA Data Source	000	(I)
27-25	SEROUTB Data Source	010	(|r|)
24-21	Number of Serial Word Links in a Chain	100	(4)
20-18	Link following I data	001	(Q)
17-15	Link following Q data	011	(ϕ)
14-12	Link following |r| data	100	(*f*)
11-9	Link following ϕ data	111	(Zeros)
8-6	Link following ***f*** data	101	(Timing)
5-3	Link following AGC data	XXX	(N/A)
2-0	Link following Timing Error data	110	(AGC)

NOTE: Because all but the first data word in the serial output is identified by the data type that it follows, SEROUTB can only be fully independent of the sequence in SEROUTA if it does not use any of the same data word types. This implies a partition as described in Example 1. Once a data word that is used in SEROUTA is called out in SEROUTB, the remaining sequence in SEROUTB will be identical to that portion of SEROUTA sequence that follows the duplicate data type. This follows from using the "Link follows 'data type' data" for word linkage.

NOTE: Each type of data word should be used only once in each data stream. If the "Link following I data" is programmed with the data type identifier for I, then the part will repeat the I data word until all of the data word locations are filled. In Example 1, if bits 20-18 were erroneously programmed to 000 (I data) then the SEROUTA would be four sequential repeats of the I data word.

Serial Output Configuration Example 2:

It is desired to output only three data words on each serial output. The I data word, followed by the Q data word, followed by the Magnitude data word is to be output on SEROUTA. The Q data word followed by the Magnitude data word, followed by the one other data word to be output on SEROUTB. The choices for the remaining data word in the SEROUTB signal are: phase, frequency, AGC level and timing error. Table 15 illustrates how Control Word 19 should be programmed.

TABLE 15. EXAMPLE 2 SERIAL OUTPUT CONTROL SETTINGS

CONTROL WORD 19 BIT POSITION	FUNCTION	BIT VALUE	RESULT
30-28	SEROUTA Data Source	000	(I)
27-25	SEROUTB Data Source	001	(Q)
24-21	Number of Serial Word Links in a Chain	011	(3)
20-18	Link following I data	001	(Q)
17-15	Link following Q data	010	(|r|)
14-12	Link following |r| data	TBD	TBD
11-9	Link following ϕ data	XXX	(N/A)
8-6	Link following ***f*** data	XXX	(N/A)
5-3	Link following AGC data	XXX	(N/A)
2-0	Link following Timing Error data	XXX	(N/A)

The serial data stream looks like:

SEROUTA:	**CONTROL WORD 19 FIELD**
start	
I data word >	SEROUTA source data = 000
Q data word >	Link following I data = 001
|r|data word >	Link following Q data = 010
end >	

SEROUTB:	**CONTROL WORD 19 FIELD**
start	
Q data word >	SEROUTB source data = 001
|r|data word >	Link following Q data = 010
TBD data word>	Link following |r| data = TBD
end >	

As shown by this example, once Q was linked to |r| in the SEROUTA chain, the SEROUTB chain must have |r| following Q, if Q is selected. Figure 35 illustrates the construction of the serial output streams. If the serial data stream was changed to be a length of four data words, then, by default, the SEROUTA would be whatever is selected for SEROUTB data word 3. SEROUTB would need to identify the fourth data word. ***Thus, SEROUTA and SEROUTB are not fully independent because they share the Q data word*** (and by default, the MAGNITUDE follows Q data link and whatever is selected for data word 3 to follow MAGNITUDE data in SEROUTB).

The other signals provided with the SEROUTA and SEROUTB are the SERSYNC and the SERCLK. The SERSYNC signal can be programmed in either early or late sync mode. The sync signal is pulsed active low or active high for each information word link of the chain of data created using Control Word 19. Figure 36 shows the four possible configurations of SERSYNC as programmed using Control Word 20.

As previously discussed, Control Word 20, Bits 17 and 19, set the functionality of the LSB of each data word. These bits may be programmed to be either a logic "0", logic "1" or as normal data. The fixed states are designed to allow the microprocessor to synchronize to the serial data stream.

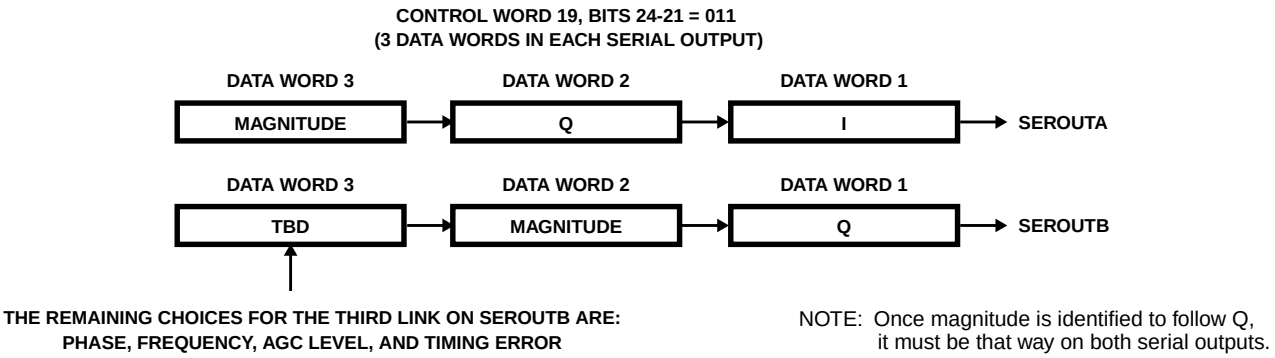


FIGURE 35. EXAMPLE 2 SERIAL OUTPUT DATA STREAM

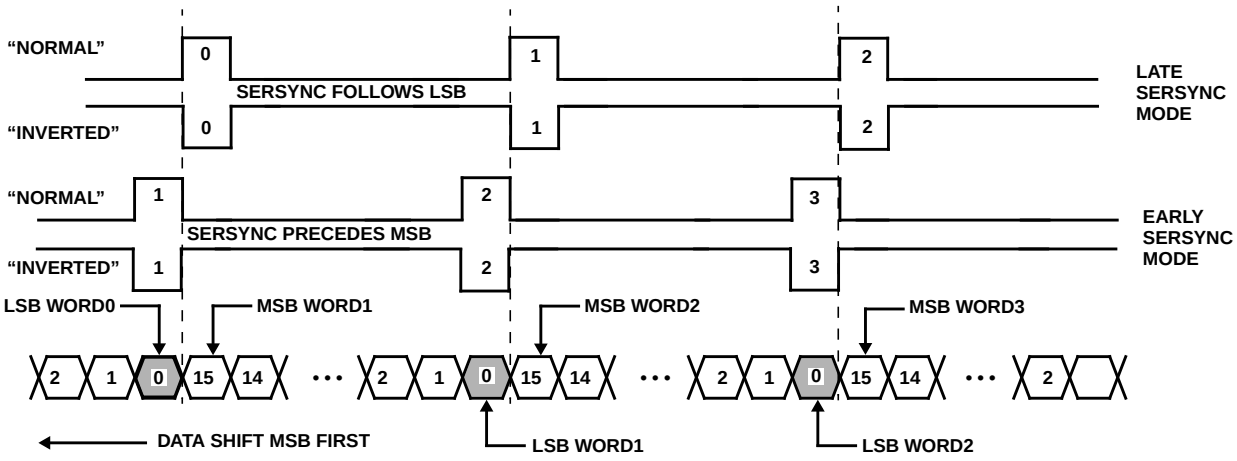


FIGURE 36. VALID SERSYNC CONFIGURATION OPTIONS

Buffer RAM Output Port

The Buffer RAM parallel output mode utilizes a RAM to store output data for future retrieval by either the 8-bit microprocessor that is configuring the PDC or by a 16-bit baseband processing engine (which could also be a microprocessor). Data is output from the RAM only on request and can be obtained from either the 8-bit µP interface or from a 16-bit interface that uses the two LSBytes of AOUT and BOUT. The RAM holds up to eight 80-bit sample sets. Each sample set includes 16 bits of each I, Q, magnitude, phase, and frequency data. The RAM samples are mapped as shown in Table 16. The Buffer RAM controller supports both FIFO and Snapshot modes.

TABLE 16. RAM DATA STORAGE MAP

RAM SAMPLE SET	I DATA (000)	Q DATA (001)	|r| DATA (010)	Φ DATA (011)	*F* DATA (100)
0	$I_0(15:0)$	$Q_0(15:0)$	$\|r\|_0(15:0)$	$\phi_0(15:0)$	$f_0(15:0)$
1	$I_1(15:0)$	$Q_1(15:0)$	$\|r\|_1(15:0)$	$\phi_1(15:0)$	$f_1(15:0)$
2	$I_2(15:0)$	$Q_2(15:0)$	$\|r\|_2(15:0)$	$\phi_2(15:0)$	$f_2(15:0)$
3	$I_3(15:0)$	$Q_3(15:0)$	$\|r\|_3(15:0)$	$\phi_3(15:0)$	$f_3(15:0)$
4	$I_4(15:0)$	$Q_4(15:0)$	$\|r\|_4(15:0)$	$\phi_4(15:0)$	$f_4(15:0)$
5	$I_5(15:0)$	$Q_5(15:0)$	$\|r\|_5(15:0)$	$\phi_5(15:0)$	$f_5(15:0)$
6	$I_6(15:0)$	$Q_6(15:0)$	$\|r\|_6(15:0)$	$\phi_6(15:0)$	$f_6(15:0)$
7	$I_7(15:0)$	$Q_7(15:0)$	$\|r\|_7(15:0)$	$\phi_7(15:0)$	$f_7(15:0)$

NOTE: I and Q are sample aligned in time. |r| and φ are sample aligned in time, but one sample delayed from I or Q. The frequency sample is delayed in time from I or Q by 1 sample time + 63 tap FIR impulse response. If the FIR is set to decimate, the FIR output will be repeated every sample time until a new value appears at the filter output. (i.e., the frequency samples are clocked out at the I, Q sample rate regardless of decimation.)

The FIFO mode allows the processor to service the interface only when enough samples are present in the RAM. This mode is provided so that the µProcessor does not have to service the PDC every output sample. An interrupt, $\overline{\text{INTRRPT}}$, is asserted when the desired number of samples are available. The PDC can be programmed to assert the interrupt when up to 7 samples are available. Control Word 21, Bit 15 is used to set the Buffer RAM controller to the FIFO mode, while Control Word 21, Bits 12-14 set the number of RAM samples to be stored (0 to 7) before the interrupt ($\overline{\text{INTRRPT}}$) is asserted. Control Word 20, Bit 24 determines whether the RAM output interface is the 8-bit microprocessor interface or the 16-bit processor interface. In the 16-bit interface the MSByte is sent to AOUT(7:0) while the LSByte is sent to BOUT(7:0).

The $\overline{\text{INTRRP}}$ output signal goes low for 8 PROCCLK cycles when the number of samples in the Buffer RAM (depth) reaches the programmed depth. The depth of the RAM is calculated using Equation 23. A DSP microprocessor or the data processing engine can use the $\overline{\text{INTRRP}}$ signal to know that the RAM is ready to be read.

$$D_{RAM} = [(ADDR_{WRITE} - ADDR_{READ}) - 1]_{MOD8} \quad \text{(EQ. 23)}$$

FIFO Operation via 16-Bit µProcessor Interface

Figure 37 shows the conceptual configuration of the 16-bit µProcessor interface. This interface looks like a 16-bit µProcessor read-only microprocessor interface. The SEL(2:0) lines are the address bus and the $\overline{\text{OEAL}}$ and $\overline{\text{OEBL}}$ lines are the read lines. The address is decoded as shown in Table 17.

Use of the 16-bit interface for Buffer RAM output requires Control Word 20, Bit 25, to be set to a logic “0” and Control Word 20, Bit 24, to be set to a logic “1”. Once the Control Word 20 has been set to route data to AOUT(7:0) and BOUT(7:0), then the microprocessor must place a value on the PDC input pins SEL(2:0), to choose which data type will be output on AOUT(7:0) and BOUT(7:0). Table 17 defines the data types in terms of SEL(2:0). With the control lines set, the selected data is read MSByte on AOUT(7:0) and LSByte on BOUT(7:0) when $\overline{\text{OEAL}}$ and $\overline{\text{OEBL}}$ (are low). New data only read when $\overline{\text{OEBL}}$ goes low, so use µP for 8-bit modes. Programming SEL(2:0) = 110 outputs a 16-bit status signal on AOUT and BOUT. The FIFO status includes FULL, EMPTY, FIFO Depth, and READYB. These status signals are defined in Table 18.

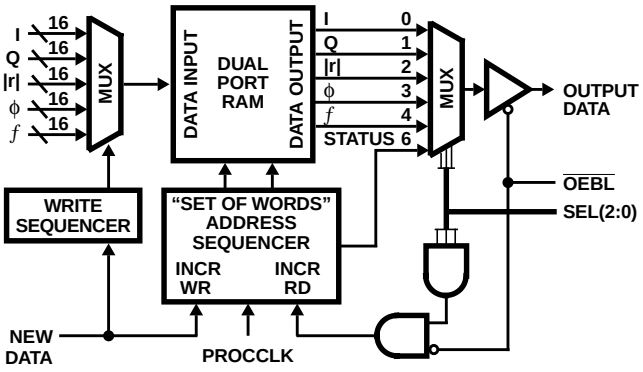


FIGURE 37. 16-BIT MICROPROCESSOR INTERFACE BUFFER RAM MODE BLOCK DIAGRAM

TABLE 17. BUFFER RAM OUTPUT SELECT DEFINITIONS

SEL(2:0)	OUTPUT DATA TYPE
000	I Data
001	Q Data
010	Magnitude
011	Phase
100	Frequency
101	Unused
110	Memory Status
111	Reading this address increments to the next sample set

TABLE 18. STATUS BIT DEFINITIONS

AOUT BIT LOCATION	INFORMATION
(7:5)	FIFO depth - When in FIFO mode, these bits are the current depth of the FIFO.
4	EMPTY - When in FIFO mode, the FIFO is empty, and the read pointer cannot be advanced. Active High.
3	FULL - When in FIFO mode, the FIFO is full, and new samples will not be written. Active High.
2	READYB - When in FIFO mode, the output buffer has reached the programmed threshold. In the snapshot mode, the programmed number of samples have been taken. Active Low.
1-0	GND

NOTE: In the Status output, BOUT(7:0) are all GND.

Figure 38 shows the interface between a 16-bit microprocessor (or other baseband processing engine) and the Buffer RAM Output Section of the Programmable Down Converter, configured for data output via the parallel outputs AOUT and BOUT. In the 16-bit microprocessor interface configuration, the Buffer RAM pointer is incremented when the µProcessor reads address SEL(2:0) = 7 and $\overline{OEBL}$ = 0.

After reset, the FIFO must be incremented to read the first sample set. This is because the RAM read and write pointers cannot point to the same address. Thus, the FIFO pointer must move to the next address before reading the next set of data (I, Q, |r|, ϕ, and *f*) samples. 4 PROCCLK cycles are required after an increment before reading can resume. The FIFO write pointer is reset to zero (the first data sample) when Control Word 22 is written to via the 8-bit microprocessor interface. See the Microprocessor Read Section for more detail on how to obtain the Buffer RAM output with this technique. Figure 36 shows the timing diagram required for parallel output operations. In this diagram, only the I, Q and Frequency data are taken from each sample before incrementing to the next sample. Figure 36 assumes that the pointer has already been incremented into a sample.

NOTE: For the very first sample read, the pointer must be incremented first and 4 PROCCLKs must pass before this sample can be read.

Figure 39 shows $\overline{INTRRP}$ going low before the FIFO is read. The FIFO can be read before the number of samples reaches the INTRRP pointer. The number of samples in the FIFO must be monitored by the user via a status read.

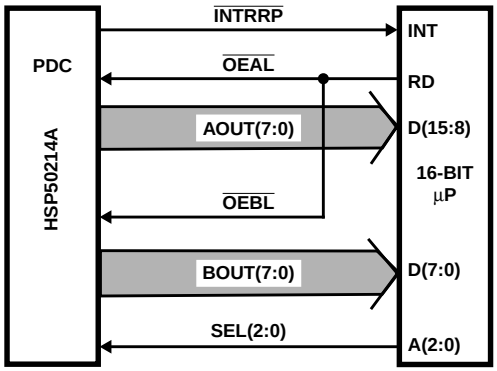


FIGURE 38. INTERFACE BETWEEN A 16-BIT MICROPROCESSOR AND PDC IN FIFO BUFFER RAM MODE

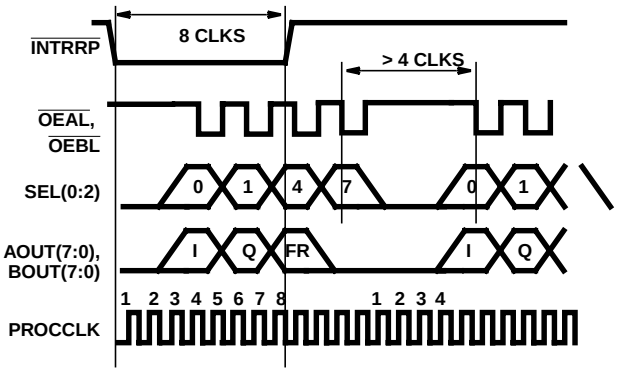


FIGURE 39. TIMING DIAGRAM FOR PDC IN FIFO MODE WITH OUTPUTS I, Q, AND FREQUENCY SENT TO AOUT(7:0) AND BOUT(7:0)

Suppose the depth of the Buffer RAM Output Section is programmed for an $\overline{INTRRP}$ pointer depth of 4. If the output is at 4 times the baud rate, the processing routine for the microprocessor may only need to read the buffer when the Buffer RAM had 4 samples since processing is usually on a baud by baud basis.

Figure 40 illustrates the conceptual view of the FIFO as a circular buffer, with the Write address one step ahead of the Read Address.

Figure 40A deals with clockwise read and write address incrementing. The FIFO depth is the difference between the Write and Read pointers, modulo 8. Figure 40B illustrates a FIFO status of Full, while Figure 40C illustrates a FIFO empty status condition. Figure 40D illustrates a programmed FIFO depth of 3 and the INTRRP signal indicating that the buffer has sufficient data to be read.

Following some simple rules for operating the FIFO will eliminate most operational errors:

Rule #1: The Read and Write Pointers cannot point at the same address (the circuitry will not allow this).

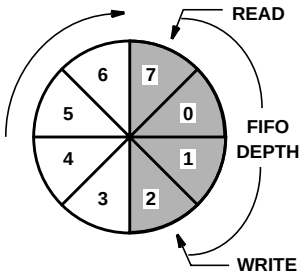
Rule #2: The FIFO is full when the Write Address = Read Address -1 (no more data will be written until some samples are read or the FIFO is reset).

Rule #3: The FIFO is empty when the Read Address = (Write Address -1) (the circuitry will not allow the read pointer to be incremented).

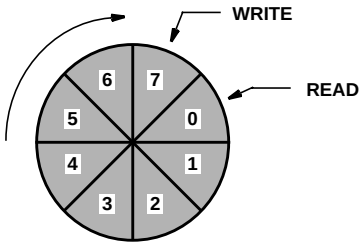
Rule #4: You cannot write over what you have not read.

Rule #5: RESET places the Write address pointer = 000 and Read address pointer = 111.

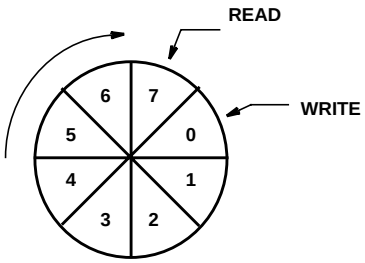
Rule #6: The best addressing scheme is to read the FIFO until it is empty. This avoids erroneous $\overline{\text{INTRRP}}$ assertions and provides for simple FIFO depth monitoring. The interrupt is generated when the depth increments past the threshold.



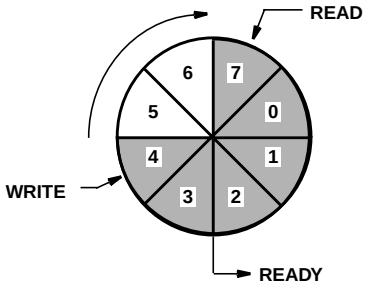
A: FIFO DEPTH IS (WRITE - READ)



B: FIFO FULL IS WHEN (WRITE - READ) = 7



C: FIFO EMPTY IS WHEN (WRITE - READ) = 1



D: FIFO READY IS WHEN (WRITE - READ) > DEPTH

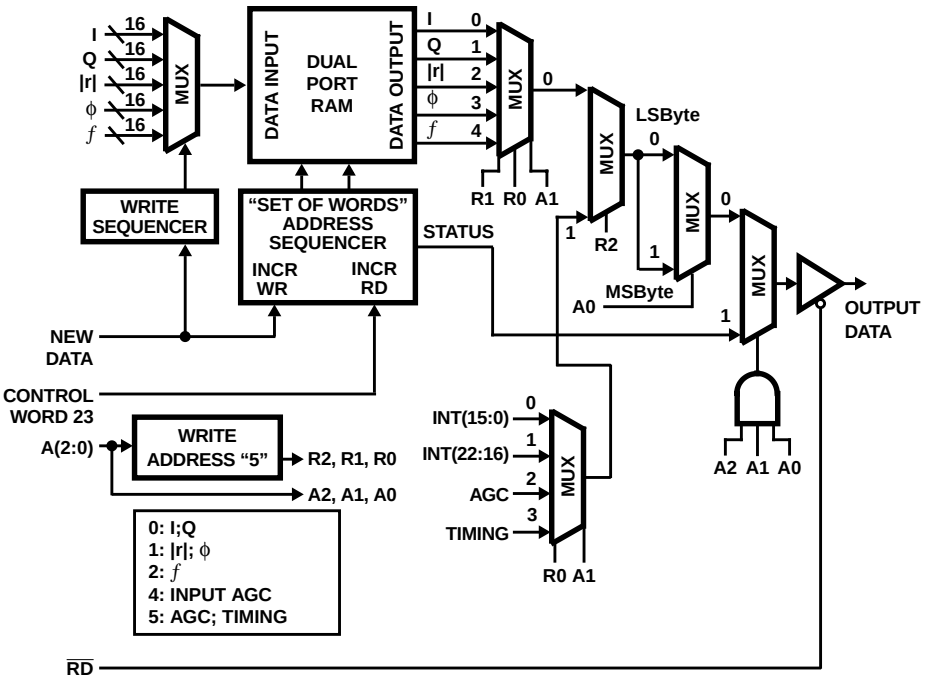
FIGURE 40. FIFO REGISTER OPERATION

FIFO Operation via 8-Bit µProcessor Interface

The Buffer RAM Output may also be accessed via the 8-bit microprocessor interface C(7:0). Figure 41 shows the conceptual configuration of the 8-bit µprocessor interface. Control Word 20, Bit 24 must be set to 0 in order to obtain Buffer RAM data to this output. The Microprocessor Read Section describes how to read the data from each sample out of the C(7:0) interface.

Recall that $\overline{\text{INTRRP}}$ stays low for 8 PROCCLK cycles. The FIFO can be read before the INTRRP signal goes low; the number of samples in the FIFO must be monitored by the user. The timing relationship of the $\overline{\text{INTRRP}}$ to the snapshot data is shown in Figure 42.

The read pointer of the FIFO is incremented when Control Word 23 is written to. The data cannot be read from the next sample until 4 PROCCLKs after the Buffer RAM pointer has been incremented. Control Word 22 is used to reset the Read and Write pointers of the Buffer RAM output to the first sample to 000 and 007 for write and read respectively.



R2	R1	R0	A2	A1	A0	SELECTION
0	0	0	0	0	0	RAM I LSB
0	0	0	0	0	1	RAM I MSB
0	0	0	0	1	0	RAM Q LSB
0	0	0	0	1	1	RAM Q MSB
0	0	1	0	0	0	RAM |r| LSB
0	0	1	0	0	1	RAM |r| MSB
0	0	1	0	1	0	RAM ϕ LSB
0	0	1	0	1	1	RAM ϕ MSB
0	1	0	0	0	0	RAM f LSB
0	1	0	0	0	1	RAM f MSB
0	1	1	X	X	X	NOT USED
1	0	0	0	0	0	INPUT INTEG LSB
1	0	0	0	0	1	INPUT INTEG NMSB
1	0	0	0	1	0	INPUT INTEG MSB
1	0	1	0	0	0	AGC LSB
1	0	1	0	0	1	AGC MSB
1	0	1	0	1	0	TIMING LSB
1	0	1	0	1	1	TIMING MSB
1	1	X	X	X	X	NOT USED
X	X	X	1	1	1	STATUS

FIGURE 41. 8-BIT MICROPROCESSOR INTERFACE BUFFER RAM MODE BLOCK DIAGRAM

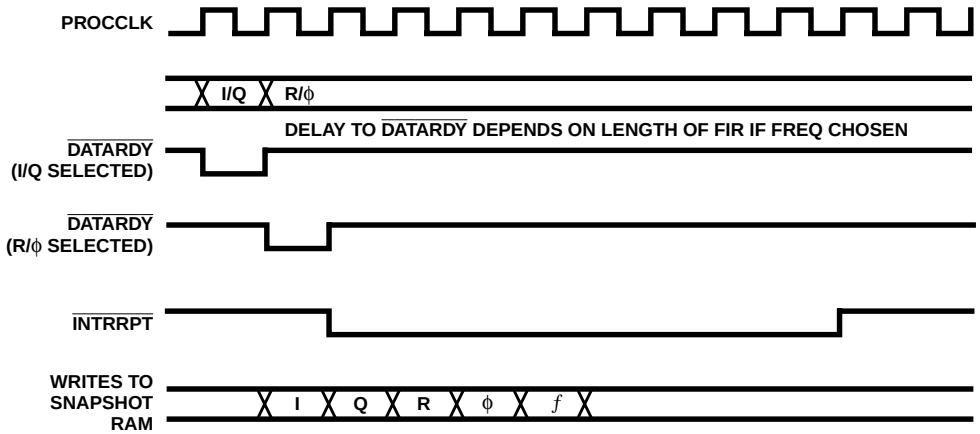


FIGURE 42. RAM LOAD SEQUENCE

Snap Shot Operation

The snapshot mode takes sets of adjacent samples at programmed intervals. It is provided for tracking algorithms that do not require processing of every sample, but do require sets of adjacent samples. For example, bit sync algorithms have narrow loop bandwidths that may not need to be updated every sample. Computing the bit phase may require 4 adjacent samples at 2 times the baud rate. The snapshot mode allows the processor to implement the tracking algorithms for high speed data without having to handle every data sample.

The interval from the start of one snapshot to the start of a second snapshot is programmed into bits 11-4 (where bit 11 is the MSB) of Control Word 21. The actual interval is the value programmed plus 1. If bits 11-4 = 11111111, then the interval is set to 256. If sample sets are to be taken every 4 samples, then bits 11-4 = 00000011.

Figure 43 shows the relationship between the snapshot samples and the snapshot interval.

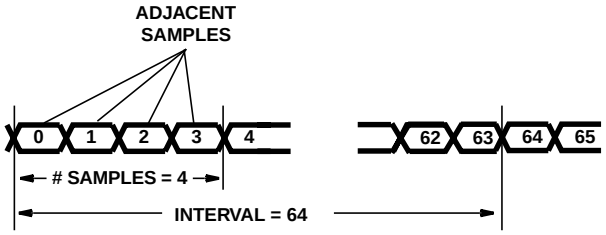


FIGURE 43. SNAP SHOT SAMPLING

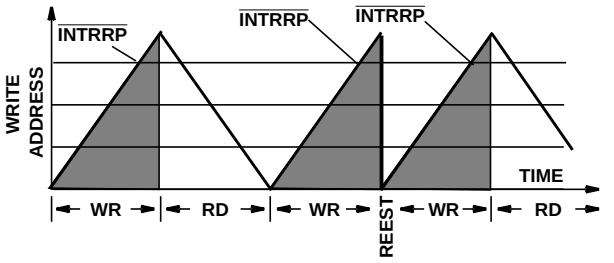
The PDC begins to fill the buffer each time an interval number of samples have passed. The number of sample sets the PDC writes into the buffer and is programmed into bits 3-0 of Control Word 21. The number of samples stored is the programmed value and may be from 1 to 8 sample sets. A sample set consists of I, Q, |r|, ϕ and f.

In snap shot operations, the buffer is read the same as for FIFO operations. Figures 37 and 39 describe the Design Blocks and Timing required to output data on AOUT(7:0) and BOUT(7:0). Table 17 summarizes the selectable output signals. The method for reading data through the Microprocessor Section in snap shot mode is identical to the method described in the FIFO mode subsection and the Microprocessor Read Section.

Avoiding Timing Pitfalls When Using the Buffer RAM Output Port

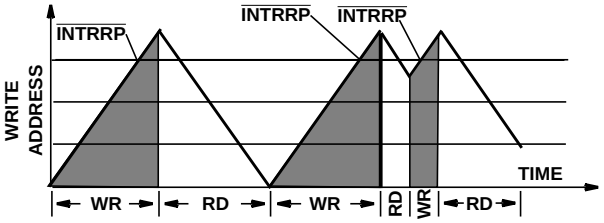
In snapshot mode, the whole buffer is written whenever the interval counter has timed-out. After time-out, old data can be written over. Thus, the data contained within the buffer must be retrieved before time-out to avoid data loss.

It may be desirable to disable the $\overline{\text{INTRRPT}}$ into the controlling microprocessor during read cycles to avoid the generating extra interrupts. Figure 44 details how the WRITE address can trigger extra interrupts. Care must be taken to either read sufficient data out of memory or RESET the addressing to ensure that a complete set of data is the cause of the interrupt.



A COMPLETE SET OF 3 DATA SAMPLES IS IN MEMORY AT $\overline{\text{INTRRP}}$

A: NORMAL READ/WRITE SEQUENCE



THE THIRD INTERRUPT HAS ONLY 1 NEW DATA ENTRY (INSTEAD OF 3) AT $\overline{\text{INTRRP}}$

B: FALSE TRIGGERED INTERRUPT READ/WRITE SEQUENCE

FIGURE 44. AVOIDING FALSE $\overline{\text{INTRRP}}$ ASSERTIONS

Microprocessor Write Section

The Microprocessor Write Section uses an indirect addressing scheme where a 32-bit data word is first loaded into four 8-bit byte master registers using four writes via C(7:0). The desired destination register address is then written to another address using C(7:0). Writing this address triggers a circuit that generates a pulse, synchronous to clock, that loads the Destination Register. The sync circuits and data words are synchronized to different clocks, CLKIN or PROCCLK, depending on the Destination Registers.

A(2:0) determines the destination for the data on bus, C(7:0). Table 19 shows the address map for microprocessor interface. Figure 42 shows the Control Register loading sequence. The data in C(7:0) and address map in A(2:0) is loaded into the PDC on the rising edge of WR and is latched into the Master Register on the rising edge of WR and A(2:0) = 100. Four clocks must pass before loading the next Control Word to guarantee that the data has been transferred.

Some registers can be loaded (i.e., transferred from the Master Register to a Configuration Register or from a Holding Register to an active register) by initiating a sync. For example, to load the AGC Gain, the value of the AGC gain is first loaded into the Holding Registers, then a transfer is initiated by SYNCIN2 if Control Word 8, Bit 29 = 1. This allows the AGC gain to be loaded by detecting a system event, such as a start of a new burst. Bit 20 of Control Word 0 has the same effect on the Carrier NCO center frequency for assertion of SYNCIN1, except it transfers from a dedicated holding register - not the Master Register.

TABLE 19. DEFINITION OF ADDRESS MAP

A2-0	REGISTER DESCRIPTION
0	Holding Register 0. Transfers to bits 7-0 of the 32-bit Destination Register. Bit 0 is the LSB of the 32-bit register.
1	Holding Register 1. Transfers to bits 15-8 of a 32-bit Destination Register.
2	Holding Register 2. Transfers to bits 23-16 of a 32-bit Destination Register.
3	Holding Register 3. Transfers to bits 31-24 of a 32-bit Destination Register. Bit 31 is the MSB of the 32-bit register.
4	This is the Destination Address Register. On the fourth CLK following a write to this register, the contents of the Holding Registers are transferred to the Destination Register. All 8 bits written to this register are decoded into the Destination Register Address. The configuration destination address map is given in the tables in the Control Word Section.
5	Selects data source for reading. See Microprocessor Read Section.

Suppose a (0018D038)H needs to be loaded into Control Word 0, then Table 20 details the steps to be taken.

TABLE 20. EXAMPLE PROCESSOR WRITE SEQUENCE

STEP	A(2:0)	C(7:0)	COMMENT
1	000	0011 1000	Loads 38 into Master Register (7:0) on rising edge of $\overline{WR}$.
2	001	1101 0000	Loads D0 into Master Register (15:8) on rising edge of $\overline{WR}$.
3	010	0001 1000	Loads 18 into Master Register (23:16) on rising edge of $\overline{WR}$.
4	011	0000 0000	Loads 00 into Master Register (31:24) on rising edge of $\overline{WR}$.
5	100	0000 0000	Load “0018D038” into Configuration Control Register 0.
6			Wait 4 CLKS.

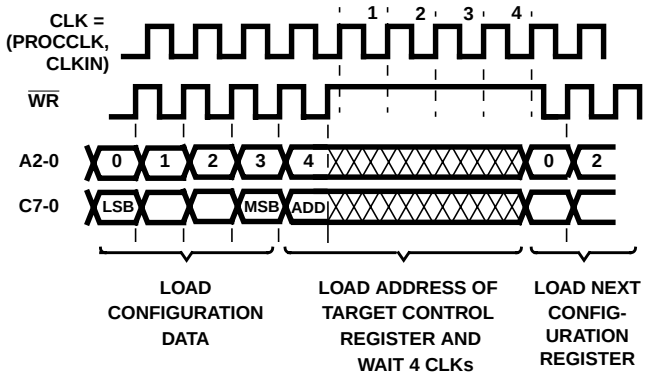


FIGURE 45. LOADING THE CONTROL REGISTERS WITH 32-BIT CONTROL WORDS

Microprocessor Read Section

The microprocessor read uses both read and write procedures to obtain data from the PDC. A write must be done to location 5 to select the source of data to be read. The read source is determined by the value placed on the lower three bits of C(7:0). The output from a particular read code is selected using a read address placed on A(2:0). The output is sent to C(7:0) on the falling edge of $\overline{RD}$.

If the Read Address is equal to 111, the Read Code is ignored, and the status bits shown in Table 22 in the Output Section is sent to C(7:0). This state was provided so that the user could obtain the status bits quickly.

Refer to the Timing Diagram in Figure 43. Suppose the input level detector has a hex value of (321AF5)H, then Table 21 details the steps to be taken.

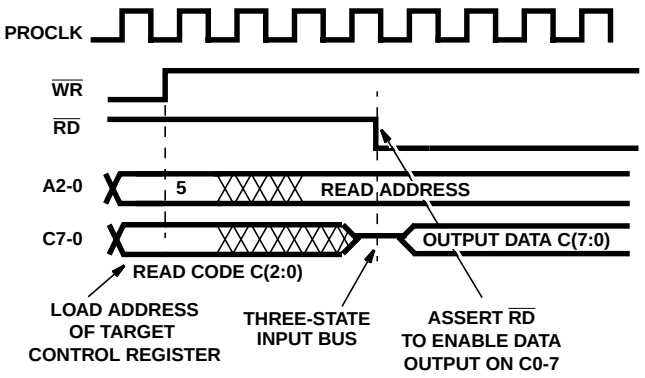


FIGURE 46. READING THE CONTROL REGISTERS USING A LATCH CODE EQUAL TO A 5, A READ ADDRESS AND A READ CODE

TABLE 21. PROCESSOR READ SEQUENCE (INPUT LEVEL SELECTOR)

STEP	A(2:0)	C(7:0)	COMMENT
1	101	100	Write Read Code, 100 to Address 5, $\overline{WR}$ pulled high to generate rising edge.
2	000	1111 1000 (F4)H	Drop $\overline{RD}$ low, Read AGC LSB.
3	001	0001 1010 (1A)H	Pull $\overline{RD}$ high, then drop low, Read AGC NLSB.
4	010	0011 0010 (32)H	Pull $\overline{RD}$ high, then drop low, Read AGC MSB.

TABLE 22. DEFINITION OF ADDRESS MAP

READ CODE C2-0	STATUS TYPE	READ ADDRESS A(2:0)
0	Buffer RAM I and Q	000- I LSB. 001- I MSB. 010- Q LSB. 011- Q MSB. See Output Section.
1	Buffer RAM Output (|r| and ϕ)	000- MAG LSB (7-0). 001- MAG MSB (15-8). 010- PHASE LSB (7-0). 011- PHASE MSB (15-8). See Output Section.
2	Buffered Frequency	000- FREQ LSB. 001- FREQ MSB. See Output Section.
3	Not Used	
4	Input Level Detector	Input AGC 000- input AGC LSB (0-7). 001- input AGC NLSB (8-15). 010- input AGC MSB (16-23).
5	AGC Data and Timing Error	AGC (must write to location 10 to sample) 000- AGC LSB (lower 8 bits of linear Control Word 3 used by multiplier) mmmmmmmm LSB. 001- AGC MSB (4 shift control bits and first three bits of linear) Control Word oeeeemmm MSB. This yields 11 bits of the linear control mantissa. 010- Timing error LSB, not stabilized. 011- Timing error MSB, not stabilized.
6	Not Used	
7	Not Used	
Don't Care	Status	111- Status (6:0) consisting of (6:4)-FIFO depth when output is in FIFO Buffer RAM Output Mode. (3)-EMPTY signalling the FIFO is empty and the read pointer cannot be advanced (Active High). (2)-FULL signalling the FIFO is full and new samples will not be written (Active High). (1)-READYB Output buffer has reached the programmed threshold in FIFO mode or the programmed number of samples have been taken in snapshot mode. (Active Low). (0)-INTEGRATION has been completed in the input level detector and is ready to be read. (Active High).

Applications

Composite Filter Response Example

For this example consider a total receive band roughly 25MHz wide containing 124 200kHz wide FDM channels as shown in Figure 44. The design goal for the PDC is to tune to and filter out a single 200kHz FDM channel from the FDM band, passing only baseband samples onto the baseband processor at a multiple of the 270.8 KBPS bit rate.

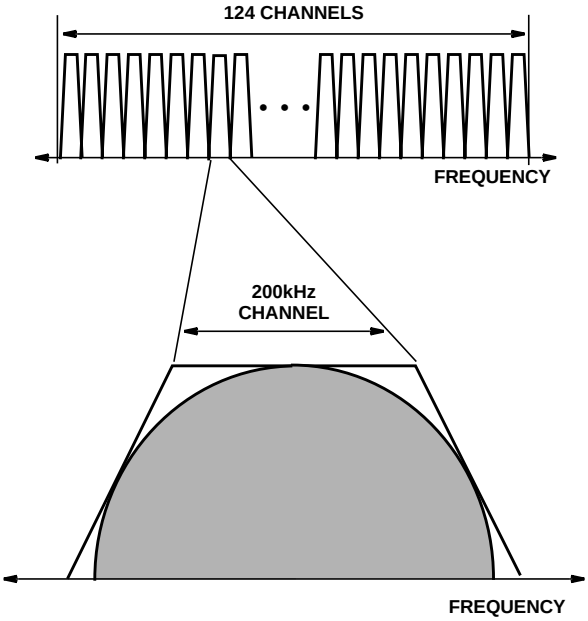


FIGURE 47. RECEIVE SIGNAL FREQUENCY SPECTRUM

RF/IF Considerations

The input frequency to the PDC is dependent on the A/D converter selected, the RF/IF frequency, the bandwidth of interest and the sample rate of the converter. If the A/D converter has sufficient bandwidth, then undersampling techniques can be used to downconvert IF/RF frequencies as part of the digitizing process, using the PDC to process a lower frequency alias of the input signal.

For example, a 70MHz IF can be sampled at 40MHz and the resulting 10MHz signal alias can be processed by the PDC to perform the desired downconversion/tuning and filtering. If the IF signal is less than 1/2 the sample frequency then standard oversampling techniques can be used to process the signal. Of the two techniques, only undersampling allows part of the down conversion function to be brought into the digital domain just through sampling, assuming that a sampling frequency can be found that keeps the alias signals low and that the A/D converter has the bandwidth to accept the unconverted analog signal.

PDC Configuration

For this example, the PDC is configured as follows:

CLKIN: 39MHz
Mode: . . . . . Gated
Input Format: . . . . . As required by Digital Source
Carrier NCO Fc: . . . . . As determined by Channel Freq.
Carrier NCO Phase Offset: 0
Carrier NCO Offset Frequency: . . . . . Disabled
CIC Filter: . . . . . Enabled
Decimation: 18
PROCCLK: 28MHz
Half Band Filters: . . . . . HB3 and 5 Enabled
FIR Filter:. . . . . gsmtemp file
. . . . . f_S = 541.667kHz
. . . . . Decimation = 1
. . . . . Passband: 90kHz
. . . . . Transition Band: 25kHz
. . . . . Passband Atten: 3dB
. . . . . Stop Band Atten: 111.25713
. . . . . FIR Order: 90
. . . . . FIR Symmetry: Even
Resampling Filter: . . . . . HB1 Enabled

The basis for this configuration is:

Sampling Rate: Select a high rate PROCCLK

Output Rate: 1.083MHz (4x Bit Rate; 8x Baud Rate)

CIC Filtering: Primarily Rate Reduction (39/18 = 2.166MHz).

HB Filtering: Flat passband with rate reduction by 4 - low enough (541.66kHz) for sufficient FIR Taps to be used.

FIR Filtering: Primary shaping filter/set final out of band suppression.

Polyphase/HalfBand Filtering: Interpolate by two to output 8x baud rate or 4x bit rate.

The CIC and halfband filter responses are shown in Figures 48A and B.

The composite filter response, constrained primarily by halfband filter 5 and the FIR filter, are shown in Figure 45.

For a more detailed discussion of design approaches and trades when designing with the PDC, refer to AN9720 [3], “Calculating the Maximum Processing Rates of the PDC”.

References

For Intersil documents available on the web, see http://www.intersil.com/
Intersil AnswerFAX (407) 724-7800.

[1] *HSP50210 Data Sheet,* Intersil Corporation, AnswerFAX Doc. No. 3652.

[2] *Cellular Radio and Personal Communications: A Book of Selected Readings*, Theodore S. Rappaport, 1995 by IEEE, Inc.

[3] *AN9720 Application Note,* Intersil Corporation, “Calculating Maximum Processing Rates of the PDC (HSP50214A)”, AnswerFAX Doc. No. 99720.

[4] FO-007 Block Diagram of HSP50214.

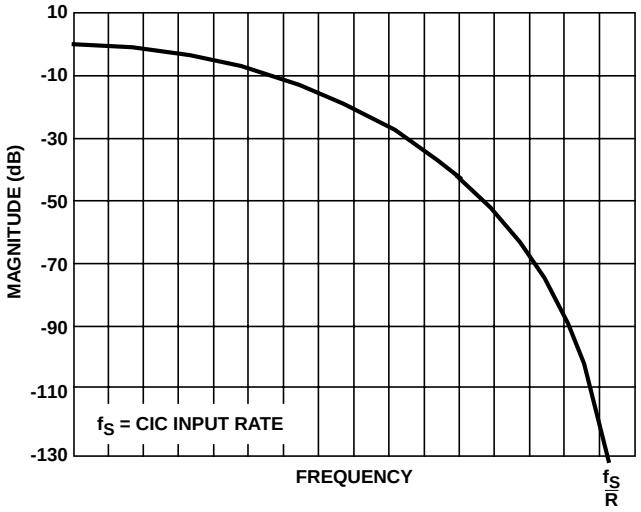


FIGURE 48A. CIC FILTER RESPONSE

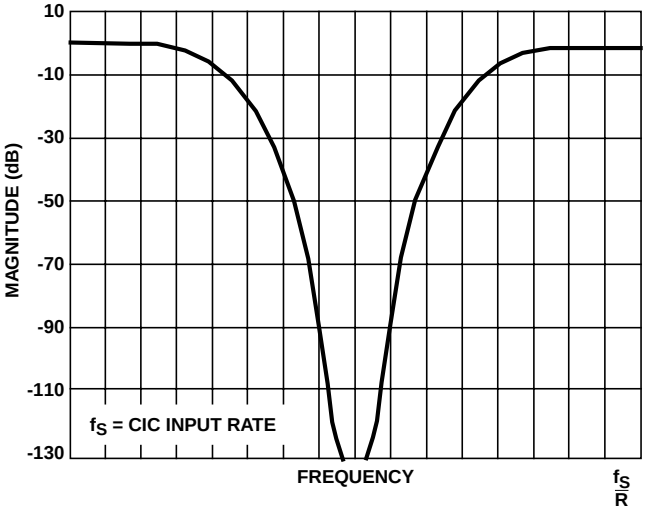


FIGURE 48B. HB3 FILTER RESPONSE

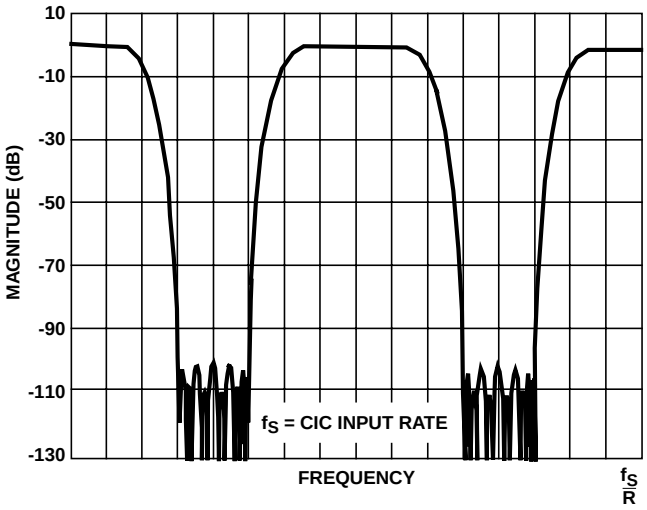


FIGURE 49A. HB5 FILTER RESPONSE

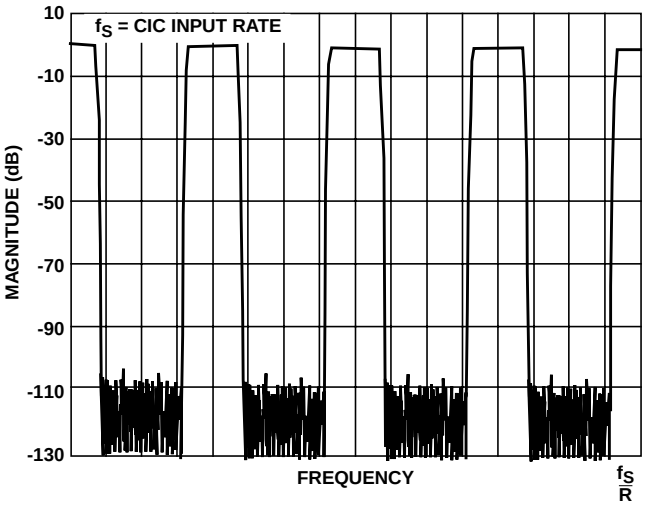


FIGURE 49B. 255 FIR TAP FILTER RESPONSE

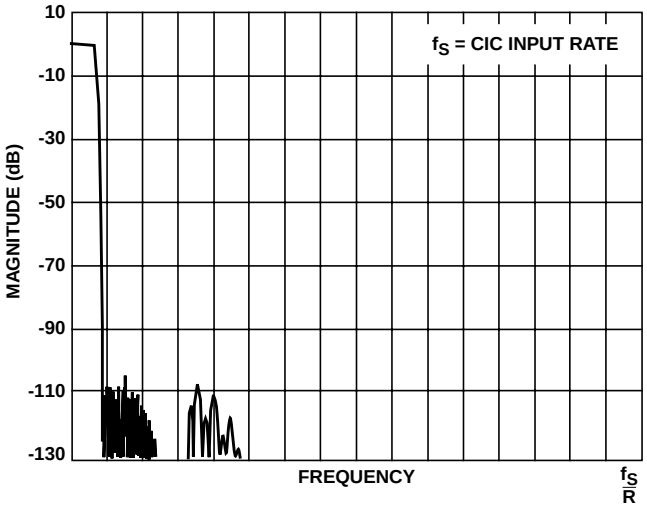


FIGURE 49C. COMPOSITE FILTER RESPONSE

FIGURE 49. PDC FILTER FREQUENCY SPECTRUMS EXAMPLE (NORMALIZED TO SAME SCALE)

Configuration Control Word Definitions

Note that in the Configuration Control Register Tables, some of the available 32 bits in a Control Word are not used. Unused bits do not need to be written to the Master Register. If the destination only has 16 bits, then only 2 bytes need to be written to the Master Register. Figure 45 details the timing for proper operation of the Microprocessor Write Section. Bits identified as “Reserved” should be programmed to a zero.

CONTROL WORD 0: CHIP CONFIGURATION, INPUT SECTION, CIC GAIN (SYNCHRONOUS TO CLKIN)

BIT POSITION	FUNCTION	DESCRIPTION
31-21	Reserved	Reserved.
20	Carrier NCO External Sync Enable	0- The SYNCIN1 pin has no effect on the Carrier NCO. 1- When the SYNCIN1 pin is asserted, the carrier center frequency and phase are updated from the holding registers to the active register. Also, if bit 0 of this word is active, the carrier phase accumulator feedback will be zeroed to set the Carrier NCO to a known phase, allowing the NCOs of multiple parts to be initialized and updated synchronously.
19	CIC External Sync Enable	0- The SYNCIN1 pin has no effect on the CIC filter. 1- When the SYNCIN1 pin is asserted, the decimation counter is loaded, allowing the decimation counters in multiple chips to be synchronized. When CW27 bit-22 is set to a 1, SYNCIN1 will reset both front end and back end circuitry.
18	Input Format	0- Two’s Complement Input Format. 1- Offset Binary Input Format.
17	Input Mode	0- Input operates in Gated Mode. 1- Input operates in Interpolated Mode.
16-13	CIC Shift Gain	These bits control the barrel shifter at the input to the CIC filter. These bits are added to the GAINADJ(2:0) pins to determine the total shift. The sum is saturated at 15. See the CIC Decimation Filter Section for values to be programmed in this field based on CIC filter decimation. Bit 16 is the MSB. SG = Floor [39 - (number of input bits) - $5\log_2(R)$] for $4 < R < 31$ SG = 15 for R = 4. SG = 0 for R = 32.
12-7	CIC Decimation Counter Preload	These bits control the decimation in the CIC filter. Program this field to R-1, where R is the desired decimation factor in the filter. The decimation factor range is 4-32. See CIC Filter Section for effective decimation factor range relative to the CIC Shift Gain value. Bit 12 is the MSB. While this field allows values from 0 - 63, the valid values are in the range from 4- 32.
6	CIC Bypassed	Active high, this bit routes the output of the input shifter to the output of the CIC with no filtering. When the CIC filter is bypassed, CLKIN must be at least twice the input sample rate (ENI should be toggled to achieve this). When the CIC filter is bypassed, the bottom 24 bits of the barrel shifter output are routed to the halfband filters.
5-4	Number of Offset Frequency Bits	00 - 8 bits. 01 - 16. 10 - 24. 11 - 32.
3	Syncout CLK Select	This bit selects whether the SYNCOUT signal is generated from CLKIN of from PROCCLK 0- CLKIN. 1- PROCLK.
2	Clear Phase Accum	0- Enable accumulator in Carrier NCO. 1- Zero feedback in accumulator.
1	Carrier NCO Offset Frequency Enable	When set to 1, this bit enables the offset frequency word to be added to the center frequency Control Word. The offset is loaded serially via the COF and COFSYNC pins.
0	Carrier NCO Load Phase Accum On Update	When this bit is set to 1, the µP update to the Carrier NCO frequency or an external carrier NCO load using SYNCIN1 will zero the feedback of the phase accumulator, as well as update the phase or frequency. This function can be used to set the NCO to a known phase synchronized to an external event.

CONTROL WORD 1: INPUT LEVEL DETECTOR (SYNCHRONOUS TO CLKIN)

BIT POSITION	FUNCTION	DESCRIPTION
31	Reserved	Reserved.
30	Integration Mode	0- Integration of magnitude error stops when the interval counter times out. 1- Integration runs continuously. When the interval counter times out, the integrator reloads, and the results of the integration is sent to a register for the processor to read.
29-14	Integration Interval	These are the top 16 bits of the 18-bit integration counter, ICPrel. ICPrel = (N)/4+1; where N is the desired integration period in CLKIN cycles, defined as the number of input samples to be integrated. N must be a multiple of 4: [0, 4, 8, 12, 16 .... , 2^{18}]. Bit 29 is the MSB. If the input is interpolated, then the zeros must be accounted for, as they will be added to the threshold! If the gated input mode is used, the same input sample will be accumulated multiple times.
13-0	Input Threshold	Input Magnitude Threshold. Bits 12-0 correspond to input bits 12-0. The magnitude of the input is added to this threshold, where the threshold is a signed number. Bit 13 is the MSB.

CONTROL WORD 2: INPUT LEVEL DETECTOR START STROBE (SYNCHRONIZED TO CLKIN)

BIT POSITION	FUNCTION	DESCRIPTION
N/A	Start Input Level Detector AGC Integrator	Writing to this location starts/restarts the input AGC error integrator. The integrator will either restart or stop when the integration interval counter times out depending on bit 30 of Control Register 1 (see Microprocessor Write Section).

CONTROL WORD 3: CARRIER NCO CENTER FREQUENCY (SYNCHRONIZED TO CLKIN)

BIT POSITION	FUNCTION	DESCRIPTION
31-0	Carrier Center Frequency	These bits control the frequency of the Carrier NCO. The frequency range of the NCO is $\pm F_S/2$ where f_S is the input sample rate. The bits are computed by the equation $N = (F_{NCO} / F_S)*2^{32}$. Bit 31 is the MSB. This location is a holding register. After loading, a transfer to the active register is done by writing to Control Word 5 or by generating a SYNCIN1 with Control Word 0, Bit 20 set to 1. The Carrier NCO only updates when $\overline{ENI}$ is active.

NOTE: In the HSP50214A, if the SYNCIN1 occurs when the NCO is not updating, the load signal is held internal to the part until the next NCO update.

CONTROL WORD 4: CARRIER PHASE OFFSET (SYNCHRONIZED TO CLKIN)

BIT POSITION	FUNCTION	DESCRIPTION
31-10	Reserved	Reserved.
9-0	Carrier Phase Offset	These bits, PO, are used to offset the phase of the carrier NCO. The bits are computed by the Equation $PO = INT[(2^{10}\phi_{off})/ 2\pi]_{HEX}$; $(-\pi < \phi_{off} < \pi)$ for 10-bit 2's complement representation or from 0 to 2π for 10-bit offset binary representation. Bit 9 is the MSB. This location is a holding register. After loading, a transfer to the active register is done by writing to Control Word 6 or by generating a SYNCIN1 with Control Word 0, Bit 20 set to 1.

CONTROL WORD 5: CARRIER FREQUENCY STROBE (SYNCHRONIZED TO CLKIN)

BIT POSITION	FUNCTION	DESCRIPTION
N/A	Carrier Frequency Strobe	Writing to this address updates the carrier frequency Control Word from the Holding Register.

CONTROL WORD 6: CARRIER PHASE STROBE (SYNCHRONIZED TO CLKIN)

BIT POSITION	FUNCTION	DESCRIPTION
N/A	Carrier Phase Strobe	Writing to this address updates the carrier phase offset Control Word with the value written to the phase offset (PO) register.

CONTROL WORD 7: HB, FIR CONFIGURATION (SYNCHRONIZED TO PROCCLK)

BIT POSITION	FUNCTION	DESCRIPTION
31-22	Reserved	Reserved.
21	Enable External Filter Sync	0- The SYNCIN2 pin has no effect on the halfband and FIR filters. 1- When the SYNCIN2 pin is asserted, the filter control circuitry in the halfband filters, the FIR, the resampler, and the discriminator are reset. SYNCIN2 can be used to synchronize the computations of the filters in multiple parts for the alignment (see Synchronization Section).
20	Halfband (HB) Bypass	1- Bypass Halfband Filters. 0- Enable HB Filters (at least one HB must be enabled).
19	HB5 Enable	0- Disables HB number 5 (the last in the cascade). 1- Enables HB filter number 5.
18	HB4 Enable	Setting this bit enables HB filter number 4.
17	HB3 Enable	Setting this bit enables HB filter number 3.
16	HB2 Enable	Setting this bit enables HB filter number 2.
15	HB1 Enable	Setting this bit enables HB filter number 1.
14-11	FIR Decimation	Load decimation from 1-16, where 0000 = 16. Bit 14 is the MSB.
10	FIR Real/Complex	0- Complex Filter. 1- Dual Real Filters.
9	FIR Sym Type	0- Odd Symmetry. 1- Even Symmetry.
8	FIR Symmetry	0- Symmetric Filters. 1- Asymmetric Filters.
7-0	FIR Taps	Number of taps in the FIR filter. Range is 1 to 255, where 0000000 is invalid.

CONTROL WORD 8: AGC CONFIGURATION 1 (SYNCHRONIZED TO PROCCLK)

BIT POSITION	FUNCTION	DESCRIPTION
31-30	Reserved	Reserved.
29	Sync AGC Updates to SYNCIN2	When this bit is 1, the SYNCIN2 pin loads the contents of the master registers into the AGC accumulator.
28-16	Threshold	The magnitude measurement out of the cartesian to polar converter is subtracted from this value to get the gain error. A gain of 1.647 in the cartesian to polar conversion that must be taken into account when computing this threshold. These bits are weighted -2^{2} down to 2^{-10}. Bit 28 is the MSB.
15-12	Loop Gain 1 Mantissa	Selected when AGCGNSEL = 1. These bits, MMMM, together with the exponent bits, EEEE (11-8), set the loop gain for the AGC loop. The gain adjustment per output sample is: 1.5dB (Threshold -[Magnitude * 1.6]) 0.MMMM * $2^{-(15 - EEEE)}$ where magnitude ranges from 0 to 1.414 and the threshold is programmed in bits 28-16. The decimal value for the mantissa is calculated as DEC(MMMM)/16. Bit 15 is the MSB.
11-8	Loop Gain 1 Exponent	Selected when AGCGNSEL = 1. These bits are EEEE. See description of bits 15-12. Bit 11 is the MSB.
7-4	Loop Gain 0 Mantissa	Selected when AGCGNSEL = 0. These bits are MMMM. See description for bits 15-12. Same equations are used for Loop 0. Bit 7 is the MSB.
3-0	Loop Gain 0 Exponent	Selected when AGCGNSEL = 0. These bits are EEEE. See description for bits 15-12. Same equations are used for Loop 0. Bit 3 is the MSB.

CONTROL WORD 9: AGC CONFIGURATION 2 (SYNCHRONIZED TO PROCCLK)

BIT POSITION	FUNCTION	DESCRIPTION
31-28	Reserved	Reserved.
27-16	Upper Limit	Maximum Gain/Minimum Signal. The upper four bits are used for exponent; the remaining bits form the mantissa in the fractional offset binary: [eeeemmmmmmmm]. See the AGC Section for details. Bit 27 is the MSB. The gain is in dB. G = (6.02)(eeee) + $20\log_{10}(1.0 + 0.mmmmmmmm)$ eeee = Floor $[\log_2(10^{GAIN\ dB/20})]$ mmmmmmmm = Floor $[512(10^{GAIN\ dB/20}/2^{eeee} - 1)]$
15-12	Reserved	Reserved.
11-0	Lower Limit	Minimum Gain/Maximum Signal. The upper four bits are used for exponent; the remaining bits form the mantissa in the fractional offset binary: [eeeemmmmmmmm]. See the AGC Section for details. Bit 11 is the MSB. The gain is in dB. G = (6.02)(eeee) + $20\log_{10}(1.0 + 0.mmmmmmmm)$ eeee = Floor $[\log_2(10^{GAIN\ dB/20})]$ mmmmmmmm = Floor $[512(10^{GAIN\ dB/20}/2^{eeee} - 1)]$

CONTROL WORD 10: AGC SAMPLE GAIN CONTROL STROBE (SYNCHRONIZED TO PROCCLK)

BIT POSITION	FUNCTION	DESCRIPTION
N/A	Sample AGC Gain Level	Writing to this location samples the output of the AGC loop filter to stabilize the value for µP reading.

CONTROL WORD 11: TIMING NCO CONFIGURATION (SYNCHRONIZED TO PROCCLK)

BIT POSITION	FUNCTION	DESCRIPTION
31-6	Reserved	Reserved.
5	Enable External Timing NCO Sync	0- SYNCIN2 has no effect on the timing NCO. 1- When SYNCIN2 is asserted, the timing NCO center frequency and phase are updated with the value loaded in their holding registers. If bit 0 of this word is set to 1, the phase accumulator feedback is also zeroed.
4-3	Number of Offset Frequency Bits	00 - 8 bits. 01 - 16. 10 - 24. 11 - 32.
2	Enable Offset Frequency	0- Zero Offset Frequency to Adder. 1- Enable Offset Frequency.
1	Clear Phase Accumulator	0- Enable Accumulator. 1- Zero Feedback in Accumulator.
0	Timing NCO Phase Accumulator Load On Update	When this bit is set to 1, the µP update to the timing NCO frequency or an external timing NCO load using SYNCIN2 will zero the feedback of the phase accumulator as well as update the phase and frequency. This function can be used to set the NCO to a known phase synchronized to an external event.

CONTROL WORD 12: TIMING NCO CENTER FREQUENCY (SYNCHRONIZED TO PROCCLK)

BIT POSITION	FUNCTION	DESCRIPTION
31-0	Timing NCO Center Frequency	These bits control the frequency of the timing NCO. The frequency range of the NCO is from 0 to F_{RESAMP} where F_{RESAMP} is the input sample rate to the resampling filter. The bits are computed by the equation: $N = (f_{OUT}/F_{RESAMP})*2^{32}$. Bit 31 is the MSB. This location is a holding register. After loading, a transfer to the Active Register is done by writing to Control Word 14 or by generating a SYNCIN2 with Control Word 11, Bit 5 set to 1.

CONTROL WORD 13: TIMING PHASE OFFSET (SYNCHRONIZED TO PROCCLK)

BIT POSITION	FUNCTION	DESCRIPTION
31-8	Reserved	Reserved.
7-0	Timing NCO Phase Offset	These bits are used to offset the phase of the Timing NCO. The range is 0 to 1 times the resampler input period interpreted either as ± T/2 (2's complement) or 0 to T (offset binary). Bit 7 is the MSB. This location is a holding register. After loading, a transfer to the Active Register is done by writing to Control Word 15 or by generating a SYNCIN2 with Control Word 11, Bit 5 set to 1.

CONTROL WORD 14: TIMING FREQUENCY STROBE (SYNCHRONIZED TO PROCCLK)

BIT POSITION	FUNCTION	DESCRIPTION
N/A	Timing Frequency Strobe	Writing to this address updates the active timing NCO Frequency Register in the timing NCO (see Timing NCO Section).

CONTROL WORD 15: TIMING PHASE STROBE (SYNCHRONIZED TO PROCCLK)

BIT POSITION	FUNCTION	DESCRIPTION
N/A	Timing Phase Strobe	Writing to this address updates the active timing NCO Phase Offset Register in the timing NCO (see Timing NCO Section).

CONTROL WORD 16: RESAMPLING FILTER CONTROL (SYNCHRONIZED TO PROCCLK)

BIT POSITION	FUNCTION	DESCRIPTION
31-12	Reserved	Reserved.
11-4	Re-Sampler Output Pulse Delay	NOTE: These bits program the delay between output samples when interpolating. The extra outputs can be delayed from 2 to 255 clocks from the first output. A delay of 2 equals 255 clocks of delay. A delay of 0 or 1 is an invalid mode. When interpolating by 2, one extra output is generated; when interpolating by 4, 3 extra outputs are generated. Program by the equation (PROCCLK/f_{OUT}) - 1. Bit 11 is the MSB. ***NOTE: If less than 5 is programmed, there will not be sufficient time to fully update the output buffer. If less than 16 is programmed, the serial output may be preempted. This means that it won't finish and if the sync is programmed to follow the data, there may never be a sync.***
3	Re-Sampler Bypass	0- Resampling Filter Enabled. A valid combination of bits 2-0 must also be selected. 1- Resampling Filter Section (including Interpolation halfband filters) is bypassed.
2-0	Filter Mode Select; 2- HB2 Enabled 1- HB1 Enabled 0- Re-Sampler Enabled	000- Not Valid. 001- Resampler Enabled. 010- Halfband 1 Enabled. 011- Resampler and Halfband Filter 1 Enabled. 100- Not Valid. 101- Not Valid. 110- Both Halfband Filters Enabled. 111- Resampler and Both Halfband Filters Enabled.

CONTROL WORD 17: DISCRIMINATOR FILTER CONTROL, DISCRIMINATOR DELAY (SYNCHRONIZED TO PROCCLK)

BIT POSITION	FUNCTION	DESCRIPTION
31-17	Reserved	Reserved.
16-15	Phase Multiplier	These bits program allow the phase output of the cartesian to polar converter to be multiplied by 1, 2, 4, or 8 (modulo 2π) to remove phase modulation before the frequency is measured. 00- No Shift on Phase Input to frequency discriminator. 01- Shift Phase Input to frequency discriminator up 1 (one bit), discarding the MSB and zero filling the LSB. 10- Shift Phase Input to frequency discriminator up 2 (two) bits, discarding the MSB and zero filling the LSB. 11- Shift Phase Input to frequency discriminator up 3 (three) bits, discarding the MSB and zero filling the LSB.
14	Discriminator Enable	0- Disable Discriminator. 1- Enable Discriminator.
13-11	Discriminator FIR Decimation	The decimation can be programmed from 1 to 8, where 000 = decimate by 8; 001 = decimate by 1; 010 = decimate by 2; 011 = decimate by 3; 100 = decimate by 4; 101 = decimate by 5; 110 = decimate by 6; and 111 - decimate by 7.
10	FIR Symmetry Type	0- Odd Symmetry. 1- Even Symmetry.
9	FIR Symmetry	0- Symmetric. 1- Asymmetric.
8-3	Number of FIR Taps	Number of FIR taps from 1 to 63, where 00000 is not valid (00001 = 1 tap, 00010 = 2 taps, etc. up to 11111 = 63 taps). Bit 8 is the MSB.
2-0	Discriminator Delay	Sets the number of delays from 1 to 8 in the discriminator. Set delay ddd to delay minus 1, where 000 represents 1 delay; 001 represents 2 delays, 010 represents 3 delays, 011 represents 4 delays, 100 represents 5 delays, 101 represents 6 delays, 110 represents 7 delays, and 111 represents 8 delays. If ddd the decimal representation bits 2-0, then the discriminator a transfer function $H(Z) = 1\text{-}Z^{-(ddd + 1)}$.

CONTROL WORD 18: TIMING ERROR PRELOADS (SYNCHRONIZED TO PROCCLK)

BIT POSITION	FUNCTION	DESCRIPTION
31-28	Reserved	Reserved.
27-16	NCO Divide	The Re-Sampler NCO output is divided down by the value loaded into this register plus 1. Load with a value that is one less than the desired period. Bit 27 is the MSB.
11-0	Reference Divide	The reference clock is divided down by the value loaded into this register plus 1. Load with a value that is one less than the desired period. Bit 27 is the MSB. A minimum preload of “I” is required.

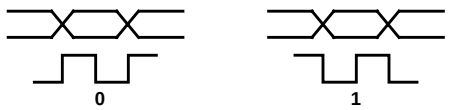
CONTROL WORD 19: SERIAL OUTPUT ORDER (SYNCHRONIZED TO PROCCLK)

BIT POSITION	FUNCTION	DESCRIPTION
31	Reserved	Reserved.
30-28	Data Source for SEROUTA	Serial Output A Source. The serial data source is selected using Table 12 (see Output Section).
27-25	Data Source for SEROUTB	Serial Output B Source. The serial data source is selected using Table 12 (see Output Section).
24-21	Number of Serial Word Links in a Chain	This parameter determines the number of SERSYNC pulses generated. It can be set from 1 to 7. If this parameter matches the number of serial words that are linked together to form a serial output chain, then there will be a sync pulse for every word in the serial output. In applications where a processor is receiving the serial data, it may be desirable to have a single SERSYNC pulse for the whole serial output chain, instead of a SERSYNC for each word in the data chain. The processor then parses out the various data words. As an example, if the I and Q are chained together and a single SERSYNC pulse is generated for this serial output chain, no ambiguity exists in the processor about which two data samples (one from I and one from Q) are related.

CONTROL WORD 19: SERIAL OUTPUT ORDER (SYNCHRONIZED TO PROCCLK) (Continued)

BIT POSITION	FUNCTION	DESCRIPTION
20-18	Link Following I Data	The serial data word, or link, following the I data word is selected using Table 12 (see Output Section).
17-15	Link Following Q Data	The serial data word, or link, following the Q data word is selected using Table 12 (see Output Section).
14-12	Link Following Magnitude Data	The serial data word, or link, following the MAG data word is selected using Table 12 (see Output Section).
11-9	Link Following Phase Data	The serial data word, or link, following the PHAS data word is selected using Table 12 (see Output Section).
8-6	Link Following Frequency Data	The serial data word, or link, following the FREQ data word is selected using Table 12 (see Output Section).
5-3	Link Following AGC Level Data	The serial data word, or link, following the AGC data word is selected using Table 12 (see Output Section).
2-0	Link Following Timing Error Data	The serial data word, or link, following the TIMER data word is selected using Table 12 (see Output Section).

CONTROL WORD 20: BUFFER RAM, DIRECT PARALLEL, AND DIRECT SERIAL OUTPUT CONFIGURATION (SYNCHRONIZED WITH PROCCLK)

BIT POSITION	FUNCTION	DESCRIPTION
31-26	Reserved	Reserved.
25	Data Source for Least Significant Bytes of AOUT and BOUT	Output LSBytes, bits (7:0), of AOUT and BOUT can provide: 0- Buffer RAM Mode Output or, 1- Parallel Direct Mode Output.
24	Buffered Output Mode Interface	Buffered Mode Output interfaces to either: 0- 8-bit µP (address = µP ASEL(5:#); CLK = µP RAM read). 1- 16-bit µP (address = SEL(2:0); CLK = $\overline{\text{OEBL}}$).
23-22	AOUT Direct Parallel Output Mode Data Source	The data word sent by the Direct Parallel Output Mode to AOUT is: 00- I Data. 01- Magnitude. 1X- Frequency.
21-20	BOUT Direct Parallel Output Mode Data Source	The data word sent by the Direct Parallel Output Mode to BOUT is: 00- Q Data. 01- Phase. 1X- Magnitude.
19	Serial Output Sync Polarity	0- Normal Sync Mode (active high). 1- Sync Inverted (active low).
18	Serial Output Clock Polarity	0- Output Clock Inverted rising edge aligns with data transitions. 1- Output Clock Normal falling edge aligns with data transitions.  0 1
17	Serial Output Sync Position	0- Sync is asserted one bit time after the last bit of the serial word (Late Mode). 1- Sync is asserted one bit time prior to the first bit of the serial word (Early Mode).
16-14	Serial Out Clock Divider	000- Serial Output at PROCCLK/16. 001- Serial Output at PROCCLK/8. 010- Serial Output at PROCCLK/4. 011- Serial Output at PROCCLK/2. 1XX- Serial Output at PROCCLK rate.
13-12	I Data Serial Output Tag Bit	00- No Tag Bit. LSB of word is passed. 01- 0 Tag Bit. LSB of word is set to zero. 1X- 1 Tag Bit. LSB of word is set to one.

CONTROL WORD 20: BUFFER RAM, DIRECT PARALLEL, AND DIRECT SERIAL OUTPUT CONFIGURATION (SYNCHRONIZED WITH PROCCLK) (Continued)

BIT POSITION	FUNCTION	DESCRIPTION
11-10	Q Data Serial Output Tag Bit	(See I Data Serial Output Tag selection above).
9-8	Magnitude Data Serial Output Tag Bit	(See I Data Serial Output Tag selection above).
7-6	Phase Data Serial Output Tag Bit	(See I Data Serial Output Tag selection above).
5-4	Frequency Data Serial Output Tag Bit	(See I Data Serial Output Tag selection above).
3-2	AGC Data Serial Output Tag Bit	(See I Data Serial Output Tag selection above).
1-0	Timing Error Data Serial Output Tag Bit	(See I Data Serial Output Tag selection above).

CONTROL WORD 21: BUFFER RAM OUTPUT CONTROL REGISTER (SYNCHRONIZED TO PROCCLK)

BIT POSITION	FUNCTION	DESCRIPTION
31-16	Reserved	Reserved.
15	Output Buffer Mode	0- The output buffer operates in snapshot mode. 1- The output buffer operates in FIFO mode.
14-12	FIFO Mode Depth Threshold	In FIFO mode, when the FIFO depth reaches this threshold, an interrupt is generated and the READY flag is asserted. The threshold may be set from 0 to 7. Bit 14 is the MSB. The interrupt is generated when the FIFO depth reaches the threshold, as the FIFO fills.
11-4	Snapshot Mode Interval	In snapshot mode, the interval between snapshots in the output sample times is determined by this 8-bit binary number, i.e. 256, (2^8), sample time counts between snapshot samples. Program this parameter to 1 less than the desired interval. Bit 11 is the MSB.
3-0	Snapshot Mode Number of Samples	In snapshot mode, the number of samples stored each time the snapshot interval counter times out is equal to the decimal version of this 4-bit number. The range is 1- 8. Bit 3 is the MSB.

CONTROL WORD 22: BUFFER RAM OUTPUT FIFO RESET (SYNCHRONIZED TO PROCCLK)

BIT POSITION	FUNCTION	DESCRIPTION
N/A	FIFO reset	A write to this address increments the output FIFO RAM address pointers to READ = 111 and WRITE = 000.

CONTROL WORD 23: INCREMENT OUTPUT FIFO (SYNCHRONIZED TO PROCCLK)

BIT POSITION	FUNCTION	DESCRIPTION
N/A	FIFO Strobe	A write to this address increments the output FIFO/buffer to the next sample set.

CONTROL WORD 24: SYNCOUT STROBE OUTPUT PIN (SYNCHRONIZED TO CLKIN OR PROCCLK DEPENDING ON PROGRAMMING IN CONTROL WORD 0)

BIT POSITION	FUNCTION	DESCRIPTION
N/A	SYNCOUT Strobe	A write to this address generates a one clock period wide strobe on the SYNCOUT pin that is synchronized to the clock. This strobe may be synchronized to CLKIN or PROCCLK based on the programming of bit 3 of Control Word 0.

CONTROL WORD 25: COUNTER AND ACCUMULATOR RESET (SYNCHRONIZED TO BOTH CLKIN AND PROCCLK)

BIT POSITION	FUNCTION	DESCRIPTION
N/A	Counter and Accumulator Reset	A write to this address initializes the counters and accumulators for testing. Items that are reset are: Carrier NCO. 1. Loads phase offset <9:0> into register to be used for adding to accumulator. 2. Enables feedback on the accumulator. CIC Filter 1. Resets the decimation counter. 2. Clears enables to CIC. 3. Clears accumulators in CIC. 4. Clears enable leaving CIC. Halfband Filters 1. Resets compute counter in Halfband control. 2. Resets read address for all Halfband Filters. 3. Resets write address for all Halfband Filters. 4. Clears input available strobe. 5. Resets Halfband control logic. 255 Tap FIR 1. Resets FIR read and write address pointers. 2. Zero's coefficient read address. AGC Loop 1. Clears accumulator in loop filter. Re-Sampler and Interpolation Halfband Filters. 1. Resets counters for Halfband addresses for writing. 2. Resets output enable. 3. Reset controller for Re-Sampler. Timing NCO 1. Initializes counters for inserting extra pulses when interpolating halfbands are enabled. In the HSP50214A, a configuration control word bit determines if a Timing NCO reset is executed. If Control Word 27, Bit 20 is set to a logic one, a reset will clear the feedback in the timing NCO phase accumulator. If Control Word 27, Bit 20 is zero, a reset will not clear the timing NCO phase accumulator feedback, which is how the HSP50214 operated. Discriminator 1. Resets read and write address pointers. 2. Zero's coefficient read address. Cartesian to Polar Coordinate Counter 1. Resets Cordic counters (stops current computation). FIFO Control 1. Resets decoder for controlling FIFO. 2. Resets write address for FIFO. 3. Clears $\overline{RD}$ and $\overline{INTRRPT}$. 4. Resets "depth" and "full" flags. 5. Sets the empty flag. 6. Sets the read address to "7", write address to "0". Snapshot Control 1. Zeros the group number. 2. Load interval counter. 3. Resets write address and read address for FIFO. Output Serial Control 1. Reloads shift counter. 2. Reloads "Number of Words" counter. 3. Reloads counter for sync (for early or late). 4. Reloads counter for dividing down SERCLK. 5. In the HSP50214A, the Control Word 25 reset signal is designed such that the front end reset is 10 CLKIN periods wide and the back end reset is 10 PROCCLK periods wide. This guarantees that no enables will be caught in the pipelines.

CONTROL WORD 25: COUNTER AND ACCUMULATOR RESET (SYNCHRONIZED TO BOTH CLKIN AND PROCCLK) (Continued)

BIT POSITION	FUNCTION	DESCRIPTION
24	Test Circuit Disable	The A Version includes test circuitry for the ROM and RAM blocks that was not present in the original release part. This circuitry must be disabled before loading the coefficient RAM's. This is done by setting bit 24 to zero. ***NOTE: Because the HSP50214 did not require a "write" to Control Word 25 and the HSP50214A does require that Control Word 25, Bit 24 be set to zero for normal operation, software that was written for the HSP50214 will require modification to work properly with the HSP50214A.***

CONTROL WORD 26: LOAD AGC GAIN (SYNCHRONIZED TO PROCCLK)

BIT POSITION	FUNCTION	DESCRIPTION
N/A	AGC Load	Writing to this location generates a strobe to load the AGC loop accumulator with bits (15:5) to the master registers. These bits are loaded into the MSBs of the AGC loop filter accumulator with bits (15:12) mapping to the shift (exponent) control bits and bits (11:5) mapping to the multiplier (mantissa) bits. Bits (11:5) represent a binary mantissa mapped to the linear gain as: 01.XXXXXXX. See AGC Section.

CONTROL WORD 27: TEST REGISTER (SYNCHRONIZED TO CLKIN)

BIT POSITION	FUNCTION	DESCRIPTION
31-25	Reserved	A fixed value of 0000 000 is loaded here for normal operation.
24	RAM Test Enable	0 = Normal Operation; 1 = RAM Test Enabled.
23	Input Level Detector Counter Preload Select	0 = The two LSB's of the interpolation period preload are set to zero. 1 = The two LSB's of the interpolation period preload are set to one.
22	SYNCIN1 Reset Control	0: SYNCIN1 causes only front end reset. 1: SYNCIN1 causes front end and back end resets.
21	Timing Error Input Select	0 = Operates as HSP50214. 1 = Corrects an error in the 4 LSB's.
20	Timing NCO Reset Control Select	0 = Backend reset will not clear the timing NCO phase accumulator feedback. 1 = Backend reset clears the timing NCO phase accumulator.
19 - 18	Discriminator FIR Input	00 = 18 bits of delayed and subtracted (optionally shifted) phase. 01 = 18 bits of magnitude from coordinate converter. 1X = 18 bits of resampler/halfband filer I output.
17	Input Level Detector Integration Start Select	0 = No external sync control of input end detector start/restart of integration period. 1 = SYNCIN causes the input level detector to start/restart its integration period.
16	AGC Average Control	0: AGC settles to mean. 1: AGC settles to median.
15	AGC Clear Inhibit	When set to zero, this bit will clear the AGC loop filter accumulator on a SYNCIN2 assertion or a WRITE to CW 25. When set to a one, a WRITE to CW25 will not clear the AGC loop filter accumulator.
14	Q Input to Coordinate Converter (see bits 19 - 15)	0 = I and Q enabled to coordinate converter. I = Q input to coordinate converter is zeroed.
13	Coordinate Converter Input	0 = The Resampler HB filter output is routed to coordinate converter. 1 = The output of 255 tap FIR is routed to coordinate converter.
12-0	Reserved	A fixed value 0 0010 0111 1000 [0278]hex is loaded here for normal operation. A fixed value 0 0010 0111 1010 [027A]hex is loaded here for setting the Sin/Cos Generator outputs to 7FFF.

CONTROL WORDS 64-95: DISCRIMINATOR COEFFICIENT REGISTERS (SYNCHRONIZED TO PROCCLK)

BIT POSITION	FUNCTION	DESCRIPTION
31-10	Discriminator FIR Coefficient	The discriminator FIR coefficients are 22-bit-two's complement. If the filter is symmetric, the coefficients are loaded from the center coefficient at address 64 to the last coefficient. If the filter is asymmetric the coefficients C_0 to C_N are loaded with C_0 in address 64 up to 64+N, where N is number of asymmetric coefficients.

CONTROL WORDS 128-255: 255 PROGRAMMABLE COEFFICIENT REGISTERS

BIT POSITION	FUNCTION	DESCRIPTION
31-10	Programmable FIR Coefficient	The programmable FIR coefficients are 22-bit-two's complement. If the filter is symmetric, the coefficients are loaded from the center coefficient at address 128 to the last coefficient. If the filter is asymmetric the coefficients C_0 to C_N are loaded with C_0 in address 128 up to 128+N, where N is number of asymmetric coefficients. Real Filters are computed as: Xn-k+1 Ck1 + Xn-k+2 Ck-2 + ... XnC0), where C0 is the coefficient in address 128 and Xo is the oldest data sample. Complex filters outputs are computed as follows: Xn is the most recent data sample. k is the number of samples = number of (complex) taps. C0_re is the coefficient loaded into CW128. C0_im is the coefficient loaded into CW129. The convolution starts with the oldest data, times the last complex coefficient, and ends with the newest data, times the first complex coefficient loaded. Iout = (-Xn-k+1_q * Ck-1_im + Xn-k+1_i * Ck-1_re). + (-Xn-k+2_q * Ck-2_im + Xn-1+2_i * Ck-2_re). + ... + (-Xn_q * C0_im + Xn_i * C0_re). Qout = (Xn-k+1_i * Ck-1_im + Xn-k+1_q * Ck-1_re). + (Xn-k+2_i * Ck-2_im + Xn-1+2_q * Ck-2_re). + ... + (Xn_i * C0_im + Xn_q * C0_re).

Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input, Output or I/O Voltage . . . . . GND-0.5V to V_{CC} +0.5V
ESD Classification . . . . . Class 2

Operating Conditions

Voltage Range . . . . . +4.75V to +5.25V
Temperature Range
Commercial . . . . . 0^oC to 70^oC
Industrial . . . . . -40^oC to 85^oC
Input Low Voltage . . . . . 0V to +0.8V
Input High Voltage . . . . . 2V to V_{CC}
Input Rise and Fall Time . . . . . 1V/ns Max

Thermal Information

Thermal Resistance (Typical, Note 4)	θ_{JA} ($^oC/W$)
MQFP Package	28

Maximum Junction Temperature . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

4. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

V_{CC} = 5 ±5%, T_A = 0^oC to 70^oC, Commercial; -40^oC to 85^oC, Industrial

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Logical One Input Voltage	V_{IH}	V_{CC} = 5.25V	2.0	-	V
Logical Zero Input Voltage	V_{IL}	V_{CC} = 4.75V	-	0.8	V
Clock Input High	V_{IHC}	V_{CC} = 5.25V	3.0	-	V
Clock Input Low	V_{ILC}	V_{CC} = 4.75V	-	0.8	V
Output High Voltage	V_{OH}	I_{OH} = -400µA, V_{CC} = 4.75V	2.6	-	V
Output Low Voltage	V_{OL}	I_{OL} = +2.0mA, V_{CC} = 4.75V	-	0.4	V
Input Leakage Current	I_I	V_{IN} = V_{CC} or GND, V_{CC} = 5.25V	-10	+10	µA
Standby Power Supply Current	I_{CCSB}	V_{CC} = 5.25V, Outputs Not Loaded	-	500	µA
Output Leakage Current	I_O	V_{IN} = V_{CC} or GND, V_{CC} = 5.25V	-10	+10	µA
Operating Power Supply Current	I_{CCOP}	CLK = PROCCLK = 55MHz, V_{IN} = V_{CC} or GND, V_{CC} = 5.25V, Outputs Not Loaded	-	420	mA (Note 5)
Input Capacitance	C_{IN}	Freq = 1MHz, V_{CC} open, all measurements are referenced to device ground	-	8	pF (Note 6)
Output Capacitance	C_{OUT}				

NOTES:

5. Power Supply current is proportional to operation frequency. Typical rating for I_{CCOP} is 7.0mA/MHz.
6. Capacitance T_A = 25^oC, controlled via design or process parameters and not directly tested. Characterized upon initial design and at major process or design changes.

AC Electrical Specifications

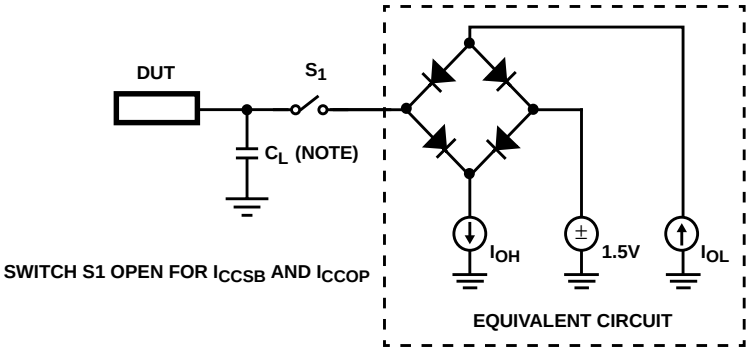
V_{CC} = 5 ±5%, T_A = 0^o to 70^oC, Commercial; -40^oC to 85^oC, Industrial (Note 7)

PARAMETER	SYMBOL	65MHz		UNITS
		MIN	MAX	
CLKIN Clock Period	t_{CP}	15	-	ns
CLKIN High	t_{CH}	6	-	ns
CLKIN Low	t_{CL}	6	-	ns
PROCCLK Period	t_{PCP}	18/24 (Note 10)	-	ns
PROCCLK High	t_{PCH}	7	-	ns
PROCCLK Low	t_{PCL}	7	-	ns
REFCLK Clock Frequency	f_{RCP}	-	PROCCLK/2	Hz
REFCLK High	t_{RCH}	7	-	ns
REFCLK Low	t_{RCL}	7	-	ns
Setup Time GAINADJ(2:0), IN(13:0), $\overline{ENI}$, COF, COFSYNC, and SYNCIN1 to CLKIN	t_{DS}	7	-	ns
Hold Time GAINADJ(2:0), IN(13:0), $\overline{ENI}$, COF, COFSYNC, and SYNCIN1 from CLKIN	t_{DH}	0	-	ns
Setup Time AGCGNSEL, SOF, MCSYNCI, SOFSYNC, and SYNCIN2 to PROCCLK	t_{DSS}	7	-	ns
Hold Time AGCGNSEL, SOF, MCSYNCI, SOFSYNC, and SYNCIN2 from PROCCLK	t_{DHS}	0	-	ns
Setup Time, A(2:0) to Rising Edges of $\overline{WR}$	t_{WSA}	8	-	ns
Setup Time, C(7:0) to Rising Edges of $\overline{WR}$	t_{WSC}	10	-	ns
Hold Time, A(2:0) from Rising Edges of $\overline{WR}$	t_{WHA}	2	-	ns
Hold Time, C(7:0) from Rising Edges of $\overline{WR}$	t_{WHC}	0	-	ns
$\overline{WR}$ to CLKIN	t_{WC}	14	-	ns (Note 9)
PROCCLK to AOUT(15:0), BOUT (15:0), $\overline{DATARDY}$, SEROUTA, SEROUTB, $\overline{INTRRP}$	t_{DO_OUT}	-	8	ns
PROCCLK to SYNCOUT	t_{DO_SYNCO}	-	8	ns
PROCCK to MCSYNCO	$t_{DO\_MCSYNCO}$	-	6	ns
PROCCLK to SERCLK, SERSYNC Valid	t_{DOS}	-	12	ns
$\overline{WR}$ High	t_{WRH}	15	-	ns
$\overline{WR}$ Low	t_{WRL}	8	-	ns
$\overline{RD}$ Low	t_{RL}	20	-	ns
Address Setup to Read Low	t_{AS}	-	3	ns
$\overline{RD}$ LOW to Data Valid	t_{RDO}	-	18	ns
$\overline{RD}$ HIGH to Output Disable	t_{ROD}	-	10	ns (Note 8)
Output Enable Time	t_{OE}	-	6	ns
Output Enable Time - FIFO Read Mode	t_{OEBL}	-	15	ns
Output Disable Time	t_{OD}	-	8	ns (Note 8)
Output Rise, Fall Time	t_{RF}	-	3	ns (Note 8)

NOTES:

7. AC tests performed with C_L = 40pF, I_{OL} = 2mA, and I_{OH} = -400µA. Input reference level for CLK is 2.0V, all other inputs 1.5V. Test V_{IH} = 3.0V, V_{IHC} = 4.0V, V_{IL} = 0V.
8. Controlled via design or process parameters and not directly tested. Characterized upon initial design and at major process or design changes.
9. Without discriminator/with discriminator.

AC Test Load Circuit



NOTE: Test head capacitance.

Waveforms

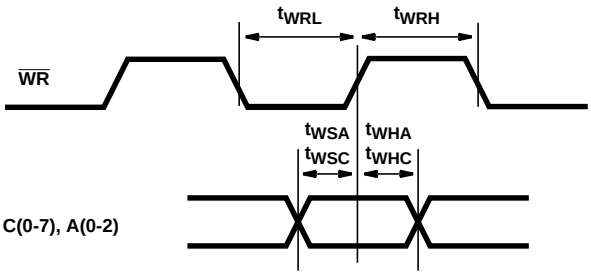


FIGURE 50. TIMING RELATIVE TO $\overline{WR}$

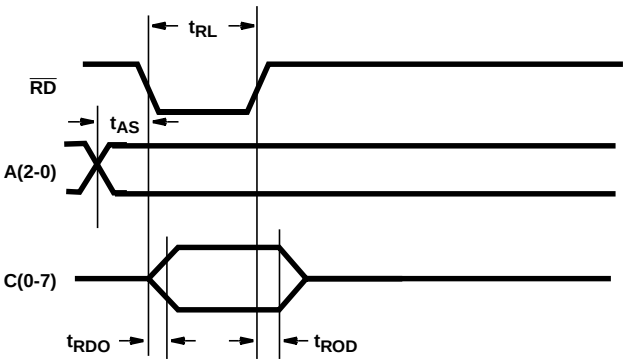


FIGURE 51. TIMING RELATIVE TO $\overline{RD}$

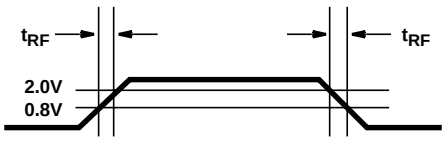


FIGURE 52. OUTPUT RISE AND FALL TIMES

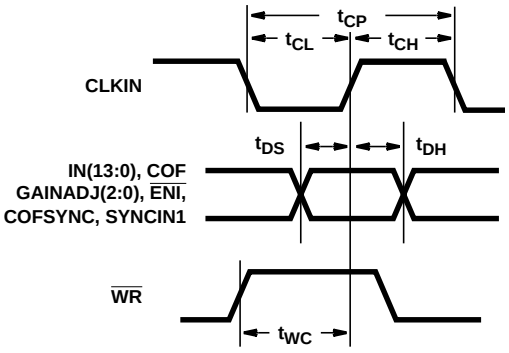


FIGURE 53. TIMING RELATIVE TO CLKIN

Waveforms (Continued)

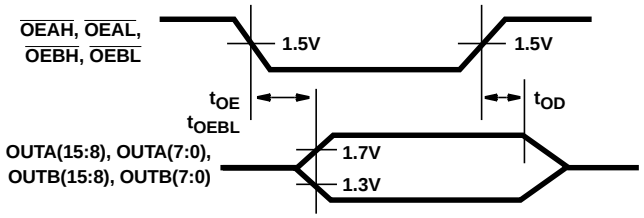


FIGURE 54. OUTPUT ENABLE/DISABLE

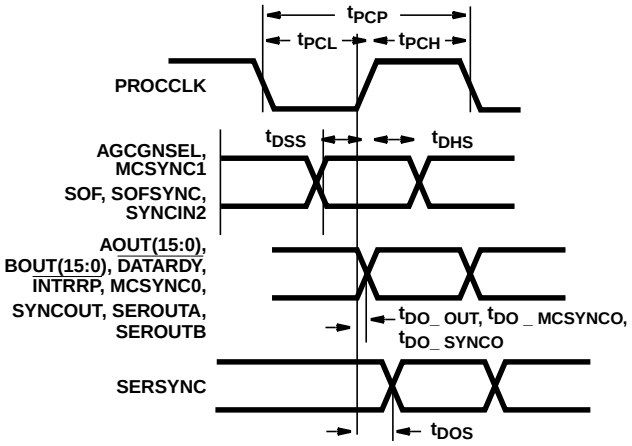


FIGURE 55. TIMING RELATIVE TO PROCCLK

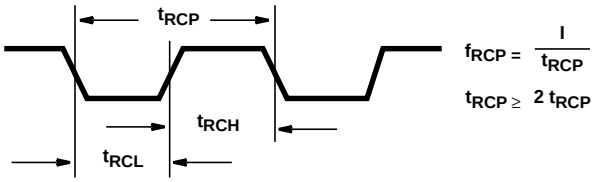


FIGURE 56. REFCLK

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