SIEMENS

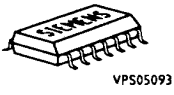
PLL-Frequency Synthesizer with I²C-Bus

TBB 200

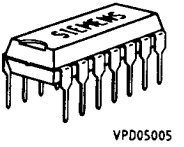
CMOS IC

Features

- Bit serial control with 2 lines (I²C)
- Modulus control
- Voltage doubler for high phase detector output voltage
- Linearization of phase detector output by current sources
- High input sensitivity (50 mV), high input frequencies (70 MHz) in single-modulus operation (at V_{DD} = 5 V, T_A = 25 °C)
- Low operating current consumption (2 mA)
- Standby circuit
- Extremely fast phase detector with very short anti-backlash pulse
- Lock detector output
- Large dividing ratios
  - A divider 0 to 127
  - N divider 3 to 4095
  - R divider 3 to 65535
- Switchable polarity and current rate of phase detector
- Port-output addressable via I²C bus, e.g.
  - for prescaler standby
  - for prescaler programming (128 or 64)



P-DSO-14



P-DIP-14

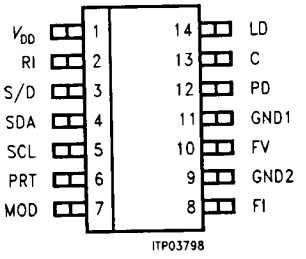
Type	Ordering Code	Package
TBB 200 G	Q67100-H8216	P-DSO-14 (SMD)
TBB 200	Q67100-H8215	P-DIP-14

TBB 200 is a CMOS IC specially developed for use in radio equipment and telephones. It is suitable for both simple frequency synthesis and dual-modulus synthesis.

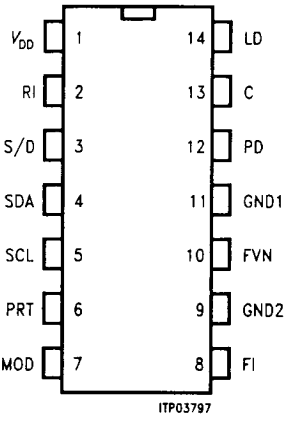
I²C-Bus is a bus system from the Philips Company and is protected by patent.

Pin Configuration
(top view)

P-DSO



P-DIP

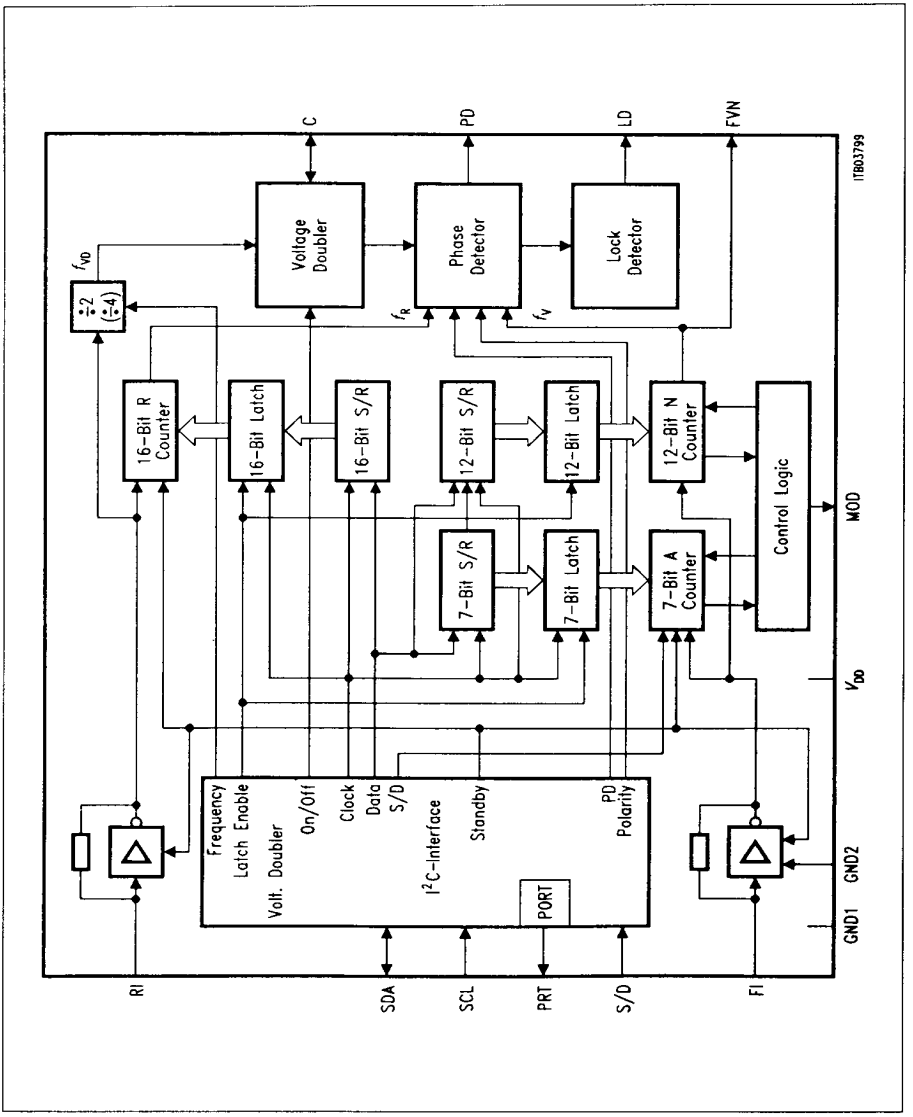


Pin Definitions and Functions

Pin No.	Symbol	Function	
1	V_{DD}	Supply voltage	
2	RI	Input for 16-bit R-divider (reference divider). The input has a sensitive preamplifier. AC coupling should be provided for small input signals, DC coupling being possible for large input signals.	
3	S/D	Input for setting single-modulus or dual-modulus operation.	
4	SDA	I²C bus data input	Each I²C-bus telegram begins with a START signal and ends with a STOP signal. With the STOP signal the received data are read into the latches. The IC acknowledges correct receipt of the IC-address with an acknowledge pulse on the data line.
5	SCL	I²C bus clock input	
6	PRT	Port-output (push-pull), status can be set on the bus, data are read with the STOP signal.	
7	MOD	Modulus control output for external dual-modulus prescaler. The modulus output is low at the beginning of the cycle. When the A-divider has reached its set value, MOD goes high. When the N-divider has reached its set value, MOD goes low again and the cycle starts again. If the prescaler has the divider factors P or P+1 (P for MOD = high, P+1 for MOD = low), the total division factor is N × P + A. The value of the A-divider must be smaller than that of the N-divider. In single-modulus operation and standby in dual-modulus operation the output is high-impedance for open-drain and tristate for push-pull.	
8	FI	Input with highly sensitive preamplifier for 12-bit N-divider and 7-bit A-divider. AC coupling should be provided for small input signals, DC coupling being possible for large input signals.	
9	GND2	Ground of the internal sensitive preamplifier of input FI. This must be connected externally to GND1.	
10	FVN	Comparison frequency output (open-drain); the output signal corresponds to the input frequency FI divided by the N-divider.	
11	GND1	Ground	
12	PD	Tristate charge pump output. The integrated negative and positive current sources can be programmed in current density via the bus. The activation/deactivation depends on the phase relationship of the scaled down input signals FI:N, RI:R (see pulse diagram for phase detector). $f_V < f_R$ or f_V lagging: p-channel current source active $f_V > f_R$ or f_V leading: n-channel current source active $f_V = f_R$ and PLL locked in: current sources disabled, output is high-impedance (tristate) In standby mode tristate is set. The assignment of the current sources to the output signals of the phase detector can be exchanged by status bit PD-polarity, ie the sign of the phase detector constant is controllable.	

Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Function
13	C	Voltage doubler output. The internal, capacitive voltage doubler works into an external capacitance on pin 13 (C: + on pin 11, – on pin 13). A typical capacitance value is 1 to 10 µF. The capacitor should have low leakage currents. If the voltage doubler is not required, connect pin C to GND1. Pin 13 is at the same time the foot of the n-channel current source of the PD-output. The clock frequency of the converter is derived via a programmable divider (:1, :2, :4) from the signal on RI. The internal clock frequency should be greater than 2 MHz.
14	LD	Lock detector output (open-drain). Unipolar output of the phase detector in the form of a pulse-width-modulated signal. In the locked-in state the low pulse width corresponds to the anti-backlash pulse. In standby mode the output is high-impedance.



Block Diagram

Circuit Description

TBB 200 is a complex PLL-component in CMOS-technology for processor controlled frequency synthesis. Pin S/D selects **S**ingle or **D**ual modulus operation. Functions and dividing ratios are selected via an I²C-bus (Philips license) at pins SDA and SCL. An output port PRT permits control (eg standby) of additional circuitry. The reference frequency is applied at input RI; its maximum value is 30 MHz. The VCO frequency is applied at input FI. Its maximum value in single-modulus operation is 70 MHz and in dual-modulus operation 30 MHz. The PLL can be operated optionally with or without an internal voltage doubler, depending on the required frequency variation (Varicap). For operation with a voltage doubler, a capacitance of typ. 1 to 10 µF (MKH) must be connected at pin C. C must be grounded when the voltage doubler is not in use.

Output PD supplies the phase detector signal with especially short anti-backlash pulses to neutralize even the smallest phase deviations. Output LD supplies a static lock-detector signal, and output FVN the divided VCO-frequency. LD and FVN are open-drain outputs.

By means of a short message (3 bytes) via the I²C-bus the component can be switched to standby mode. Depending on the type of standby the quiescent current consumption is below 1 µA. The PLL can be re-activated from this state by one command. Reloading of the R, N, A dividers and of additional information is not necessary since this is internally stored.

Mode	S/D	MOD
Single-modulus	L	(not activated)
Dual-modulus	H	L/H

Absolute Maximum Ratings
T_A = – 40 to 85 °C

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Supply voltage	V_{DD}	– 0.3		6	V	
Input voltage	V_I	– 0.3		V_{DD} + 0.3	V	
Output voltage at C	V_C	– V_{DD}		0	V	Exception: C (internally generated)
Power dissipation per output	P_Q			10	mW	
Total power dissipation	P_{tot}			300	mW	
Ambient temperature	T_A	– 40		85	°C	
Storage temperature	T_{stg}	– 50		125	°C	

Operating Range

Supply voltage		V_{DD}	3	5	5.5	V	
Supply current	single-modulus	I_{DD}		2.5	3.5	mA	1)
	dual-modulus	I_{DD}		2	3	mA	2)
	standby	I_{DD}			1	µA	3)
	standby preamplifier ON/ divider OFF/	I_{DD}		1.5		mA	4)
Ambient temperature		T_A	– 40		85	°C	

Test conditions, PLL locked, RI = 10 MHz

1)
f_I = 50 MHz
$V_{FI\,rms}$ = 150 mV
NT, RT > 1000
without voltage doubler
$I_{PD} = I_{PD\,min}$

2)
f_I = 10 MHz
$V_{FI\,rms}$ = 500 mV
NT, RT > 1000
without voltage doubler
$I_{PD} = I_{PD\,min}$

3)
f_I = 50 MHz
$V_{FI\,rms}$ = 150 mV
NT, RT > 1000
without voltage doubler
for output wiring refer to test circuit

4)
For output wiring refer to test circuit
inputs RI, FI open
$V_{IH\,min}$ (SDA, SCL): V_{DD} – 0.5 V
$V_{IH\,max}$ (SDA, SCL): V_{DD}

Characteristics

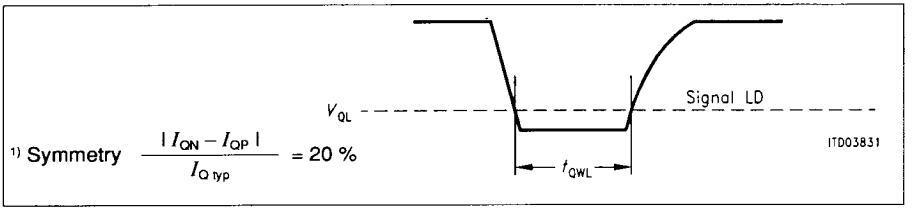
V_{DD} = 4.5 to 5.5 V; T_A = – 40 to 85 °C

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input Signals SDA, SCL					
H-input voltage	V_{IH}	$0.7 \times V_{DD}$	V_{DD}	V	
L-input voltage	V_{IL}	0	$0.3 \times V_{DD}$	V	
Input capacitance	C_I		10	pF	
Input current	I_I		10	µA	$V_I = V_{DD}$ = 5.5 V
Input Signal S/D					
H-input voltage	V_{IH}	$0.7 \times V_{DD}$	V_{DD}	V	
L-input voltage	V_{IL}	0	$0.3 \times V_{DD}$	V	
Input capacitance	C_I		10	pF	
Input current	I_I		10	µA	$V_I = V_{DD}$ = 5.5 V
Input Signal RI					
Input frequency	f_I		30	MHz	V_{DD} = 4.5 V
Input voltage	V_I	100		mVrms	(sine)*
Input capacitance	C_I		10	pF	
Input current	I_I		10	µA	$V_I = V_{DD}$ = 4.5 V
Input Signal FI (dual-modulus)					
Input frequency	f_I	0.1	30	MHz	V_{DD} = 4.5 V
Input voltage	V_I	50		mVrms	(sine)*
Input capacitance	C_I		10	pF	
Input current	I_I		10	µA	$V_I = V_{DD}$ = 4.5 V
Input Signal FI (single-modulus)					
Input frequency	f_I	70		MHz	V_{DD} = 4.5 V
Input voltage	V_I	50		mVrms	(sine)*
Input frequency	f_I		20	MHz	V_{DD} = 3 V
Input voltage	V_I	50		mVrms	(sine)
Input capacitance	C_I		10	pF	
Input current	I_I		10	µA	$V_I = V_{DD}$ = 4.5 V
Output Signal SDA					
L-output voltage	V_{QL}		0.4	V	I_{QL} = 3.0 mA V_{DD} = 5 V C_L = 400 pF

*only functional measurement, for input sensitivity see appendix

Characteristics
V_{DD} = 4.5 to 5.5 V; T_A = – 40 to 85 °C

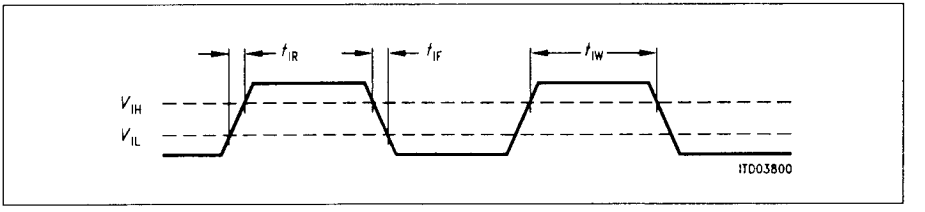
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Output Signal PD[1] (Tristate output)						
H-current mode	I_{QH}	± 1.9	± 2.5	± 3.1	mA	V_{DD} = 5 V, V_C = 0 V
L-current mode	I_{QL}	± 0.475	± 0.625	± 0.775	mA	T_A = – 25 °C to 60 °C
Tristate	I_Q		± 50		nA	
Output Signal FVN (Open-drain output)						
L-output voltage	V_{QL}			0.4	V	I_{QL} = 1 mA, V_{DD} = 5 V, C_L = 30 pF
L-output pulse width	t_{QWL}			1/FI	s	
Output Signals MOD, PRT						
H-output voltage	V_{QH}	V_{DD} – 0.4			V	I_{QH} = 0.5 mA, V_{DD} = 5 V
L-output voltage	V_{QL}			0.4	V	I_{QL} = 0.5 mA, V_{DD} = 5 V
Output Signal MOD (N-channel open-drain)						
L-output voltage	V_{QL}			0.4	V	I_{QL} = 0.5 mA, V_{DD} = 5 V
Output Signal LD (Open-drain output)						
L-output signal	V_{QL}			0.4	V	I_{QL} = 3 mA, V_{DD} = 5 V, C_L = 30 pF
L-output pulse width	t_{QWL}		20	40	ns	



Pulse Diagram

Dynamic Characteristics
V_{SS} = 5 V; T_A = – 40 to 85 °C

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input Signal RI					
Rise time	t_{IR}	5		ns	V_{DD} = 5 V
Fall time	t_{IF}	5		ns	V_{DD} = 5 V
Pulse width	t_{IW}	10		ns	V_{DD} = 5 V
Input Signal FI Dual-Modulus					
Rise time	t_{IR}	3.5		ns	V_{DD} = 5 V
Fall time	t_{IF}	3.5		ns	V_{DD} = 5 V
Pulse width	t_{IW}	3.5		ns	V_{DD} = 5 V
Single-Modulus					
Rise time	t_{IR}	5		ns	V_{DD} = 5 V
Fall time	t_{IF}	5		ns	V_{DD} = 5 V
Pulse width	t_{IW}	10		ns	V_{DD} = 5 V



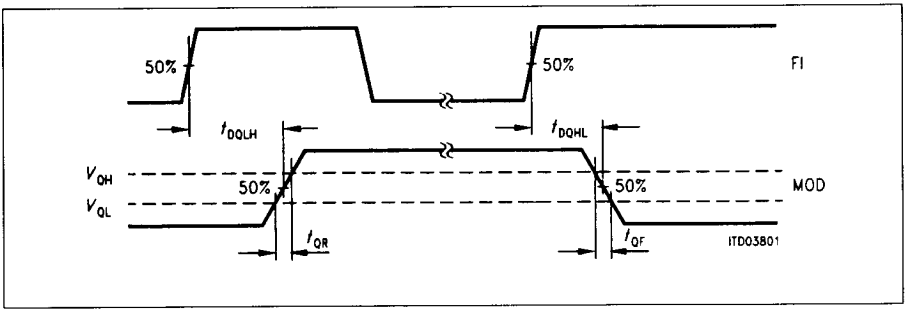
Pulse Diagram

Dynamic Characteristics
V_{SS} = 5 V; T_A = – 40 to 85 °C

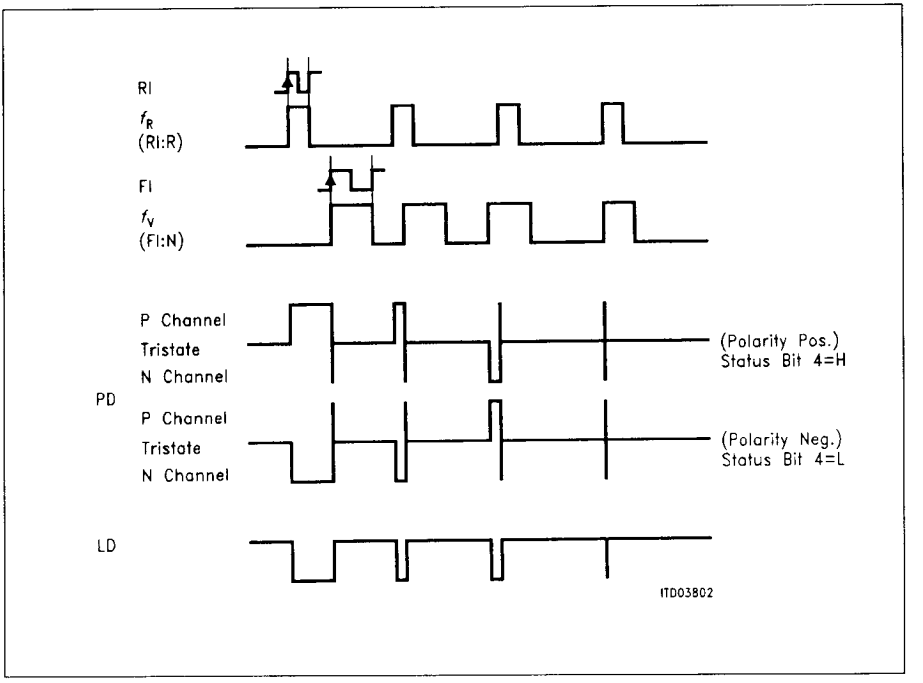
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Voltage Doubler						
Output voltage	V_{QC}	$-V_{DD}$ + 0.8 V		$-V_{DD}$	V	f_{VD} = 2 MHz I_{QC} = 0 µA V_{DD} = 5 V
	V_{QC}	$-V_{DD}$ + 1.5 V		$-V_{DD}$	V	f_{VD} = 2 MHz I_{QC} = 100 µA V_{DD} = 5 V
	V_{QC}	$-V_{DD}$ + 0.8 V		$-V_{DD}$	V	f_{VD} = 2 MHz I_{QC} = 0 µA V_{DD} = 3 V
	V_{QC}	$-V_{DD}$ + 1.5 V		$-V_{DD}$	V	f_{VD} = 2 MHz I_{QC} = 100 µA V_{DD} = 3 V
Current consumption	I_{VD}		250		µA	V_{DD} = 5 V I_{QC} = 0 µA f_{VD} = 2 MHz
	I_{VD}		180		µA	V_{DD} = 3 V I_{QC} = 0 µA f_{VD} = 2 MHz

Dynamic Characteristics
V_{SS} = 5 V; T_A = – 40 to 85 °C

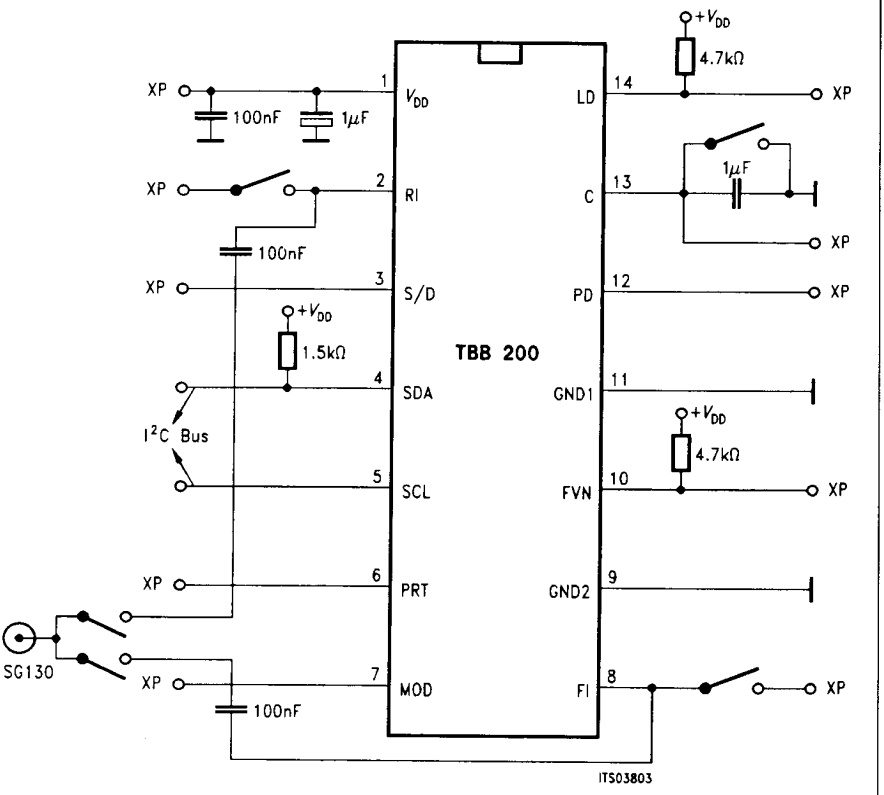
Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Output Signal PRT					
Rise time	t_{QR}		1	µs	C_L = 30 pF
Fall time	t_{QF}		1	µs	C_L = 30 pF
Output Signal FV					
Fall time	t_{QF}		20	ns	C_L = 30 pF
Output Signal MOD					
Rise time	t_{QR}		10	ns	C_L = 30 pF
Fall time	t_{QF}		10	ns	C_L = 30 pF
Delay time L-H to FI	t_{DQLH}		25	ns	C_L = 30 pF
Delay time H-L to FI	t_{DQHL}		15	ns	C_L = 30 pF



Pulse Diagram



Phase Detector / Lock Detector



XP = Measurement or test pin acc. to data sheet
SG = signal generator

Test Circuit

Input Sensitivity of Preamplifier

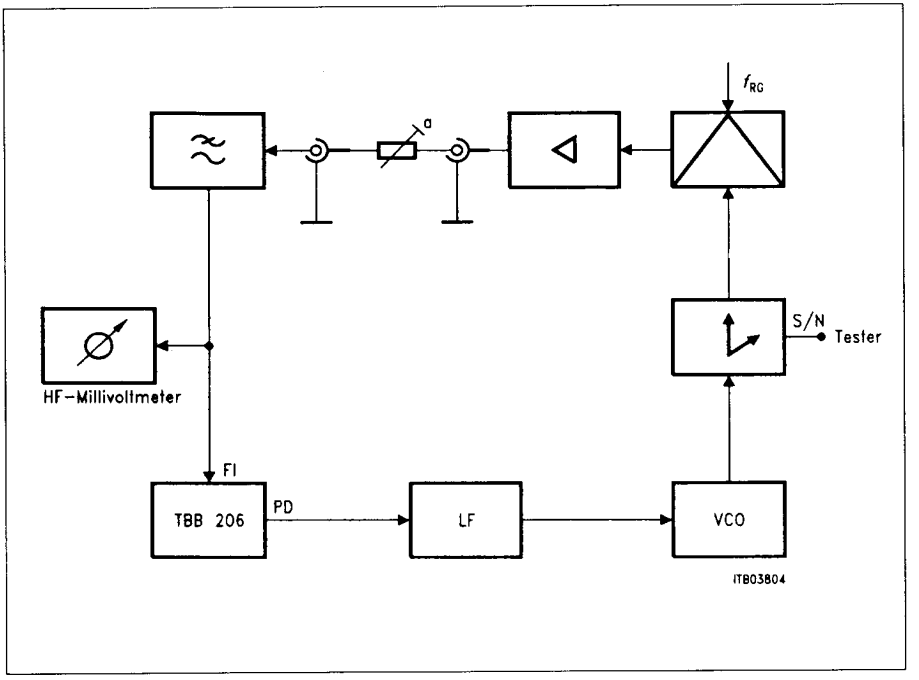
Measuring Procedure

1. Determine S/N-ratio of VCO with CCITT weighting:
   Input voltage on FI: 0 dBm
   Input frequency on FI: $f_{VCO} - f_{RF}$
2. Increase attenuation a until – 3 dB point is reached.
   Sensitivity = input voltage on FI

Boundary Condition

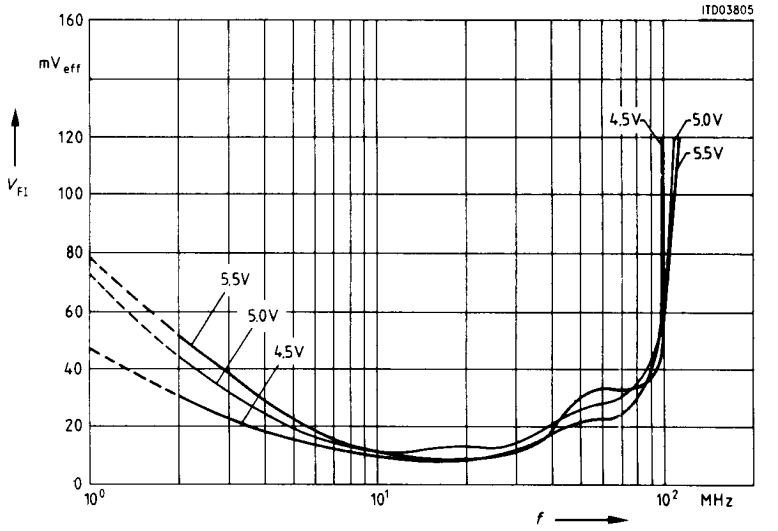
The frequency of the control loop must be substantially greater than the upper cutoff frequency of the CCITT filter.

The lock detector is not wired.

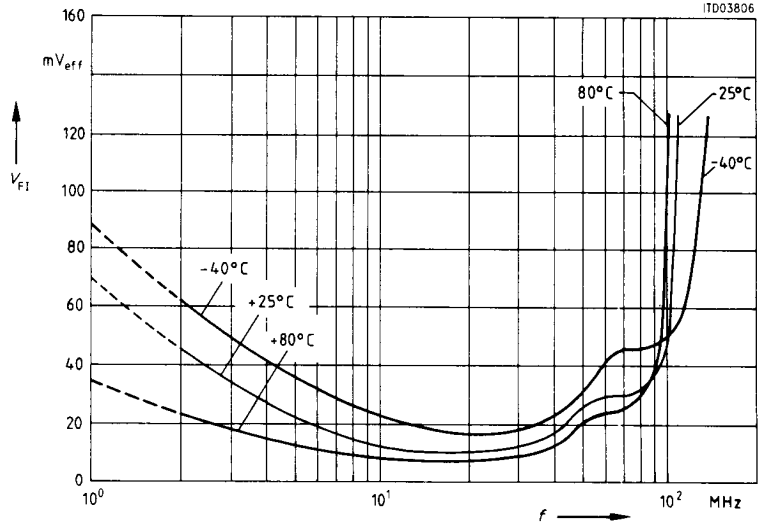


Test Circuit
Block Diagram

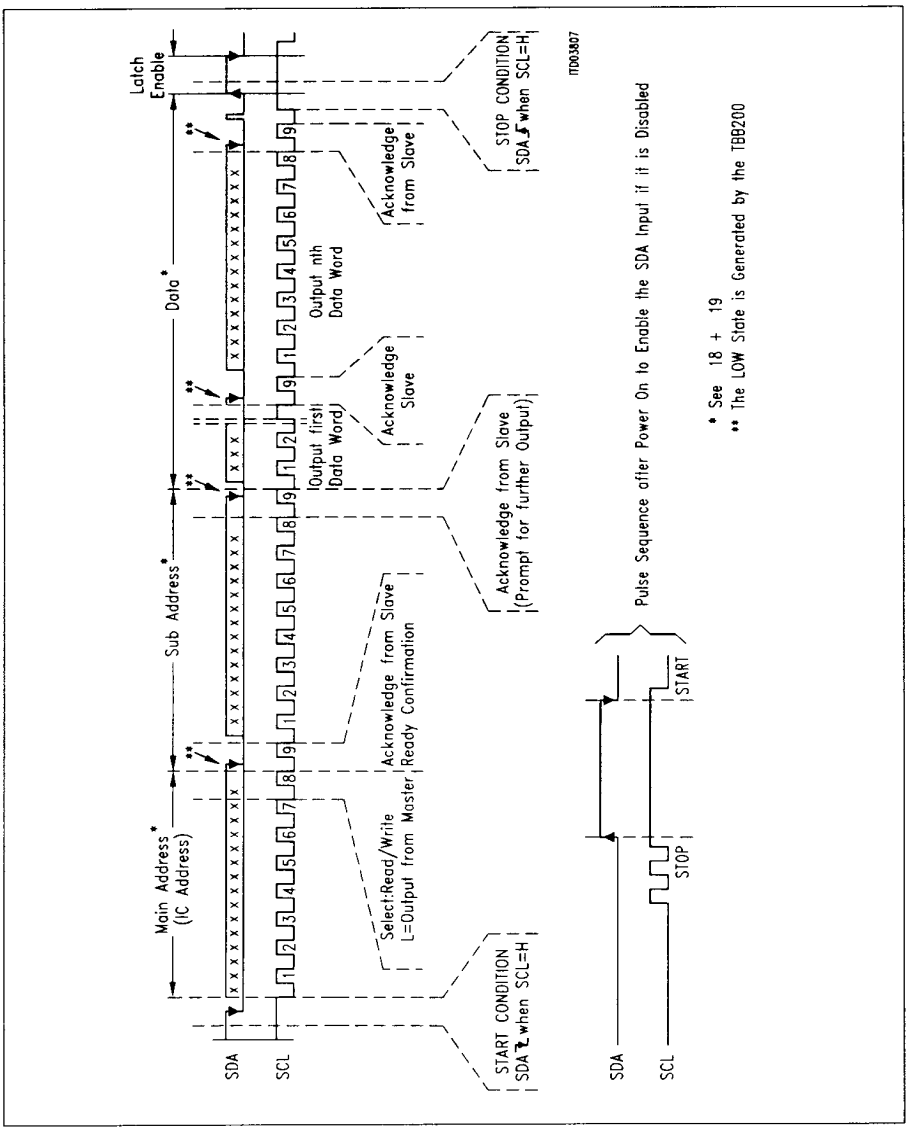
Typical Input Sensitivity of Preamplifier FI at T_A = 25 °C



Typical Input Sensitivity of Preamplifier FI at V_{DD} = 5 V



I²C-Bus Transmission Protocol



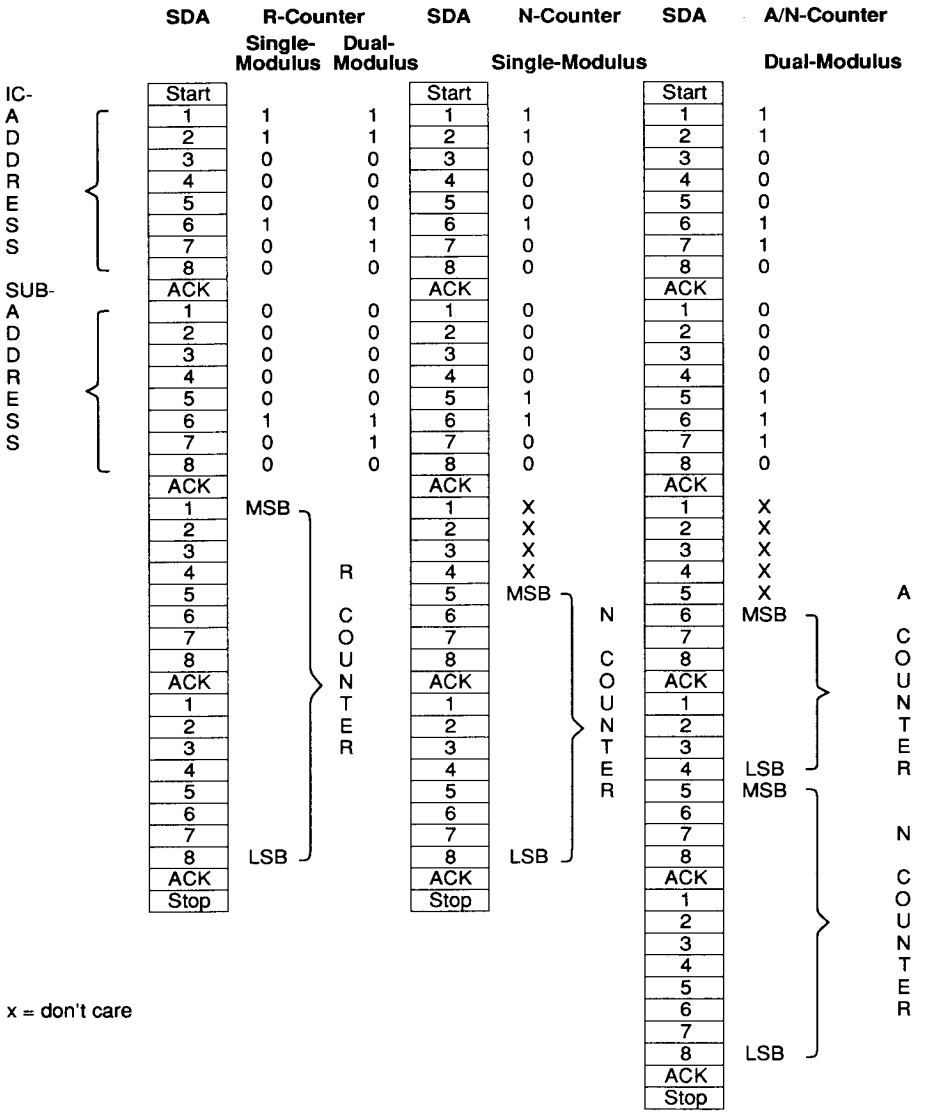
Transmission Protocol for Programming

SDA		STATUS Single-Modulus	Dual-Modulus
Start			
1	IC-	1	1
2	A	1	1
3	D	0	0
4	D	0	0
5	R	0	0
6	E	1	1
7	S	0	1
8	S	0	0
ACK			
1	SUB-	0	0
2	A	0	0
3	D	0	0
4	D	0	0
5	R	1	1
6	E	0	0
7	S	0	1
8	S	0	0
ACK			
1		PORT	
2	S	Counter	
3	T	FI, RI	
4	A	PD-polarity	
5	T	PD-current	
6	U	Voltage doubler frequency	
7	S	Voltage doubler status	
8		Modulus output	
ACK			
Stop			

Status Bit	
0	1
Low[2]	High[2]
off[1]	on
off[1]	on
neg.	pos.
0,625 mA	2,5 mA
÷ 2	÷ 4
off	on
push-pull	open-drain

[1] Standby: FVN, LD, MOD are in H-state, PD is in tristate
[2] PORT-output state

Transmission Protocol for Programming

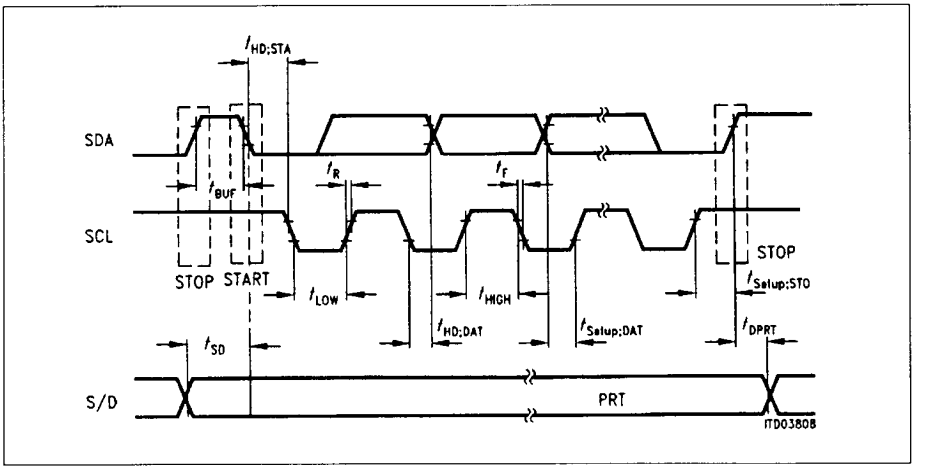


Switching Times

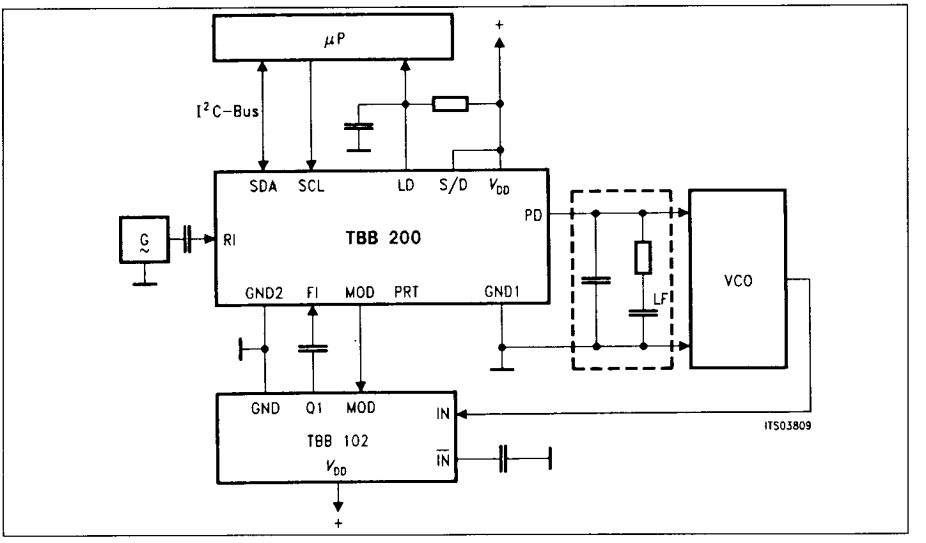
Parameter	Symbol	Limit Values		Unit
		min.	max.	
Clock frequency	f_{SCL}	0	100	kHz
Hold time data to SCL low	$t_{HD;\,DAT}$	0		µs
Inactive time prior next transmission	t_{BUF}	4.7		µs
Start condition hold time (first clock pulse is generated after this time period)	$t_{HD;\,STA}$	4.0		µs
Clock low phase	t_L	4.7		µs
Clock high phase	t_H	4.0		µs
Data setup time	$t_{SU;\,DAT}$	250		ns
SDA and SCL signal rise time	t_R		1	µs
SDA and SCL signal fall time	t_F		300	ns
SCL pulse setup time with stop condition	$t_{SU;\,STO}$	4.7		µs
Status programming setup time (S/D)	t_{SD}	500		ns
PRT delay time relative to stop condition	t_{DPRT}		500	ns

All values with reference to specified input levels V_{IH} and V_{IL}.

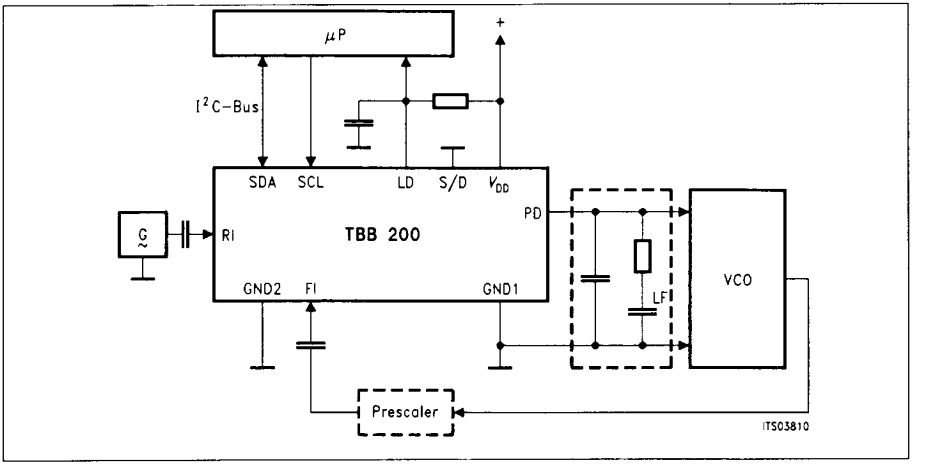
Pulse Diagrams for I²C Bus, S/D, PRT



Application Circuits

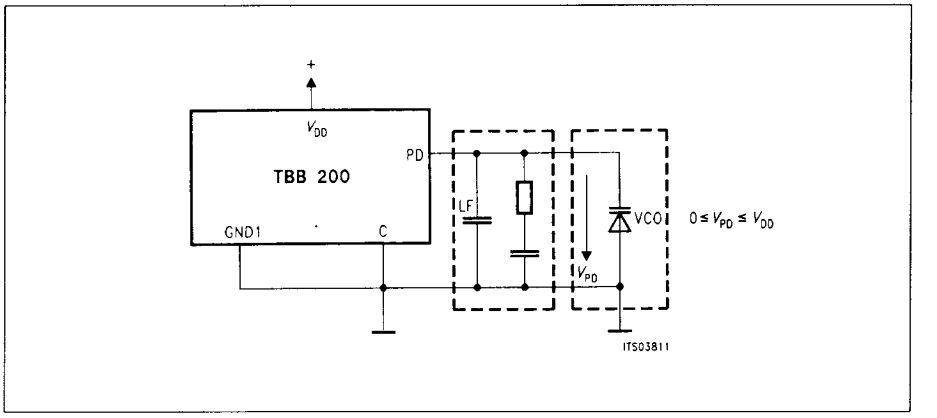


Operation: dual-modulus (f_{max} = 30 MHz at FI)

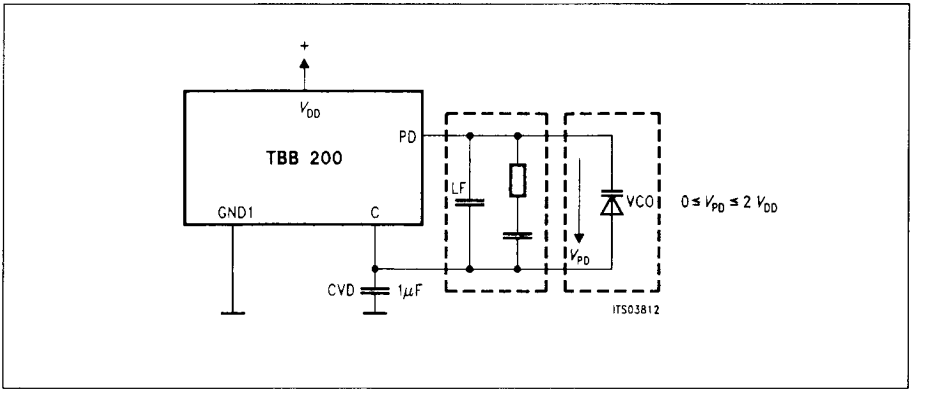


Operation: single-modulus (f_{max} = 70 MHz at FI)
LF: loop filter

Application Circuits VCO-Coupling



Operation without voltage doubler (status bit 7 = 0)



Operation with voltage doubler (status bit) = 1
LF: loop filter

Example of Loop-Filter Configuration

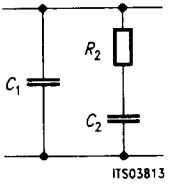
The following requirements are made for the loop-filter configuration:

a) the PLL should behave as a PT_2 network,

b) an additional time constant should provide effective attenuation of the reference frequency lines in the spectrum.

The network shown satisfies these requirements.

Figure 1
Loop Filter

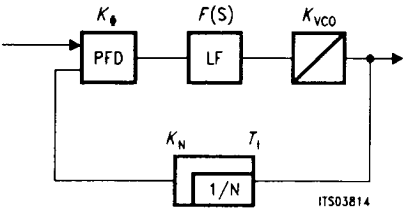


$$F(S) = \frac{1+s\tau_2}{sK\,C_1\,(1+s\tau_2\,\frac{1}{K})}$$

$$\tau_2 = C_2 \cdot R_2$$

According to Gardner /1/ this circuit corresponds to a PLL, type 2, 3rd order. A deeper examination of this control circuit can be made in the Bode diagram (**fig. 3**).

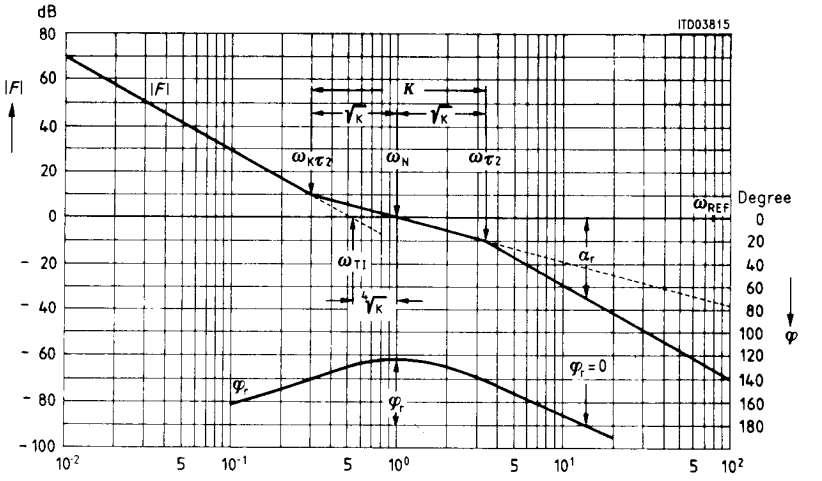
Figure 2
Complete control circuit with corresponding frequency response of the open loop circuit.



$$F_o = \frac{K_{VCO}\;K_\phi\;K_N\;(1+s\tau_2)\,e^{s\,T_1}}{sK^2\,C_1\,(1+s\tau_2\,\frac{1}{K})}$$

$$K = \frac{C_2}{C_1} + 1$$

Figure 3
Bode Diagram for the Open-loop Control Circuit, Normalized to $\omega_N = 1$



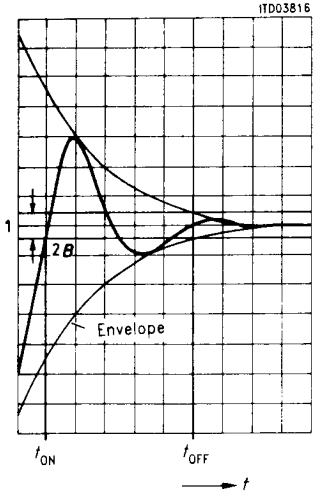
In this diagram a point ω_N is indicated where the true curve cuts the asymptotic amplitude characteristic. Also the phase edge ω, reaches its maximum exactly at this point, which

can be calculated from $\omega_N = \sqrt{\omega_{\tau 2} \times \omega_{\tau 2}}$ (3)

In the region of this point the amplitude characteristic approaches a positive slope of 20 dB/dec. There is therefore the possibility of being able to dscribe the control circuit with the PT_2 parameter attenuation d and the self-resonant frequency ω_N. In order to obtain the required phase margin at the point ω_N, the ratio K of the time constants (**see fig. 2**) is varied.

Figure 4
Transient Response

With regard to applications it is interesting to know after which period t a given tolerance band B is entered but not left again for a step in frequency. The step response of a PT_2 network is therefore analyzed for $d < 1$.



$$h(t) = M\left[1 + \frac{e^{-d\omega_N t}}{\sqrt{1-d^2}}\sin\left(\sqrt{1-d^2}\,\omega_N t + \varphi\right)\right] \quad (4)$$

The computational formulae result from these observations. The chosen attenuation factor d, the stabilization period T_{OFF} and the tolerance band B. The natural frequency ω_N can be calculated from these given parameters.

$$\omega_N = \frac{-\ln\left(B\sqrt{1-d^2}\right)}{d \times T_{OFF}} \quad (5)$$

$$A = \mathrm{tg}\left(\frac{\omega_N}{\omega_{REF}} + \arctan(2d)\right) \quad (6)$$

$$K = \left(A + \sqrt{A^2+1}\right)^2 \quad (7)$$

The relationship 7 can be simplified for the case $\omega_N \ll \omega_{REF}$ to

$$K = \left(2d + \sqrt{4d^2+1}\right)^2$$

If the parameters K_Φ K_{VCO} and N are known, the loop filter elements C_1, C_2 and R_2 can be calculated.

$$C_1 = \frac{K_{VCO} \times K_\Phi}{N\omega_N^2 \times \sqrt{K}} \quad (8)$$

$$C_2 = (K-1)\, C_1 \quad (9)$$

$$R_2 = \frac{\sqrt[4]{K}}{\omega_N \times C_2} \quad (10)$$

Application Example (in loop filter corresponding to **fig. 1**)

The frequency range should be varied in steps of 25 kHz with half channel displacement. The reference frequency is therefore set to f_{REF} = 12.5 kHz. The IF-bandwidth is 6 kHz. For a change of channel the oscillator frequency should have come so close to the final frequency in the given time of 10 ms that the channel can be evaluated. The tolerance band is chosen as 1/4 of the IF-bandwidth.

$$B = \frac{1{,}5 \text{ kHz}}{25 \text{ kHz}} = 0{,}06$$

Phase-detector constant $K_\Phi = \frac{I}{2\pi} = 0{,}398 \frac{\text{mA}}{\text{rad}}$

VCO constant $K_{VCO} = 5{,}03 \times 10^6 \frac{\text{rad}}{\text{Vs}}$

$d = d_{opt} = 0{,}7$

f_{min} = 900.0125 MHz f_{max} = 900.9875 MHz

$N_{min} = \frac{f_{min}}{f_{REF}} = 72001$ $N_{max} = \frac{f_{max}}{f_{REF}} = 72079$

The PLL should be designed for the average dividing factor N:

$$N = \sqrt{N_{max} \times N_{min}} = 72040$$

$$\omega_N = \frac{-\ln (B\sqrt{1-d^2})}{d \times T_{OFF}} = 450 \text{ 1/s}$$

$$A = \tan\left(\frac{\omega_N}{\omega_{REF}} + \arctan(2d)\right)$$

$$K = (A + \sqrt{A^2+1})^2 = 9.9$$

$$C_1 = \frac{K_\Phi K_{VCO}}{N \times \omega_N^2 \times K} = 43.5 \text{ nF} \qquad 43 \text{ nF selected}$$

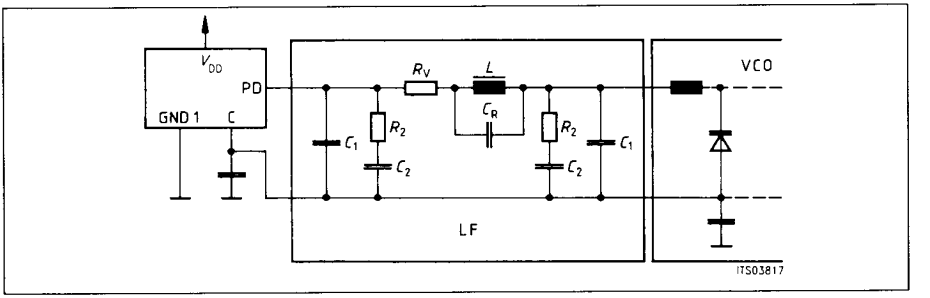
$$C_2 = (K-1)\, C_1 = 308.6 \text{ nF} \qquad 390 \text{ nF selected}$$

$$R_2 = \frac{\sqrt[4]{K}}{\omega_N \times C_2} = 17.9 \text{ k}\Omega \qquad 17.8 \text{ k}\Omega \text{ selected}$$

Loop Filter Higher-Order

A higher-order filter is often necessary because of strict requirements regarding phase noise. The simple three-element filter is devided into two identical parts and connected by the additional components R_V, L and C_R.

Figure 5
Loop Filter



By using R_V and L additional limit frequencies can be inserted in the Bode diagram, and with C_R spectral components can be suppressed, e.g. the reference frequencies or their multiples. There is a program available for optimizing this filter on AT/XT-compatible PCs.

Ordering NO. Q 67100-H 8729.

Explanation of Symbols:

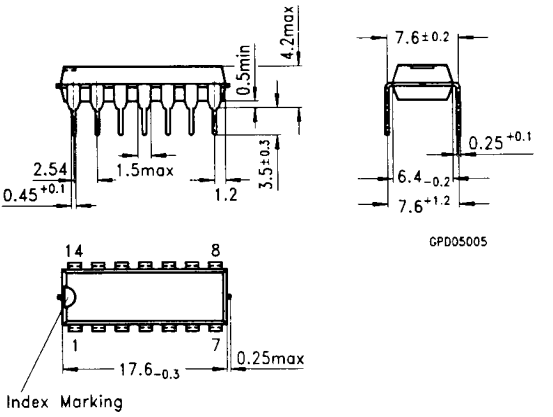
PFD	Phase Frequency Detector
N	Divider ratio
f_{VCO}	VCO frequency
K_N	Transfer coefficient of the divider
K_Φ	Transfer coefficient of the PFD
K_{VCO}	Transfer coefficient of the VCO
t_d	Dead time
f_{REF}	Reference frequency
F_O	Frequency response of the open-loop control circuit
K	Ratio of the time constants
B	Tolerance band
t_{OFF}	Setting time
d	Attenuation damping factor
ω_N	Natural frequency of the loop
I	Output current of the PFD

Literature:

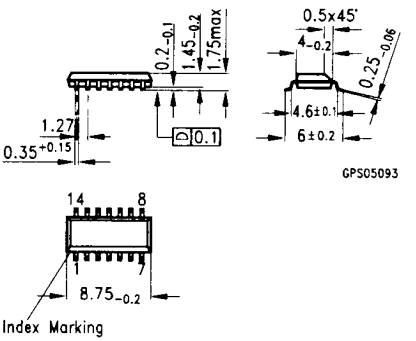
Gardner, Floyd: Charge-Pump Phase Locked Loops
IEEE Vol. COM-28, 11.80

Package Outlines

Plastic-Package, P-DIP-14
(Dual-In-Line)



Plastic-Package, P-DSO-24-4 (Shrink) (SMD)
(Dual-Small-Outlines)



Sorts of Packing
Package outlines for tubes, trays ect. are contained in our Data Book "Package Information"

SMD = Surface Mounted Device

Dimensions in mm