Features

- **Besides the serial IEEE-1355 link, the T7906E provides several different interface types:**
  - **Host interface**
    The host interface provides 8 multiplexed data and address lines to program and control the T7906E locally
  - **FIFO interface**
    The FIFO interface provides the control signals FULL, WRITE, EMPTY and READ depending on the direction of the data flow (receive / transmit)
  - **ADC interface**
    The ADC interface allows to connect an ADC with a width of up to 16 bits directly to the T7906E
  - **DAC interface**
    The DAC interface provides up to 16 bits data lines and the required control signals. The data to be sent to the DAC are stored until a command "start DAC" is received
  - **RAM interface**
    The RAM interface provides a 16-bit data bus and a 16-bit address bus. Four chip select allow to address 4 different memory partitions. The memory interface can be programmed to use up to 7 wait states
  - **UART interface**
    Two independent UART interfaces are included. One UART uses dedicated I/O lines whereas the second UART is sharing its pins with the GPIO port
  - **General purpose I/O**
    This general Purpose Interface provides up to 24 bidirectional signal lines. The direction of each GPIO line can be set individually via register
  - **Timer / Event Counter**
    Two 32-Bit on-chip timers are available. Each timer provides a 32-Bit counter and a 32-Bit reload register. The two timers can be operated independently or cascaded
  - **JTAG (IEEE 1149.1)**
    For testing purposes, a standard IEEE 1149.1 interface is provided. It supports the JTAG function Bypass, Extest, Sample/preload, All-tristate and IDCode
- **Designed on Atmel MG1090E sea of gates matrix and packaged into MQFPF100**
- **Also called SMCS Lite (or SMCS116)**

Description

The T7906E provides one IEEE-1355 serial communication link with 0 to 200 Mbit/s data transmit rate. It supports both the standard IEEE-1355 link protocol (transparent mode) as well as the header generation required for the enhanced transaction layer of the TSS901E. This protocol uses specific protocol headers that can be generated by the T7906E without requiring an external host controller. These headers are stored in specific header registers which allows headers with a length of 0 (equaling the transparent mode) to eight bytes per packet. Packetization of data sent by the T7906E over the link is also done automatically according to the settings of a packet length register.

Another feature provided by the transaction layer supported by the T7906E is an automatic checksum generation on the link. This is generated and checked automatically by the T7906E without requiring support from a host or other external source. Errors on the link are flagged and a special error packet is sent over the link to signal the error condition.

Programming the T7906E internal registers is done via the IEEE-1355 link. All internal registers are 8-bit wide addressable. Two simple commands (read and write) suffice to access all functions and registers of the T7906E.

ATMEL WIRELESS & µC

Single Point to Point IEEE 1355 High Speed Controller

T7906E

Rev. A – 27-Aug.-01

The interfaces of the T7906E such as the FIFO, UART, ADC/DAC and memory interface are accessed by a simple read or write operation to the corresponding interface address. In the case of FIFO, Host, UART and memory interface, a packet oriented access is also possible (meaning transferring multiple bytes with a single command). In case a communication memory

is connected to the T7906E, this can be read and written to via the link specific registers.

The IEEE-1355 links can support a range of communication speeds, which are programmed by writing to registers. At reset all links are configured to run at the base speed of 10 Mbits/sec. Only the transmission speed of a link is programmed as reception is asynchronous. This means that links running at different speeds can be connected, provided that each device is capable of receiving at the speed of the connected transmitter.

Introduction

Connecting a non-intelligent node to a processing element requires not only the communication controller, but usually a controlling instance for the communication circuitry. The latter has to be configured for settings like bit rate, packet sizes, handshake protocols etc. Should the non-intelligent node require remote control via commands, usually a second link, dedicated for commands is introduced. Using an IEEE-1355 link for that purpose eliminates the need for separate data and control paths, since the communication controller can differentiate between the two entities. In addition, it can be remotely configured, can execute simple commands and provides special I/O pins to control the interface unit.

The T7906E provides one IEEE-1355 serial communication link together with additional features to support non-intelligent nodes as well as to control ADC and DAC converters.

The T7906E is targeted at two main applications areas:

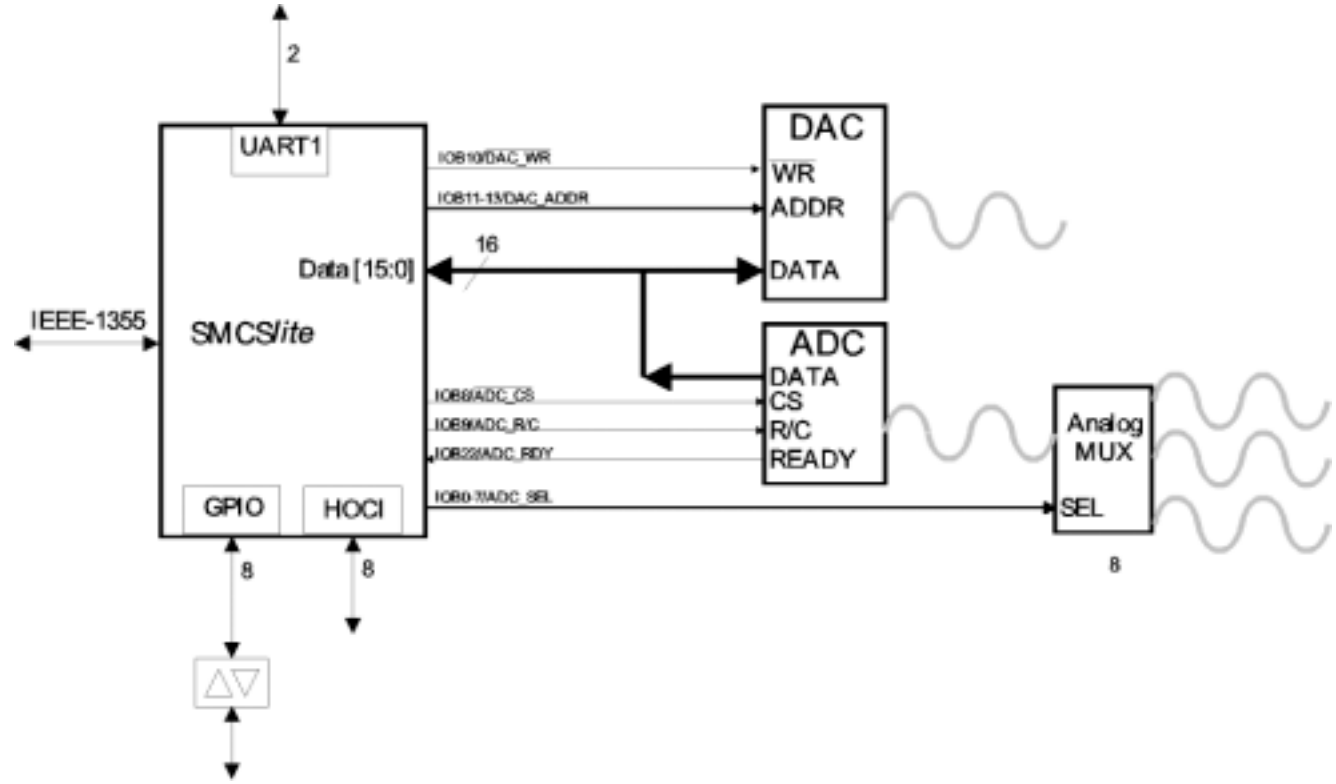
- Embedded systems
- Communication device for processor systems

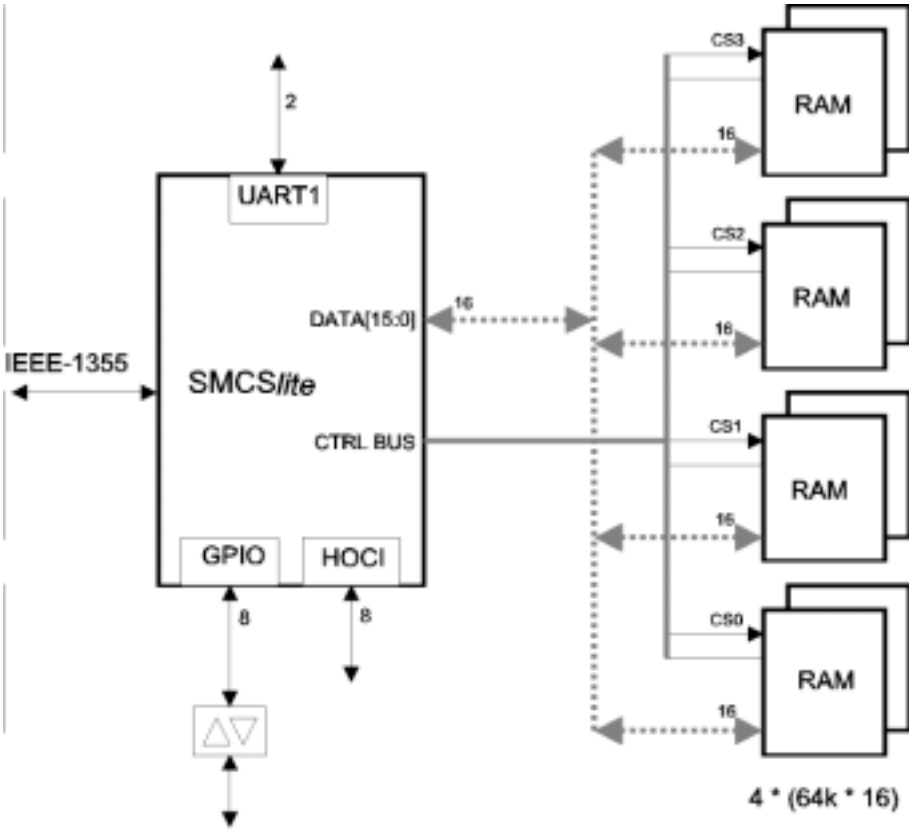
Embedded systems

The main application targets of the T7906E are modules and units without any built-in communication features, such as special image compression chips, application specific programmable logic or mass memory. The T7906E is perfectly suited to be used on "non-intelligent" modules such as A/D-converter or sensor interfaces, due to its "control by link" feature and system control facilities. In addition, its fault tolerance feature make the device very interesting for many critical industrial measurement and control systems.

Example applications of the T7906E as communication and system controller on an interface node consisting of an ADC and DAC and one where the T7906E is connected to four banks of memory are given in the figures below:

Figure 1. Example applications

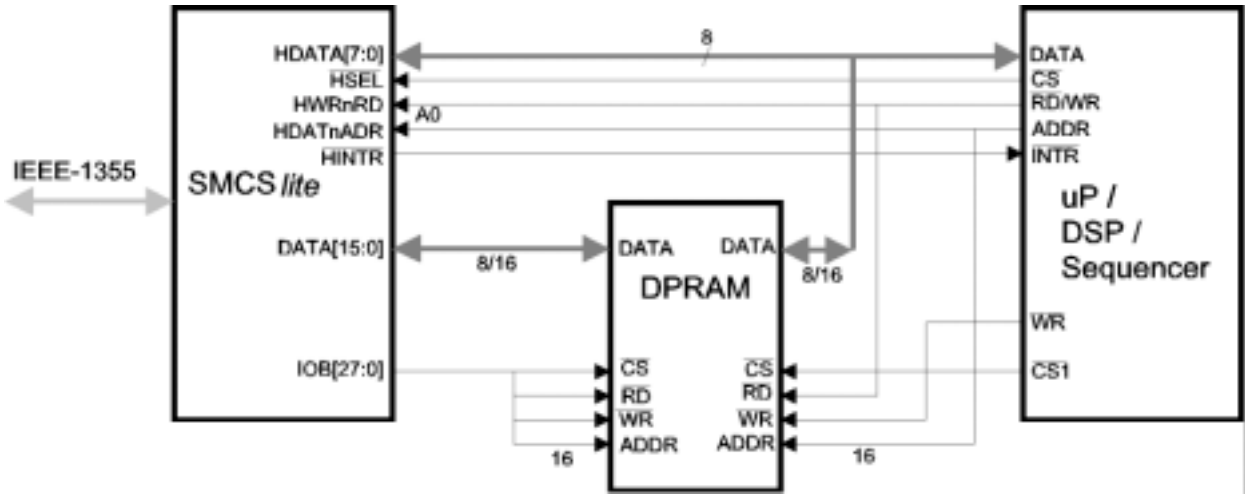




Communication device for microprocessors

Many applications require a link front end providing one link, but no controller instance on that unit. Due to the communication memory interface of the SMCS*lite*, it is also satisfying the requirements of these applications. Due to its small package and low power consumption it is an excellent alternative to FPGA based solutions. A system using the SMCS*lite* as a communication front-end for a microcontroller is shown in the figure below:

Figure 2. Example application



Interfaces

FIFO interface

The FIFO interface provides the control signals full, write, empty and read, depending on the direction of the data flow (receive/transmit).

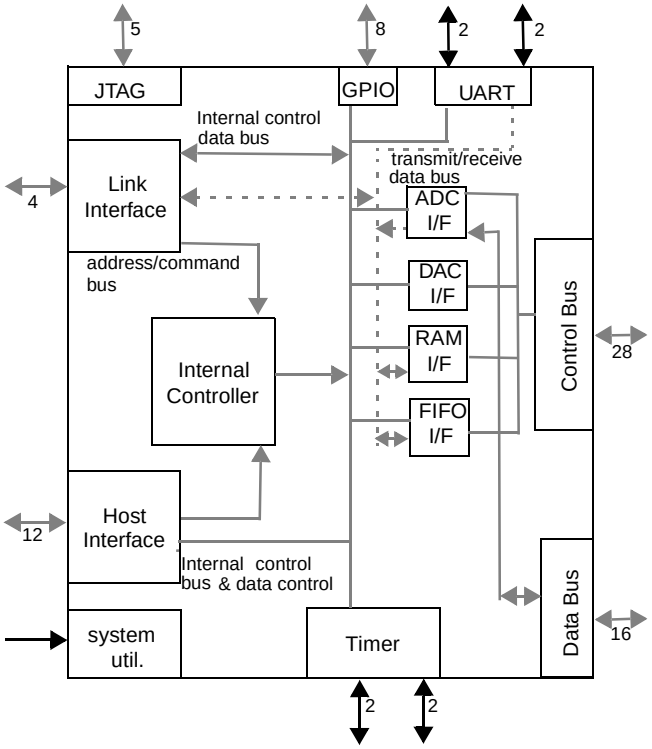
Data received from the FIFO interface is sent over the IEEE-1355 link grouped in packets. The length of a packet (in bytes) can be specified either by setting an internal counter or by external signals. This interface can be programmed to use 0 to 7 wait states.

ADC/DAC interface

The ADC interface allows to connect an ADC with a width of up to 16 bits directly to the T7906E. The AD conversion can be started by request via link or in a cyclic manner triggered by the on-chip timers. When the AD conversion is ready, this is recognized by an external signal like "ready" or by an internal trigger, for example from the on-chip timer. After reading the sample from the ADC it is then sent over the link. An 8-bit address generator is provided to allow multiplexing of analog signals. The address generator will start at a pre-programmed start address and will be incremented after each conversion.

The DAC interface is very similar to the ADC interface. It provides up to 16 data lines and the required control signals. The data to be sent to the DAC is received from the link and is stored in a register until the command "start DAC" is received. After that command the register values will be put to the DAC.

Block Diagram



Memory Interface

The RAM interface provides a 16-bit data bus and 16-bit address bus. Four chip select lines allow to address four different memory partitions (banks). This partitioning into different banks is done using 4 internal address boundary registers. These are 8 bit wide and provide a minimum page size of 1024 words. The memory interface can be programmed to use 0 to 7 wait states.

GPIO Interface

The general purpose I/O (GPIO Interface) provides up to 24 bidirectional signal lines. The direction (input or output) of each GPIO line can be set individually via register. Data to/from the GPIO lines is written/read via the GPIO data register. The GPIO provides 8 dedicated I/O lines, the remaining 16 lines of the port are shared with the ADC address and host data bus. These GPIO lines are available when the corresponding unit (e.g. the host data bus) of the T7906Eis not being used (disabled).

UART interface

Two independent UARTs are included in the T7906E as well. One UART uses dedicated I/O lines whereas the second UART is sharing its pins with the GPIO port. The transmit rate of the UARTs in bps can be programmed via a 12-bit wide register with a maximum bit rate of about 780 kbit/s. The UARTs can optionally use hardware handshake (rts/cts).

Host Interface

Although the T7906E is primarily designed to be remotely controlled, it can nevertheless be programmed and controlled by a local host if required. For that purpose a host interface provides 8 multiplexed data and address lines.

Timers / Event Counter

Two 32-bit on-chip timers are available on the T7906E. Each timer provides a 32 bit counter and a 32 bit reload register. The two timers can be operated independently or

cascaded. The timers can also be used to set an external signal when the timeout value is reached.

Configuration

After a chip reset the T7906E is configured by the internal controller. This can be either by receiving the configuration data from the IEEE-1355 link or by an external controller connected to the host port of the T7906E.

Shared I/O

Some of the functions of the T7906E presented above share the same I/O pins. This means, that some functions are mutually exclusive. As an example, the GPIO port shares some of its I/O pins with the host interface. If the host interface is not used, these pins are available for GPIO, otherwise they are used as the host address and data bus. The selection of which functions are being used is made by programming the appropriate registers after a chip reset. A short overview of the pin allocation and combinations of functions is given in the table below:

Interface Type	Example Mode 1	Interface Type 2	Example Mode 3
Host / GPIO2	•	•	•
Timer1	•	•	•
Timer2	•	•	•
UART1	•	•	•
UART2	•	•	•
GPIO0	GPIO7-0	-	GPIO7-0
GPIO1	IOB7-0		IOB7-0
FIFO	active mode	-	passive mode
RAM	-	•	-
ADC	•	-	-
DAC	•	-	-

Note: If the passive FIFO mode is used on the T7906E, the ADC and DAC interfaces can then not be used.

JTAG interface

For testing purposes a standard IEEE 1149.1 interface is provided. It supports the JTAG functions Bypass, Extest, Sample/Preload, All-Tristate and IDCode.

Programming the T7906E

Programming the T7906E internal registers is done via a simple protocol over the IEEE-1355 link or directly via the host interface. The link protocol consists of a command byte and, if necessary, one or more data bytes.

All internal registers are 8-bit wide addressable. Two commands (read and write) suffice to access all registers of the T7906E.

The T7906E provides **registers** and **ports**; a register contains exactly one byte (read / write), whereas a port (e.g. a FIFO interface) behaves like a FIFO, meaning that multiple data bytes can be read or written from/to the port.

The ports of the T7906E such as the FIFO, UART, ADC and RAM interface are accessed by a read/write command to the corresponding port address. In the case of FIFO, Host, UART and memory interface, a packet oriented access is also possible (meaning transferring multiple data bytes with a single command).

The read/write selection of a command is done by setting bit7 (msb) of the first byte to one (read) or zero (write).

Signal Description

This section describes the signals of the T7906E. Groups of signals represent busses where the highest number is the MSB.

Signal	Direction	Description	max. output load	Signal
			[mA]	[pF]
HSEL*	I	when low, the external host selects the T7906E host interface		
HWRnRD	I	host interface write/read signal if HWRnRD is high during HSEL* low, the host writes data to the address register or to the T7906E registers. if HWRnRD is low during HSEL* low, the host reads data from the address register or the T7906E registers.		
HDATnADR	I	host interface data/address signal if HDATnADR is high during read, the host reads/writes data from/to the internal T7906E (data) registers. if HDATnADR is low during read, the host reads/writes address from/to the address register.		
HDATA(7:0)	I/O	T7906E data bus. This data lines will be used to access the T7906E registers. HDATA(7:0) can also be used as GPIO(2), if Host interface is disabled.	3	50
HINTR*	O	host interrupt request line	3	50
TMR1_CLK	I	timer1 clock (max. 12.5 MHz)		
TMR1_EXP	O	timer1 expired. Asserted for one cycle if the value of counter1 is equal to the content of register TPERIOD1(3:0).	3	50

Signal	Direction	Description	max. output load	Signal
			[mA]	[pF]
TMR2_CLK	I	timer2 clock (max. 12.5 MHz)		
TMR2_EXP.	O	timer2 expired. Asserted for one cycle if the value of counter2 is equal to the content of register TPERIOD2(3:0)	3	50
RxD1	I	receive data to UART1		
TxD1	O	transmit data from UART1	3	50
LDI	I	Link Data Input		
LSI	I	Link Strobe Input		
LDO	O	Link Data Output	12	25
LSO	O	Link Strobe Output	12	25
DATA(15:0)	I/O	common T7906E data bus	3	25
GPIO(7:0)	I/O	General purpose input/output lines.	3	25
IOB(27:0)	I/O	Control bus. The T7906E controls the connected interface via these lines. The function of each control signal is described in a separate table.	see note (1)	25
TRST*	I	Test Reset. Resets the test state machine.		
TCK	I	Test Clock. Provides an asynchronous clock for JTAG boundary scan		
TMS	I	Test Mode Select. Used to control the test state machine. This input should be left unconnected or tied to ground during normal operation!		
TDI	I	Test Data Input. Provides serial data for the boundary scan logic		
TDO	O/Z	Test Data Output. Serial scan output of the boundary scan path	3	50
RESET*	I	T7906E Reset. Sets the T7906E to a known state. This input must be asserted (low) at power-up. The minimum width of RESET low is 2 cycles when CLK is running		
CLK	I	External clock input to T7906E (max. 5 MHz)		
PLLOUT	O	Output of internal PLL. Used to connect a network of external RC devices		
VCC		Power Supply		
GND		Ground		

Note: 1. IOB15-0, IOB21-18: 6 mA
IOB17-16: 8mA
IOB24-22: 3mA
IOB27-25: input only

All inputs have an internal pull-up resistor, with the following exceptions, which have an internal pull-down resistor: LDI, LSI, TRST*, TMS.

IOB Control Bus

The allocation of the I/O busses is shown in the table below:

Signal	Function	Signal	Function	Signal	Function
	RAM Interface	I/O	ADC/DAC/FIFO Interface	I/O	GPIO
IOB[7:0]	RAM_ADDR[7:0]	O	ADC_ADDR[7:0]	O	GPIO1[7:0]
IOB8	RAM_ADDR8	O	ADC_CS*	O	
IOB9	RAM_ADDR9	O	ADC_R/C*	O	
IOB10	RAM_ADDR10	O	DAC_WR*	O	
IOB11	RAM_ADDR11	O	DAC_ADDR0	O	
IOB12	RAM_ADDR12	O	DAC_ADDR1	O	
IOB13	RAM_ADDR13	O	DAC_ADDR2	O	
IOB14	RAM_ADDR14	O	FIFO_TRM_EOP_ACK	O	
IOB15	RAM_ADDR15	O	FIFO_RCV_PAR	O	
IOB16	RAM_WR*	O	FIFO_RCV_EOP1	O	
IOB17	RAM_RD*	O	FIFO_RCV_EOP2	O	
IOB18	RAM_CS0*	O	FIFO_RD*	B	
IOB19	RAM_CS1*	O	FIDO_WR*	B	
IOB20	RAM_CS2*	O	FIFO_EMPTY*	B	
IOB21	RAM_CS3*	O	FIFO_FULL*	B	
IOB22	RAM_TEST	O	ADC:_RDY	I	
IOB23	RAM_ TRM_RDY	O	ADC_TRIG	I	
IOB24	RAM_RCV_RDY	O	FIFO_TRM_EOP1	I	
IOB25	RAM_BUS_REQ*	I	FIFO_TRM_EOP2	I	
IOB26	RAM_START_TRM	I	FIFO_RCV_EOP_ACK	I	
IOB27	RAM_START_RCV	I	FIFO_TRM_PAR	I	

GPIO Signals

The pins GPIO0 to GPIO7 are either mapped on register GPIO0 (0x63 / 0x64) or miscellaneous I/O signals, depending on the register settings as shown in the table below:

Pin	Mapped to	I/O	Register
GPIO0	RTS1*UART1	O	UART1_CTRL (0x59): D7
GPIO1	CTS1*UART1	I	UART1_CTRL (0x59): D 7
GPIO2	EXT_IREQ0*	I	IFCONF (0x01): D6
GPIO3	EXT_IREQ1*	I	IFCONF (0x01): D 6
GPIO4	TxD2UART2	O	IFCONF (0x01): D7
GPIO5	RxD2UART2	I	IFCONF (0x01): D7
GPIO6	RTS2*UART2	O	UART2_CTRL (0x72): D7
GPIO7	CTS2*UART2	I	UART2_CTRL (0x72): D7

ELECTRICAL Specifications

This data is given for information only. For guaranteed values refer to Atmelk procurement specifications.

Table 1. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0,5 to +7	V
I/O Voltage		-0,5 to V_{cc}+0,5	V
Operating Temperature Range (Ambient)	T_A	-55 to +125	°C
Junction Temperature	T_J	T_j < TA+20	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Thermal Resistance	R_{thje}	1	°C/W
	R_{thja}	35	

Stresses above those listed may cause permanent damage to the device.

DC Electrical Characteristics

Table 2. DC Characteristics
Specified at VCC = + 5 V ± 10%

Parameter	Symbol	Min.	Max.	Unit	Conditions
Operating Voltage	V_{CC}	4,5	5,5	V	
Input HIGH Voltage (TTL)	V_{IH}	2,0		V	
Input LOW Voltage (TTL)	V_{IL}		0,8	V	
Output HIGH Voltage	V_{OH}	2,4		V	max. output current (1)
Output LOW Voltage	V_{OL}		0,4	V	max. output current (1)
Output Short circuit current	I_{OS}		160 130	mA mA	V_{OUT} = VCC V_{OUT} = GND

Note: see also the signal description in section 4.

Power Consumption

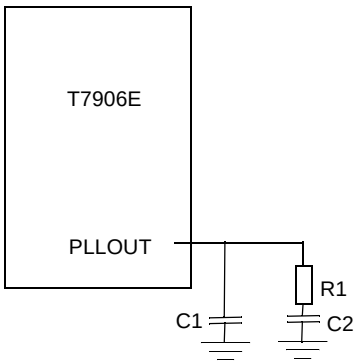
Although specified for TTL outputs, all T7906E outputs are CMOS compatible and will drive VCC and GND assuming no DC loads.

The max. power consumption figures (at 5,5V, -55×C) are:

Operating Mode	Symbol	Max.	Unit
at Reset	I	15	mA
in Idle	I	50	mA
operating	I	80	mA

PLL-Filter

The pin PLLOUT should be connected as shown below:



- R1 = 249_ ± 5%, ¼W
- C1 = 1nF, ± 5%, 200V
- C2 = 15nF, ± 5%, 200V

Power and Ground Guidelines

To achieve its fast cycle time, the T7906E is designed with high speed drivers on output pins. Large peak currents may pass through a circuit board's ground and power lines, especially when many output drivers are simultaneously charging or discharging their load capacitances. These transient currents can cause disturbances on the power and ground lines. To minimize these effects, the T7906E provides separate supply pins for its internal logic and for its external drivers.

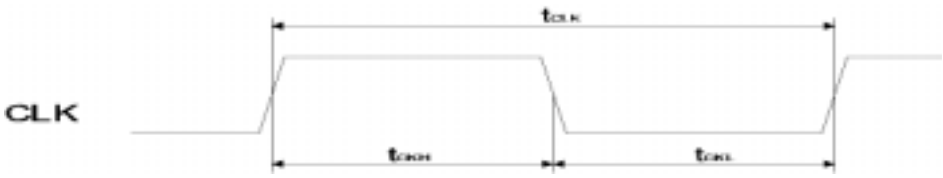
All GND pins should have a low impedance path to ground. A ground plane is required in T7906E systems to reduce this impedance, minimizing noise.

The VCC pins should be bypassed to the ground plane using 8 high-frequency capacitors (0.1 mF ceramic). Keep each capacitor's lead and trace length to the pins as short as possible. This low inductive path provides the T7906E with the peak currents required when its output drivers switch. The capacitors' ground leads should also be short and connect directly to the ground plane. This provides a low impedance return path for the load capacitance of the T7906E output drivers.

The following pins must have a capacitor: 1, 4, 16, 27, 56, 61, 88 and 99.

Timing Parameters

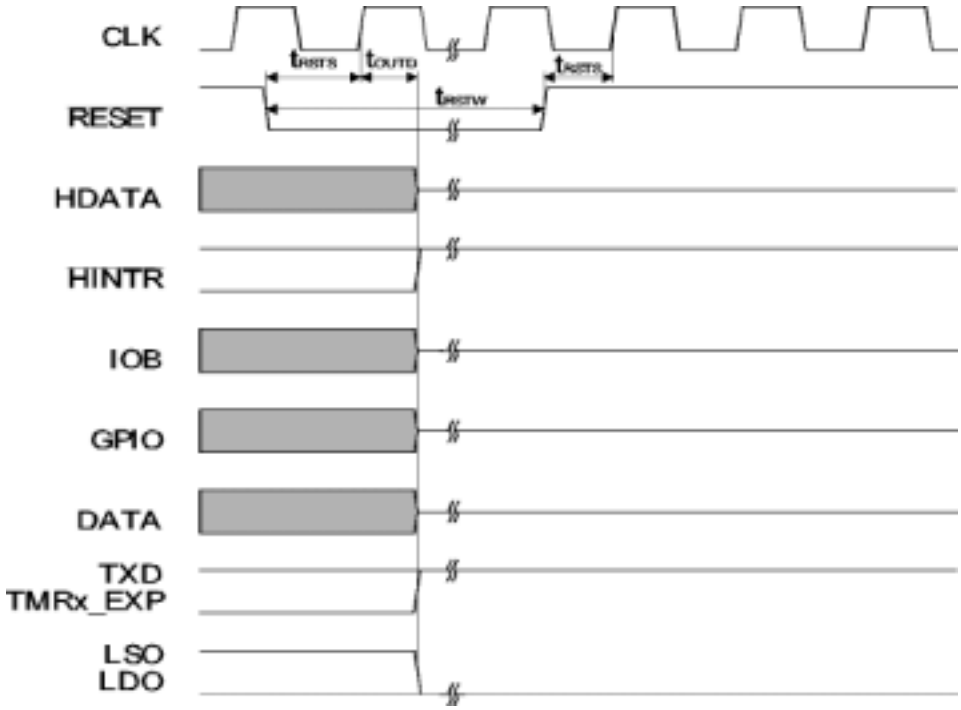
Clock



Description	Symbol	Min.	Max.	Unit
CLK period	t_{CLK}	1)	1)	ns
CLK width high	t_{CLKH}	80	120	ns
CLK width low	t_{CLKL}	80	120	ns

Note: 1) Nominal 5MHz

Reset

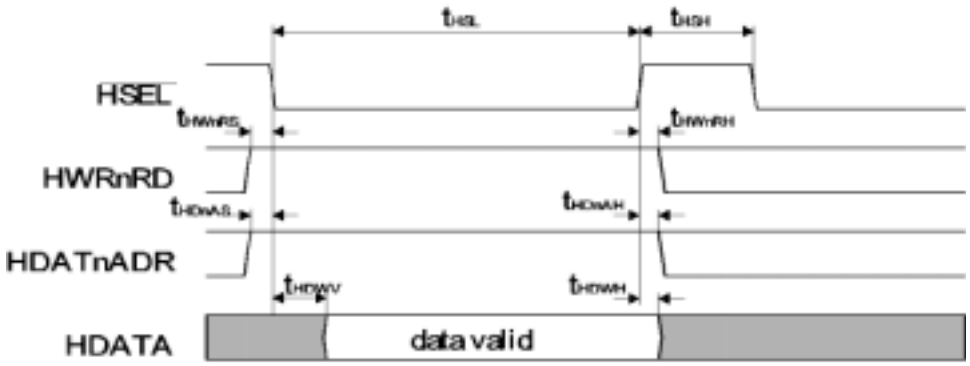


Description	Symbol	Min.	Max.	Unit
RESET* setup before CLK high	t_{RSTS}	10		ns
RESET* low pulse width	t_{RSTW}	$2*t_{CLK}$		ns
Output disable after CLK high	t_{OUTD}		38	ns

Host write address

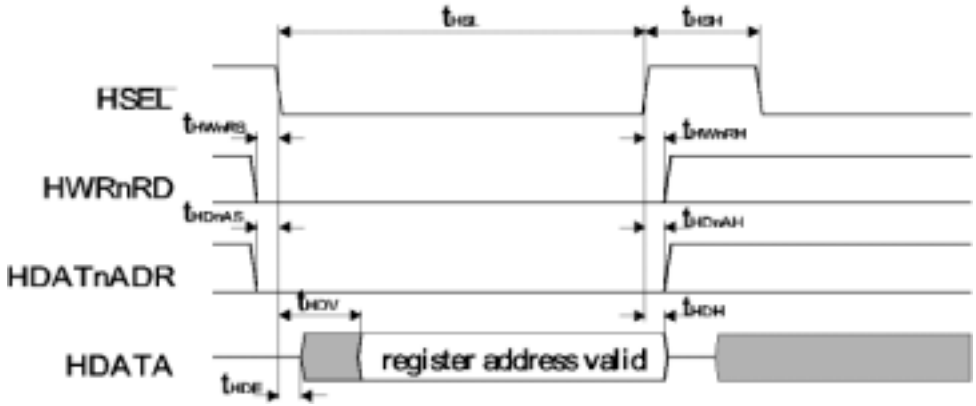
Description	Symbol	Min.	Max.	Unit
HSEL* active low pulse width	t_{HSL}	150		ns
HSEL* inactive high pulse width	t_{HSH}	60		ns
HWRnRD setup before HSEL* active low	t_{HWnRS}	5		ns
HDATnADR setup before HSEL* active low	t_{HWnRH}	5		ns
HWRnRD hold after HSEL* inactive high	t_{HWnRH}	0		ns
HDATnADR hold after HSEL* inactive high	t_{HDnAH}	0		ns
HDATA valid after HSEL active low and HWRnRD high	t_{HDWV}		25	ns
HDATA hold after HSEL inactive high	t_{HDWH}	0		ns

Host write data



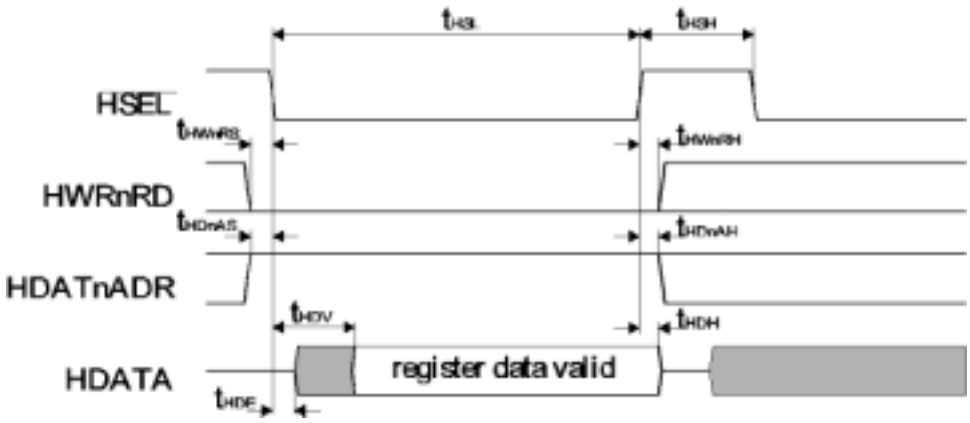
Description	Symbol	Min.	Max.	Unit
HSEL* active low pulse width	t_{HSL}	150		ns
HSEL* inactive high pulse width	t_{HSH}	60		ns
HWRnRD setup before HSEL* active low	t_{HWnRS}	5		ns
HDATnADR setup before HSEL* active low	t_{HWnRH}	5		ns
HWRnRD hold after HSEL* inactive high	t_{HWnRH}	0		ns
HDATnADR hold after HSEL* inactive high	t_{HDnAH}	0		ns
HDATA valid after HSEL active low and HWRnRD high	t_{HDWV}		25	ns
HDATA hold after HSEL inactive high	t_{HDWH}	0		ns

Host read address



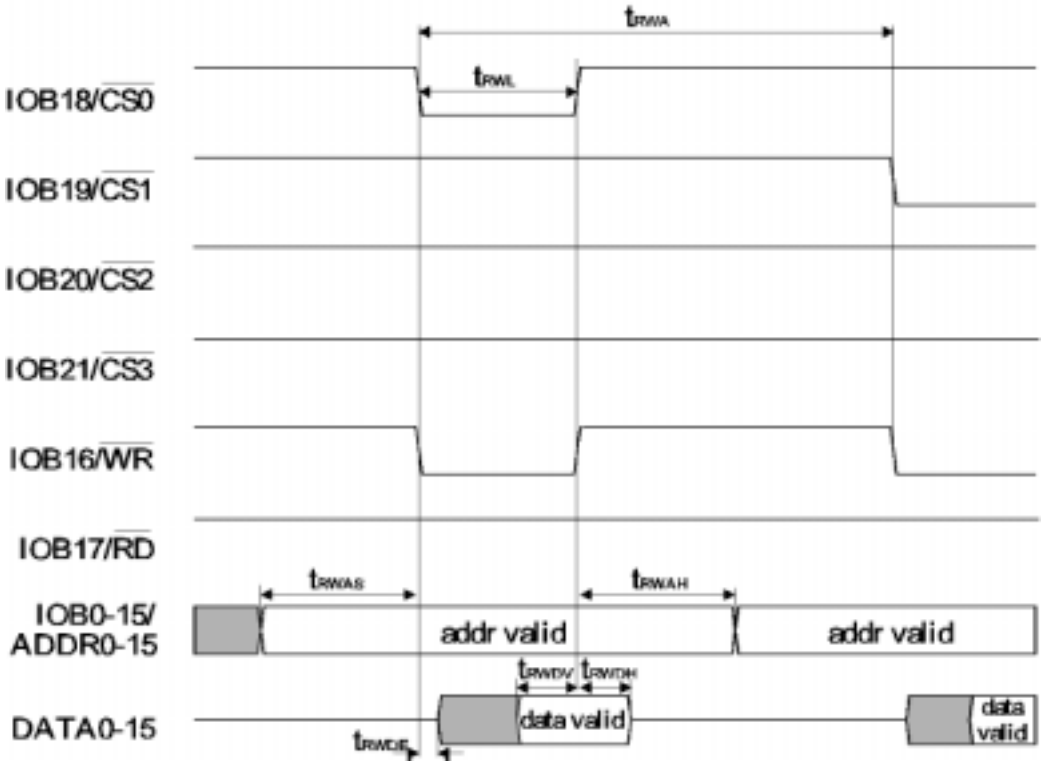
Description	Symbol	Min.	Max.	Unit
HSEL* active low pulse width	t_{HSL}	150		ns
HSEL* inactive high pulse width	t_{HSH}	60		ns
HWRnRD setup before HSEL* active low	t_{HWnRS}	5		ns
HDATnADR setup before HSEL* active low	t_{HWnRH}	5		ns
HWRnRD hold after HSEL* inactive high	t_{HWnRH}	0		ns
HDATnADR hold after HSEL* inactive high	t_{HDnAH}	0		ns
HDATA enable after HSEL* active low and HWRnRD low	t_{HDE}	4	18	ns
HDATA valid after HSEL* active low and HWRnRD low	t_{HDV}		125	ns
HDATA hold after HSEL* inactive high	t_{HDH}	4	18	ns

Host read data



Description	Symbol	Min.	Max.	Unit
HSEL* active low pulse width	t_{HSL}	150		ns
HSEL* inactive high pulse width	t_{HSH}	60		ns
HWRnRD setup before HSEL* active low	t_{HWnRS}	5		ns
HDATnADR setup before HSEL* active low	t_{HWnRH}	5		ns
HWRnRD hold after HSEL* inactive high	t_{HWnRH}	0		ns
HDATnADR hold after HSEL* inactive high	t_{HDnAH}	0		ns
HDATA enable after HSEL* active low and HWRnRD low	t_{HDE}	4	18	ns
HDATA valid after HSEL* active low and HWRnRD low	t_{HDV}		125	ns
HDATA hold after HSEL* inactive high	t_{HDH}	4	18	ns

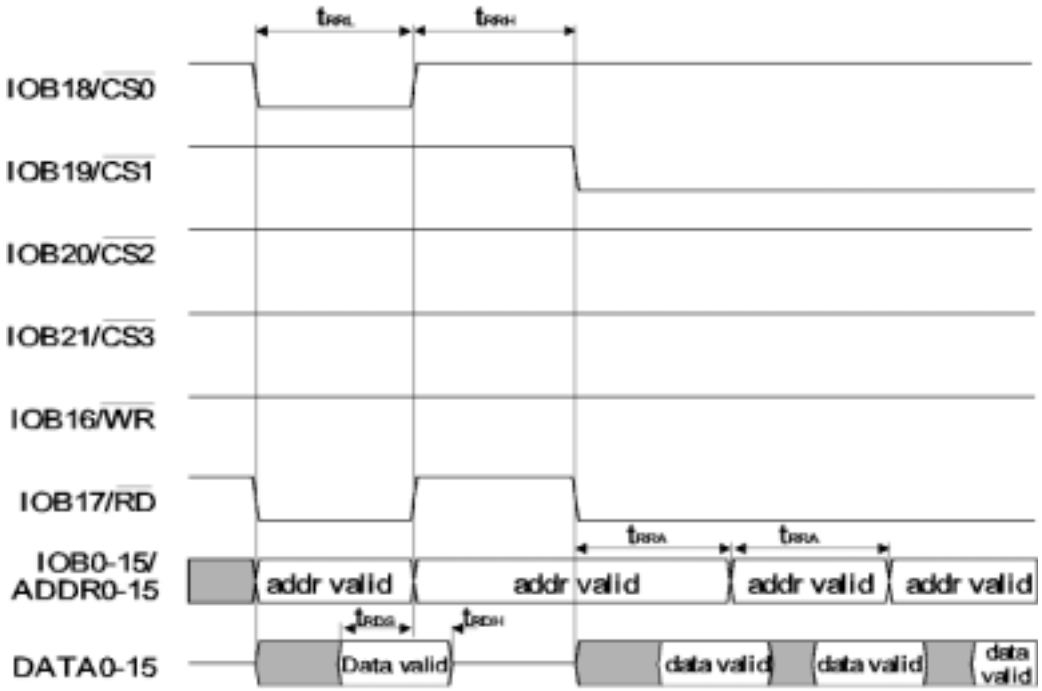
RAM interface write



Description	Symbol	Min.	Max.	Unit
RAM I/F write access time	t_{RWA}	120	120+ws[1)]*40	ns
CS0-3*, WR* active low pulse width	t_{RWL}	40+ws[1)]*40	42+ws[1)]*40	ns
Address ADDR0-15 valid before CS0*, WR* active low	t_{RWAS}	38	42	ns
Address ADDR0-15 hold after CS0-3*, WR* inactive high	t_{RWAH}	38	42	ns
DATA0-15 enable after CS0-3*, WR* active low	t_{RWDE}	0	6	ns
DATA0-15 valid before CS0-3*, WR* inactive high	t_{RWDV}	32		ns
DATA0-15 hold after CS0-3*, WR* inactive high	t_{RWDH}	20	26	ns

Note: ws = wait states (0 - 7)

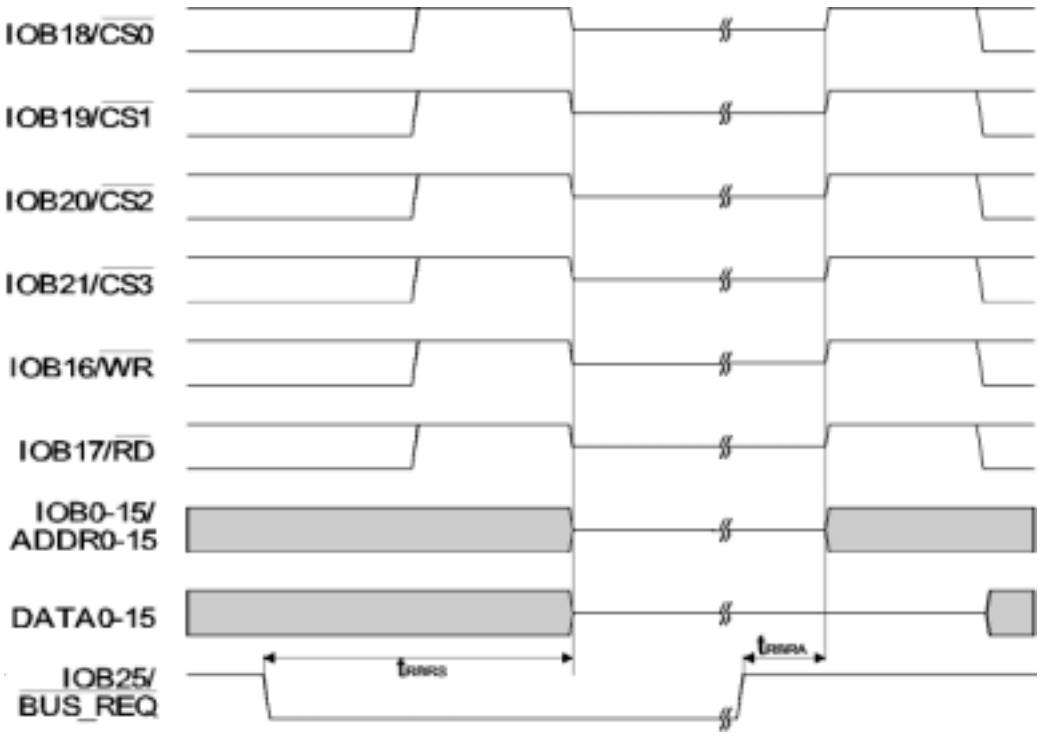
RAM interface read



Description	Symbol	Min.	Max.	Unit
CS0-3*, WR*, RD* and ADDR valid active low pulse width	t_{RRL}	40+ws[1)]*40	42+ws[1)]*40	ns
CS0-3*, WR*, RD* and ADDR valid inactive high pulse width	t_{RRH}	38	40	ns
ADDRESS change[2)]	t_{RRA}	40+ws[1)]*40	42+ws[1)]*40	ns
DATA0-15 setup before CS0-3*, RD* high or new address on ADDR0-15 valid	t_{RDS}	14		ns
DATA hold after CS0-3*, RD* high or new address on ADDR0-15	t_{RDH}	0	40	ns

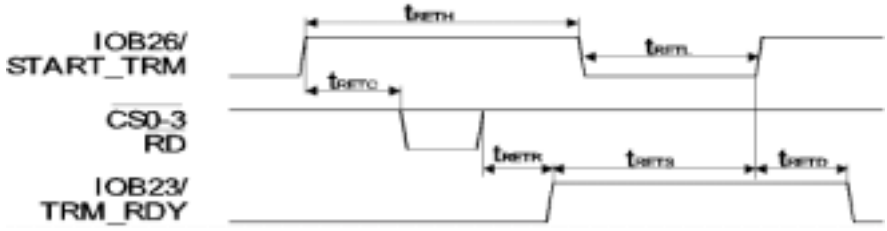
Notes: 1. ws = wait states (0 - 7)
2. Internal clock runs at 25 MHz, ticlk = 40 ns

RAM interface external bus request



Description	Symbol	Min.	Max.	Unit
CS0-3*, WR*, RD*, ADDR0-15 and DATA0-15 disable after BUS_REQ* active low	t_{RBRS}	40	160	ns
CS0-3*, WR*, RD*, ADDR0-15 and DATA0-15 enable after BUS_REQ inactive high	t_{RBRA}	20	65	ns

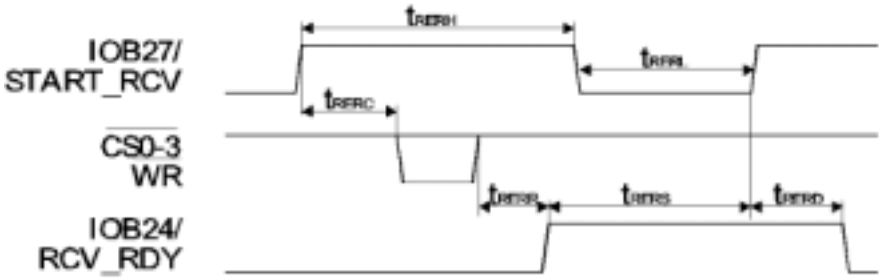
RAM interface external control read



Description	Symbol	Min.	Max.	Unit
START_TRM high active pulse width	t_{RETH}	47		ns
START_TRM low inactive pulse width	t_{RETL}	47		ns
first read access (CS0-3* / RD* low active) after START_TRM high	t_{RETC}	120	1)	ns
TRM_RDY (transmit ready) high active after the last read from memory	t_{RETR}	160	1)	ns
time between the rising edge of TRM_RDY and the next start (rising edge from START_TRM)	t_{RETS}	0		ns
TRM_RDY hold after START_TRM high	t_{RETD}		170	ns

Note: 1) depends on:
- data bandwidth over the IEEE-1355 link
- simultaneous read from the memory with wait states

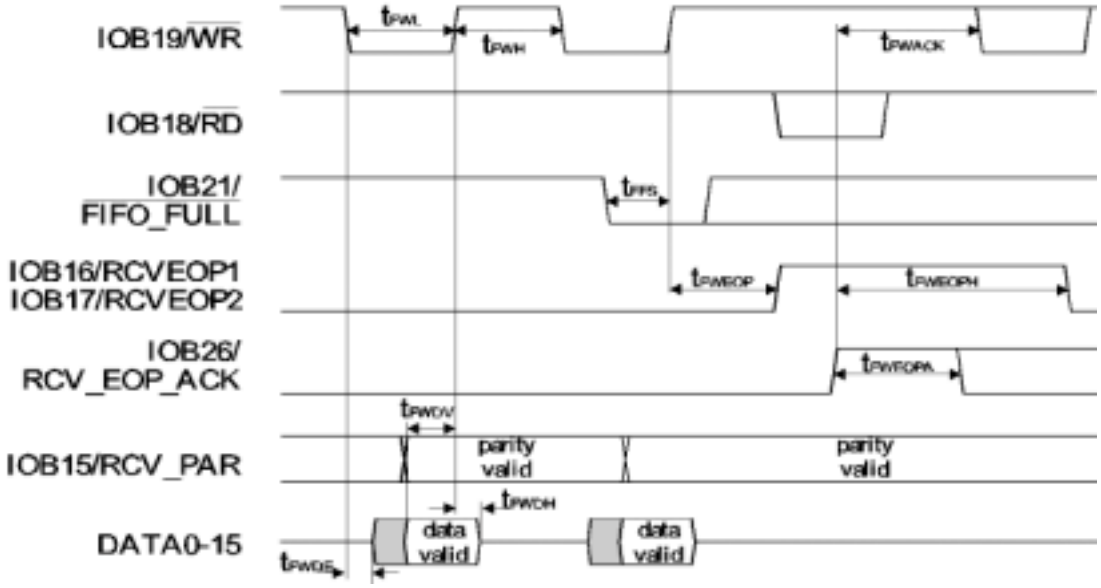
RAM interface external control write



Description	Symbol	Min.	Max.	Unit
START_RCV high active pulse width	t_{RERH}	47		ns
START_RCV low inactive pulse width	t_{RERL}	47		ns
first write access (CS0-3* / WR* low active) after START_RCV high	t_{RERC}	120	1)	ns
RCV_RDY (receive ready) high inactive after the last write to memory	t_{RERR}	160	170	ns
time between the rising edge of RCV_RDY and the next start (rising edge from START_RCV)	t_{RERS}	0		ns
RCV_RDY hold after START_RCV high	t_{RERD}		170	ns

Note: 1) depends on
- data bandwidth over the IEEE-1355 link
- simultaneous write to the memory with wait states
- internal write to fifo full

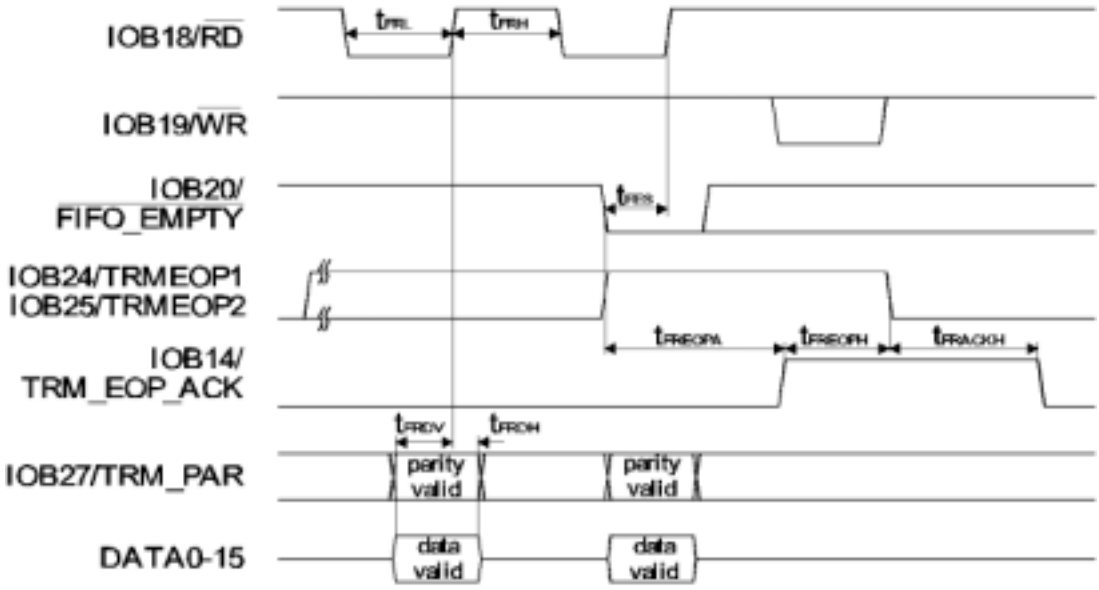
FIFO interface write



Description	Symbol	Min.	Max.	Unit
WR* active low pulse width	t_{FWL}	40+ws[1)]*40	42+ws[1)]*40	ns
WR* inactive high pulse width	t_{FWH}	38	40	ns
WR* active low after RCV_EOP_ACK high	t_{FWACK}	120		ns
FIFO_FULL* setup before WR* high	t_{FFS}	8		ns
RCVEOP1, RCVEOP2 high after last write and WR* high	t_{FWEOP}	40	2)	ns
RCV_EOP_ACK active high pulse width	t_{FWEOPA}	49		ns
RCVEOP1, RCVEOP2 low after RCV_EOP_ACK high	t_{FWEOPH}		128	ns
DATA0-7 enable after WR* low	t_{FWDE}	0	6	ns
DATA0-7 valid before WR* high	t_{FWDV}	32		ns
DATA0-7 hold after WR* high	t_{FWDH}	2		ns

Notes: 1. ws = wait states (0 - 7)
2. depends on:
- data bandwidth over the IEEE-1355 link

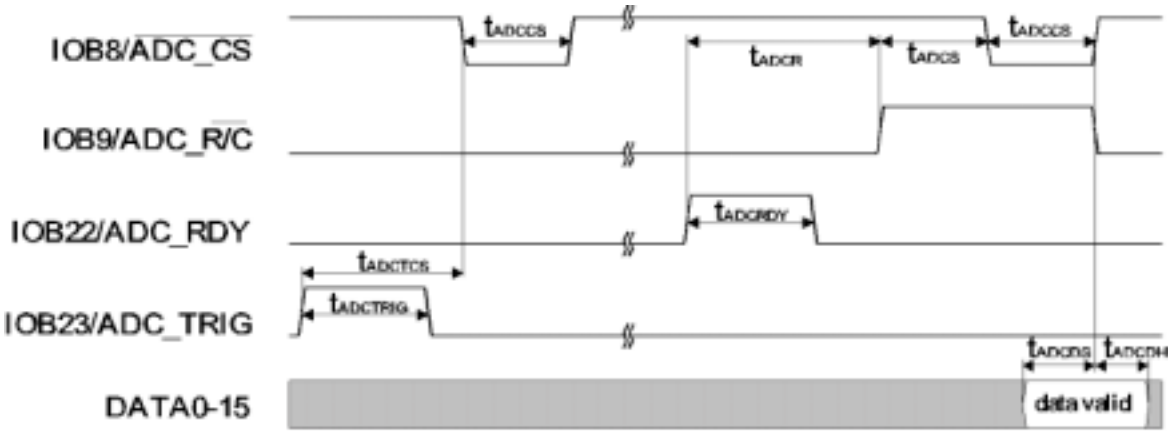
FIFO interface read



Description	Symbol	Min.	Max.	Unit
RD* active low pulse width	t_{FRL}	40+ws[1)]*40	42+ws[1)]*40	ns
RD* inactive high pulse width	t_{FRH}	38	40	ns
FIFO_EMPTY* setup before RD* high	t_{FES}	8		ns
TRM_EOP_ACKnowledge active high after TRMEOP1, TRMEOP2 high AND FIFO_EMPTY active low	t_{FREOPA}	160	2)	ns
TRMEOP1, TRMEOP2 hold after TRM_EOP_ACK high	t_{FREOPH}	0		ns
TRM_EOP_ACK hold after TRMEOP1, TRMEOP2 low	t_{FRACKH}	122	128	ns
DATA0-7 setup before RD* inactive high	t_{FRDV}	9		ns
DATA0-7 hold after RD* inactive high	t_{FRDH}	0		ns

Notes: 1. ws = wait states (0 - 7)
2. depends on:
- data bandwidth over the IEEE-1355 link

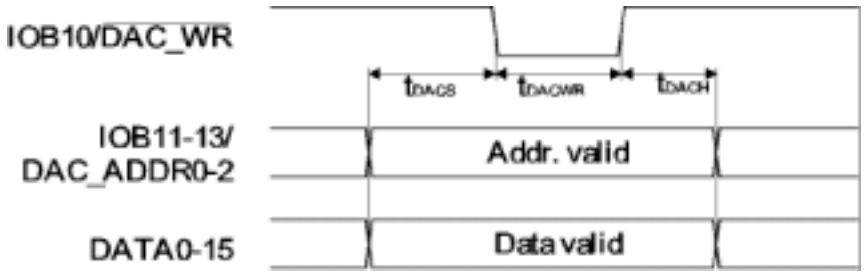
ADC interface



Description	Symbol	Min.	Max.	Unit
ADC_CS* low pulse width	t_{ADCCS}	40+ws*40	42+ws*40	ns
ADC_RDY high pulse width	t_{ADCRDY}	45		ns
ADC_RDY high to ADC_R/C* high	t_{ADCR}	200		ns
ADC_R/C* setup before ADC_CS* low	t_{ADCS}	40+ws*40	42+ws*40	ns
ADC_TRIG high pulse width	$t_{ADCTRIG}$	45		ns
ADC_TRIG high to ADC_CS* low	t_{ADCTCS}	200+ws*40		ns
DATA 0-15 setup to ADC_CS* high	t_{ADCDS}	19		ns
DATA 0-15 hold after ADC_CS* high	t_{ADCDH}	0		ns

Note: ws = wait states (0 to 15)

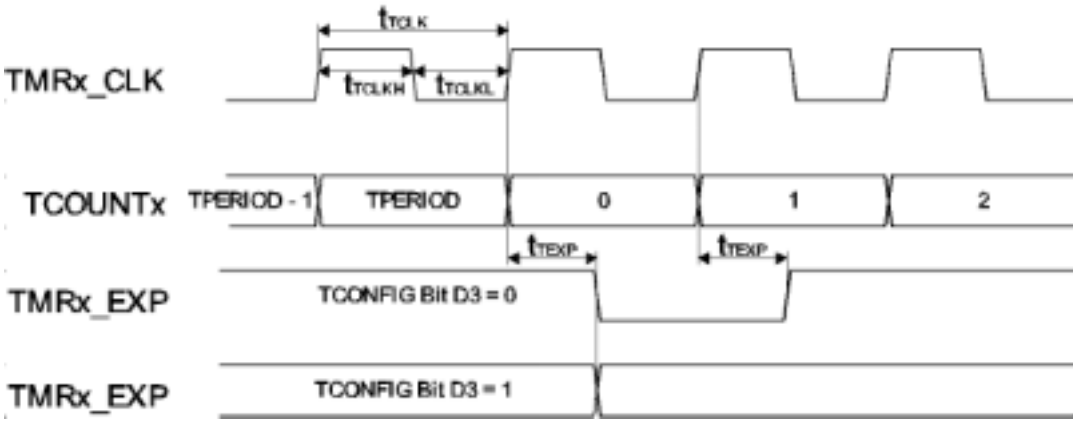
DAC interface



Description	Symbol	Min.	Max.	Unit
DAC_ADDR 0-2 and DATA 0-15 setup before DAC_WR* low	t_{DACS}	40+ws*40	42+ws*40	ns
DAC_WR* low pulse width	t_{DACWR}	40+ws*40	42+ws*40	ns
DATA 0-15 hold after DAC_WR* high	t_{DACH}	38	42	ns

Note: ws = wait states (0 to 15)

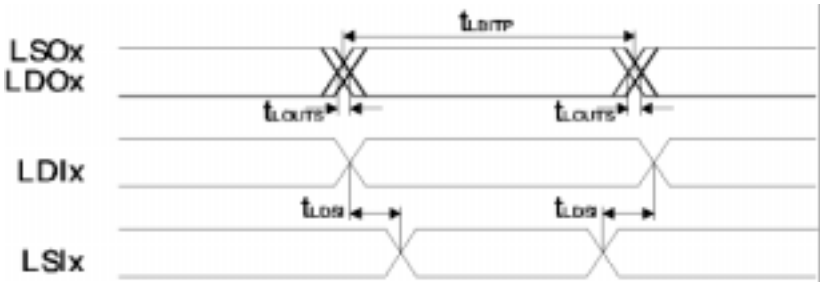
Timer



Description	Symbol	Min.	Max.	Unit
TMRx_CLK period	t_{TCLK}	80		ns
TMRx_CLK width high	t_{TCLKH}	35	45	ns
TMRx_CLK width low	t_{TCLKL}	35	45	ns
TMRx_EXP low / high after TMRx_CLK high	t_{TEXP}	9	24	ns

External Interrupt

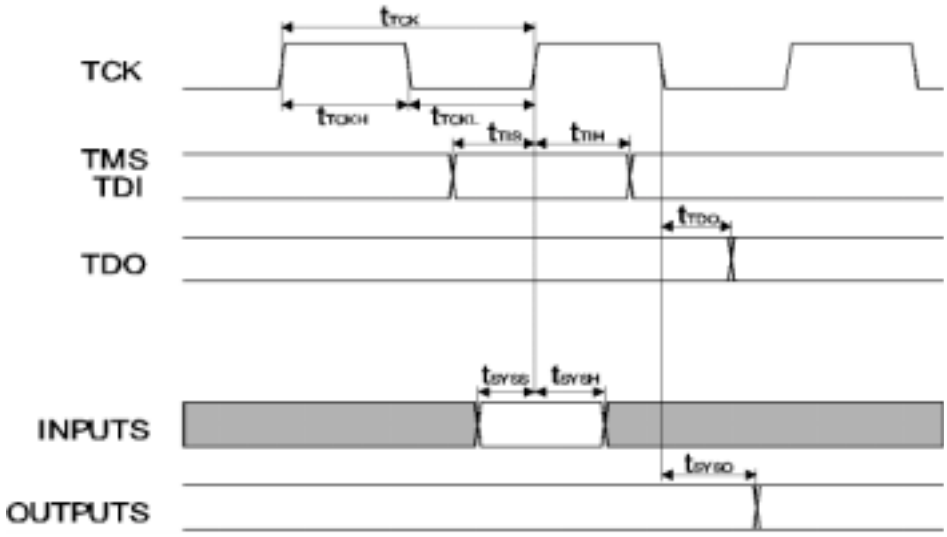
Description	Symbol	Min.	Max.	Unit
EXT_IREQx low pulse width	t_{EXINT}	10		ns



Description	Symbol	Min.	Max.	Unit
Bit Period	t_{LBITP}	4		ns
LDOx, LSOx output skew [1)]	t_{LOUTS}		0.5	ns
Data/Strobe edge separation	t_{LDSI}	1		ns

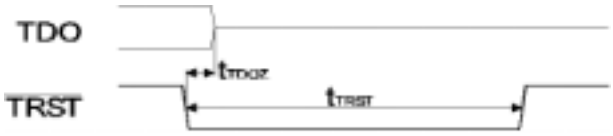
Note: 1) Output skew includes jitter

Test Port (JTAG)



Description	Symbol	Min.	Max.	Unit
TCK period	t_{TCK}	100		ns
TCK width high	t_{TCKH}	40		ns
TCK width low	t_{TCKL}	40		ns
TMS, TDI setup before TCK high	t_{TIS}	8		ns
TMS, TDI hold after TCK high	t_{TIH}	8		
TDO delay after TCK low	t_{TDO}		17	
SMCS Inputs setup before TCK high	t_{SYSS}	8		ns
SMCS Inputs hold after TCK high	t_{SYSM}	8		ns
SMCS Outputs delay after TCK low	t_{SYSO}		27	ns

Test Port Reset

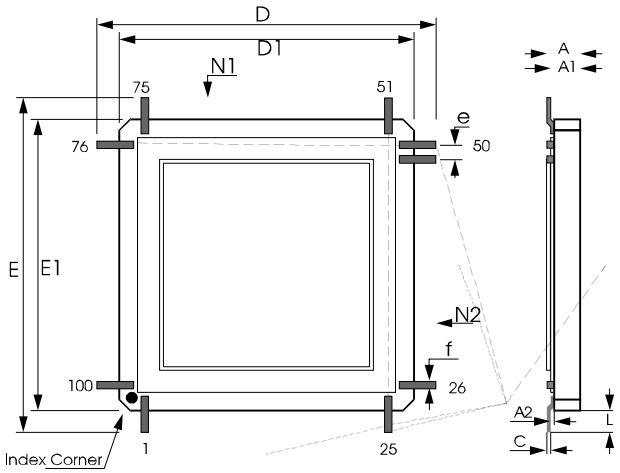


Description	Symbol	Min.	Max.	Unit
TDO disable after TRST* active low	t_{TDOZ}		5	ns
TRST* pulse width	t_{TRST}	2 * t_{TCK}		ns

Mechanical Data

Package Dimensions

Figure 3. 100-Pin Ceramic Quad Flat Pack (MQFPF)



Symbol	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.21	2.67	0.087	0.105
C	0.15	0.2	0.006	0.008
D	3 1.8	32.8	1.252	1.291
D1	18.8	19.3	0.74	0.76
E	31.8	32.8	1.252	1.45
E1	18.8	19.3	0.74	0.76
e	0.635 typ	0.025 typ	e	0.635 typ
f	0.254 ref	0.010 ref	f	0.254 ref
A1	1.83	2.24	0.072	0.088
A2	0.203 ref	0.008 ref	A2	0.203 ref
L	6.5	6.75	0.256	0.266
N1, N2	25		25	

Pin Assignment

The table below lists the pins and their function.

Pin Number	Name	Pin Number	Name	Pin Number	Name
1	VCC	35	IOB16	69	GPIO2
2	GND	36	IOB17	70	GPIO3
3	GND	37	IOB18	71	GPIO4
4	VCC	38	IOB19	72	GPIO5
5	LD0	39	IOB20	73	GPIO6
6	LS0	40	IOB21	74	GPIO7
7	LDI	41	IOB22	75	TMR1_CLK
8	LSI	42	IOB23	76	TMR2_CLK
9	GND	43	IOB24	77	RxD1
10	TCK	44	IOB25	78	TMR1_EXP
11	TMS	45	IOB26	79	TMR2_EXP
12	TDI	46	IOB27	80	TxD1
13	TRST*	47	DATA0	81	HDATA0
14	TD0	48	DATA1	82	HDATA1
15	GND	49	DATA2	83	HDATA2
16	VCC	50	DATA3	84	HDATA3
17	IOB0	51	DATA4	85	HDATA4
18	IOB1	52	DATA5	86	HDATA5
19	IOB2	53	DATA6	87	HDATA6
20	IOB3	54	DATA7	88	VCC
21	IOB4	55	DATA8	89	GND
22	IOB5	56	VCC	90	HDATA7
23	IOB6	57	GND	91	HDATNADR
24	IOB7	58	DATA9	92	HSEL*
25	IOB8	59	DATA10	93	HWRNRD
26	IOB9	60	DATA11	94	HINTR*
27	VCC	61	VCC	95	RESET*
28	GND	62	GND	96	CLK
29	IOB10	63	DATA12	97	GND
30	IOB11	64	DATA13	98	GND
31	IOB12	65	DATA14	99	VCC
32	IOB13	66	DATA15	100	PLLOUT
33	IOB14	67	GPIO0		
34	IOB15	68	GPIO1		

Glossary

BSDL Boundary Scan Description Language

CPU Central Processing Unit

DPRAM Dual-Port RAM

DSM Ds-link Macrocell

DSP Digital Signal Processor

EOP End Of Packet

GPIO General Purpose Input/Output

FIFO First In, First Out

HOCI Host Control Interface

HW Hardware

JTAG Joint Test Action Group

LSB Least Significant Bit (or Byte)

MSB Most Significant Bit (or Byte)

PLL Phase Locked Loop

SIC Simple Interprocessor Communication

SMCS Scalable Multichannel Communication Subsystem

UART Universal Asynchronous Receiver Transmitter

Ordering Information

Part-Number	Temperature Range	Package	Quality
T7906EKT-E	+25°C	MQFPF100	Engineering Samples
T7906EKT	-55° to +125°C	MQFPF100	MIL
T7906EKT/SC	-55° to +125°C	MQFPF100	SCC B
T7906EKT/SB	-55° to +125°C	MQFPF100	SCC C
T7906EKT/883*	-55° to +125°C	MQFPF100	MIL 883 B
T7906EKST/883*	-55° to +125°C	MQFPF100	MIL 883 S
T7906EKTMQ	-55° to +125°C	MQFPF100	QML Q
T7906EKTSV	-55° to +125°C	MQFPF100	QML V
T7906EDD-E	+25°C	Die	Engineering Samples
T7906EDDMQ	-55° to +125°C	Die	QML Q
T7906EDDSV	-55° to +125°C	Die	QML V

Note: (*)contact factory.

Appendix

```
-- BSDL for SMCSlite
-- Uses HP's BSDL format and compiles correctly using HP's
-- parser or compiler of JTAG Technologies

-- Author Paul Rastetter,  Astrium GmbH
-- Tel.: +49-89-607-25015, Fax: +49-89-607-28964
-- e-mail: paul.rastetter@astrium-space.com
-- date: 24-11-00

entity SMCSLITE is


  generic (PHYSICAL_PIN_MAP : string := "UNDEFINED");

  PORT (BYPPLL :   IN bit;
        CLK :      IN bit;
        HDATNADR : IN bit;
        HWRNRD :   IN bit;
        LDI :      IN bit;
        LSI :      IN bit;
        NHSEL :    IN bit;
        NRESET :   IN bit;
        TRST :     IN bit;
        RXD :      IN bit;
        TCK :      IN bit;
        TDI :      IN bit;
        TMR1_CLK : IN bit;
        TMR2_CLK : IN bit;
        TMS :      IN bit;
        iob25 :    IN bit;
        iob26 :    IN bit;
        iob27 :    IN bit;
        LDO :      OUT bit;
        LSO :      OUT bit;
        NHINTR :   OUT bit;
        TDO :      OUT bit;
        TMR1_EXP : OUT bit;
        TMR2_EXP : OUT bit;
        TXD :      OUT bit;
        IOB8 :     OUT bit;
        IOB9 :     OUT bit;
        iob10 :    OUT bit;
        iob11 :    OUT bit;
        iob12 :    OUT bit;
        iob13 :    OUT bit;
        iob14 :    OUT bit;
        iob15 :    OUT bit;
        iob16 :    OUT bit;
        iob17 :    OUT bit;
```

```
        DATA :     INOUT bit_vector(0 TO 15);
        GPIO :     INOUT bit_vector(0 TO 7);
        HDATA :    INOUT bit_vector(0 TO 7);
        IOB0 :     INOUT bit;
        iob1 :     INOUT bit;
        iob2 :     INOUT bit;
        iob3 :     INOUT bit;
        iob4 :     INOUT bit;
        iob5 :     INOUT bit;
        iob6 :     INOUT bit;
        iob7 :     INOUT bit;
        iob18 :    INOUT bit;
        iob19 :    INOUT bit;
        iob20 :    INOUT bit;
        iob21 :    INOUT bit;

        iob22 :    INOUT bit;
        iob23 :    INOUT bit;
        iob24 :    INOUT bit;
        VDD :      linkage bit_vector(0 to 7);
        GND :      linkage bit_vector(0 to 7);
        NC :       linkage bit_vector(0 to 1) );


use STD_1149_1_1990.all;

attribute PIN_MAP of SMCSLITE : entity is PHYSICAL_PIN_MAP;

constant MCQFP_PACKAGE : PIN_MAP_STRING :=
   "LDO:      5," &
   "LSO:      6," &
   "LDI:      7," &
   "LSI:      8," &
   "TCK:     10," &
   "TMS:     11," &
   "TDI:     12," &
   "TRST:    13," &
   "TDO:     14," &
   "IOB0:    17," &
   "IOB1:    18," &
   "IOB2:    19," &
   "IOB3:    20," &
   "IOB4:    21," &
   "IOB5:    22," &
   "IOB6:    23," &
   "IOB7:    24," &
   "IOB8:    25," &
   "IOB9:    26," &
   "IOB10:   29," &
   "IOB11:   30," &
   "IOB12:   31," &
```

```
 "IOB13:   32," &
 "IOB14:   33," &
 "IOB15:   34," &
 "IOB16:   35," &
 "IOB17:   36," &
 "IOB18:   37," &
 "IOB19:   38," &
 "IOB20:   39," &
 "IOB21:   40," &
 "IOB22:   41," &
 "IOB23:   42," &
 "IOB24:   43," &
 "IOB25:   44," &
 "IOB26:   45," &
 "IOB27:   46," &
 "DATA:   (47,48,49,50,51,52,53,54,55,58,59,60,63,64,65,66)," &
 "GPIO:   (67,68,69,70,71,72,73,74)," &
 "TMR1_CLK:75," &
 "TMR2_CLK:76," &
 "RXD:     77," &
 "TMR1_EXP:78," &
 "TMR2_EXP:79," &
 "TXD:     80," &
 "HDATA:  (81,82,83,84,85,86,87,90)," &
 "HDATNADR:91," &
 "NHSEL:   92," &
 "HWRNRD:  93," &
 "NHINTR:  94," &
 "NRESET:   95," &
 "CLK:     96," &
 "BYPPLL:  97," &
 "VDD:    (1,4,16,27,56,61,88,99)," &
 "GND:    (2,3,15,28,57,62,89,98)," &

 "NC:     (9,100)";  -- for completeness: scan_en, pllout,


attribute TAP_SCAN_IN    of TDI :  signal is true;
attribute TAP_SCAN_MODE  of TMS :  signal is true;
attribute TAP_SCAN_OUT   of TDO :  signal is true;
attribute TAP_SCAN_RESET of TRST : signal is true;
attribute TAP_SCAN_CLOCK of TCK :  signal is (10.0e6, BOTH);


attribute INSTRUCTION_LENGTH of SMCSLITE : entity is 3;


attribute INSTRUCTION_OPCODE of SMCSLITE : entity is
    "BYPASS     (111,110,101,100)," &
    "EXTEST     (000)," &
    "SAMPLE     (001)," &
```

```
      "IDCODE     (010)," &
      "HIGHZ      (011)";


  attribute INSTRUCTION_CAPTURE of SMCSLITE : entity is
      "101";


  attribute INSTRUCTION_DISABLE of SMCSLITE : entity is
      "HIGHZ";


  attribute IDCODE_REGISTER of SMCSLITE : entity is
      "0001" &              -- Version
      "0101001101001100" &  -- Part number  534C = SL
      "00001011000" &       -- ID of manufacturer; MATRA MHS is 58 hex
      "1";                  -- required by IEEE Std 1149.1-1990 (LSB)


  attribute REGISTER_ACCESS of SMCSLITE : entity is
--      "BSREG (EXTEST, SAMPLE)," &
      "BOUNDARY (EXTEST, SAMPLE),"&
--      "IDREG (IDCODE)," &
      "BYPASS (BYPASS, HIGHZ)";
--      "BPREG (BYPASS, HIGHZ)";


  attribute BOUNDARY_CELLS of SMCSLITE : entity is
     "BC_1";
  -- BC_1: output, control; BC_1: input;


  attribute BOUNDARY_LENGTH of SMCSLITE : entity is 155;


  attribute BOUNDARY_REGISTER of SMCSLITE : entity is

--  num   cell  port       func   safe  [ccell  disval  rslt]
   "  0   (BC_1, LSI,       input,   X)," &
   "  1   (BC_1, LDI,       input,   X)," &
   "  2   (BC_1, LSO,       output2, X)," &
   "  3   (BC_1, LDO,       output2, X)," &
   "  4   (BC_1, BYPPLL,    input,   X)," &
   "  5   (BC_1, CLK,       input,   X)," &
   "  6   (BC_1, NRESET,    input,   X)," &
   "  7   (BC_1, NHINTR,    output2, X)," &  -- output2 for internal tristate
   "  8   (BC_1, HWRNRD,    input,   X)," &
   "  9   (BC_1, NHSEL,     input,   X)," &
   "  10  (BC_1, HDATNADR,  input,   X)," &
   "  11  (BC_1, *         , control, 0)," &  -- HOCI Data Output Enable7
```

```
" 12  (BC_1, HDATA(7),   output3, X, 11,    0,     Z)," &

" 13  (BC_1, HDATA(7),   input,   X)," &
" 14  (BC_1, *       , control, 0)," &  -- HOCI Data Output Enable6
" 15  (BC_1, HDATA(6),   output3, X, 14,    0,     Z)," &
" 16  (BC_1, HDATA(6),   input,   X)," &
" 17  (BC_1, *       , control, 0)," &  -- HOCI Data Output Enable5
" 18  (BC_1, HDATA(5),   output3, X, 17,    0,     Z)," &
" 19  (BC_1, HDATA(5),   input,   X)," &
" 20  (BC_1, *       , control, 0)," &  -- HOCI Data Output Enable4
" 21  (BC_1, HDATA(4),   output3, X, 20,    0,     Z)," &
" 22  (BC_1, HDATA(4),   input,   X)," &
" 23  (BC_1, *       , control, 0)," &  -- HOCI Data Output Enable3
" 24  (BC_1, HDATA(3),   output3, X, 23,    0,     Z)," &
" 25  (BC_1, HDATA(3),   input,   X)," &
" 26  (BC_1, *       , control, 0)," &  -- HOCI Data Output Enable2
" 27  (BC_1, HDATA(2),   output3, X, 26,    0,     Z)," &
" 28  (BC_1, HDATA(2),   input,   X)," &
" 29  (BC_1, *       , control, 0)," &  -- HOCI Data Output Enable1
" 30  (BC_1, HDATA(1),   output3, X, 29,    0,     Z)," &
" 31  (BC_1, HDATA(1),   input,   X)," &
" 32  (BC_1, *       , control, 0)," &  -- HOCI Data Output Enable0
" 33  (BC_1, HDATA(0),   output3, X, 32,    0,     Z)," &
" 34  (BC_1, HDATA(0),   input,   X)," &
" 35  (BC_1, TXD,        output2, X)," &  -- output2 for internal tristate
" 36  (BC_1, TMR2_EXP,   output2, X)," &  -- output2 for internal tristate
" 37  (BC_1, TMR1_EXP,   output2, X)," &  -- output2 for internal tristate
" 38  (BC_1, RXD,        input,   X)," &
" 39  (BC_1, TMR2_CLK,   input,   X)," &
" 40  (BC_1, TMR1_CLK,   input,   X)," &
" 41  (BC_1, *       , control, 0)," &  -- GPIO Output Enable7
" 42  (BC_1, GPIO(7),    output3, X, 41,    0,     Z)," &
" 43  (BC_1, GPIO(7),    input,   X)," &
" 44  (BC_1, *       , control, 0)," &  -- GPIO Output Enable6
" 45  (BC_1, GPIO(6),    output3, X, 44,    0,     Z)," &
" 46  (BC_1, GPIO(6),    input,   X)," &
" 47  (BC_1, *       , control, 0)," &  -- GPIO Output Enable5
" 48  (BC_1, GPIO(5),    output3, X, 47,    0,     Z)," &
" 49  (BC_1, GPIO(5),    input,   X)," &
" 50  (BC_1, *       , control, 0)," &  -- GPIO Output Enable4
" 51  (BC_1, GPIO(4),    output3, X, 50,    0,     Z)," &
" 52  (BC_1, GPIO(4),    input,   X)," &
" 53  (BC_1, *       , control, 0)," &  -- GPIO Output Enable3
" 54  (BC_1, GPIO(3),    output3, X, 53,    0,     Z)," &
" 55  (BC_1, GPIO(3),    input,   X)," &
" 56  (BC_1, *       , control, 0)," &  -- GPIO Output Enable2
" 57  (BC_1, GPIO(2),    output3, X, 56,    0,     Z)," &
" 58  (BC_1, GPIO(2),    input,   X)," &
" 59  (BC_1, *       , control, 0)," &  -- GPIO Output Enable1
" 60  (BC_1, GPIO(1),    output3, X, 59,    0,     Z)," &
" 61  (BC_1, GPIO(1),    input,   X)," &
" 62  (BC_1, *       , control, 0)," &  -- GPIO Output Enable0
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" 63  (BC_1, GPIO(0),    output3, X, 62,     0,      Z)," &
" 64  (BC_1, GPIO(0),    input,   X)," &
" 65  (BC_1, *         , control, 0)," &  -- DATA Output Enable
" 66  (BC_1, DATA(15),   output3, X, 65,     0,      Z)," &
" 67  (BC_1, DATA(15),   input,   X)," &
" 68  (BC_1, DATA(14),   output3, X, 65,     0,      Z)," &
" 69  (BC_1, DATA(14),   input,   X)," &
" 70  (BC_1, DATA(13),   output3, X, 65,     0,      Z)," &
" 71  (BC_1, DATA(13),   input,   X)," &
" 72  (BC_1, DATA(12),   output3, X, 65,     0,      Z)," &
" 73  (BC_1, DATA(12),   input,   X)," &
" 74  (BC_1, DATA(11),   output3, X, 65,     0,      Z)," &
" 75  (BC_1, DATA(11),   input,   X)," &
" 76  (BC_1, DATA(10),   output3, X, 65,     0,      Z)," &
" 77  (BC_1, DATA(10),   input,   X)," &
" 78  (BC_1, DATA(9),    output3, X, 65,     0,      Z)," &
" 79  (BC_1, DATA(9),    input,   X)," &
" 80  (BC_1, DATA(8),    output3, X, 65,     0,      Z)," &

" 81  (BC_1, DATA(8),    input,   X)," &
" 82  (BC_1, DATA(7),    output3, X, 65,     0,      Z)," &
" 83  (BC_1, DATA(7),    input,   X)," &
" 84  (BC_1, DATA(6),    output3, X, 65,     0,      Z)," &
" 85  (BC_1, DATA(6),    input,   X)," &
" 86  (BC_1, DATA(5),    output3, X, 65,     0,      Z)," &
" 87  (BC_1, DATA(5),    input,   X)," &
" 88  (BC_1, DATA(4),    output3, X, 65,     0,      Z)," &
" 89  (BC_1, DATA(4),    input,   X)," &
" 90  (BC_1, DATA(3),    output3, X, 65,     0,      Z)," &
" 91  (BC_1, DATA(3),    input,   X)," &
" 92  (BC_1, DATA(2),    output3, X, 65,     0,      Z)," &
" 93  (BC_1, DATA(2),    input,   X)," &
" 94  (BC_1, DATA(1),    output3, X, 65,     0,      Z)," &
" 95  (BC_1, DATA(1),    input,   X)," &
" 96  (BC_1, DATA(0),    output3, X, 65,     0,      Z)," &
" 97  (BC_1, DATA(0),    input,   X)," &
" 98  (BC_1, IOB27,      input,   X)," &
" 99  (BC_1, IOB26,      input,   X)," &
" 100 (BC_1, IOB25,      input,   X)," &
" 101 (BC_1, *         , control, 0)," &  -- IOB Output Enable
" 102 (BC_1, IOB24,      output3, X, 101,    0,      Z)," &
" 103 (BC_1, IOB24,      input,   X)," &
" 104 (BC_1, IOB23,      output3, X, 101,    0,      Z)," &
" 105 (BC_1, IOB23,      input,   X)," &
" 106 (BC_1, IOB22,      output3, X, 101,    0,      Z)," &
" 107 (BC_1, IOB22,      input,   X)," &
" 108 (BC_1, *         , control, 0)," &  -- IOB Output Enable
" 109 (BC_1, IOB21,      output3, X, 108,    0,      Z)," &
" 110 (BC_1, IOB21,      input,   X)," &
" 111 (BC_1, *         , control, 0)," &  -- IOB Output Enable
" 112 (BC_1, IOB20,      output3, X, 111,    0,      Z)," &
" 113 (BC_1, IOB20,      input,   X)," &
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  "  114 (BC_1, *        , control, 0)," &  -- IOB Output Enable
  "  115 (BC_1, IOB19,      output3, X, 114,    0,      Z)," &
  "  116 (BC_1, IOB19,      input,   X)," &
  "  117 (BC_1, *        , control, 0)," &  -- IOB Output Enable
  "  118 (BC_1, IOB18,      output3, X, 117,    0,      Z)," &
  "  119 (BC_1, IOB18,      input,   X)," &
  "  120 (BC_1, *        , control, 0)," &  -- IOB Output Enable
  "  121 (BC_1, IOB17,      output3, X, 120,    0,      Z)," &
  "  122 (BC_1, IOB16,      output3, X, 120,    0,      Z)," &
  "  123 (BC_1, IOB15,      output3, X, 120,    0,      Z)," &
  "  124 (BC_1, IOB14,      output3, X, 120,    0,      Z)," &
  "  125 (BC_1, IOB13,      output3, X, 120,    0,      Z)," &
  "  126 (BC_1, IOB12,      output3, X, 120,    0,      Z)," &
  "  127 (BC_1, IOB11,      output3, X, 120,    0,      Z)," &
  "  128 (BC_1, IOB10,      output3, X, 120,    0,      Z)," &
  "  129 (BC_1, IOB9,       output3, X, 120,    0,      Z)," &
  "  130 (BC_1, IOB8,       output3, X, 120,    0,      Z)," &
  "  131 (BC_1, *        , control, 0)," &  -- IOB Output Enable
  "  132 (BC_1, IOB7,       output3, X, 131,    0,      Z)," &
  "  133 (BC_1, IOB7,       input,   X)," &
  "  134 (BC_1, *        , control, 0)," &  -- IOB Output Enable
  "  135 (BC_1, IOB6,       output3, X, 134,    0,      Z)," &
  "  136 (BC_1, IOB6,       input,   X)," &
  "  137 (BC_1, *        , control, 0)," &  -- IOB Output Enable
  "  138 (BC_1, IOB5,       output3, X, 137,    0,      Z)," &
  "  139 (BC_1, IOB5,       input,   X)," &
  "  140 (BC_1, *        , control, 0)," &  -- IOB Output Enable
  "  141 (BC_1, IOB4,       output3, X, 140,    0,      Z)," &
  "  142 (BC_1, IOB4,       input,   X)," &
  "  143 (BC_1, *        , control, 0)," &  -- IOB Output Enable
  "  144 (BC_1, IOB3,       output3, X, 143,    0,      Z)," &
  "  145 (BC_1, IOB3,       input,   X)," &
  "  146 (BC_1, *        , control, 0)," &  -- IOB Output Enable
  "  147 (BC_1, IOB2,       output3, X, 146,    0,      Z)," &
  "  148 (BC_1, IOB2,       input,   X)," &
"  149 (BC_1, *        , control, 0)," &  -- IOB Output Enable
  "  150 (BC_1, IOB1,       output3, X, 149,    0,      Z)," &
  "  151 (BC_1, IOB1,       input,   X)," &
  "  152 (BC_1, *        , control, 0)," &  -- IOB Output Enable
  "  153 (BC_1, IOB0,       output3, X, 152,    0,      Z)," &
  "  154 (BC_1, IOB0,       input,   X)";
end SMCSLITE;
```

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