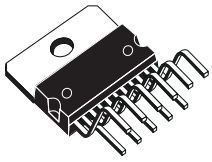
STA7360

20W BRIDGE/STEREO AUDIO AMPLIFIER WITH CLIPPING DETECTOR

- VERY FEW EXTERNAL COMPONENTS
- NO BOUCHEROT CELLS
- NO BOOSTRAP CAPACITORS
- HIGH OUTPUT POWER
- NO SWITCH ON/OFF NOISE
- VERY LOW STAND-BY CURRENT
- FIXED GAIN (20dB STEREO)
- PROGRAMMABLE TURN-ON DELAY
- CLIPPING DETECTOR
- ST-BY FUNCTION

Protections:

- OUTPUT AC-DC SHORT CIRCUIT TO GROUND AND TO SUPPLY VOLTAGE
- VERY INDUCTIVE LOADS
- LOUDSPEAKER PROTECTION
- OVERRATING CHIP TEMPERATURE
- ESD PROTECTION



MULTIWATT11V

ORDERING NUMBER: STA7360

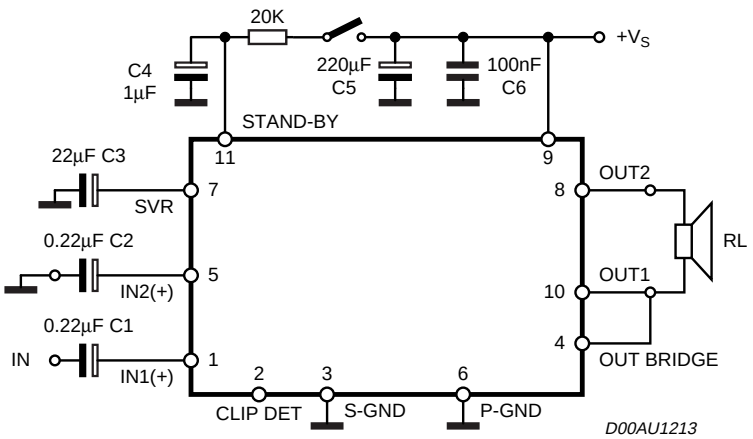
DESCRIPTION

The STA7360 is a new technology class AB Audio Power Amplifier in the Multiwatt® package.Thanks to the fully complementary PNP/NPN output configuration the high power performance of the STA7360 is obtained without bootstrap capacitors.

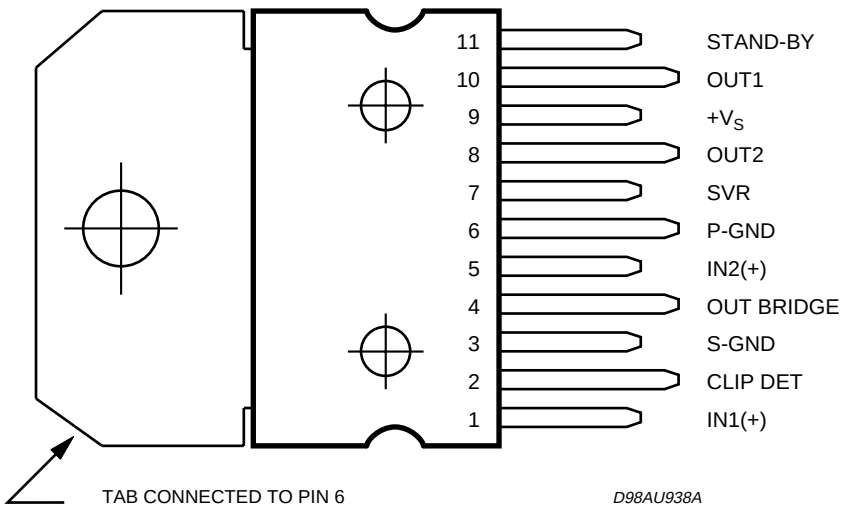
A delayed turn-on mute circuit eliminates audible on/off noise, and a novel short circuit protection system prevents spurious intervention with highly inductive loads.

The device provides a circuit for the detection of clipping in the output stages. The output, an open collector is able to drive systems with automatic volume control.

APPLICATION CIRCUIT



PIN CONNECTION (Top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Operating Supply Voltage	20	V
I_o	Output Peak Current (non rep. for t = 100µs)	5	A
I_o	Output Peak Current (rep. freq. > 10Hz)	4	A
P_{tot}	Power Dissipation at T_{case} = 85°C	36	W
T_{stg},T_J	Storage and Junction Temperature	-40 to 150	°C

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case Max	1.8	°C/W

ELECTRICAL CHARACTERISTCS (Refer to the test circuits, T_{amb} = 25°C, V_S = 14.4V, f = 1KHz unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Supply Voltage Range		8		18	V
I_d	Total Quiescent Drain Current	stereo configuration		65	120	mA
A_{SB}	Stand-by attenuation		60	80		dB
I_{SB}	Stand-by Current				100	µA
I_{CO}	Clip Detector Prog. Current	pin 2 pull up to 5V d = 1% with 10KW d = 5%		70 130		µA µA
STEREO						
P_O	Output Power (each channel) THD = 10%	R_L = 2Ω R_L = 3.2Ω R_L = 4Ω,12V R_L = 4Ω	7	11 8 4.5 6.5		W W W W
d	Distortion	P_o = 0.1 to 2.5W; R_L = 4Ω Po = 0.1 to 4W; R_L = 3.2Ω		0.05 0.05	0.5 0.5	% %
SVR	Supply Voltage Rejection	R_g = 10KΩ C3 = 22µF f = 100Hz C3 = 100µF	45	 62		dB dB
CT	Crosstalk	f = 1KHz f = 10KHz	45	 55		dB dB
R_I	Input Resistance			50		KΩ
G_V	Voltage Gain		19	20	21	dB
G_V	Voltage Gain Match				1	dB
E_{IN}	Input Noise Voltage	22 Hz to 22KHz R_g = 50Ω R_g = 10KΩ Rg =		2.5 3 3.5	5 7	µV µV µV
BRIDGE						
V_{os}	Output Offset Voltage				250	mV
P_o	Output Power THD = 10%	R_L = 4Ω,12V R_L = 4Ω; 14.4V	16	15 20		W W
d	Distortion	P_o = 0.1 to 7W; R_L = 4Ω		0.05	0.5	%
SVR	Supply Voltage Rejection	Rg = 10KΩ; C3 = 22µF f = 100Hz; C3 = 100µF	45	 62		dB dB
R_I	Input Resistance			50		KΩ
G_V	Voltage Gain			26		dB
EIN	Input Noise Voltage	22Hz to 22KHz R_g = 50Ω R_g = 10KΩ		3.5 4		µV µV

Figure 1. STEREO Test and Application Circuit

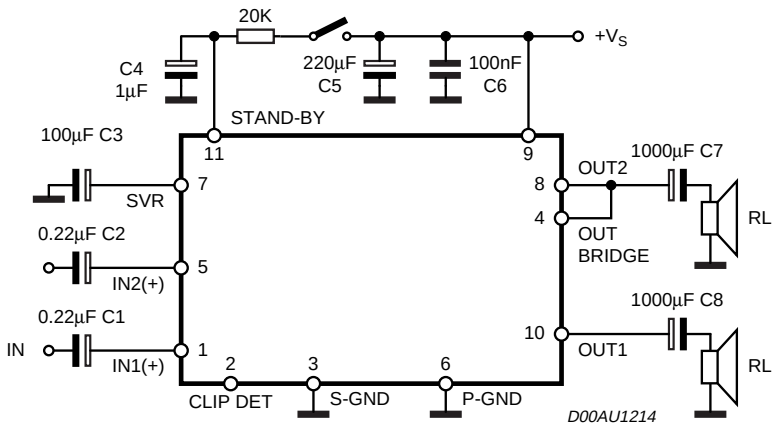


Figure 2. P.C. Board and Component Layout (STEREO) of the circuit of fig. 1 (1:1 scale)

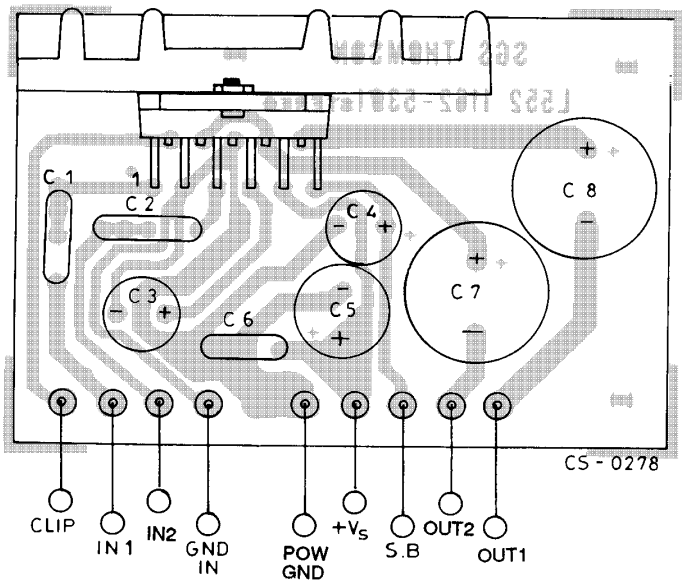


Figure 3. BRIDGE Test and Appication Circuit

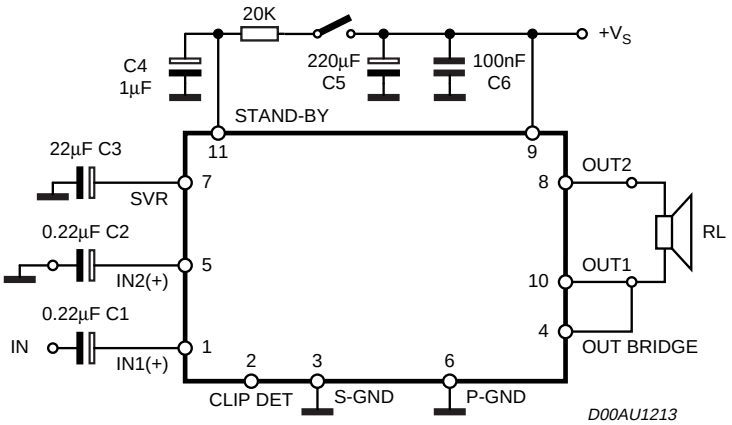


Figure 4. Board and Layout (BRIDGE) of the circuit of fig. 3 (1:1 scale)

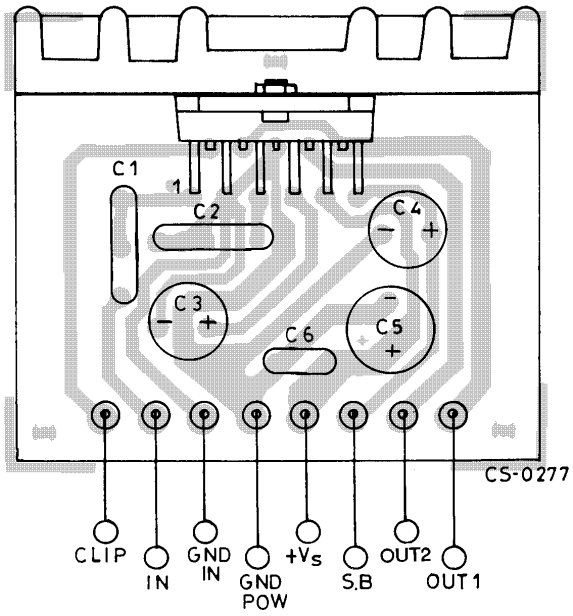


Figure 5. Output Power vs. Supply Voltage (Stereo)

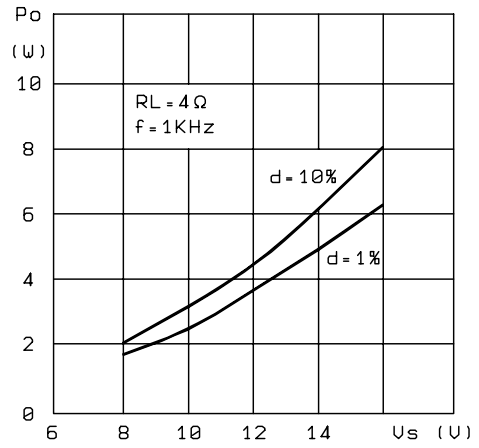


Figure 6. Output Power vs. Supply Voltage (Stereo)

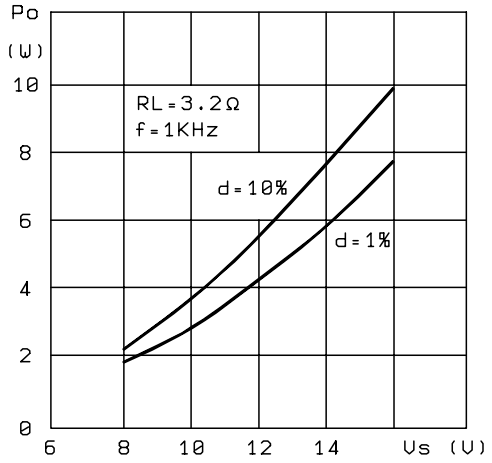


Figure 7. Output Power vs. Supply Voltage (Stereo)

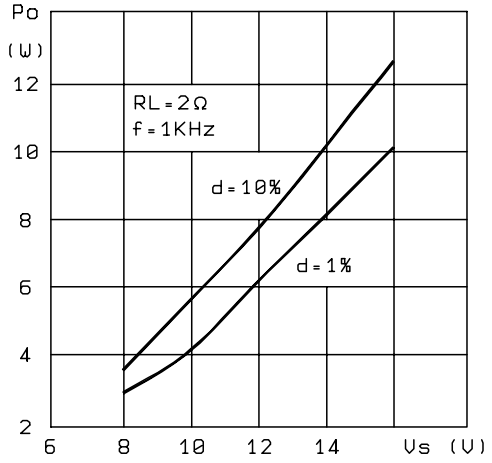


Figure 8. Output Power vs. Supply Voltage (Bridge)

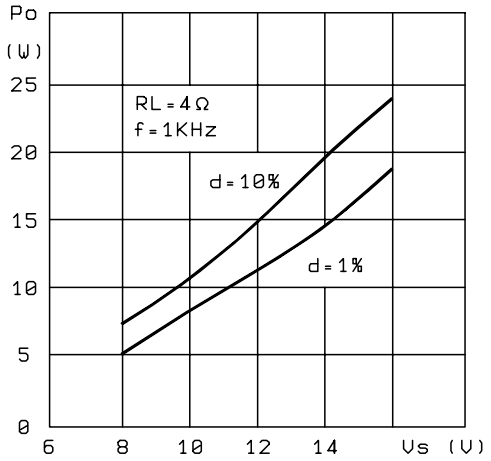


Figure 9. Drain Current vs Supply Voltage (Stereo)

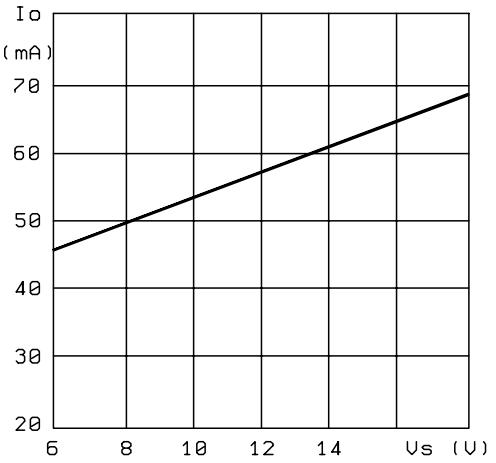


Figure 10. Distortion vs Output Power (Stereo)

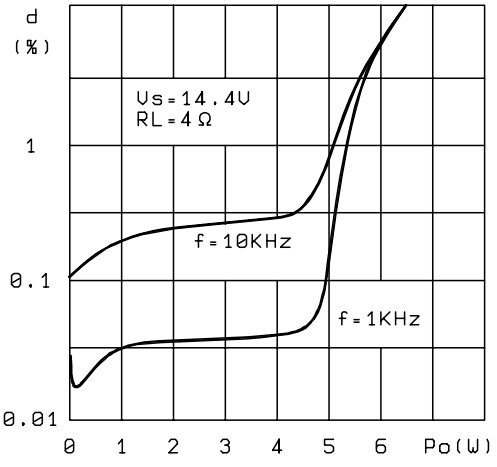


Figure 11. Distortion vs Output Power (Stereo)

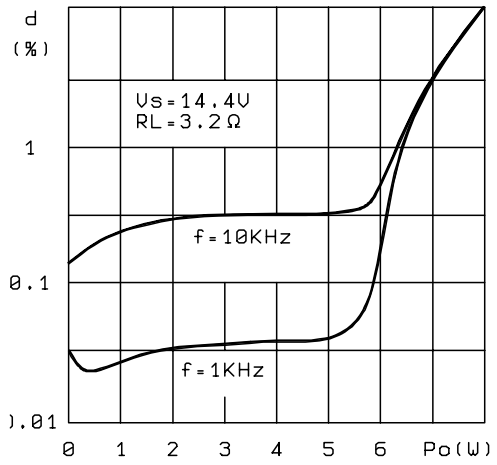


Figure 12. Distortion vs Output Power (Stereo)

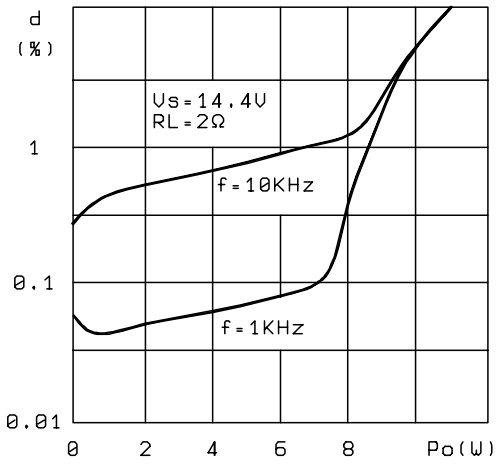


Figure 13. Distortion vs Output Power (Bridge)

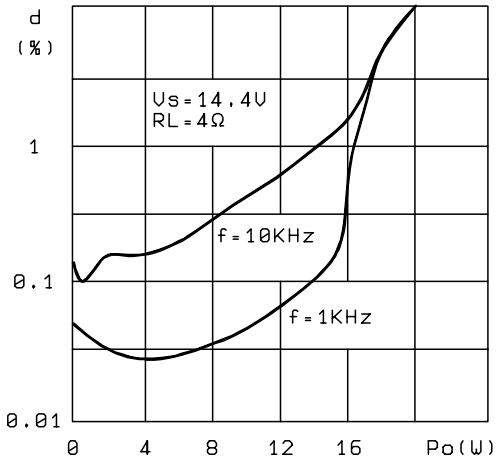


Figure 14. SVR vs. Frequency & C3 (Stereo)

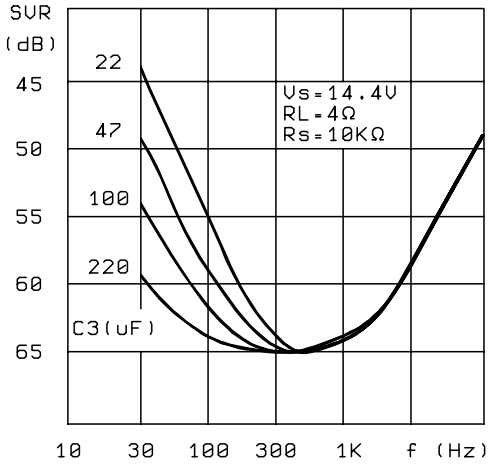


Figure 15. SVR vs. Frequency & C3 (Bridge)

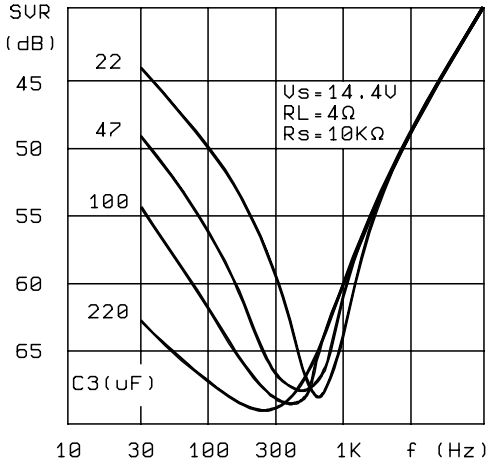


Figure 16. Crosstalk vs. Frequency (Stereo)

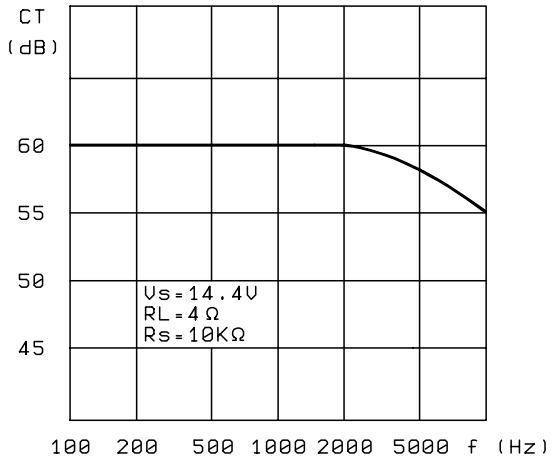


Figure 17. Power Dissipation& Efficiency vs. Output Power(Stereo)

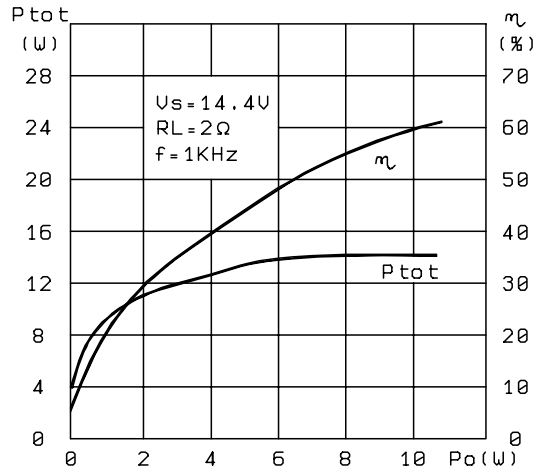


Figure 18. Power Dissipation& Efficiency vs. Output Power (Stereo)

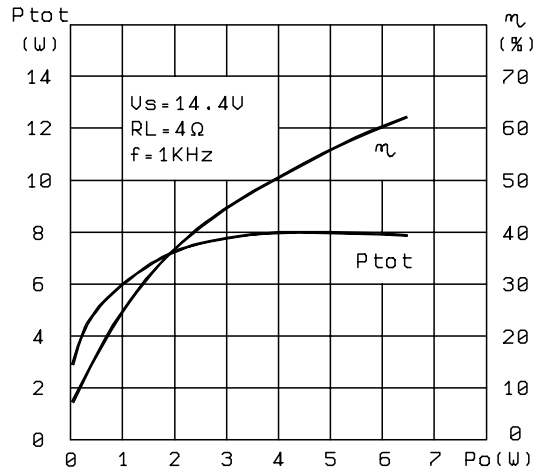
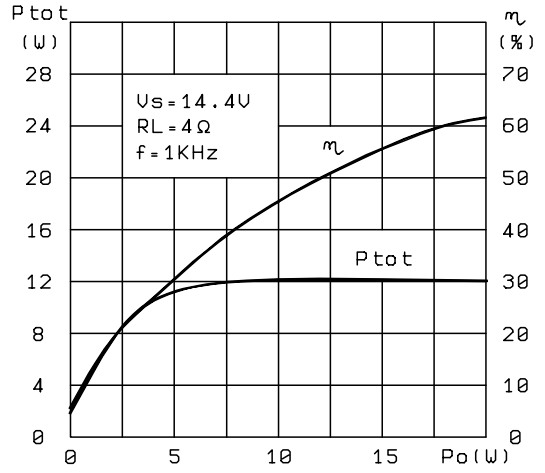


Figure 19. Power Dissipation& Efficiency vs. Output Power (Bridge)



BLOCK DESCRIPTION

PolarizationThe device is organized with the gain resistors directly connected to the signal ground pin i.e. without gain capacitors (fig. 20).

The non inverting inputs of the amplifiers are connected to the SVR pin by means of resistor dividers, equal to the feedback networks. This allows the outputs to track the SVR pin which is sufficiently slow to avoid audible turn-on and turn-off transients.

SVR

The voltage ripple on the outputs is equal to the one on SVR pin: with appropriate selection of CSVR, more than 60dB of ripple rejection can be obtained.

Delayed Turn-on (muting)

The CSVR sets a signal turn-on delay too. A circuit is included which mutes the device until the voltage on SVR pin reaches ~2.5V typ. (fig. 22). The mute function is obtained by duplicating the input differential pair (fig. 21): it can be switched to the signal source or to an internal mute input. This feature is necessary to prevent transients at the inputs reaching the loudspeaker(s) immediately after power-on).

Fig. 22 represents the detailed turn-on transient with reference to the stereo configuration.At the power-on the output decoupling capacitors are charged through an internal path but the device itself remains switched off (phase 1 of the represented diagram).

When the outputs reach the voltage level of about 1V (this means that there is no presence of short circuits) the device switches on, the SVR capacitor starts charging itself and the output tracks exactly the SVR pin.During this phase the device is muted until the SVR reaches the "Play" threshold (~2.5V typ.), after that the music signal starts being played.

Stereo/Bridge Switching

There is also no need for external components for changing from stereo to bridge configuration (figg. 20, 22). A simple short circuit between two pins allows phase reversal at one output, yet maintaining the quiescent output voltage.

Stand-by

The device is also equipped with a stand-by function, so that a low current, and hence low cost switch, can be used for turn on/off.

Stability

The device is provided with an internal compensation wich allows to reach low values of closed loop gain.In this way better performances on S/N ratio and SVR can be obtained.

RECOMMENDED VALUES OF THE EXTERNAL COMPONENTS (ref to the Stereo Test and Application Circuit)

Comp.	Recommended Value	Purpose	Larger than the Recomm. Value	Smaller than the Recomm. Value
C1	0.22µF	Input Decoupling (CH1)	–	–
C2	0.22µF	Input Decoupling (CH2)	–	–
C3	100µF	Supply Voltage Rejection Filtering Capacitor	Longer Turn-On Delay Time	- Worse Supply Voltage Rejection. - Shorter Turn-On Delay Time - Danger of Noise (POP
C4	1µF	Stand-By ON/OFF Delay	Delayed Turn-Off by Stand-By Switch	Danger of Noise (POP)
C5	220µF (min)	Supply By-Pass		Danger of Oscillations
C6	100nF (min)	Supply By-Pass		Danger of Oscillations
C7	2200µF	Output Decoupling CH2	- Decrease of Low Frequency Cut Off - Longer Turn On Delay	- Increase of Low Frequency Cut Off - Shorter Turn On Delay
C8	2200µF	Output Decoupling CH1	- Decrease of Low Frequency Cut Off - Longer Turn On Delay	- Increase of Low Frequency Cut Off - Shorter Turn On Delay

Figure 20. Block Diagram; Stereo Configuration

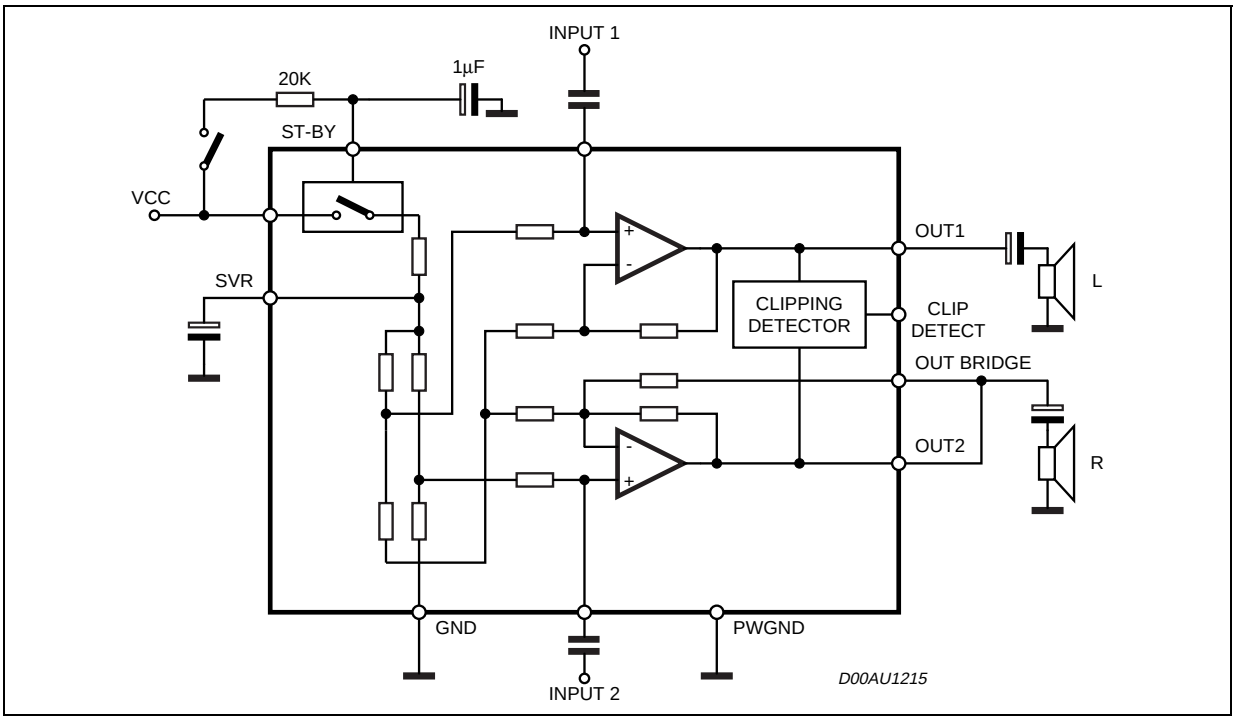


Figure 21. Mute Function Diagram

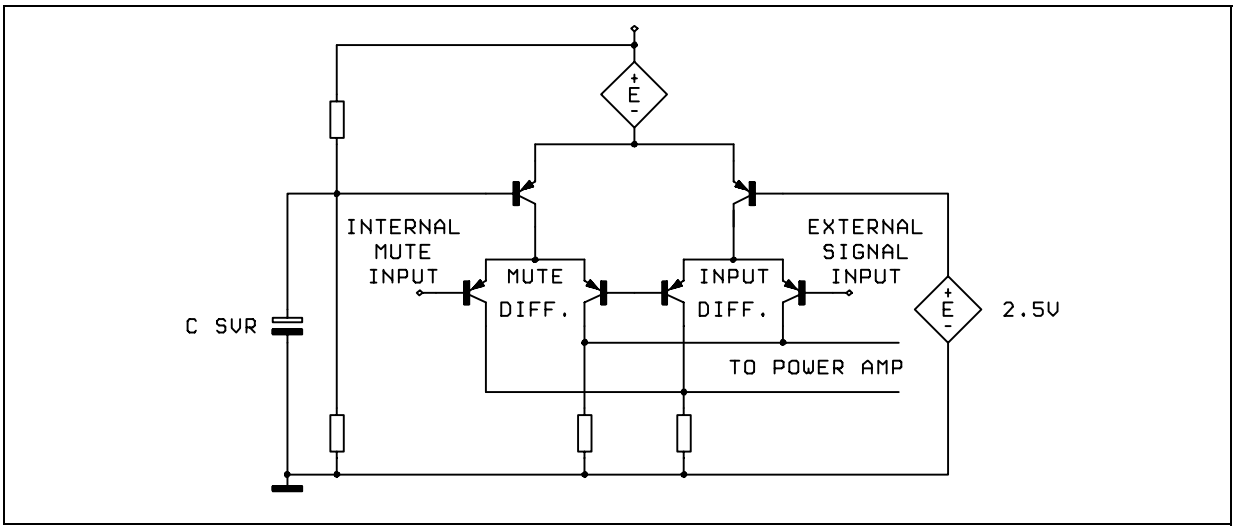


Figure 22. Turn-on Delay Circuit

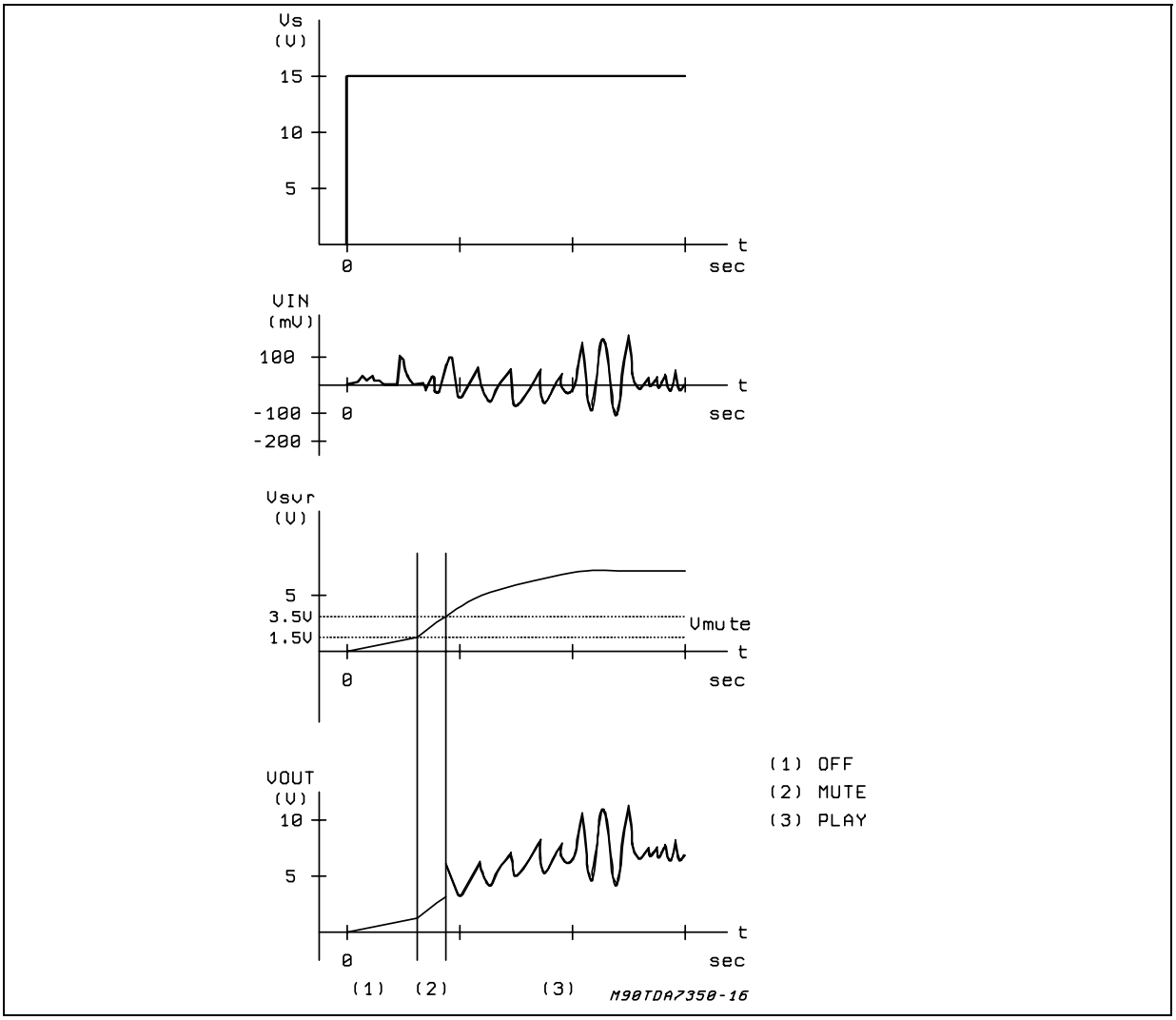


Figure 23. Block Diagram; Bridge Configuration

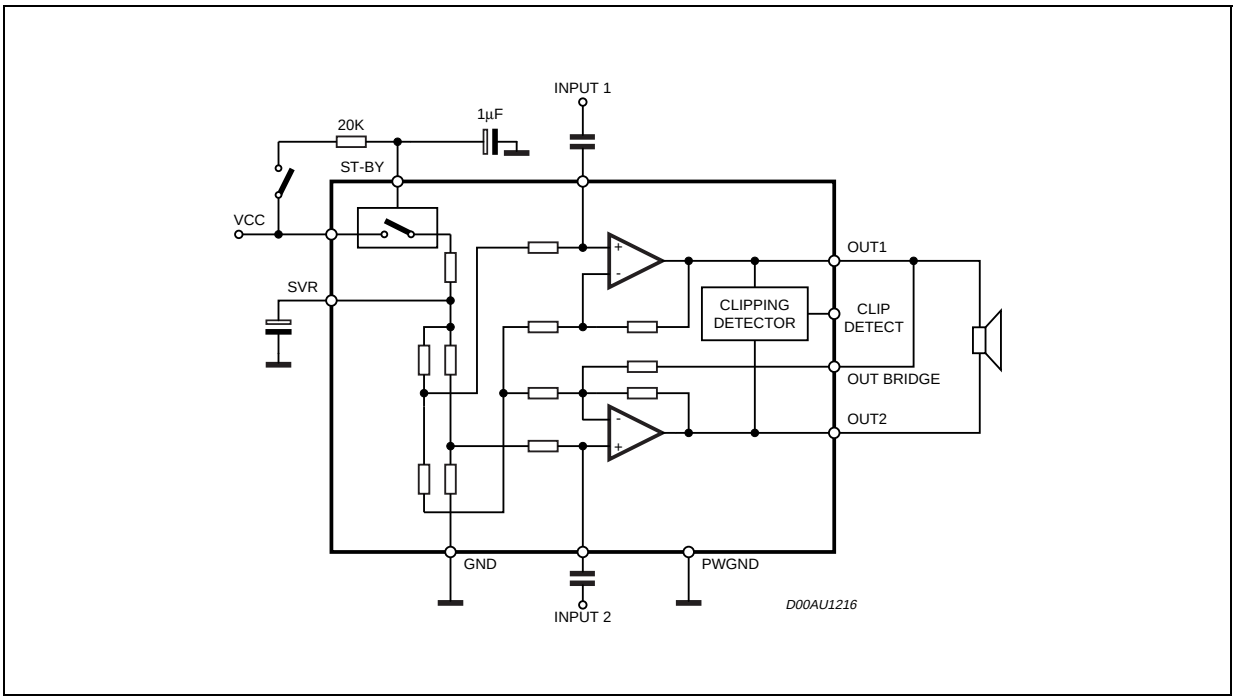


Figure 24. Dual Channel Distortion Detector

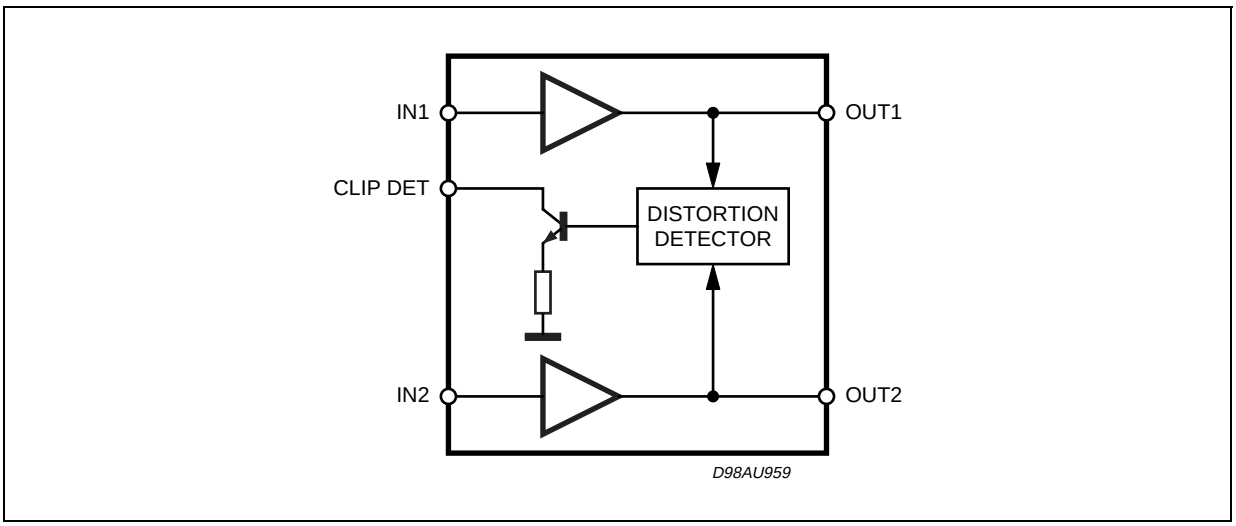


Figure 25. ICV - PNP Gain vs. I_C

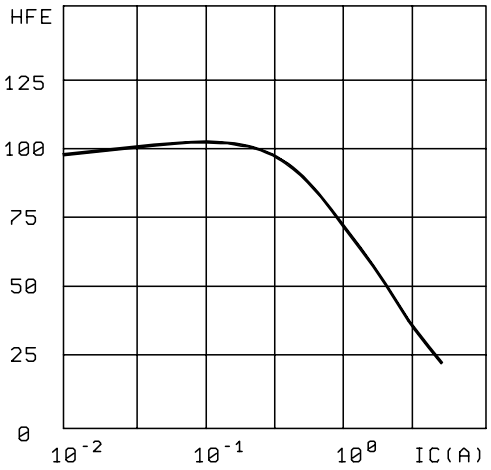


Figure 26. ICV - PNP VCE(sat) vs. I_C

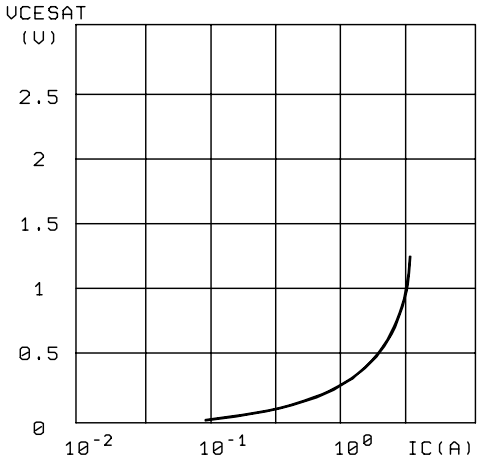
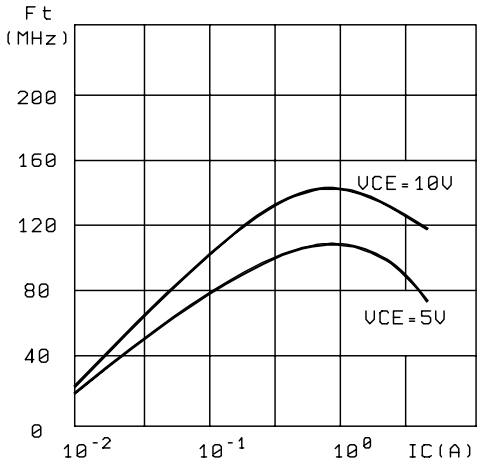


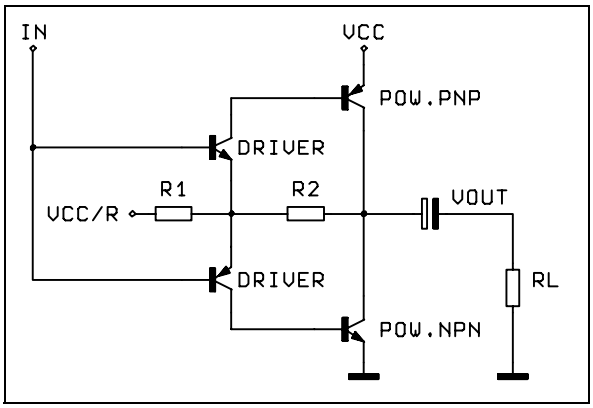
Figure 27. ICV - PNP cut-off frequency vs. I_C



OUTPUT STAGE

Poor current capability and low cutoff frequency are well known limits of the standard lateral PNP. Composite PNP-NPN power output stages have been widely used, regardless their high saturation drop. This drop can be overcome only at the expense of external components, namely, the bootstrap capacitors. The availability of 4A isolated collector PNP (ICV PNP) adds versatility to the design. The performance of this component, in terms of gain, VCEsat and cut-off frequency, is shown in fig. 25, 26, 27 respectively. It is realized in a new bipolar technology, characterized by top-bottom isolation techniques, allowing the implementation of low leakage diodes, too. It guarantees BVCEO >20V and BVCBO >50V both for NPN and PNP transistors. Basically, the connection shown in fig. 13 has been chosen. First of all because its voltage swing is rail-to-rail, limited only by the VCEsat of the output transistors, which are in the range of 0.3W each. Then, the gain VOUT/VIN is greater than unity, approximately 1+R2/R1. (VCC/2 is fixed by an auxiliary amplifier common to both channel). It is possible, controlling the amount of this local feedback, to force the loop gain (A * b) to less than unity at frequencies for which the phase shift is 180°. This means that the output buffer is intrinsically stable and not prone to oscillation.

Figure 28. The New Output Stage



In contrast, with the circuit of fig. 29, the solution adopted to reduce the gain at high frequencies is the use of an external RC network.

AMPLIFIER BLOCK DIAGRAM

The block diagram of each voltage amplifier is shown in fig. 30. Regardless of production spread, the current in each final stage is kept low, with enough margin on the minimum, below which cross-over distortion would appear.

Figure 29. A Classical Output Stage

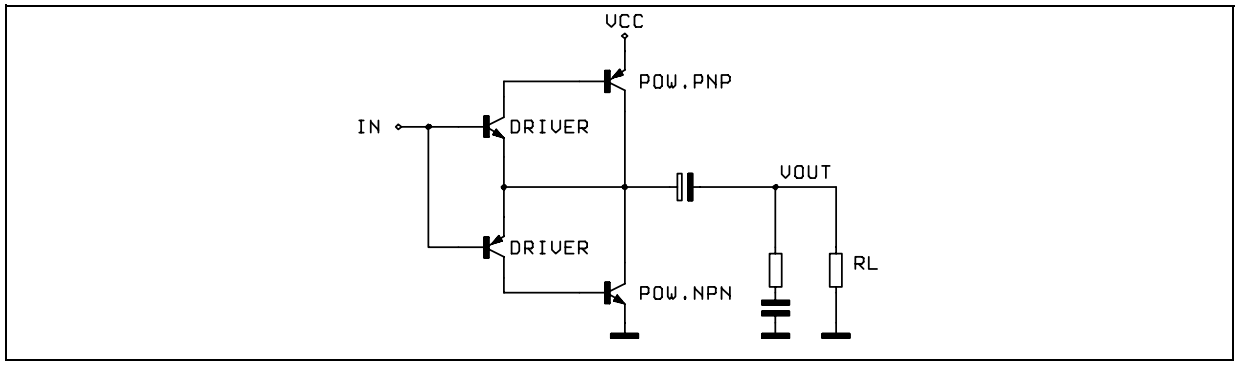
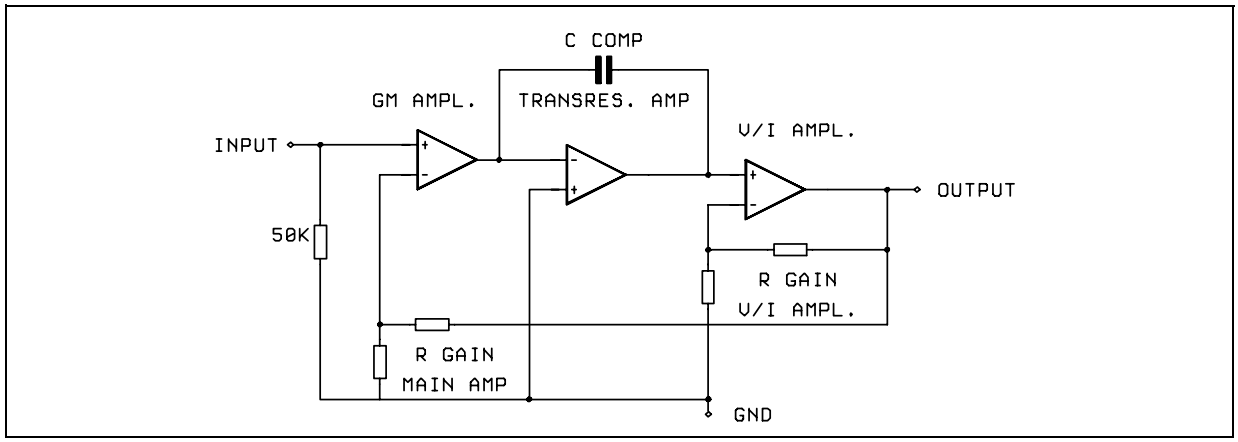


Figure 30. Amplifier Block Diagram



BUILT-IN PROTECTION SYSTEMS

Short Circuit ProtectionThe maximum current the device can deliver can be calculated by considering the voltage that may be present at the terminals of a car radio amplifier and the minimum load impedance.

Apart from consideration concerning the area of the power transistors it is not difficult to achieve peak currents of this magnitude (5A peak).However, it becomes more complicated if AC and DC short circuit protection is also required.In particular, with a protection circuit which limits the output current following the SOA curve of the output transistors it is possible that in some conditions (highly reactive loads, for example) the protection circuit may intervene during normal operation. For this reason each amplifier has been equipped with a protection circuit that intervenes when the output current exceeds 4A

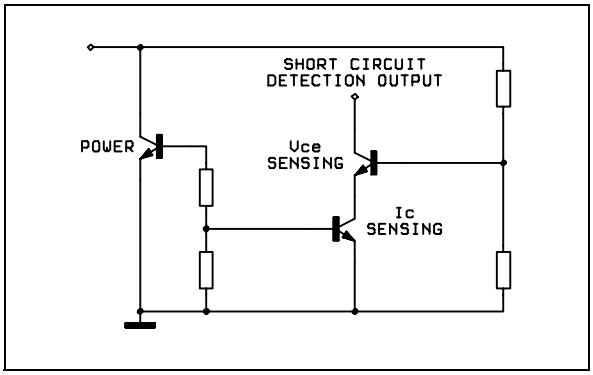
Fig 16 shows the protection circuit for an NPN power transistor (a symmetrical circuit applies to PNP). The VBE of the power is monitored and gives out a signal,available through a cascode.

This cascode is used to avoid the intervention of the short circuit protection when the saturation is below a given limit.

The signal sets a flip-flop which forces the amplifier outputs into a high impedance state.

In case of DC short circuit when the short circuit is removed the flip-flop is reset and restarts the circuit (fig. 36). In case of AC short circuit or load shorted in Bridge configuration, the device is continuously switched in ON/OFF conditions and the current is limited.

Figure 31. Circuitry for Short Circuit Detection



Polarity Inversion

High current (up to 10A) can be handled by the device with no damage for a longer period than the blow-out time of a quick 2A fuse (normally connected in series with the supply). This features is added to avoid destruction, if during fitting to the car, a mistake on the connection of the supply is made.

DC Voltage

The maximum operating DC voltage for the STA7360 is 18V.

Thermal Shut-down

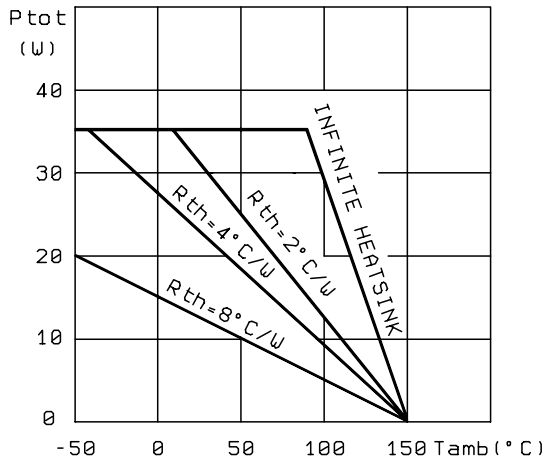
The presence of a thermal limiting circuit offers the following advantages:

1) an overload on the output (even if it is permanent), or an excessive ambient temperature can be easily withstood.

2)the heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no device damage in the case of excessive junction temperature: all happens is that Po (and therefore Ptot) and Id are reduced.

The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance); Fig. 32 shows the dissipable power as a function of ambient temperature for different thermal resistance.

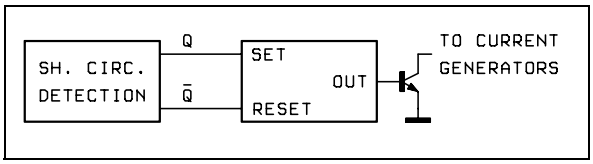
Figure 32. Maximum Allowable Power Dissipation vs. Ambient Temperature



Loudspeaker Protection

The STA7360 guarantees safe operations even for the loudspeaker in case of accidental shortcircuit.Whenever a single OUT to GND, OUT to V_S short circuit occurs both the outputs are switched OFF so limiting dangerous DC current flowing through the loudspeaker.

Figure 33. Restart Circuit



APPLICATION HINTS

This section explains briefly how to get the best from the STA7360 and presents some application circuits with suggestions for the value of the components. These values can change depending on the characteristics that the designer of the car radio wants to obtain,or other parts of the car radio that are connected to the audio block.

To optimize the performance of the audio part it is useful (or indispensable) to analyze also the parts outside this block that can have an interconnection with the amplifier.

This method can provide components and system cost saving.

Reducing Turn On-Off Pop

The STA7360 has been designed in a way that the turn on(off) transients are controlled through the charge(discharge) of the Csvr capacitor.

As a result of it, the turn on(off) transient spectrum contents is limited only to the subsonic range. The following section gives some brief notes to get the best from this design feature(it will refer mainly to the stereo application which appears to be in most cases the more critical from the pop viewpoint. The bridge connection in fact,due to the common mode waveform at the outputs, does not give pop effect).

TURN-ON

Fig 34 shows the output waveform (before and after the "A" weighting filter) compared to the value of Csvr.

Better pop-on performance is obtained with higher Csvr values (the recommended range is from 22uF to 220uF).

The turn-on delay (during which the amplifier is in mute condition) is a function essentially of : Cout , Csvr .

Being:

$$T1 \approx 120 \cdot C_{out}$$

$$T2 \approx 1200 \cdot C_{svr}$$

The turn-on delay is given by:

T1+T2 STEREO

T2 BRIDGE

The best performance is obtained by driving the st-by pin with a ramp having a slope slower than 2V/ms

TURN-OFF

A turn-off pop can occur if the st-by pin goes low with a short time constant.This pop is due to the fast switch-off of the internal current generator of the amplifier.If the voltage present across the load becomes rapidly zero (due to the fast switch off) a small pop occurs, depending also on Cout,Rload.

The parameters that set the switch off time constant of the st-by pin are:

- the st-by capacitor (C4)
- the SVR capacitor (Csvr)
- resistors connected from st-by pin to the logical input (Rext)

BALANCED INPUT IN BRIDGE CONFIGURATION

A helpful characteristic of the STA7360 is that,in bridge configuration, a signal present on both the input capacitors is amplified by the same amount and it is present in phase at the outputs,so this signal does not produce effects on the load.The typical value of CMRR is 46dB.

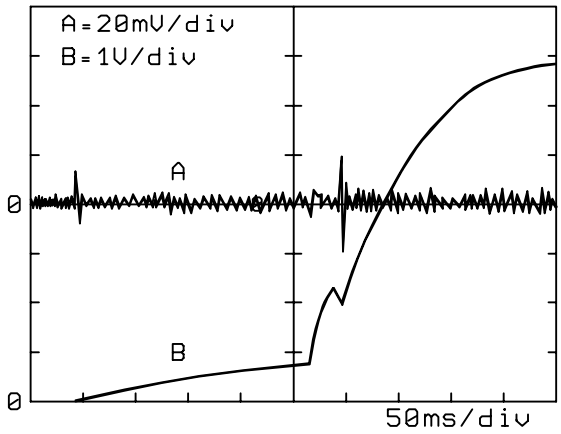
Looking at fig 35, we can see that a noise signal from the ground of the power amplifier to the ground of the hypothetical preamplifier is amplified of a factor equal to the gain of the amplifier (2 * Gv).

Using a configuration of fig. 36 the same ground noise is present at the output multiplied by the factor 2 * Gv/200.

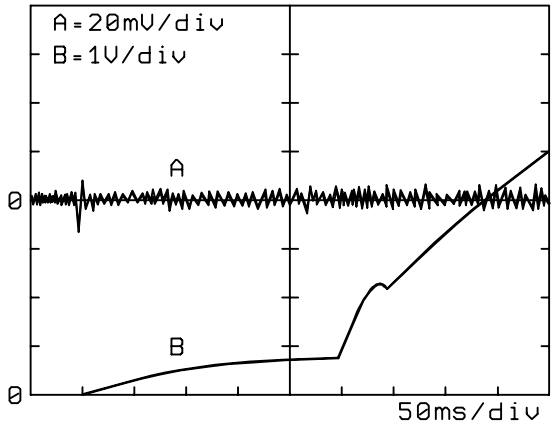
This means less distortion,less noise (e.g. motor cassette noise) and/or a simplification of the layout of PC board.

The only limitation of this balanced input is the maximum amplitude of common mode signals (few tens of millivolt) to avoid a loss of output power due to the common mode signal on the output, but in a large number of cases this signal is within this range.

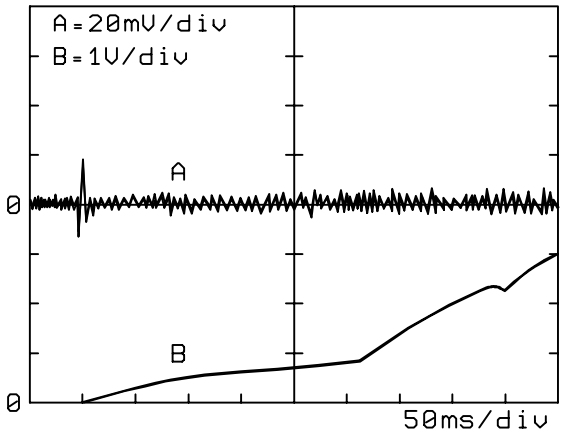
Figure 34.



b) C_{svr} = 47 µF



c) C_{svr} = 100 µF



(*) These parameters must be validated after final silicon characterization.

Figure 35.

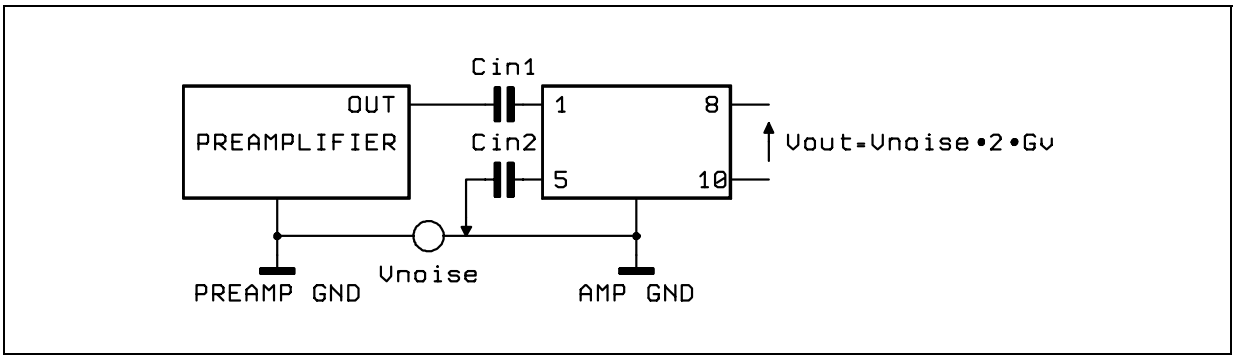
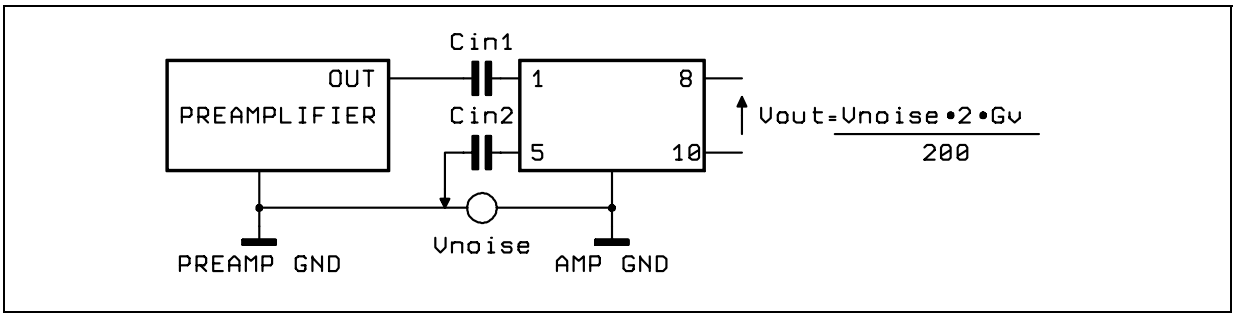
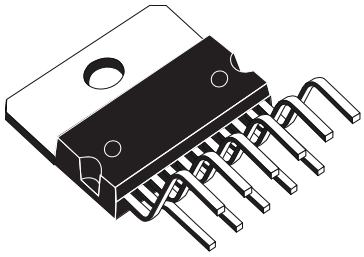


Figure 36.



DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			5			0.197
B			2.65			0.104
C			1.6			0.063
D		1			0.039	
E	0.49		0.55	0.019		0.022
F	0.88		0.95	0.035		0.037
G	1.45	1.7	1.95	0.057	0.067	0.077
G1	16.75	17	17.25	0.659	0.669	0.679
H1	19.6			0.772		
H2			20.2			0.795
L	21.9	22.2	22.5	0.862	0.874	0.886
L1	21.7	22.1	22.5	0.854	0.87	0.886
L2	17.4		18.1	0.685		0.713
L3	17.25	17.5	17.75	0.679	0.689	0.699
L4	10.3	10.7	10.9	0.406	0.421	0.429
L7	2.65		2.9	0.104		0.114
M	4.25	4.55	4.85	0.167	0.179	0.191
M1	4.73	5.08	5.43	0.186	0.200	0.214
S	1.9		2.6	0.075		0.102
S1	1.9		2.6	0.075		0.102
Dia1	3.65		3.85	0.144		0.152

OUTLINE AND MECHANICAL DATA



Multiwatt11 V