DS05-20877-1E

FLASH MEMORY

CMOS

16M (2M × 8/1M × 16) BIT

MBM29SL160TD-10/-12/MBM29SL160BD-10/-12

■ FEATURES

- **Single 1.8 V read, program, and erase**
  Minimizes system level power requirements
- **Compatible with JEDEC-standard commands**
  Uses same software commands as E^2PROMs
- **Compatible with JEDEC-standard world-wide pinouts**
  48-pin TSOP(I) (Package suffix: PFTN – Normal Bend Type, PFTR – Reversed Bend Type)
  48-ball FBGA (Package suffix: PBT)
- **Minimum 100,000 program/erase cycles**
- **High performance**
  100 ns maximum access time
- **Sector erase architecture**
  Eight 4K word and thirty one 32K word sectors in word mode
  Eight 8K byte and thirty one 64K byte sectors in byte mode
  Any combination of sectors can be concurrently erased. Also supports full chip erase.
- **Boot Code Sector Architecture**
  T = Top sector
  B = Bottom sector
- **One Time Protect (OTP) region**
  256 Byte of OTP, accessible through a new “OTP Enable” command sequence
  Factory serialized and protected to provide a secure electronic serial number (ESN)
- **$\overline{\text{WP}}$/ACC input pin**
  At V_{IL}, allows protection of boot sectors, regardless of sector protection/unprotection status
  At V_{IH}, allows removal of boot sector protection
  At V_{HH}, increases program performance
- **Embedded Erase™ Algorithms**
  Automatically pre-programs and erases the chip or any sector
- **Embedded Program™ Algorithms**
  Automatically writes and verifies data at specified address
- **$\overline{\text{Data}}$ Polling and Toggle Bit feature for detection of program or erase cycle completion**
- **Ready/Busy output (RY/$\overline{\text{BY}}$)**
  Hardware method for detection of program or erase cycle completion

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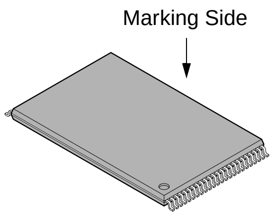
- **Automatic sleep mode**
  When addresses remain stable, automatically switch themselves to low power mode.
- **Erase Suspend/Resume**
  Suspends the erase operation to allow a read in another sector within the same device
- **Sector group protection**
  Hardware method disables any combination of sector groups from program or erase operations
- **Sector Group Protection Set function by Extended sector group protection command**
- **Fast Programming Function by Extended Command**
- **Temporary sector group unprotection**
  Temporary sector group unprotection via the $\overline{\text{RESET}}$ pin.
- **In accordance with CFI (Common Flash Memory Interface)**

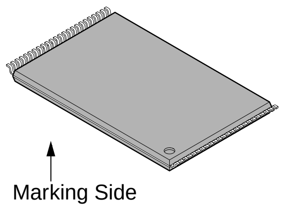
■ PACKAGE

48-pin plastic TSOP (I)



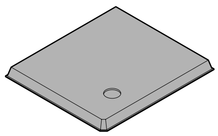
(FPT-48P-M19)

48-pin plastic TSOP (I)



(FPT-48P-M20)

48-ball FBGA



(BGA-48P-M13)

■ GENERAL DESCRIPTION

The MBM29SL160TD/BD are a 16M-bit, 1.8 V-only Flash memory organized as 2M bytes of 8 bits each or 1M words of 16 bits each. The MBM29SL160TD/BD are offered in a 48-pin TSOP(I) and 48-ball FBGA Package. These devices are designed to be programmed in-system with the standard system 1.8 V V_{CC} supply. 12.0 V V_{PP} and 5.0 V V_{CC} are not required for write or erase operations. The devices can also be reprogrammed in standard EPROM programmers.

The standard MBM29SL160TD/BD offer access times 100 ns and 120 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention the devices have separate chip enable ($\overline{CE}$), write enable ($\overline{WE}$), and output enable ($\overline{OE}$) controls.

The MBM29SL160TD/BD are pin and command set compatible with JEDEC standard E^2PROMs. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the devices is similar to reading from 5.0 V and 12.0 V Flash or EPROM devices.

The MBM29SL160TD/BD are programmed by executing the program command sequence. This will invoke the Embedded Program Algorithm which is an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. Typically, each sector can be programmed and verified in about 0.7 seconds. Erase is accomplished by executing the erase command sequence. This will invoke the Embedded Erase Algorithm which is an internal algorithm that automatically preprograms the array if it is not already programmed before executing the erase operation. During erase, the devices automatically time the erase pulse widths and verify proper cell margin.

A sector is typically erased and verified in 1.5 second. (If already completely preprogrammed.)

The devices also feature a sector erase architecture. The sector mode allows each sector to be erased and reprogrammed without affecting other sectors. The MBM29SL160TD/BD are erased when shipped from the factory.

The devices feature single 1.8 V power supply operation for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. A low V_{CC} detector automatically inhibits write operations on the loss of power. The end of program or erase is detected by $\overline{\text{Data}}$ Polling of DQ_7, by the Toggle Bit feature on DQ_6, or the RY/$\overline{BY}$ output pin. Once the end of a program or erase cycle has been completed, the devices internally reset to the read mode.

Fujitsu's Flash technology combines years of EPROM and E^2PROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The MBM29SL160TD/BD memories electrically erase the entire chip or all bits within a sector simultaneously via Fowler-Nordhiem tunneling. The bytes/words are programmed one byte/word at a time using the EPROM programming mechanism of hot electron injection.

Table 1 .1 Sector Address Tables (MBM29SL160TD)

Sector	Sector Address								Sector Size (Kbytes/ Kwords)	(×8) Address Range	(×16) Address Range
	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}			
SA0	0	0	0	0	0	X	X	X	64/32	000000H to 00FFFFH	000000H to 007FFFH
SA1	0	0	0	0	1	X	X	X	64/32	010000H to 01FFFFH	008000H to 00FFFFH
SA2	0	0	0	1	0	X	X	X	64/32	020000H to 02FFFFH	010000H to 017FFFH
SA3	0	0	0	1	1	X	X	X	64/32	030000H to 03FFFFH	018000H to 01FFFFH
SA4	0	0	1	0	0	X	X	X	64/32	040000H to 04FFFFH	020000H to 027FFFH
SA5	0	0	1	0	1	X	X	X	64/32	050000H to 05FFFFH	028000H to 02FFFFH
SA6	0	0	1	1	0	X	X	X	64/32	060000H to 06FFFFH	030000H to 037FFFH
SA7	0	0	1	1	1	X	X	X	64/32	070000H to 07FFFFH	038000H to 03FFFFH
SA8	0	1	0	0	0	X	X	X	64/32	080000H to 08FFFFH	040000H to 048000H
SA9	0	1	0	0	1	X	X	X	64/32	090000H to 09FFFFH	048000H to 04FFFFH
SA10	0	1	0	1	0	X	X	X	64/32	0A0000H to 0AFFFFH	050000H to 058000H
SA11	0	1	0	1	1	X	X	X	64/32	0B0000H to 0BFFFFH	058000H to 05FFFFH
SA12	0	1	1	0	0	X	X	X	64/32	0C0000H to 0CFFFFH	060000H to 068000H
SA13	0	1	1	0	1	X	X	X	64/32	0D0000H to 0DFFFFH	068000H to 06FFFFH
SA14	0	1	1	1	0	X	X	X	64/32	0E0000H to 0EFFFFH	070000H to 078FFFH
SA15	0	1	1	1	1	X	X	X	64/32	0F0000H to 0FFFFFH	078000H to 07FFFFH
SA16	1	0	0	0	0	X	X	X	64/32	100000H to 10FFFFH	080000H to 088000H
SA17	1	0	0	0	1	X	X	X	64/32	110000H to 11FFFFH	088000H to 08FFFFH
SA18	1	0	0	1	0	X	X	X	64/32	120000H to 12FFFFH	090000H to 098000H
SA19	1	0	0	1	1	X	X	X	64/32	130000H to 13FFFFH	098000H to 09FFFFH
SA20	1	0	1	0	0	X	X	X	64/32	140000H to 14FFFFH	0A0000H to 0A7FFFH
SA21	1	0	1	0	1	X	X	X	64/32	150000H to 15FFFFH	0A8000H to 00AFFFH
SA22	1	0	1	1	0	X	X	X	64/32	160000H to 16FFFFH	0B0000H to 0B7000H
SA23	1	0	1	1	1	X	X	X	64/32	170000H to 17FFFFH	0B8000H to 0BFFFFH
SA24	1	1	0	0	0	X	X	X	64/32	180000H to 18FFFFH	0C0000H to 0C7FFFH
SA25	1	1	0	0	1	X	X	X	64/32	190000H to 19FFFFH	0C8000H to 0CFFFFH
SA26	1	1	0	1	0	X	X	X	64/32	1A0000H to 1AFFFFH	0D0000H to 0D7FFFH
SA27	1	1	0	1	1	X	X	X	64/32	1B0000H to 1BFFFFH	0D8000H to 0DFFFFH
SA28	1	1	1	0	0	X	X	X	64/32	1C0000H to 1CFFFFH	0E0000H to 0E7FFFH
SA29	1	1	1	0	1	X	X	X	64/32	1D0000H to 1DFFFFH	0E8000H to 0EFFFFH
SA30	1	1	1	1	0	X	X	X	64/32	1E0000H to 1EFFFFH	0F0000H to 0F7000H
SA31	1	1	1	1	1	0	0	0	8/4	1F0000H to 1F1FFFH	0F8000H to 0F8FFFH
SA32	1	1	1	1	1	0	0	1	8/4	1F2000H to 1F3FFFH	0F9000H to 0F9FFFH
SA33	1	1	1	1	1	0	1	0	8/4	1F4000H to 1F5FFFH	0FA000H to 0FAFFFH
SA34	1	1	1	1	1	0	1	1	8/4	1F6000H to 1F7FFFH	0FB000H to 0FBFFFH
SA35	1	1	1	1	1	1	0	0	8/4	1F8000H to 1F9FFFH	0FC000H to 0FCFFFH
SA36	1	1	1	1	1	1	0	1	8/4	1FA000H to 1FBFFFH	0FD000H to 0FDFFFH
SA37	1	1	1	1	1	1	1	0	8/4	1FC000H to 1FDFFFH	0FE000H to 0FEFFFH
SA38	1	1	1	1	1	1	1	1	8/4	1FE000H to 1FFFFFH	0FF000H to 0FFFFFH

Note: The address range is A_{19}: A_{-1} if in byte mode ($\overline{BYTE} = V_{IL}$).
The address range is A_{19}: A_0 if in word mode ($\overline{BYTE} = V_{IH}$)

Table 1 .2 Sector Address Tables (MBM29SL160BD)

Sector	Sector Address								Sector Size (Kbytes/ Kwords)	(×8) Address Range	(×16) Address Range
	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}			
SA38	1	1	1	1	1	X	X	X	64/32	1F0000H to 1FFFFFH	0F8000H to 0FFFFFH
SA37	1	1	1	1	0	X	X	X	64/32	1E0000H to 1EFFFFH	0F0000H to 0F7FFFH
SA36	1	1	1	0	1	X	X	X	64/32	1D0000H to 1DFFFFH	0E8000H to 0EFFFFH
SA35	1	1	1	0	0	X	X	X	64/32	1C0000H to 1CFFFFH	0E0000H to 0E7FFFH
SA34	1	1	0	1	1	X	X	X	64/32	1B0000H to 1BFFFFH	0D8000H to 0DFFFFH
SA33	1	1	0	1	0	X	X	X	64/32	1A0000H to 1AFFFFH	0D0000H to 0D7FFFH
SA32	1	1	0	0	1	X	X	X	64/32	190000H to 19FFFFH	0C8000H to 0CFFFFH
SA31	1	1	0	0	0	X	X	X	64/32	180000H to 18FFFFH	0C0000H to 0C7FFFH
SA30	1	0	1	1	1	X	X	X	64/32	170000H to 17FFFFH	0B8000H to 0BFFFFH
SA29	1	0	1	1	0	X	X	X	64/32	160000H to 16FFFFH	0B0000H to 0B7FFFH
SA28	1	0	1	0	1	X	X	X	64/32	150000H to 15FFFFH	0A8000H to 0AFFFFH
SA27	1	0	1	0	0	X	X	X	64/32	140000H to 14FFFFH	0A0000H to 0A7FFFH
SA26	1	0	0	1	1	X	X	X	64/32	130000H to 13FFFFH	098000H to 09FFFFH
SA25	1	0	0	1	0	X	X	X	64/32	120000H to 12FFFFH	090000H to 097FFFH
SA24	1	0	0	0	X	X	X	X	64/32	110000H to 11FFFFH	088000H to 08FFFFH
SA23	1	0	0	0	0	X	X	X	64/32	100000H to 10FFFFH	080000H to 087FFFH
SA22	0	1	1	1	1	X	X	X	64/32	0F0000H to 0FFFFFH	078000H to 07FFFFH
SA21	0	1	1	1	0	X	X	X	64/32	0E0000H to 0EFFFFH	070000H to 077FFFH
SA20	0	1	1	0	1	X	X	X	64/32	0D0000H to 0DFFFFH	068000H to 06FFFFH
SA19	0	1	1	0	0	X	X	X	64/32	0C0000H to 0CFFFFH	060000H to 067FFFH
SA18	0	1	0	1	1	X	X	X	64/32	0B0000H to 0BFFFFH	058000H to 05FFFFH
SA17	0	1	0	1	0	X	X	X	64/32	0A0000H to 0AFFFFH	050000H to 057FFFH
SA16	0	1	0	0	1	X	X	X	64/32	090000H to 0FFFFFH	048000H to 04FFFFH
SA15	0	1	0	0	0	X	X	X	64/32	080000H to 08FFFFH	040000H to 047FFFH
SA14	0	0	1	1	1	X	X	X	64/32	070000H to 07FFFFH	038000H to 03FFFFH
SA13	0	0	1	1	0	X	X	X	64/32	060000H to 06FFFFH	030000H to 037FFFH
SA12	0	0	1	0	1	X	X	X	64/32	050000H to 05FFFFH	028000H to 02FFFFH
SA11	0	0	1	0	0	X	X	X	64/32	040000H to 04FFFFH	020000H to 027FFFH
SA10	0	0	0	1	1	X	X	X	64/32	030000H to 03FFFFH	018000H to 01FFFFH
SA9	0	0	0	1	0	X	X	X	64/32	020000H to 02FFFFH	010000H to 017FFFH
SA8	0	0	0	0	1	X	X	X	64/32	010000H to 01FFFFH	008000H to 008FFFH
SA7	0	0	0	0	0	1	1	1	8/4	00E000H to 00FFFFH	007000H to 007FFFH
SA6	0	0	0	0	0	1	1	0	8/4	00C000H to 00DFFFH	006000H to 006FFFH
SA5	0	0	0	0	0	1	0	1	8/4	00A000H to 00BFFFH	005000H to 005FFFH
SA4	0	0	0	0	0	1	0	0	8/4	008000H to 009FFFH	004000H to 004FFFH
SA3	0	0	0	0	0	0	1	1	8/4	006000H to 007FFFH	003000H to 003FFFH
SA2	0	0	0	0	0	0	1	0	8/4	004000H to 005FFFH	002000H to 002FFFH
SA1	0	0	0	0	0	0	0	1	8/4	002000H to 003FFFH	001000H to 001FFFH
SA0	0	0	0	0	0	0	0	0	8/4	000000H to 001FFFH	000000H to 000FFFH

Note: The address range is A_{19}: A_{-1} if in byte mode ($\overline{BYTE}$ = V_{IL}).
The address range is A_{19}: A_0 if in word mode ($\overline{BYTE}$ = V_{IH}).

Table 2 .1 Sector Group Addresses (MBM29SL160TD) (Top Boot Block)

Sector Group	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	Sectors
SGA0	0	0	0	0	0	X	X	X	SA0
SGA1	0	0	0	0	1	X	X	X	SA1 to SA3
	0	0	0	1	0	X	X	X	
	0	0	0	1	1	X	X	X	
SGA2	0	0	1	X	X	X	X	X	SA4 to SA7
SGA3	0	1	0	X	X	X	X	X	SA8 to SA11
SGA4	0	1	1	X	X	X	X	X	SA12 to SA15
SGA5	1	0	0	X	X	X	X	X	SA16 to SA19
SGA6	1	0	1	X	X	X	X	X	SA20 to SA23
SGA7	1	1	0	X	X	X	X	X	SA24 to SA27
SGA8	1	1	1	0	0	X	X	X	SA28 to SA30
	1	1	1	0	1	X	X	X	
	1	1	1	1	0	X	X	X	
SGA9	1	1	1	1	1	0	0	0	SA31
SGA10	1	1	1	1	1	0	0	1	SA32
SGA11	1	1	1	1	1	0	1	0	SA33
SGA12	1	1	1	1	1	0	1	1	SA34
SGA13	1	1	1	1	1	1	0	0	SA35
SGA14	1	1	1	1	1	1	0	1	SA36
SGA15	1	1	1	1	1	1	1	0	SA37
SGA16	1	1	1	1	1	1	1	1	SA38

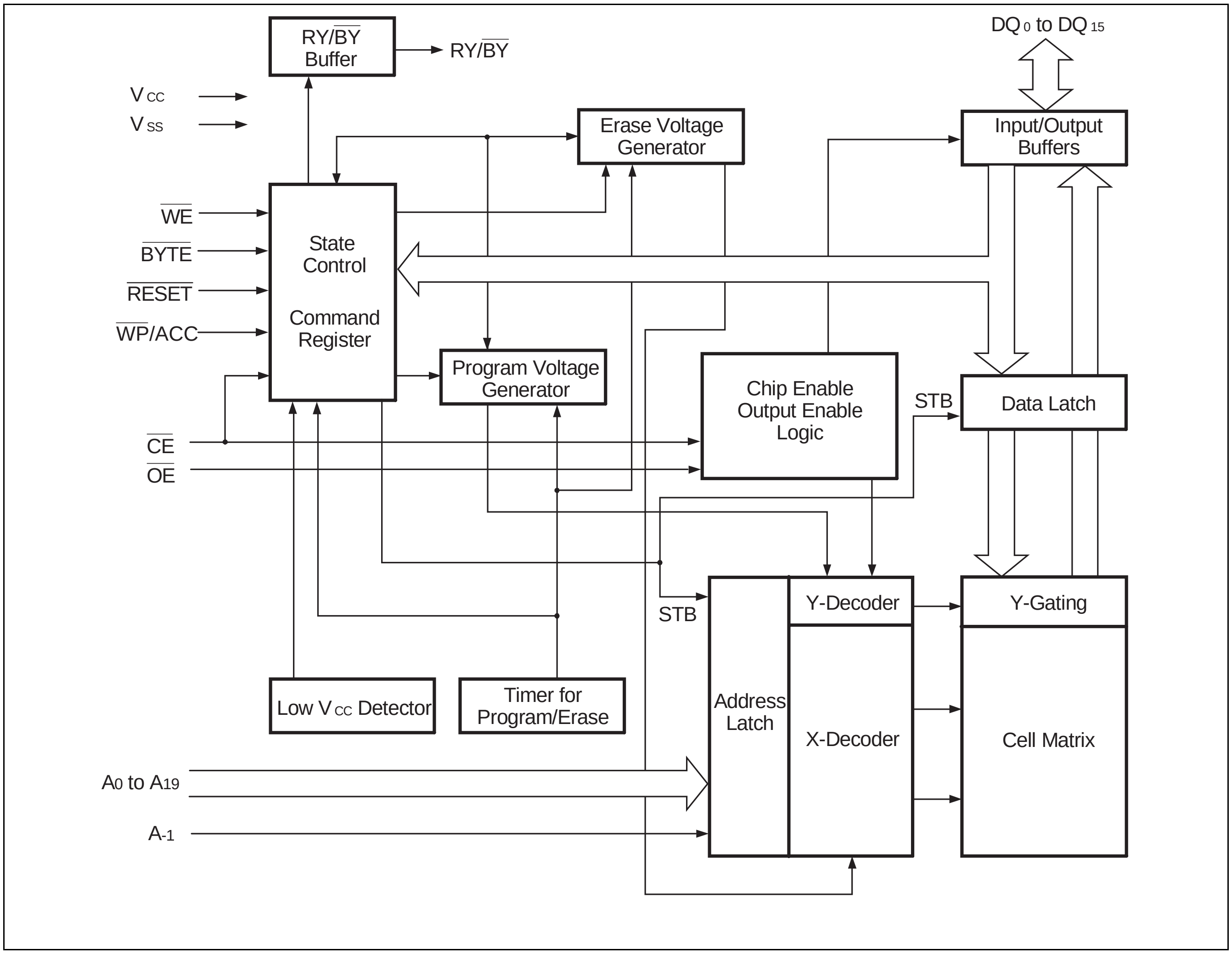
Table 2 .2 Sector Group Addresses (MBM29SL160BD) (Bottom Boot Block)

Sector Group	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	Sectors
SGA0	0	0	0	0	0	0	0	0	SA0
SGA1	0	0	0	0	0	0	0	1	SA1
SGA2	0	0	0	0	0	0	1	0	SA2
SGA3	0	0	0	0	0	0	1	1	SA3
SGA4	0	0	0	0	0	1	0	0	SA4
SGA5	0	0	0	0	0	1	0	1	SA5
SGA6	0	0	0	0	0	1	1	0	SA6
SGA7	0	0	0	0	0	1	1	1	SA7
SGA8	0	0	0	0	1	X	X	X	SA8 to SA10
	0	0	0	1	0	X	X	X	
	0	0	0	1	1	X	X	X	
SGA9	0	0	1	X	X	X	X	X	SA11 to SA14
SGA10	0	1	0	X	X	X	X	X	SA15 to SA18
SGA11	0	1	1	X	X	X	X	X	SA19 to SA22
SGA12	1	0	0	X	X	X	X	X	SA23 to SA26
SGA13	1	0	1	X	X	X	X	X	SA27 to SA30
SGA14	1	1	0	X	X	X	X	X	SA31 to SA34
SGA15	1	1	1	0	0	X	X	X	SA35 to SA37
	1	1	1	0	1	X	X	X	
	1	1	1	1	0	X	X	X	
SGA16	1	1	1	1	1	X	X	X	SA38

■ PRODUCT LINE UP

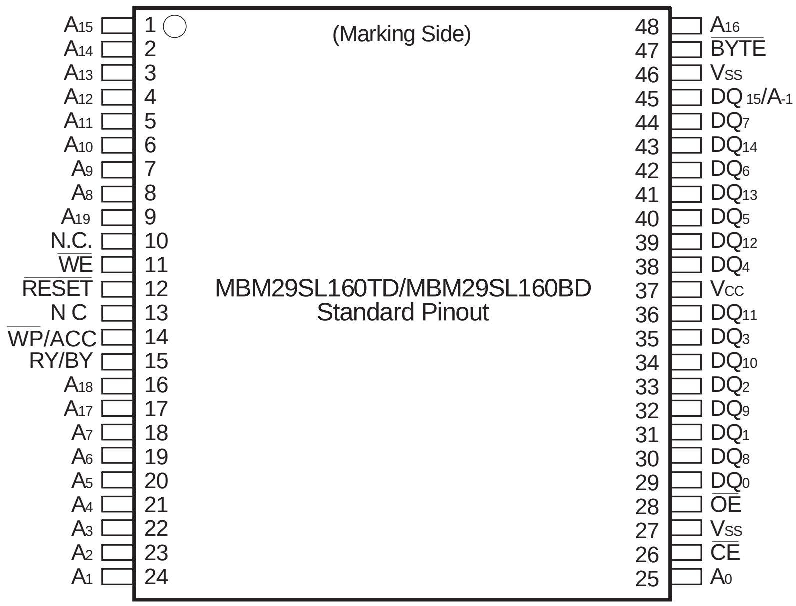
Part No.		MBM29SL160TD/MBM29SL160BD	
Ordering Part No.	V_{CC} = 2.0 V±0.2V	-10	-12
Max. Address Access Time (ns)		100	120
Max. $\overline{CE}$ Access Time (ns)		100	120
Max. $\overline{OE}$ Access Time (ns)		35	50

■ BLOCK DIAGRAM

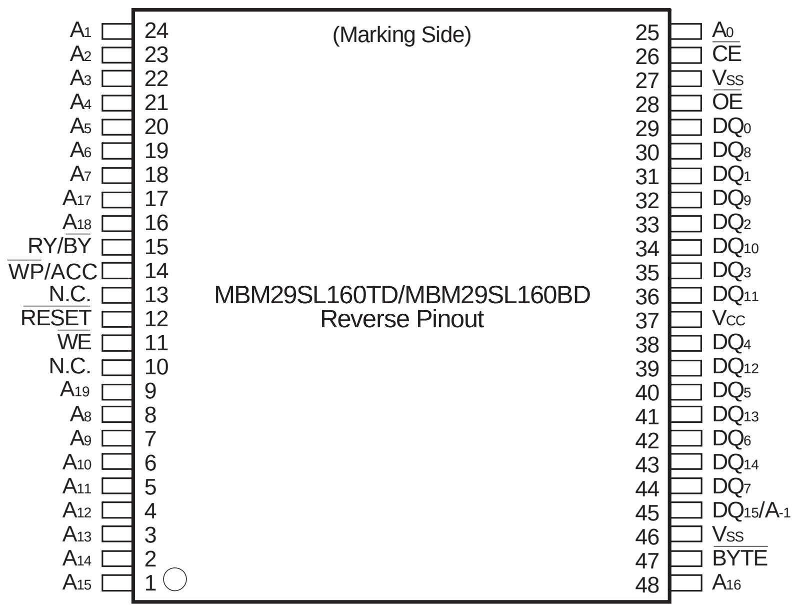


■ CONNECTION DIAGRAMS

TSOP(I)



FPT-48P-M19



FPT-48P-M20

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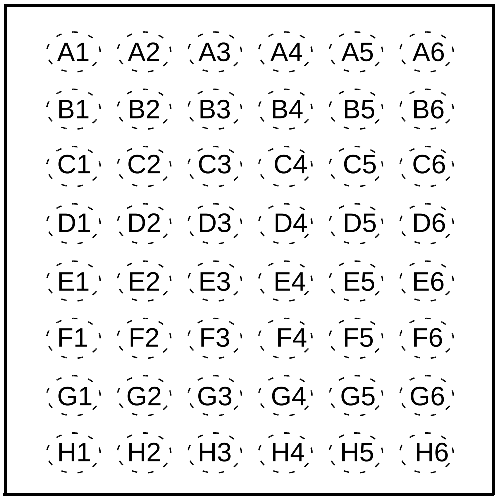
FBGA

(TOP VIEW)

Marking side



(BGA-48P-M03)

A1	A_3	A2	A_7	A3	RY/$\overline{BY}$	A4	$\overline{WE}$	A5	A_9	A6	A_{13}
B1	A_4	B2	A_{17}	B3	$\overline{WP}$/ACC	B4	$\overline{RESET}$	B5	A_8	B6	A_{12}
C1	A_2	C2	A_6	C3	A_{18}	C4	N.C.	C5	A_{10}	C6	A_{14}
D1	A_1	D2	A_5	D3	N.C.	D4	A_{19}	D5	A_{11}	D6	A_{15}
E1	A_0	E2	DQ_0	E3	DQ_2	E4	DQ_5	E5	DQ_7	E6	A_{16}
F1	$\overline{CE}$	F2	DQ_8	F3	DQ_{10}	F4	DQ_{12}	F5	DQ_{14}	F6	$\overline{BYTE}$
G1	$\overline{OE}$	G2	DQ_9	G3	DQ_{11}	G4	V_{CC}	G5	DQ_{13}	G6	DQ_{15}/A_{-1}
H1	V_{SS}	H2	DQ_1	H3	DQ_3	H4	DQ_4	H5	DQ_6	H6	V_{SS}

■ LOGIC SYMBOL

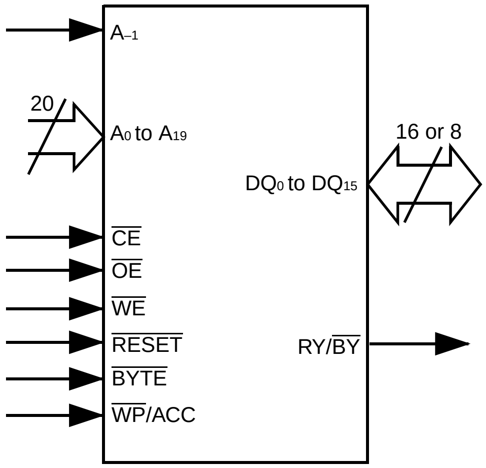


Table 3 MBM29SL160TD/BD Pin Configuration

Pin	Function
A_{-1}, A_0 to A_{19}	Address Inputs
DQ_0 to DQ_{15}	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
RY/$\overline{BY}$	Ready/Busy Output
$\overline{RESET}$	Hardware Reset Pin/Temporary Sector Group Unprotection
$\overline{BYTE}$	Selects 8-bit or 16-bit mode
$\overline{WP}$/ACC	Hardware Write Protection/Program Acceleration
N.C.	No Internal Connection
V_{SS}	Device Ground
V_{CC}	Device Power Supply

Table 4 MBM29SL160TD/BD User Bus Operations ($\overline{BYTE}$ = V_{IH})

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A_0	A_1	A_6	A_9	DQ_0 to DQ_{15}	$\overline{RESET}$	$\overline{WP}$/ACC
Auto-Select Manufacturer Code (1)	L	L	H	L	L	L	V_{ID}	Code	H	X
Auto-Select Device Code (1)	L	L	H	H	L	L	V_{ID}	Code	H	X
Read (3)	L	L	H	A_0	A_1	A_6	A_9	D_{OUT}	H	X
Standby	H	X	X	X	X	X	X	HIGH-Z	H	X
Output Disable	L	H	H	X	X	X	X	HIGH-Z	H	X
Write (Program/Erase)	L	H	L	A_0	A_1	A_6	A_9	D_{IN}	H	X
Enable Sector Group Protection (2), (4)	L	V_{ID}	⊔	L	H	L	V_{ID}	X	H	X
Verify Sector Group Protection (2), (4)	L	L	H	L	H	L	V_{ID}	Code	H	X
Temporary Sector Group Unprotection (5)	X	X	X	X	X	X	X	X	V_{ID}	X
Reset (Hardware)/Standby	X	X	X	X	X	X	X	HIGH-Z	L	X
Boot Block Sector Write Protection	X	X	X	X	X	X	X	X	X	L

Table 5 MBM29SL160TD/BD User Bus Operations ($\overline{BYTE}$ = V_{IL})

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	DQ_{15}/ A_{-1}	A_0	A_1	A_6	A_9	DQ_0 to DQ_7	$\overline{RESET}$	$\overline{WP}$/ACC
Auto-Select Manufacturer Code (1)	L	L	H	L	L	L	L	V_{ID}	Code	H	X
Auto-Select Device Code (1)	L	L	H	L	H	L	L	V_{ID}	Code	H	X
Read (3)	L	L	H	A_{-1}	A_0	A_1	A_6	A_9	D_{OUT}	H	X
Standby	H	X	X	X	X	X	X	X	HIGH-Z	H	X
Output Disable	L	H	H	X	X	X	X	X	HIGH-Z	H	X
Write (Program/Erase)	L	H	L	A_{-1}	A_0	A_1	A_6	A_9	D_{IN}	H	X
Enable Sector Group Protection (2), (4)	L	V_{ID}	⊔	L	L	H	L	V_{ID}	X	H	X
Verify Sector Group Protection (2), (4)	L	L	H	L	L	H	L	V_{ID}	Code	H	X
Temporary Sector Group Unprotection (5)	X	X	X	X	X	X	X	X	X	V_{ID}	X
Reset (Hardware)/Standby	X	X	X	X	X	X	X	X	HIGH-Z	L	X
Boot Block Sector Write Protection	X	X	X	X	X	X	X	X	X	X	L

Legend: L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}, ⊔ = Pulse input. See DC Characteristics for voltage levels.

Notes:
1. Manufacturer and device codes may also be accessed via a command register write sequence. See Table 7.
2. Refer to the section on Sector Group Protection.
3. $\overline{WE}$ can be V_{IL} if $\overline{OE}$ is V_{IL}, $\overline{OE}$ at V_{IH} initiates the write operations.
4. V_{CC} = 2.0 V ± 10%
5. It is also used for the extended sector group protection.

■ FUNCTIONAL DESCRIPTION

Read Mode

The MBM29SL160TD/BD have two control functions which must be satisfied in order to obtain data at the outputs. $\overline{CE}$ is the power control and should be used for a device selection. $\overline{OE}$ is the output control and should be used to gate data to the output pins if a device is selected.

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins. (Assuming the addresses have been stable for at least t_{ACC}-t_{OE} time.) When reading out a data without changing addresses after power-up, it is necessary to input hardware reset or to change $\overline{CE}$ pin from “H” to “L”

Standby Mode

There are two ways to implement the standby mode on the MBM29SL160TD/BD devices, one using both the $\overline{CE}$ and $\overline{RESET}$ pins; the other via the $\overline{RESET}$ pin only.

When using both pins, a CMOS standby mode is achieved with $\overline{CE}$ and $\overline{RESET}$ inputs both held at $V_{CC} \pm 0.3$ V. Under this condition the current consumed is less than 5 µA max. During Embedded Algorithm operation, V_{CC} active current (I_{CC2}) is required even $\overline{CE}$ = “H”. The device can be read with standard access time (t_{CE}) from either of these standby modes.

When using the $\overline{RESET}$ pin only, a CMOS standby mode is achieved with $\overline{RESET}$ input held at $V_{SS} \pm 0.3$ V ($\overline{CE}$ = “H” or “L”). Under this condition the current is consumed is less than 5 µA max. Once the $\overline{RESET}$ pin is taken high, the device requires t_{RH} of wake up time before outputs are valid for read access.

In the standby mode the outputs are in the high impedance state, independent of the $\overline{OE}$ input.

Automatic Sleep Mode

There is a function called automatic sleep mode to restrain power consumption during read-out of MBM29SL160TD/BD data. This mode can be used effectively with an application requested low power consumption such as handy terminals.

To activate this mode, MBM29SL160TD/BD automatically switch themselves to low power mode when MBM29SL160TD/BD addresses remain stably during access fine of 150 ns. It is not necessary to control $\overline{CE}$, $\overline{WE}$, and $\overline{OE}$ on the mode. Under the mode, the current consumed is typically 1 µA (CMOS Level).

During simultaneous operation, V_{CC} active current (I_{CC2}) is required.

Since the data are latched during this mode, the data are read-out continuously. If the addresses are changed, the mode is canceled automatically and MBM29SL160TD/BD read-out the data for changed addresses.

Output Disable

With the $\overline{OE}$ input at a logic high level (V_{IH}), output from the devices are disabled. This will cause the output pins to be in a high impedance state.

Autoselect

The autoselect mode allows the reading out of a binary code from the devices and will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the devices to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the devices.

To activate this mode, the programming equipment must force V_{ID} (10 V to 11 V) on address pin A_9. Two identifier bytes may then be sequenced from the devices outputs by toggling address A_0 from V_{IL} to V_{IH}. All addresses are DON’T CARES except A_0, A_1, and A_6 (A_{-1}). (See Tables 4 and 5.)

The manufacturer and device codes may also be read via the command register, for instances when the MBM29SL160TD/BD are erased or programmed in a system without access to high voltage on the A_9 pin. The command sequence is illustrated in Table 7. (Refer to Autoselect Command section.)

Word 0 ($A_0 = V_{IL}$) represents the manufacturer's code (Fujitsu = 04H) and word 1 ($A_0 = V_{IH}$) represents the device identifier code (MBM29SL160TD = E4H and MBM29SL160BD = E7H for ×8 mode; MBM29SL160TD = 22E4H and MBM29SL160BD = 22E7H for ×16 mode). These two bytes/words are given in the tables 6.1 to 6.2. All identifiers for manufactures and device will exhibit odd parity with DQ_7 defined as the parity bit. In order to read the proper device codes when executing the autoselect, A_1 must be V_{IL}. (See Tables 6.1 to 6.2.)

Table 6 .1 MBM29SL160TD/BD Sector Group Protection Verify Autoselect Codes

Type			A_{12} to A_{19}	A_6	A_1	A_0	A_{-1}*1	Code (HEX)
Manufacture's Code			X	V_{IL}	V_{IL}	V_{IL}	V_{IL}	04H
Device Code	MBM29SL160TD	Byte	X	V_{IL}	V_{IL}	V_{IH}	V_{IL}	E4H
		Word					X	22E4H
	MBM29SL160BD	Byte	X	V_{IL}	V_{IL}	V_{IH}	V_{IL}	E7H
		Word					X	22E7H
Sector Group Protection			Sector Group Addresses	V_{IL}	V_{IH}	V_{IL}	V_{IL}	01H*2

*1: A_{-1} is for Byte mode.

*2: Outputs 01H at protected sector group addresses and outputs 00H at unprotected sector group addresses.

Table 6 .2 Expanded Autoselect Code Table

Type			Code	DQ_{15}	DQ_{14}	DQ_{13}	DQ_{12}	DQ_{11}	DQ_{10}	DQ_9	DQ_8	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
Manufacturer's Code			04H	A_{-1}/0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
Device Code	MBM29SL160TD	(B)	E4H	A_{-1}	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	1	1	1	0	0	1	0	0
		(W)	22E4H	0	0	1	0	0	0	1	0	1	1	1	0	0	1	0	0
	MBM29SL160BD	(B)	E7H	A_{-1}	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	1	1	1	0	0	1	1	1
		(W)	22E7H	0	0	1	0	0	0	1	0	1	1	1	0	0	1	1	1
Sector Group Protection			01H	A_{-1}/0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

(B): Byte mode
(W): Word mode

Write

Device erasure and programming are accomplished via the command register. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device.

The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The command register is written by bringing $\overline{WE}$ to V_{IL}, while $\overline{CE}$ is at V_{IL} and $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happens later; while data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever happens first. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

Sector Group Protection

The MBM29SL160TD/BD feature hardware sector group protection. This feature will disable both program and erase operations in any combination of seventeen sector groups of memory. (See Tables 2.1 and 2.2). The sector group protection feature is enabled using programming equipment at the user's site. The device is shipped with all sector groups unprotected.

To activate this mode, the programming equipment must force V_{ID} on address pin A_9 and control pin $\overline{OE}$, (suggest V_{ID} = 10V to 11V), $\overline{CE}$ = V_{IL} and A_0 = A_6 = V_{IL}, A_1 = V_{IH}. The sector group addresses (A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, and A_{12}) should be set to the sector to be protected. Tables 1.1 and 1.2 define the sector address for each of the thirty nine (39) individual sectors, and tables 2.1 and 2.2 define the sector group address for each of the seventeen (17) individual group sectors. Programming of the protection circuitry begins on the falling edge of the $\overline{WE}$ pulse and is terminated with the rising edge of the same. Sector group addresses must be held constant during the $\overline{WE}$ pulse. See figures 16 and 25 for sector group protection waveforms and algorithm.

To verify programming of the protection circuitry, the programming equipment must force V_{ID} on address pin A_9 with $\overline{CE}$ and $\overline{OE}$ at V_{IL} and $\overline{WE}$ at V_{IH}. Scanning the sector group addresses (A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, and A_{12}) while (A_6, A_1, A_0) = (0, 1, 0) will produce a logical “1” code at device output DQ_0 for a protected sector. Otherwise the device will produce “0” for unprotected sector. In this mode, the lower order addresses, except for A_0, A_1, and A_6 are DON'T CARES. Address locations with A_1 = V_{IL} are reserved for Autoselect manufacturer and device codes. A_{-1} requires to apply to V_{IL} on byte mode.

It is also possible to determine if a sector group is protected in the system by writing an Autoselect command. Performing a read operation at the address location XX02H, where the higher order addresses (A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, and A_{12}) are the desired sector group address will produce a logical “1” at DQ_0 for a protected sector group. See Tables 6.1 and 6.2 for Autoselect codes.

Temporary Sector Group Unprotection

This feature allows temporary unprotection of previously protected sector groups of the MBM29SL160TD/BD devices in order to change data. The Sector Group Unprotection mode is activated by setting the $\overline{RESET}$ pin to high voltage (V_{ID}). During this mode, formerly protected sector groups can be programmed or erased by selecting the sector group addresses. Once the V_{ID} is taken away from the $\overline{RESET}$ pin, all the previously protected sector groups will be protected again. Refer to Figures 17 and 26.

$\overline{\text{RESET}}$

Hardware Reset

The MBM29SL160TD/BD devices may be reset by driving the $\overline{\text{RESET}}$ pin to V_{IL}. The $\overline{\text{RESET}}$ pin has a pulse requirement and has to be kept low (V_{IL}) for at least "t_{RP}" in order to properly reset the internal state machine. Any operation in the process of being executed will be terminated and the internal state machine will be reset to the read mode "t_{READY}" after the $\overline{\text{RESET}}$ pin is driven low. Furthermore, once the $\overline{\text{RESET}}$ pin goes high, the devices require an additional "t_{RH}" before it will allow read access. When the $\overline{\text{RESET}}$ pin is low, the devices will be in the standby mode for the duration of the pulse and all the data output pins will be tri-stated. If a hardware reset occurs during a program or erase operation, the data at that particular location will be corrupted. Please note that the RY/$\overline{\text{BY}}$ output signal should be ignored during the $\overline{\text{RESET}}$ pulse. See Figure 12 for the timing diagram. Refer to Temporary Sector Group Unprotection for additional functionality.

Boot Block Sector Protection

The Write Protection function provides a hardware method of protecting certain boot sectors without using V_{ID}. This function is one of two provided by the $\overline{\text{WP}}$/ACC pin.

If the system asserts V_{IL} on the $\overline{\text{WP}}$/ACC pin, the device disables program and erase functions in the two "outermost" 8K byte boot sectors independently of whether those sectors were protected or unprotected using the method described in "Sector Protection/Unprotection". The two outermost 8K byte boot sectors are the two sectors containing the lowest addresses in a bottom-boot-configured device, or the two sectors containing the highest addresses in a top-boot-congfigured device.
(MBM29SL160TD: SA37 and SA38, MBM29SL160BD: SA0 and SA1)

If the system asserts V_{IH} on the $\overline{\text{WP}}$/ACC pin, the device reverts to whether the two outermost 8K byte boot sectors were last set to be protected or unprotected. That is, sector protection or unprotection for these two sectors depends on whether they were last protected or unprotected using the method described in "Sector protection/unprotection".

Accelerated Program Operation

The device offers accelerated program operations through the ACC function. This is one of two functions provided by the $\overline{\text{WP}}$/ACC pin. This function is primarily intended to allow faster factory throughput by 50 percent.

If the system asserts V_{HH} on this pin, the device automatically enters the after mentioned Fast mode, temporarily unprotects any protected sectors, and uses the higher voltage on the pin to reduce the time required for program operations. The system would use a two-cycle program command sequence as required by the Fast mode. Removing V_{HH} from the $\overline{\text{WP}}$/ACC pin returns the device to normal operation.

If you use this function, please contact a Fujitsu representative for more information.

Table 7 MBM29SL160TD/BD Command Definitions

Command Sequence		Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
			Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
Read/Reset	Word	1	XXXH	F0H	—	—	—	—	—	—	—	—	—	—
	Byte													
Read/Reset	Word	3	555H	AAH	2AAH	55H	555H	F0H	RA	RD	—	—	—	—
	Byte		AAAH		555H		AAAH							
Autoselect	Word	3	555H	AAH	2AAH	55H	555H	90H	—	—	—	—	—	—
	Byte		AAAH		555H		AAAH							
Program	Word	4	555H	AAH	2AAH	55H	555H	A0H	PA	PD	—	—	—	—
	Byte		AAAH		555H		AAAH							
Chip Erase	Word	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	555H	10H
	Byte		AAAH		555H		AAAH		AAAH		555H		AAAH	
Sector Erase	Word	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	SA	30H
	Byte		AAAH		555H		AAAH		AAAH		555H			
Erase Suspend		1	XXXH	B0H	—	—	—	—	—	—	—	—	—	—
Erase Resume		1	XXXH	30H	—	—	—	—	—	—	—	—	—	—
Set to Fast Mode	Word	3	555H	AAH	2AAH	55H	555H	20H	—	—	—	—	—	—
	Byte		AAAH		555H		AAAH							
Fast Program *1	Word	2	XXXH	A0H	PA	PD	—	—	—	—	—	—	—	—
	Byte		XXXH											
Reset from Fast Mode *1	Word	2	XXXH	90H	XXXH	F0H *5	—	—	—	—	—	—	—	—
	Byte		XXXH		XXXH									
Extended Sector Group Protection *2	Word	4	XXXH	60H	SPA	60H	SPA	40H	SPA	SD	—	—	—	—
	Byte													
Query *3	Word	1	55H	98H	—	—	—	—	—	—	—	—	—	—
	Byte		AAH											
OTP Entry	Word	3	555H	AAH	2AAH	55H	555H	88H	—	—	—	—	—	—
	Byte		AAAH		555H		AAAH							
OTP Program *4	Word	4	555H	AAH	2AAH	55H	555H	A0H	PA	PD	—	—	—	—
	Byte		AAAH		555H		AAAH							
OTP Exit *4	Word	4	555H	AAH	2AAH	55H	555H	90H	XXXH	00H	—	—	—	—
	Byte		AAAH		555H		AAAH							

Notes: 1. Address bits A_{11} to A_{19} = X = “H” or “L” for all address commands except or Program Address (PA), Sector Address (SA).

2. Bus operations are defined in Tables 4 and 5.
3. RA = Address of the memory location to be read
   PA = Address of the memory location to be programmed
   Addresses are latched on the falling edge of the write pulse.
   SA = Address of the sector to be erased. The combination of A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, and A_{12} will uniquely select any sector.
4. RD = Data read from location RA during read operation.
   PD = Data to be programmed at location PA. Data is latched on the falling edge of write pulse.
5. SPA = Sector group address to be protected. Set sector group address (SGA) and (A_6, A_1, A_0) = (0, 1, 0).
   SD = Sector group protection verify data. Output 01H at protected sector group addresses and output 00H at unprotected sector group addresses.
6. OTPA = Address of the OTP area

29SL160TD (Top Boot Type)	Word Mode:	FFF7FH to FFFFFH
	Byte Mode:	1FFEFFH to 1FFFFFH
29SL160BD (Bottom Boot Type)	Word Mode:	00000H to 00080H
	Byte Mode:	00000H to 00100H

*1: This command is valid while Fast Mode.
*2: This command is valid while $\overline{\text{RESET}}$ = V_{ID}.
*3: The valid addresses are A_6 to A_0.
*4: This command is valid while OTP mode.
*5: The data "00H" is also acceptable.

7. The system should generate the following address patterns:
   Word Mode: 555H or 2AAH to addresses A_0 to A_{10}
   Byte Mode: AAAH or 555H to addresses A_{-1} and A_0 to A_{10}
8. Both Read/Reset commands are functionally equivalent, resetting the device to the read mode.

■ Command Definitions

Device operations are selected by writing specific address and data sequences into the command register. Writing incorrect address and data values or writing them in the improper sequence will reset the devices to the read mode. Table 7 defines the valid register command sequences. Note that the Erase Suspend (B0H) and Erase Resume (30H) commands are valid only while the Sector Erase operation is in progress. Moreover both Read/Reset commands are functionally equivalent, resetting the device to the read mode. Please note that commands are always written at DQ_0 to DQ_7 and DQ_8 to DQ_{15} bits are ignored.

Read/Reset Command

In order to return from Autoselect mode or Exceeded Timing Limits (DQ_5 = 1) to Read/Reset mode, the Read/Reset operation is initiated by writing the Read/Reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory. The devices remain enabled for reads until the command register contents are altered.

The devices will automatically power-up in the Read/Reset state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of the memory content occurs during the power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

Autoselect Command

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufacture and device codes must be accessible while the devices reside in the target system. PROM programmers typically access the signature codes by raising A_9 to a high voltage. However, multiplexing high voltage onto the address lines is not generally desired system design practice.

The device contains an Autoselect command operation to supplement traditional PROM programming methodology. The operation is initiated by writing the Autoselect command sequence into the command register.

Following the command write, a read cycle from address (XX)00H retrieves the manufacture code of 04H. A read cycle from address (XX)01H for ×16((XX)02H for ×8) returns the device code (MBM29SL160TD = E4H and MBM29SL160BD = E7H for ×8 mode; MBM29SL160TD = 22E4H and MBM29SL160BD = 22E7H for ×16 mode), (See Tables 6.1 and 6.2.)

All manufacturer and device codes will exhibit odd parity with DQ_7 defined as the parity bit. Sector state (protection or unprotection) will be informed by address (XX)02H for ×16 ((XX)04H for ×8). Scanning the sector group addresses (A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, and A_{12}) while (A_6, A_1, A_0) = (0, 1, 0) will produce a logical "1" at device output DQ_0 for a protected sector group. The programming verification should be performed by verify sector group protection on the protected sector. (See Tables 4 and 5.)

To terminate the operation, it is necessary to write the Read/Reset command sequence into the register, and also to write the Autoselect command during the operation, execute it after writing Read/Reset command sequence.

Byte/Word Programming

The devices are programmed on a byte-by-byte (or word-by-word) basis. Programming is a four bus cycle operation. There are two "unlock" write cycles. These are followed by the program set-up command and data write cycles. Addresses are latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever happens later and the data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever happens first. The rising edge of $\overline{CE}$ or $\overline{WE}$ (whichever happens first) begins programming. Upon executing the Embedded Program Algorithm command sequence, the system is not required to provide further controls or timings. The device will automatically provide adequate internally generated program pulses and verify the programmed cell margin.

The system can determine the status of the program operation by using DQ_7 (Data Polling), DQ_6 (Toggle Bit), or RY/BY. The Data Polling and Toggle Bit must be performed at the memory location which is being programmed.

The automatic programming operation is completed when the data on DQ_7 is equivalent to data written to this bit at which time the devices return to the read mode and addresses are no longer latched. (See Table 13, Hardware Sequence Flags.) Therefore, the devices require that a valid address to the devices be supplied by the system at this particular instance of time. Hence, Data Polling must be performed at the memory location which is being programmed.

Any commands written to the chip during this period will be ignored. If hardware reset occurs during the programming operation, it is impossible to guarantee the data are being written.

Programming is allowed in any sequence and across sector boundaries. Beware that a data “0” cannot be programmed back to a “1”. Attempting to do so may either hang up the device or result in an apparent success according to the data polling algorithm but a read from Read/Reset mode will show that the data is still “0”. Only erase operations can convert “0”s to “1”s.

Figure 21 illustrates the Embedded Program™ Algorithm using typical command strings and bus operations.

Chip Erase

Chip erase is a six bus cycle operation. There are two “unlock” write cycles. These are followed by writing the “set-up” command. Two more “unlock” write cycles are then followed by the chip erase command.

Chip erase does not require the user to program the device prior to erase. Upon executing the Embedded Erase Algorithm command sequence the devices will automatically program and verify the entire memory for an all zero data pattern prior to electrical erase (Preprogram function). The system is not required to provide any controls or timings during these operations.

The system can determine the status of the erase operation by using DQ_7 (Data Polling), DQ_6 (Toggle Bit), or RY/BY. The chip erase begins on the rising edge of the last CE or WE, whichever happens first in the command sequence and terminates when the data on DQ_7 is “1” (See Write Operation Status section.) at which time the device returns to read the mode.

Chip Erase Time; Sector Erase Time × All sectors + Chip Program Time (Preprogramming)

Figure 22 illustrates the Embedded Erase™ Algorithm using typical command strings and bus operations.

Sector Erase

Sector erase is a six bus cycle operation. There are two “unlock” write cycles. These are followed by writing the “set-up” command. Two more “unlock” write cycles are then followed by the Sector Erase command. The sector address (any address location within the desired sector) is latched on the falling edge of CE or WE whichever happens later, while the command (Data = 30H) is latched on the rising edge of CE or WE which happens first. After time-out of 50µs from the rising edge of the last sector erase command, the sector erase operation will begin.

Multiple sectors may be erased concurrently by writing the six bus cycle operations on Table 7. This sequence is followed with writes of the Sector Erase command to addresses in other sectors desired to be concurrently erased. The time between writes must be less than 50µs otherwise that command will not be accepted and erasure will start. It is recommended that processor interrupts be disabled during this time to guarantee this condition. The interrupts can be re-enabled after the last Sector Erase command is written. A time-out of 50µs from the rising edge of last CE or WE whichever happens first will initiate the execution of the Sector Erase command(s). If another falling edge of CE or WE, whichever happens first occurs within the 50µs time-out window the timer is reset. (Monitor DQ_3 to determine if the sector erase timer window is still open, see section DQ_3, Sector Erase Timer.) Any command other than Sector Erase or Erase Suspend during this time-out period will reset the devices to the read mode, ignoring the previous command string. Resetting the devices once execution has begun will corrupt the data in the sector. In that case, restart the erase on those sectors and allow them to complete. (Refer to the Write Operation Status section for Sector Erase Timer operation.) Loading the sector erase buffer may be done in any sequence and with any number of sectors (0 to 38).

Sector erase does not require the user to program the devices prior to erase. The devices automatically program all memory locations in the sector(s) to be erased prior to electrical erase (Preprogram function). When erasing a sector or sectors the remaining unselected sectors are not affected. The system is not required to provide any controls or timings during these operations.

The system can determine the status of the erase operation by using DQ_7 ($\overline{\text{Data}}$ Polling), DQ_6 (Toggle Bit), or RY/$\overline{\text{BY}}$.

The sector erase begins after the 50µs time out from the rising edge of $\overline{\text{CE}}$ or $\overline{\text{WE}}$ whichever happens first for the last sector erase command pulse and terminates when the data on DQ_7 is "1" (See Write Operation Status section.) at which time the devices return to the read mode. $\overline{\text{Data}}$ polling and Toggle Bit must be performed at an address within any of the sectors being erased.

Multiple Sector Erase Time; [Sector Erase Time + Sector Program Time (Preprogramming)] × Number of Sector Erase

Figure 22 illustrates the Embedded Erase™ Algorithm using typical command strings and bus operations.

Erase Suspend/Resume

The Erase Suspend command allows the user to interrupt a Sector Erase operation and then perform data reads from or programs to a sector not being erased. This command is applicable ONLY during the Sector Erase operation which includes the time-out period for sector erase. The Erase Suspend command will be ignored if written during the Chip Erase operation or Embedded Program Algorithm. Writting the Erase Suspend command (B0H) during the Sector Erase time-out results in immediate termination of the time-out period and suspension of the erase operation.

Writing the Erase Resume command (30H) resumes the erase operation. The address are DON'T CARES when writing the Erase Suspend or Erase Resume command (30H).

When the Erase Suspend command is written during the Sector Erase operation, the device will take a maximum of 20µs to suspend the erase operation. When the devices have entered the erase-suspended mode, the RY/$\overline{\text{BY}}$ output pin will be at Hi-Z and the DQ_7 bit will be at logic "1", and DQ_6 will stop toggling. The user must use the address of the erasing sector for reading DQ_6 and DQ_7 to determine if the erase operation has been suspended. Further writes of the Erase Suspend command are ignored.

When the erase operation has been suspended, the devices default to the erase-suspend-read mode. Reading data in this mode is the same as reading from the standard read mode except that the data must be read from sectors that have not been erase-suspended. Successively reading from the erase-suspended sector while the device is in the erase-suspend-read mode will cause DQ_2 to toggle. (See the section on DQ_2.)

After entering the erase-suspend-read mode, the user can program the device by writing the appropriate command sequence for Program. This program mode is known as the erase-suspend-program mode. Again, programming in this mode is the same as programming in the regular Program mode except that the data must be programmed to sectors that are not erase-suspended. Successively reading from the erase-suspended sector while the devices are in the erase-suspend-program mode will cause DQ_2 to toggle. The end of the erase-suspended Program operation is detected by the RY/$\overline{\text{BY}}$ output pin, $\overline{\text{Data}}$ polling of DQ_7 or by the Toggle Bit I (DQ_6) which is the same as the regular Program operation. Note that DQ_7 must be read from the Program address while DQ_6 can be read from any address.

To resume the operation of Sector Erase, the Resume command (30H) should be written. Any further writes of the Resume command at this point will be ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

Extended Command

(1) Fast Mode

MBM29SL160TD/BD has Fast Mode function. This mode dispenses with the initial two unclock cycles required in the standard program command sequence by writing Fast Mode command into the command register. In this mode, the required bus cycle for programming is two cycles instead of four bus cycles in standard program command. (Do not write erase command in this mode.) The read operation is also executed after exiting this mode. To exit this mode, it is necessary to write Fast Mode Reset command into the command register. (Refer to the Figure 27.) The V_{CC} active current is required even $\overline{CE} = V_{IH}$ during Fast Mode.

(2) Fast Programming

During Fast Mode, the programming can be executed with two bus cycles operation. The Embedded Program Algorithm is executed by writing program set-up command (A0H) and data write cycles (PA/PD). (Refer to the Figure 27.)

(3) Extended Sector Group Protection

In addition to normal sector group protection, the MBM29SL160TD/BD has Extended Sector Group Protection as extended function. This function enable to protect sector group by forcing V_{ID} on $\overline{RESET}$ pin and write a command sequence. Unlike conventional procedure, it is not necessary to force V_{ID} and control timing for control pins. The only $\overline{RESET}$ pin requires V_{ID} for sector group protection in this mode. The extended sector group protection requires V_{ID} on $\overline{RESET}$ pin. With this condition, the operation is initiated by writing the set-up command (60H) into the command register. Then, the sector group addresses pins (A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13} and A_{12}) and (A_6, A_1, A_0) = (0, 1, 0) should be set to the sector group to be protected (recommend to set V_{IL} for the other addresses pins), and write extended sector group protection command (60H). A sector group is typically protected in 150 µs. To verify programming of the protection circuitry, the sector group addresses pins (A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13} and A_{12}) and (A_6, A_1, A_0) = (0, 1, 0) should be set and write a command (40H). Following the command write, a logical "1" at device output DQ_0 will produce for protected sector in the read operation. If the output data is logical "0", please repeat to write extended sector group protection command (60H) again. To terminate the operation, it is necessary to set $\overline{RESET}$ pin to V_{IH}. (Refer to the Figures 19 and 28.)

(4) CFI (Common Flash Memory Interface)

The CFI (Common Flash Memory Interface) specification outlines device and host system software interrogation handshake which allows specific vendor-specified software algorithms to be used for entire families of devices. This allows device-independent, JEDEC ID-independent, and forward-and backward-compatible software support for the specified flash device families. Refer to CFI specification in detail.

The operation is initiated by writing the query command (98H) into the command register. Following the command write, a read cycle from specific address retrives device information. Please note that output data of upper byte (DQ_8 to DQ_{15}) is "0" in word mode (16 bit) read. Refer to the CFI code table. To terminate operation, it is necessary to write the read/reset command sequence into the register. (See Table 15.)

One Time Protect (OTP) Region

The OTP feature provides a Flash memory region that the system may access through a new command sequence. This is primarily intended for customers who wish to use an Electronic Serial Number (ESN) in the device with the ESN protected against modification. Once the OTP region is protected, any further modification of that region is impossible. This ensures the security of the ESN once the product is shipped to the field.

The OTP region is 256 bytes in length. The MBM29SL160TD occupies the address of the byte mode 1FFEFFH to 1FFFFFH (word mode FFF7FH to FFFFFH) and the MBM29SL160BD type occupies the address of the byte mode 00000H to 00100H (word mode 00000H to 00080H). After the system has written the Enter OTP command sequence, the system may read the OTP region by using the addresses normally occupied by the boot sectors. That is, the device sends all commands that would normally be sent to the boot sectors to the OTP region. This mode of operation continues until the system issues the Exit OTP command sequence, or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to sending commands to the boot sectors.

If you request Fujitsu to program the ESN in the device, please contact a Fujitsu representative for more information.

Write Operarion Status

Table 8 Hardware Sequence Flags

Status			DQ_7	DQ_6	DQ_5	DQ_3	DQ_2
In Progress	Embedded Program Algorithm		$\overline{DQ_7}$	Toggle	0	0	1
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle (Note 2)
	Erase Suspended Mode	Erase Suspend Read (Erase Suspended Sector)	1	1	0	0	Toggle
		Erase Suspend Read (Non-Erase Suspended Sector)	Data	Data	Data	Data	Data
		Erase Suspend Program (Non-Erase Suspended Sector)	$\overline{DQ_7}$	Toggle (Note 1)	0	0	1 (Note 2)
Exceeded Time Limits	Embedded Program Algorithm		$\overline{DQ_7}$	Toggle	1	0	1
	Embedded Erase Algorithm		0	Toggle	1	1	N/A
	Erase Suspended Mode	Erase Suspend Program (Non-Erase Suspended Sector)	$\overline{DQ_7}$	Toggle	1	0	N/A

Notes: 1. Performing successive read operetions from any address will cause DQ_6 to toggle.
2. Reading the byte address being programmed while in the erase-suspend program mode will indicate logic "1" at the DQ_2 bit. However, successive reads from the erase-suspend sector will cause DQ_2 to toggle.
3. DQ_0 and DQ_1 are reserve pins for future use.
4. DQ_4 is Fujitsu internal use only

DQ_7

$\overline{\text{Data}}$ Polling

The MBM29SL160TD/BD devices feature $\overline{\text{Data}}$ Polling as a method to indicate to the host that the Embedded Algorithms are in progress or completed. During the Embedded Program Algorithm an attempt to read the devices will produce the complement of the data last written to DQ_7. Upon completion of the Embedded Program Algorithm, an attempt to read the device will produce the true data last written to DQ_7. During the Embedded Erase Algorithm, an attempt to read the device will produce a “0” at the DQ_7 output. Upon completion of the Embedded Erase Algorithm an attempt to read the device will produce a “1” at the DQ_7 output. The flowchart for $\overline{\text{Data}}$ Polling (DQ_7) is shown in Figure 23.

For programming, the $\overline{\text{Data}}$ Polling is valid after the rising edge of fourth write pulse in the four write pulse sequence.

For chip erase and sector erase, the $\overline{\text{Data}}$ Polling is valid after the rising edge of the sixth write pulse in the six write pulse sequence. $\overline{\text{Data}}$ Polling must be performed at sector address within any of the sectors being erased and not a protected sector. Otherwise, the status may not be valid.

Once the Embedded Algorithm operation is close to being completed, the MBM29SL160TD/BD data pins (DQ_7) may change asynchronously while the output enable ($\overline{\text{OE}}$) is asserted low. This means that the devices are driving status information on DQ_7 at one instant of time and then that byte’s valid data at the next instant of time. Depending on when the system samples the DQ_7 output, it may read the status or valid data. Even if the device has completed the Embedded Algorithm operation and DQ_7 has a valid data, the data outputs on DQ_0 to DQ_6 may be still invalid. The valid data on DQ_0 to DQ_7 will be read on the successive read attempts.

The $\overline{\text{Data}}$ Polling feature is only active during the Embedded Programming Algorithm, Embedded Erase Algorithm or sector erase time-out. (See Table 8.)

See Figure 9 for the $\overline{\text{Data}}$ Polling timing specifications and diagrams.

DQ_6

Toggle Bit I

The MBM29SL160TD/BD also feature the “Toggle Bit I” as a method to indicate to the host system that the Embedded Algorithms are in progress or completed.

During an Embedded Program or Erase Algorithm cycle, successive attempts to read ($\overline{\text{OE}}$ toggling) data from the devices will result in DQ_6 toggling between one and zero. Once the Embedded Program or Erase Algorithm cycle is completed, DQ_6 will stop toggling and valid data will be read on the next successive attempts. During programming, the Toggle Bit I is valid after the rising edge of the fourth write pulse in the four write pulse sequence. For chip erase and sector erase, the Toggle Bit I is valid after the rising edge of the sixth write pulse in the six write pulse sequence. The Toggle Bit I is active during the sector time out.

In programming, if the sector being written to is protected, the toggle bit will toggle for about 1 µs and then stop toggling without the data having changed. In erase, the devices will erase all the selected sectors except for the ones that are protected. If all selected sectors are protected, the chip will toggle the toggle bit for about 400 µs and then drop back into read mode, having changed none of the data.

Either $\overline{\text{CE}}$ or $\overline{\text{OE}}$ toggling will cause the DQ_6 to toggle. In addition, an Erase Suspend/Resume command will cause the DQ_6 to toggle. See Figure 10 for the Toggle Bit I timing specifications and diagrams.

DQ_5

Exceeded Timing Limits

DQ_5 will indicate if the program or erase time has exceeded the specified limits (internal pulse count). Under these conditions DQ_5 will produce a "1". This is a failure condition which indicates that the program or erase cycle was not successfully completed. $\overline{\text{Data}}$ Polling is the only operating function of the devices under this condition. The $\overline{CE}$ circuit will partially power down the device under these conditions (to approximately 2 mA). The $\overline{OE}$ and $\overline{WE}$ pins will control the output disable functions as described in Tables 4 and 5.

The DQ_5 failure condition may also appear if a user tries to program a non blank location without erasing. In this case the devices lock out and never complete the Embedded Algorithm operation. Hence, the system never reads a valid data on DQ_7 bit and DQ_6 never stops toggling. Once the devices have exceeded timing limits, the DQ_5 bit will indicate a "1." Please note that this is not a device failure condition since the devices were incorrectly used. If this occurs, reset the device with command sequence.

DQ_3

Sector Erase Timer

After the completion of the initial sector erase command sequence the sector erase time-out will begin. DQ_3 will remain low until the time-out is complete. $\overline{\text{Data}}$ Polling and Toggle Bit are valid after the initial sector erase command sequence.

If $\overline{\text{Data}}$ Polling or the Toggle Bit I indicates the device has been written with a valid erase command, DQ_3 may be used to determine if the sector erase timer window is still open. If DQ_3 is high ("1") the internally controlled erase cycle has begun; attempts to write subsequent commands to the device will be ignored until the erase operation is completed as indicated by $\overline{\text{Data}}$ Polling or Toggle Bit I. If DQ_3 is low ("0"), the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of DQ_3 prior to and following each subsequent Sector Erase command. If DQ_3 were high on the second status check, the command may not have been accepted.

See Table 8: Hardware Sequence Flags.

DQ_2

Toggle Bit II

This toggle bit II, along with DQ_6, can be used to determine whether the devices are in the Embedded Erase Algorithm or in Erase Suspend.

Successive reads from the erasing sector will cause DQ_2 to toggle during the Embedded Erase Algorithm. If the devices are in the erase-suspended-read mode, successive reads from the erase-suspended sector will cause DQ_2 to toggle. When the devices are in the erase-suspended-program mode, successive reads from the byte address of the non-erase suspended sector will indicate a logic "1" at the DQ_2 bit.

DQ_6 is different from DQ_2 in that DQ_6 toggles only when the standard program or Erase, or Erase Suspend Program operation is in progress. The behavior of these two status bits, along with that of DQ_7, is summarized as follows:

For example, DQ_2 and DQ_6 can be used together to determine if the erase-suspend-read mode is in progress. (DQ_2 toggles while DQ_6 does not.) See also Table 9 and Figure 18.

Furthermore, DQ_2 can also be used to determine which sector is being erased. When the device is in the erase mode, DQ_2 toggles if this bit is read from an erasing sector.

Table 9 Toggle Bit Status

Mode	DQ_7	DQ_6	DQ_2
Program	$\overline{DQ_7}$	Toggle	1
Erase	0	Toggle	Toggle
Erase-Suspend Read (Erase-Suspended Sector)	1	1	Toggle
Erase-Suspend Program	$\overline{DQ_7}$	Toggle (Note 1)	1 (Note 2)

Note: 1.Performing successive read operetions from any address will cause DQ_6 to toggle.
2.Reading the byte address being programmed while in the erase-suspend program mode will indicate logic "1" at the DQ_2 bit. However, successive reads from the erase-suspend sector will cause DQ_2 to toggle.

RY/$\overline{\text{BY}}$

Ready/Busy

The MBM29SL160TD/BD provide a RY/$\overline{\text{BY}}$ open-drain output pin as a way to indicate to the host system that the Embedded Algorithms are either in progress or has been completed. If the output is low, the devices are busy with either a program or erase operation. If the output is high, the devices are ready to accept any read/ write or erase operation. When the RY/$\overline{\text{BY}}$ pin is low, the devices will not accept any additional program or erase commands. If the MBM29SL160TD/BD are placed in an Erase Suspend mode, the RY/$\overline{\text{BY}}$ output will be high.

During programming, the RY/$\overline{\text{BY}}$ pin is driven low after the rising edge of the fourth write pulse. During an erase operation, the RY/$\overline{\text{BY}}$ pin is driven low after the rising edge of the sixth write pulse. The RY/$\overline{\text{BY}}$ pin will indicate a busy condition during the $\overline{\text{RESET}}$ pulse. Refer to Figures 11 and 12 for a detailed timing diagram. The RY/$\overline{\text{BY}}$ pin is pulled high in standby mode.

Since this is an open-drain output, RY/$\overline{\text{BY}}$ pins can be tied together in parallel with a pull-up resistor to V_{CC}.

Byte/Word Configuration

The $\overline{\text{BYTE}}$ pin selects the byte (8-bit) mode or word (16-bit) mode for the MBM29SL160TD/BD devices. When this pin is driven high, the devices operate in the word (16-bit) mode. The data is read and programmed at DQ_0 to DQ_{15}. When this pin is driven low, the devices operate in byte (8-bit) mode. Under this mode, the DQ_{15}/A_{-1} pin becomes the lowest address bit and DQ_8 to DQ_{14} bits are tri-stated. However, the command bus cycle is always an 8-bit operation and hence commands are written at DQ_0 to DQ_7 and the DQ_8 to DQ_{15} bits are ignored. Refer to Figures 13, 14 and 15 for the timing diagram.

Data Protection

The MBM29SL160TD/BD are designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power up the devices automatically reset the internal state machine in the Read mode. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific multi-bus cycle command sequences.

The devices also incorporate several features to prevent inadvertent write cycles resulting form V_{CC} power-up and power-down transitions or system noise.

If Embedded Erase Algorithm is interrupted, there is possibility that the erasing sector(s) cannot be used.

Write Pulse "Glitch" Protection

Noise pulses of less than 5 ns (typical) on $\overline{OE}$, $\overline{CE}$, or $\overline{WE}$ will not initiate a write cycle.

Logical Inhibit

Writing is inhibited by holding any one of $\overline{OE}$ = V_{IL}, $\overline{CE}$ = V_{IH}, or $\overline{WE}$ = V_{IH}. To initiate a write cycle $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

Power-Up Write Inhibit

Power-up of the devices with $\overline{WE}$ = $\overline{CE}$ = V_{IL} and $\overline{OE}$ = V_{IH} will not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to the read mode on power-up.

Table 10 Common Flash Memory Interface Code

Description	A_0 to A_6	DQ_0 to DQ_{15}
Query-unique ASCII string "QRY"	10h 11h 12h	0051h 0052h 0059h
Primary OEM Command Set 2h: AMD/FJ standard type	13h 14h	0002h 0000h
Address for Primary Extended Table	15h 16h	0040h 0000h
Alternate OEM Command Set (00h = not applicable)	17h 18h	0000h 0000h
Address for Alternate OEM Extended Table	19h 1Ah	0000h 0000h
V_{CC} Min. (write/erase) D7-4: volt, D3-0: 100 mvolt	1Bh	0018h
V_{CC} Max. (write/erase) D7-4: volt, D3-0: 100 mvolt	1Ch	0027h
V_{PP} Min. voltage	1Dh	0000h
V_{PP} Max. voltage	1Eh	0000h
Typical timeout per single byte/word write 2^N µs	1Fh	0004h
Typical timeout for Min. size buffer write 2^N µs	20h	0000h
Typical timeout per individual block erase 2^N ms	21h	000Ah
Typical timeout for full chip erase 2^N ms	22h	0000h
Max. timeout for byte/word write 2^N times typical	23h	0005h
Max. timeout for buffer write 2^N times typical	24h	0000h
Max. timeout per individual block erase 2^N times typical	25h	0004h
Max. timeout for full chip erase 2^N times typical	26h	0000h
Device Size = 2^N byte	27h	0015h
Flash Device Interface description	28h 29h	0002h 0000h
Max. number of byte in multi-byte write = 2^N	2Ah 2Bh	0000h 0000h
Number of Erase Block Regions within device	2Ch	0002h
Erase Block Region 1 Information	2Dh 2Eh 2Fh 30h	0007h 0000h 0020h 0000h
Erase Block Region 2 Information29SL160	31h 32h 33h 34h	001Eh 0000h 0000h 0001h
Query-unique ASCII string "PRI"	40h 41h 42h	0050h 0052h 0049h
Major version number, ASCII	43h	0031h
Minor version number, ASCII	44h	0031h
Address Sensitive Unlock 0 = Required 1 = Not Required	45h	0000h
Erase Suspend 0 = Not Supported 1 = To Read Only 2 = To Read & Write	46h	0002h
Sector Protection 0 = Not Supported X = Number of sectors in per group	47h	0001h
Sector Temporary Unprotection 00 = Not Supported 01 = Supported	48h	0001h
Sector Protection Algorithm	49h	0004h
Number of Sector for Bank 2 00h = Not Supported	4Ah	0000h
Burst Mode Type 00 = Not Supported	4Bh	0000h
Page Mode Type 00 = Not Supported	4Ch	0000h
ACC (Acceleration) Supply Minimum 00h = Not Supported, D7-4: volt, D3-0: 100 mvolt	4Dh	0085h
ACC (Acceleration) Supply Maximum 00h = Not Supported, D7-4: volt, D3-0: 100 mvolt	4Eh	0095h
Boot Type 02h = MBM29SL160BD 03h = MBM29SL160TD	4Fh	00XXh

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating		Unit
			Min.	Max.	
Storage Temperature	Tstg	—	–55	+125	°C
Ambient Temperature with Power Applied	T_A	—	–40	+85	°C
Voltage with respect to Ground All pins except A_9, $\overline{OE}$, $\overline{RESET}$ (Note 1)	V_{IN}, V_{OUT}	—	–0.5	V_{CC} + 0.5	V
Power Supply Voltage (Note 1)	V_{CC}	—	–0.5	+3.0	V
A_9, $\overline{OE}$, and $\overline{RESET}$ (Note 2)	V_{IN}	—	–0.5	+11.0	V
$\overline{WP}$/ACC	V_{IN}	—	–0.5	+10.5	V

Notes: 1. Minimum DC voltage on input or I/O pins are –0.5 V. During voltage transitions, inputs may negative overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins are V_{CC} +0.5 V. During voltage transitions, outputs may positive overshoot to V_{CC} +2.0 V for periods of up to 20 ns.

2. Minimum DC input voltage on A_9, $\overline{OE}$ and $\overline{RESET}$ pins are –0.5 V. During voltage transitions, A_9, $\overline{OE}$ and $\overline{RESET}$ pins may negative overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on A_9, $\overline{OE}$ and $\overline{RESET}$ pins are +11.0 V which may positive overshoot to 12.0 V for periods of up to 20 ns. Voltage difference between input voltage and supply voltage (V_{IN} – V_{CC}) do not exceed 9 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Value		Unit
			Min.	Max.	
Ambient Temperature	T_A	—	–40	+85	°C
Power Supply Voltage	V_{CC}	—	+1.8	+2.2	V

Operating ranges define those limits between which the functionality of the devices are guaranteed.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ MAXIMUM OVERSHOOT

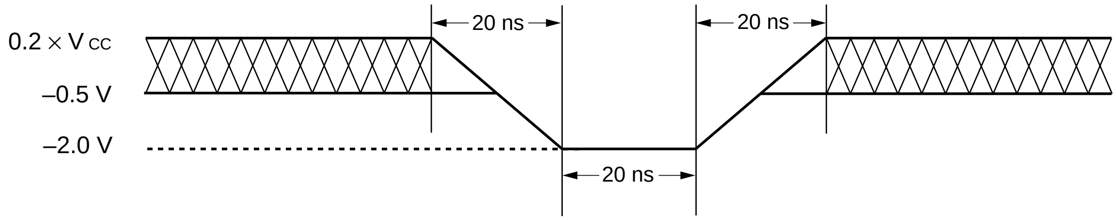


Figure 1 Maximum Negative Overshoot Waveform

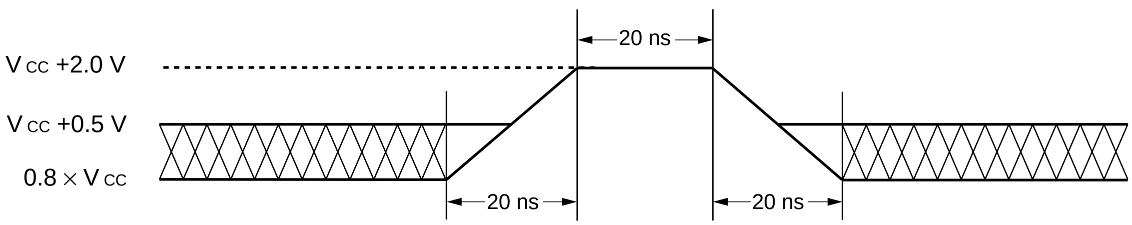
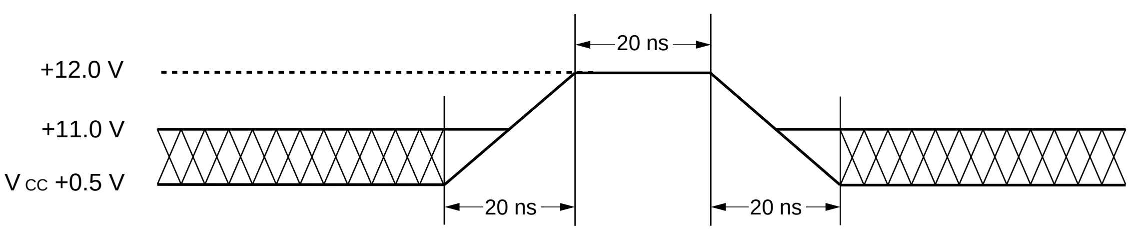


Figure 2 Maximum Positive Overshoot Waveform 1



*: This waveform is applied for A_9, $\overline{OE}$, and $\overline{RESET}$.

Figure 3 Maximum Positive Overshoot Waveform 2

■ DC CHARACTERISTICS

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
I_{LI}	Input Leakage Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max.		–1.0	+1.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max.		–1.0	+1.0	µA
I_{LIT}	A_9, $\overline{OE}$, $\overline{RESET}$ Inputs Leakage Current	$V_{CC} = V_{CC}$ Max. A_9, $\overline{OE}$, $\overline{RESET}$ = 11 V		—	35	µA
I_{LIA}	$\overline{WP}$/ACC Inputs Leakage Current	$V_{CC} = V_{CC}$ Max. $\overline{WP}$/ACC = V_{HH} Max.		—	20	mA
I_{CC1}	V_{CC} Active Current (Note 1)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$, f=10 MHz	Byte	—	25	mA
			Word		25	
		$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$, f=5 MHz	Byte	—	15	mA
			Word		15	
I_{CC2}	V_{CC} Active Current (Note 2)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		—	25	mA
I_{CC3}	V_{CC} Current (Standby)	$V_{CC} = V_{CC}$ Max., $\overline{CE} = V_{CC} \pm 0.3$ V, $\overline{RESET} = V_{CC} \pm 0.3$ V		—	5	µA
I_{CC4}	V_{CC} Current (Standby, Reset)	$V_{CC} = V_{CC}$ Max., $\overline{RESET} = V_{SS} \pm 0.3$ V		—	5	µA
I_{CC5}	V_{CC} Current (Automatic Sleep Mode) (Note 3)	$V_{CC} = V_{CC}$ Max., $\overline{CE} = V_{SS} \pm 0.3$ V, $\overline{RESET} = V_{CC} \pm 0.3$ V $V_{IN} = V_{CC} \pm 0.3$ V or $V_{SS} \pm 0.3$ V		—	5	µA
V_{IL}	Input Low Level	—		–0.5	0.2 x V_{CC}	V
V_{IH}	Input High Level	—		0.8 x V_{CC}	V_{CC}+0.3	V
V_{ACC}	Voltage for $\overline{WP}$/ACC Sector Protection/Unprotection and Program Accelaration	—		8.5	9.5	V
V_{ID}	Voltage for Autoselect and Sector Protection (A_9, $\overline{OE}$, $\overline{RESET}$) (Note 4, 5)	—		10	11	V
V_{OL}	Output Low Voltage Level	I_{OL} = 0.1 mA, $V_{CC} = V_{CC}$ Min.		—	0.1	V
V_{OH}	Output High Voltage Level	I_{OH} = –100 µA		V_{CC}–0.1	—	V

Notes: 1. The I_{CC} current listed includes both the DC operating current and the frequency dependent component.

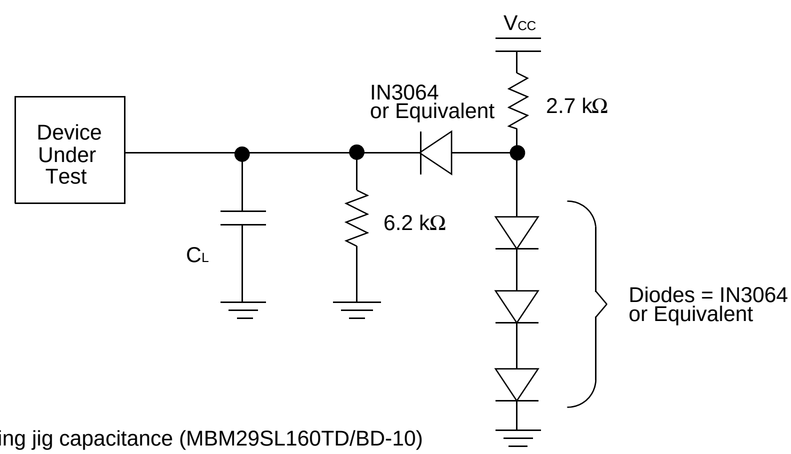
2. I_{CC} active while Embedded Algorithm (program or erase) is in progress.
3. Automatic sleep mode enables the low power mode when address remain stable for 150 ns.
4. This timing is for Sector Protection operation.
5. Applicable for only V_{CC} applying.

■ AC CHARACTERISTICS

• **Read Only Operations Characteristics**

Parameter Symbols		Description	Test Setup		-10 (Note)	-12 (Note)	Unit
JEDEC	Standard						
t_{AVAV}	t_{RC}	Read Cycle Time	—	Min.	100	120	ns
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{IL}$	Max.	100	120	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$	Max.	100	120	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay	—	Max.	35	50	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High-Z	—	Max.	30	40	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High-Z	—	Max.	30	40	ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurs First	—	Min.	0	0	ns
—	t_{READY}	$\overline{RESET}$ Pin Low to Read Mode	—	Max.	20	20	µs
—	t_{ELFL} t_{ELFH}	$\overline{CE}$ or $\overline{BYTE}$ Switching Low or High	—	Max.	5	5	ns

Notes: Test Conditions:
Output Load:1 TTL gate and 30 pF (MBM29SL160TD/BD-10)
1 TTL gate and 100 pF (MBM29SL160TD/BD-12)
Input rise and fall times: 5 ns
Input pulse levels: 0.0 V to V_{CC}
Timing measurement reference level
Input: 0.5 x V_{CC}
Output: 0.5 x V_{CC}



Notes: C_L = 30 pF including jig capacitance (MBM29SL160TD/BD-10)
C_L = 100 pF including jig capacitance (MBM29SL160TD/BD-12)

Figure 4 Test Conditions

- **Write/Erase/Program Operations**

Parameter Symbols: JEDEC	Parameter Symbols: Standard	Description		-10	-12	Unit
t_{AVAV}	t_{WC}	Write Cycle Time	Min.	100	120	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min.	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min.	50	60	ns
t_{DVWH}	t_{DS}	Data Setup Time	Min.	50	60	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min.	0	0	ns
—	t_{OES}	Output Enable Setup Time	Min.	0	0	ns
—	t_{OEH}	Output Enable Hold Time: Read	Min.	0	0	ns
		Output Enable Hold Time: Toggle and $\overline{Data}$ Polling	Min.	10	10	ns
t_{GHWL}	t_{GHWL}	Read Recover Time Before Write	Min.	0	0	ns
t_{GHEL}	t_{GHEL}	Read Recover Time Before Write	Min.	0	0	ns
t_{ELWL}	t_{CS}	$\overline{CE}$ Setup Time	Min.	0	0	ns
t_{WLEL}	t_{WS}	$\overline{WE}$ Setup Time	Min.	0	0	ns
t_{WHEH}	t_{CH}	$\overline{CE}$ Hold Time	Min.	0	0	ns
t_{EHWH}	t_{WH}	$\overline{WE}$ Hold Time	Min.	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min.	50	60	ns
t_{ELEH}	t_{CP}	$\overline{CE}$ Pulse Width	Min.	50	60	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High	Min.	30	30	ns
t_{EHEL}	t_{CPH}	$\overline{CE}$ Pulse Width High	Min.	30	30	ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation	Typ.	10.6	10.6	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 1)	Typ.	1.5	1.5	sec
—	t_{VCS}	V_{CC} Setup Time	Min.	50	50	µs
—	t_{VIDR}	Rise Time to V_{ID} (Note 2)	Min.	500	500	ns
—	t_{VACCR}	Rise Time to V_{ACC}	Min.	500	500	ns
—	t_{VLHT}	Voltage Transition Time (Note 2)	Min.	4	4	µs
—	t_{WPP}	Write Pulse Width (Note 2)	Min.	100	100	µs
—	t_{OESP}	$\overline{OE}$ Setup Time to $\overline{WE}$ Active (Note 2)	Min.	4	4	µs
—	t_{CSP}	$\overline{CE}$ Setup Time to $\overline{WE}$ Active (Note 2)	Min.	4	4	µs
—	t_{RB}	Recover Time From RY/$\overline{BY}$	Min.	0	0	ns
—	t_{RP}	$\overline{RESET}$ Pulse Width	Min.	500	500	ns
—	t_{RH}	$\overline{RESET}$ Hold Time Before Read	Min.	200	200	ns

(Continued)

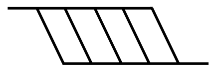
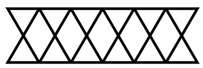
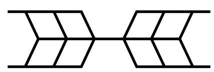
(Continued)

Parameter Symbols		Description		-10	-12	Unit
JEDEC	Standard					
—	t_{FLQZ}	$\overline{\text{BYTE}}$ Switching Low to Output High-Z	Max.	30	40	ns
—	t_{FHQV}	$\overline{\text{BYTE}}$ Switching High to Output Active	Min.	30	40	ns
—	t_{BUSY}	Program/Erase Valid to RY/$\overline{\text{BY}}$ Delay	Max.	90	90	ns
—	t_{EOE}	Delay Time from Embedded Output Enable	Max.	100	120	ns
—	t_{PS}	Power On/Off Timing	Min.	0	0	ns

Notes: 1. This does not include the preprogramming time.
2. This timing is for Sector Group Protection operation.

■ SWITCHING WAVEFORMS

- **Key to Switching Waveforms**

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	"H" or "L" Any Change Permitted	Changing State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

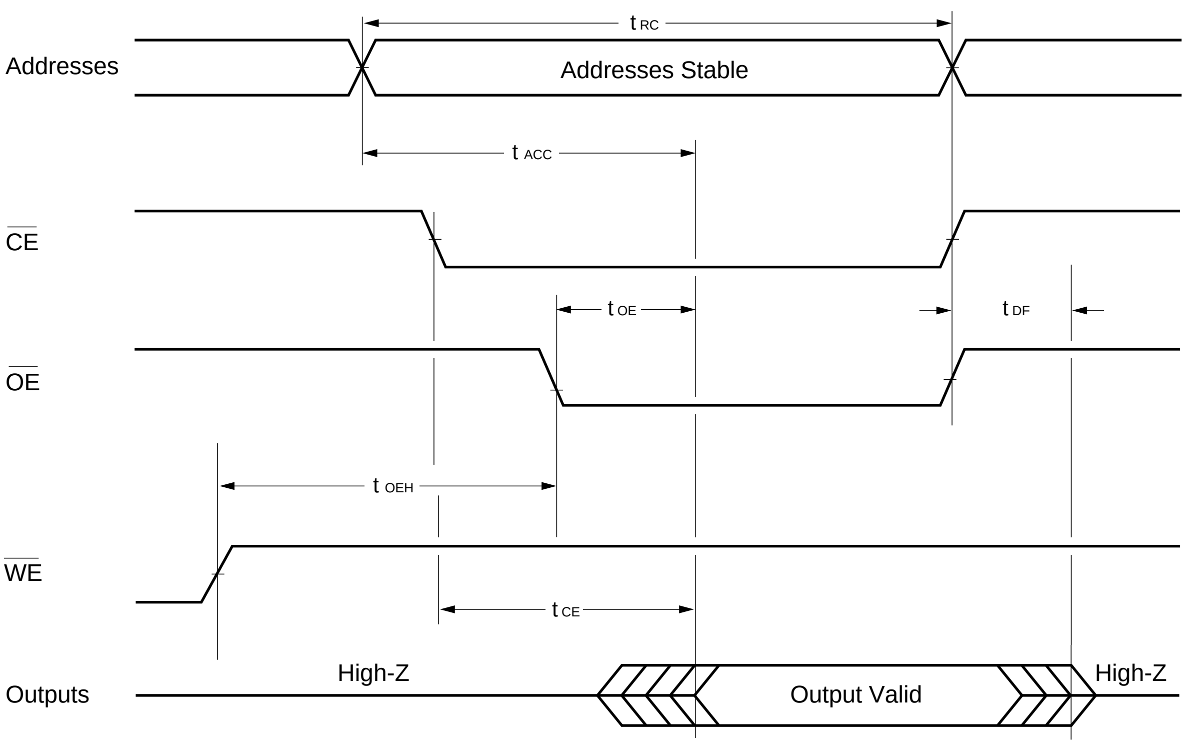


Figure 5.1 AC Waveforms for Read Operations

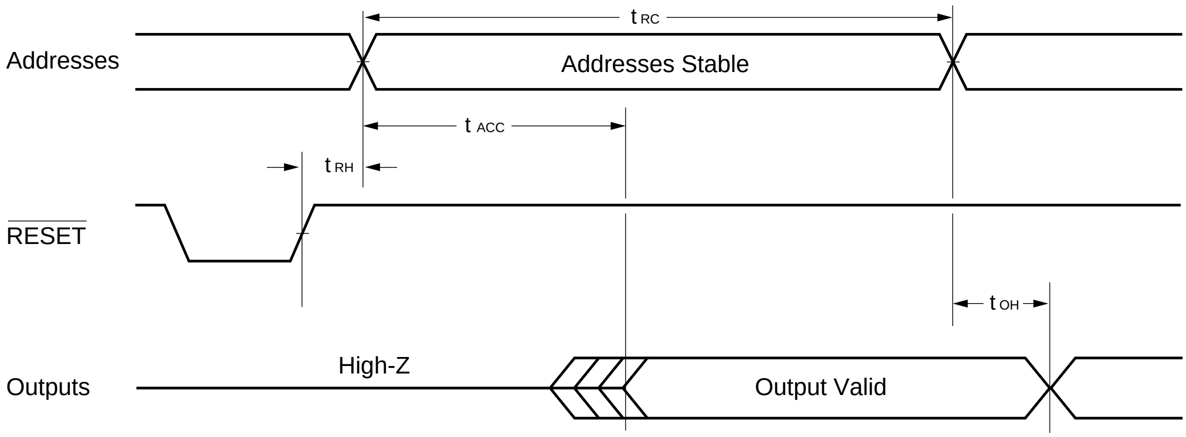
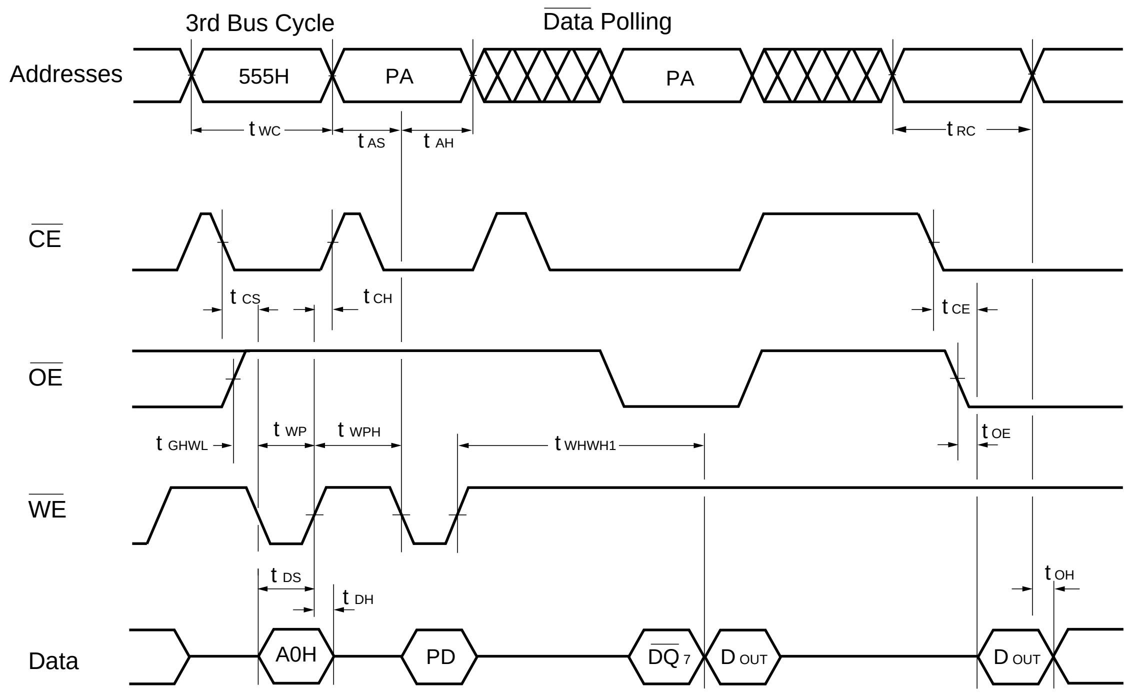
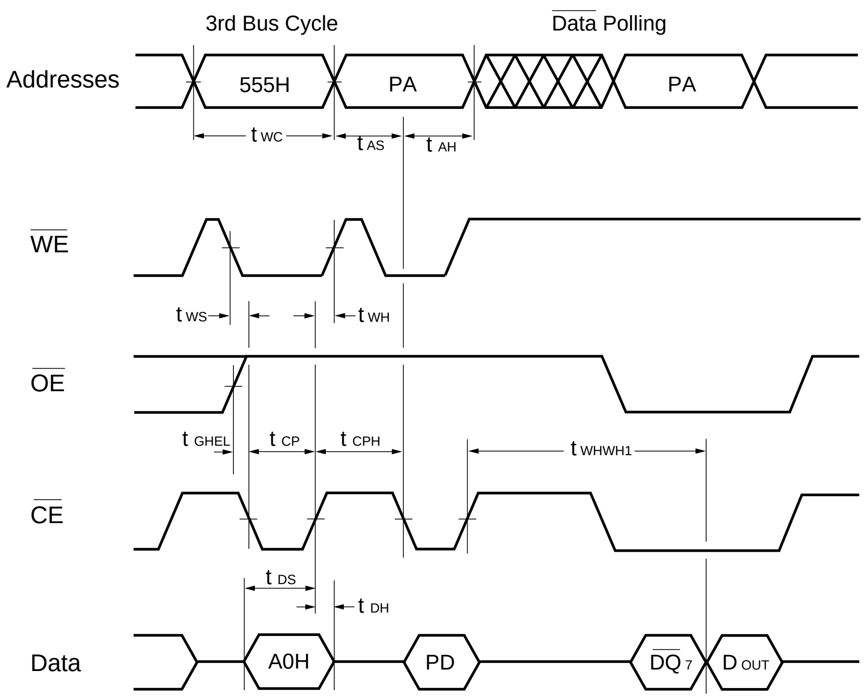


Figure 5.2 AC Waveforms for Hardware Reset/Read Operations



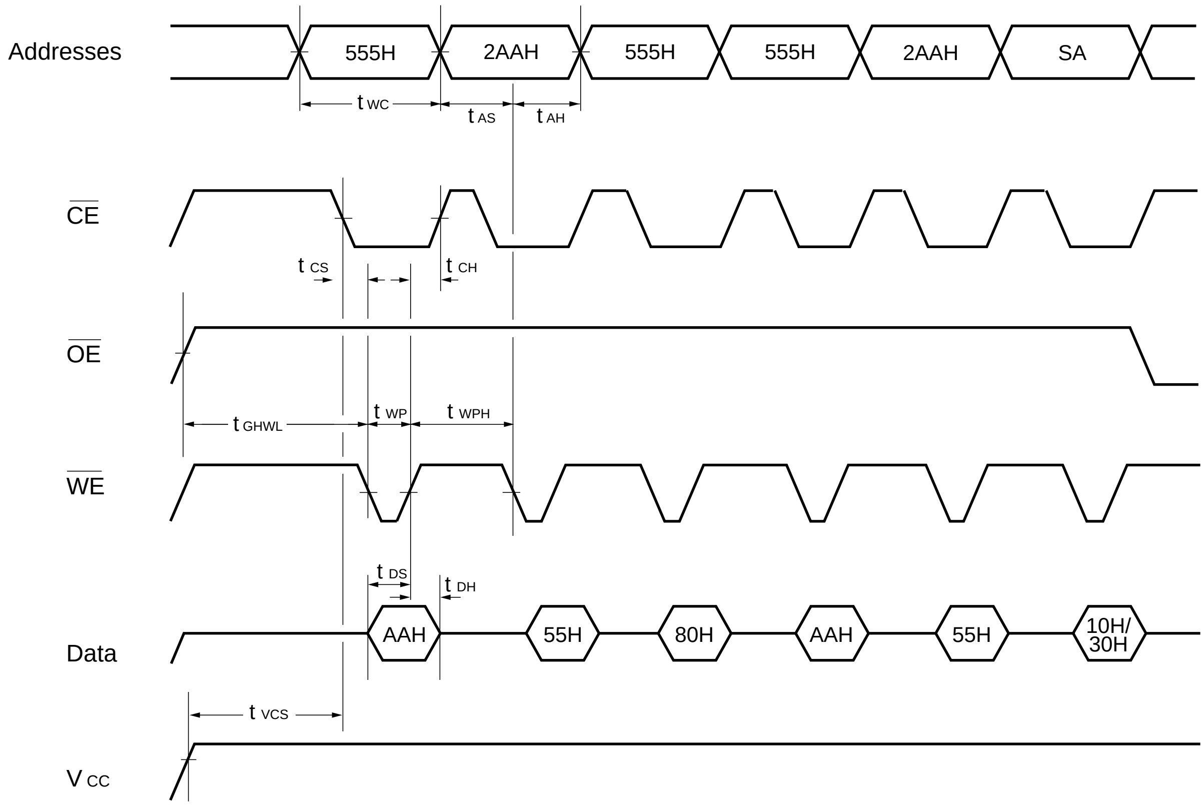
Notes: 1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at byte address.
3. $\overline{DQ_7}$ is the output of the complement of the data written to the device.
4. D_{OUT} is the output of the data written to the device.
5. Figure indicates last two bus cycles out of four bus cycle sequence.
6. These waveforms are for the ×16 mode. (The addresses differ from ×8 mode.)

Figure 6 AC Waveforms for Alternate $\overline{WE}$ Controlled Program Operations



Notes: 1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at byte address.
3. $\overline{DQ_7}$ is the output of the complement of the data written to the device.
4. D_{OUT} is the output of the data written to the device.
5. Figure indicates last two bus cycles out of four bus cycle sequence.
6. These waveforms are for the ×16 mode. (The addresses differ from ×8 mode.)

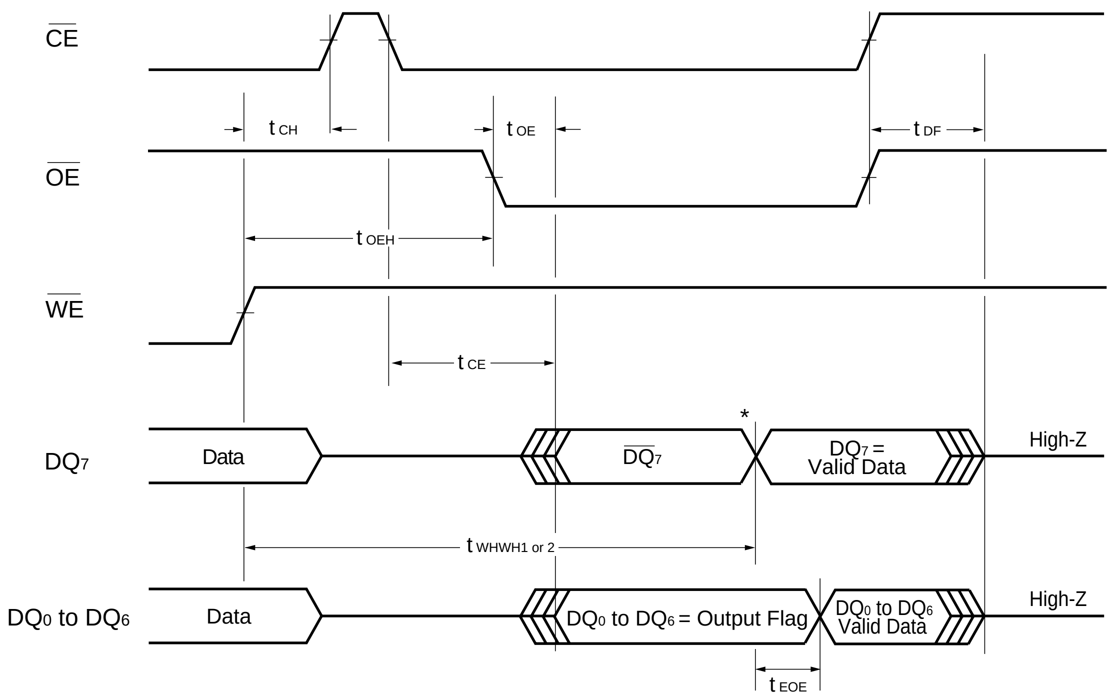
Figure 7 AC Waveforms for Alternate $\overline{CE}$ Controlled Program Operations



Notes: 1. SA is the sector address for Sector Erase. Addresses = 555H (Word), AAAH (Byte) for Chip Erase.

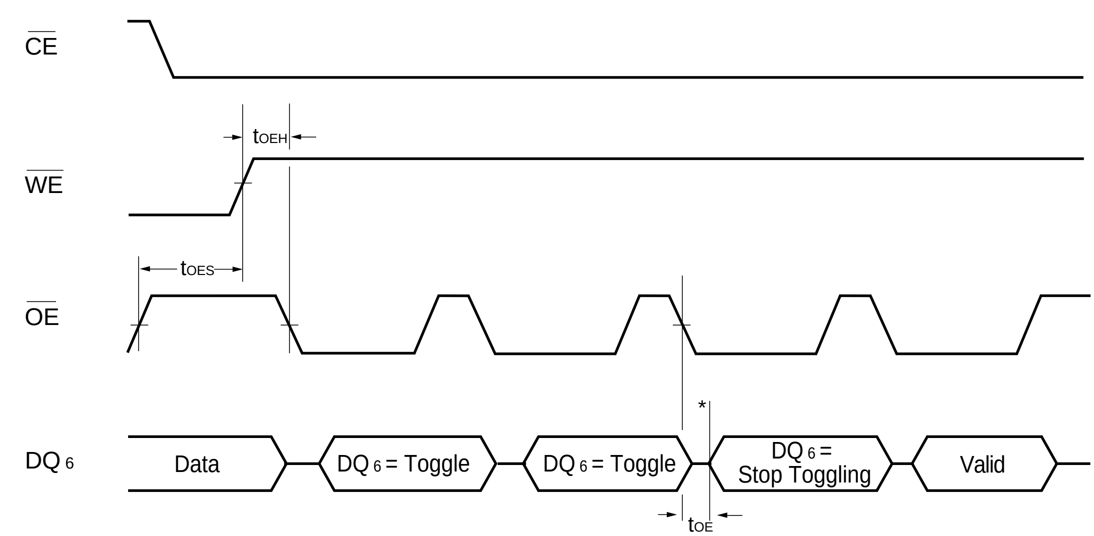
2. These waveforms are for the ×16 mode. (The addresses differ from ×8 mode.)

Figure 8 AC Waveforms Chip/Sector Erase Operations



* : DQ_7 = Valid Data (The device has completed the Embedded operation).

Figure 9 AC Waveforms for $\overline{\text{Data}}$ Polling during Embedded Algorithm Operations



* : DQ_6 stops toggling (The device has completed the Embedded operation).

Figure 10 AC Waveforms for Toggle Bit I during Embedded Algorithm Operations

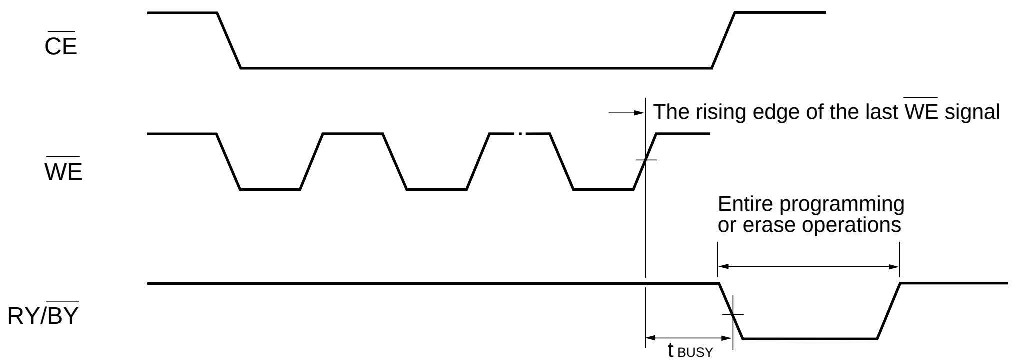


Figure 11 RY/BY Timing Diagram during Program/Erase Operations

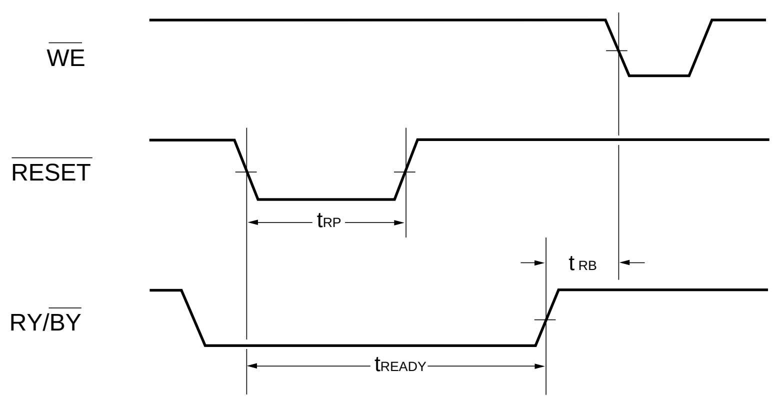


Figure 12 RESET/RY/BY Timing Diagram

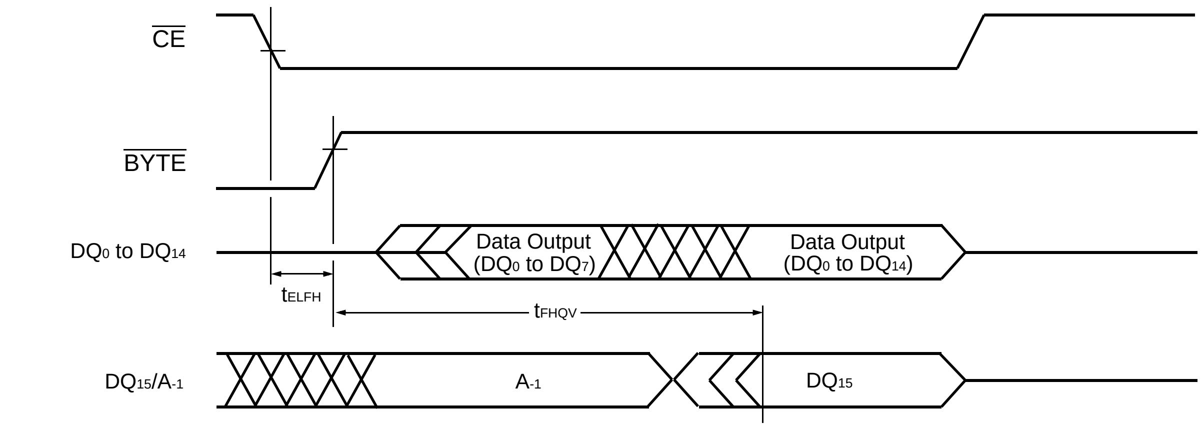


Figure 13 Timing Diagram for Word Mode Configuration

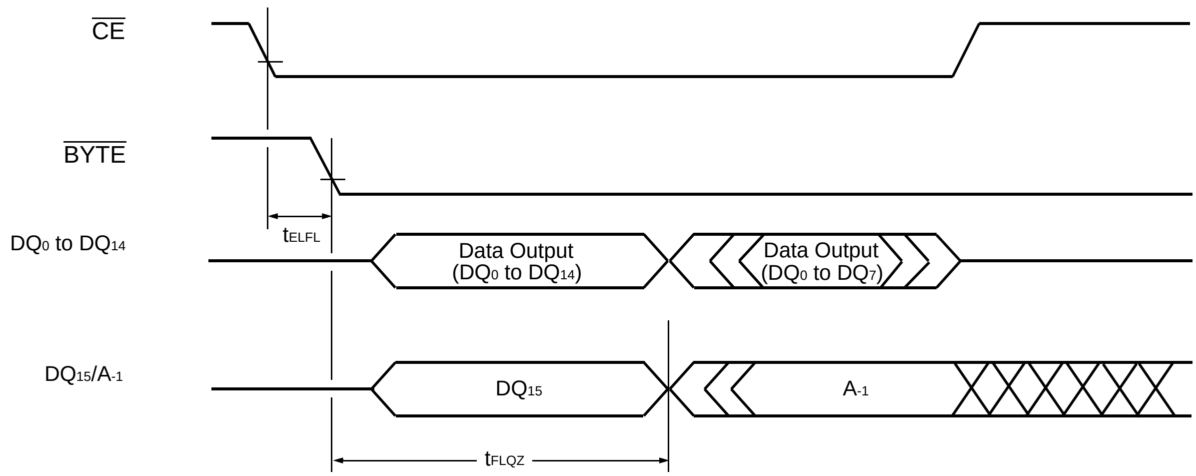


Figure 14 Timing Diagram for Byte Mode Configuration

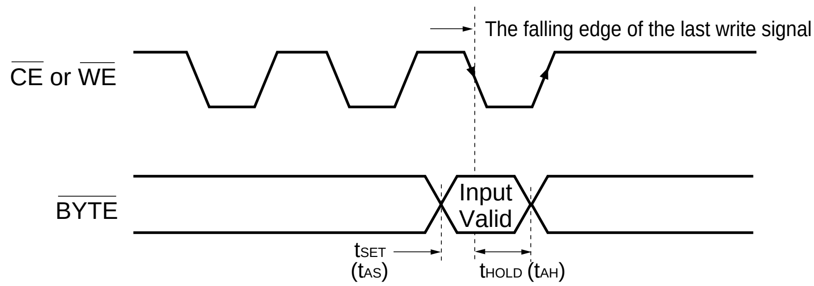
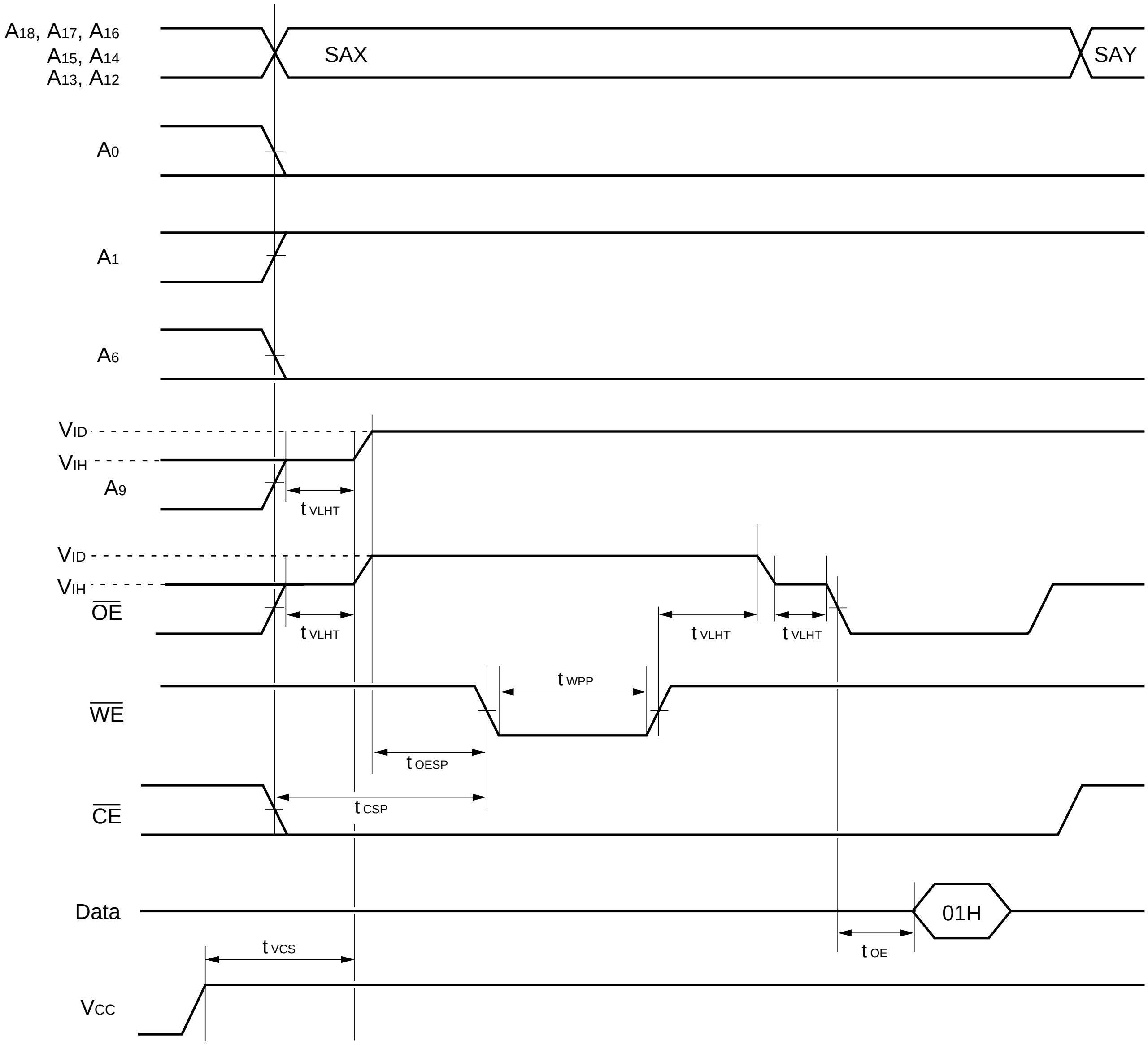


Figure 15 BYTE Timing Diagram for Write Operations



SGAX:Sector Group Address for initial sector
SGAY:Sector Group Address for next sector
Note: A_{-1} is V_{IL} on byte mode.

Figure 16 AC Waveforms for Sector Group Protection Timing Diagram

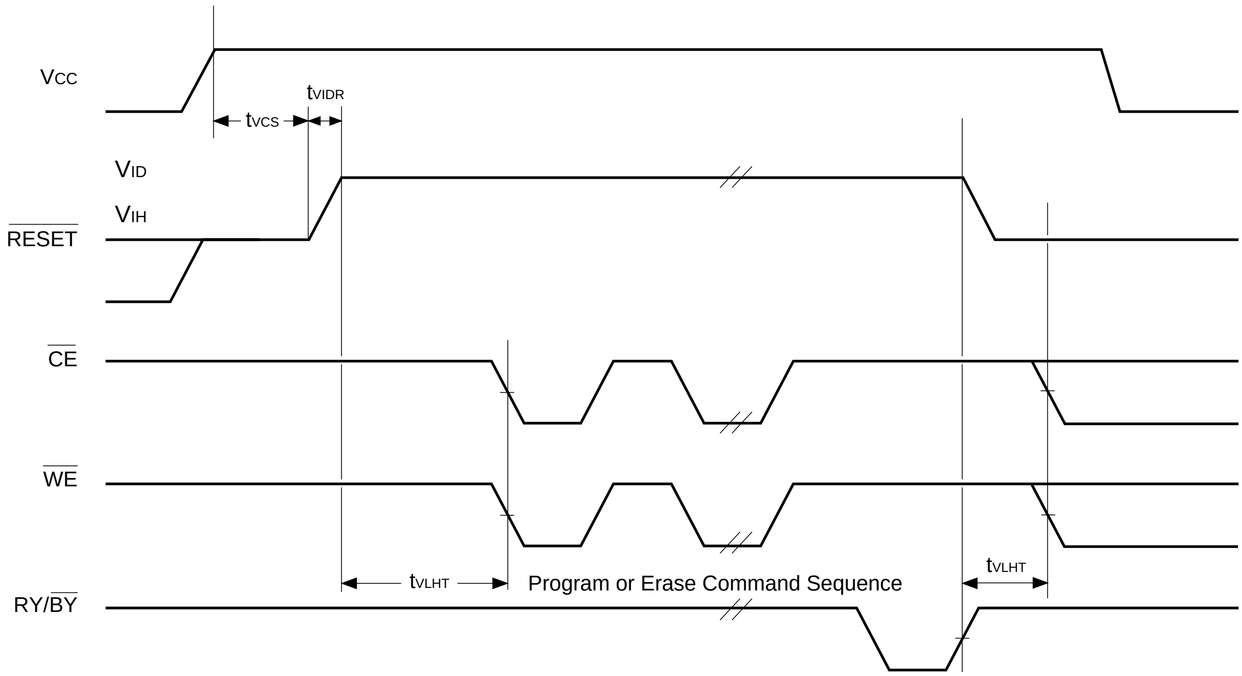
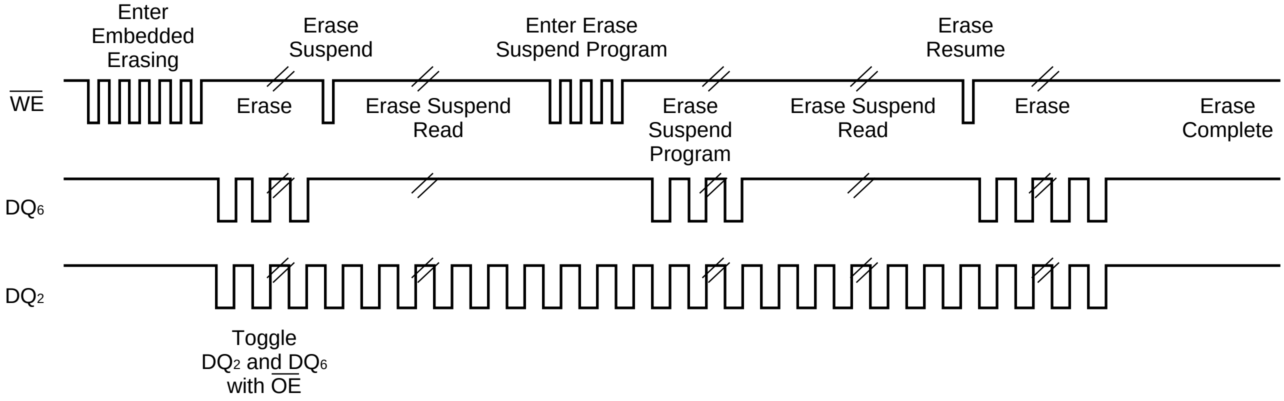
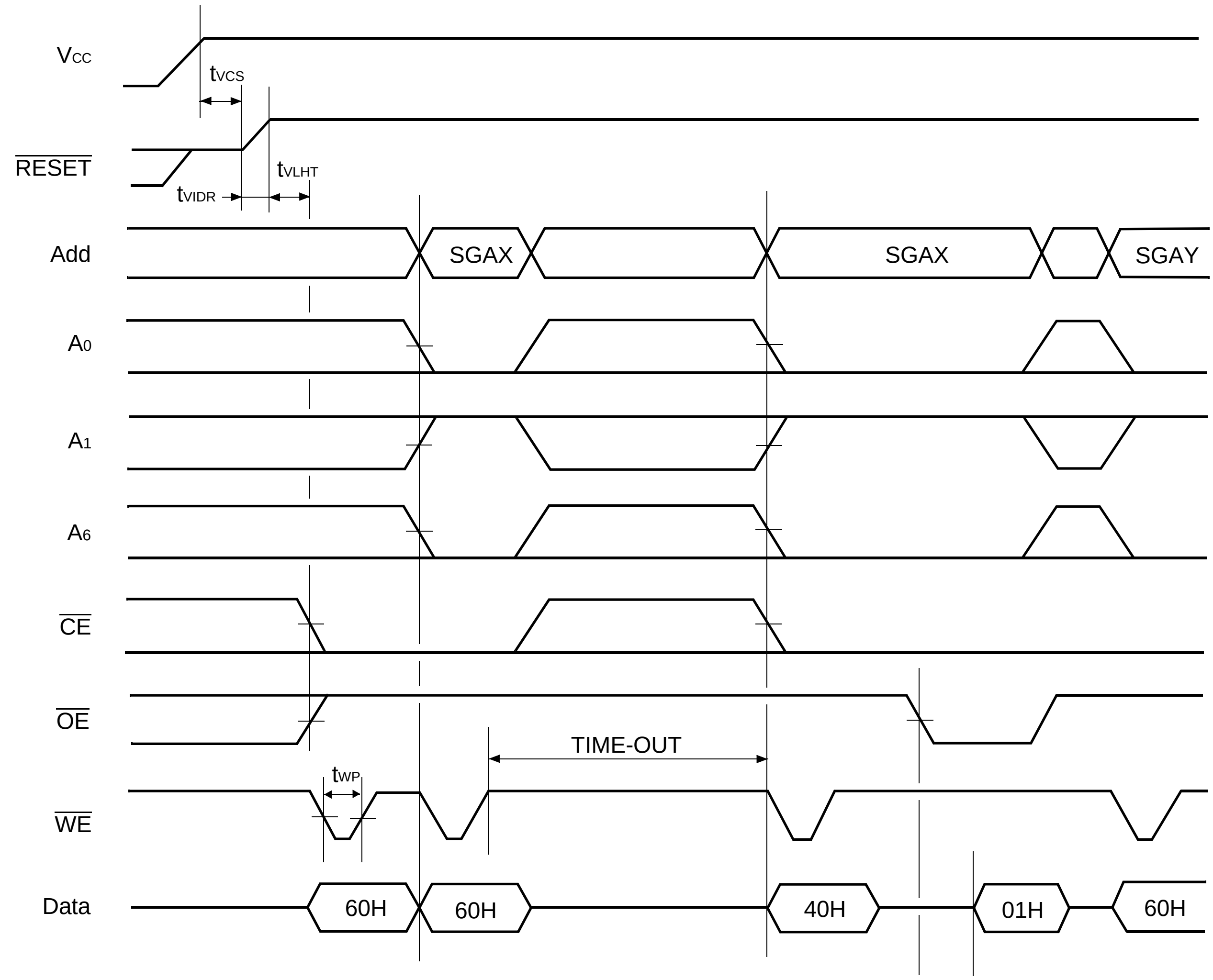


Figure 17 Temporary Sector Group Unprotection Timing Diagram



Note: DQ_2 is read from the erase-suspended sector.

Figure 18 DQ_2 vs. DQ_6



SGAX : Sector Group Address to be protected
SGAY : Next Sector Group Address to be protected
TIME-OUT : Time-Out window = 50 µs (min)

Figure 19 Extended Sector Group Protection Timing Diagram

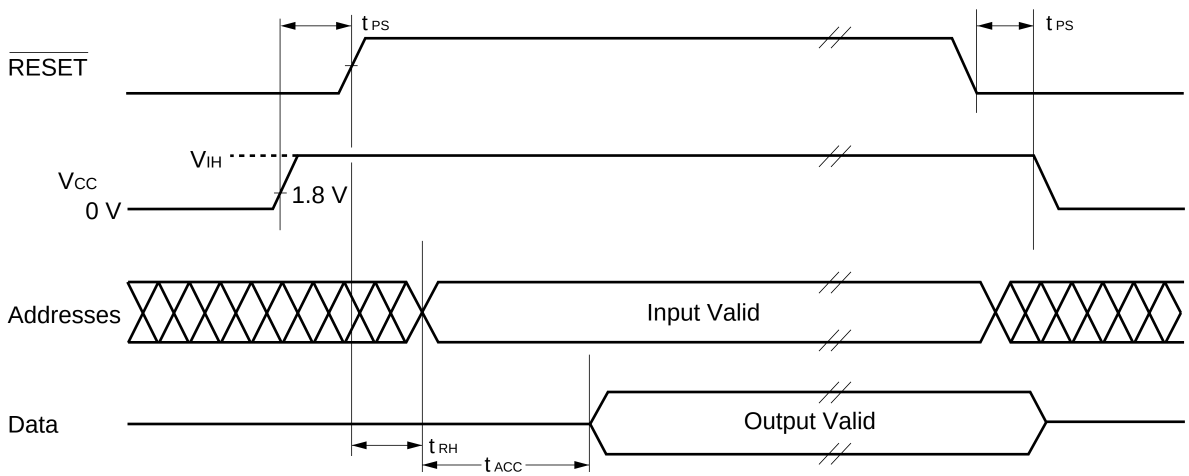


Figure 20 Power ON/OFF Timing Diagram

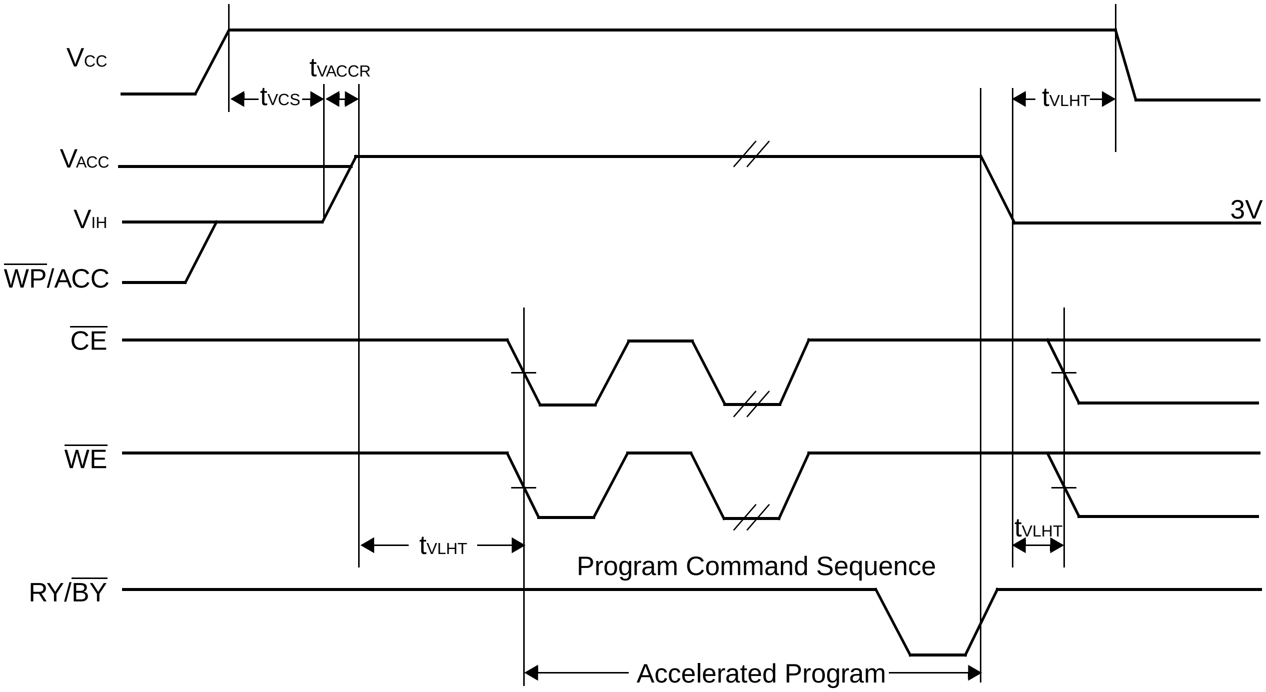
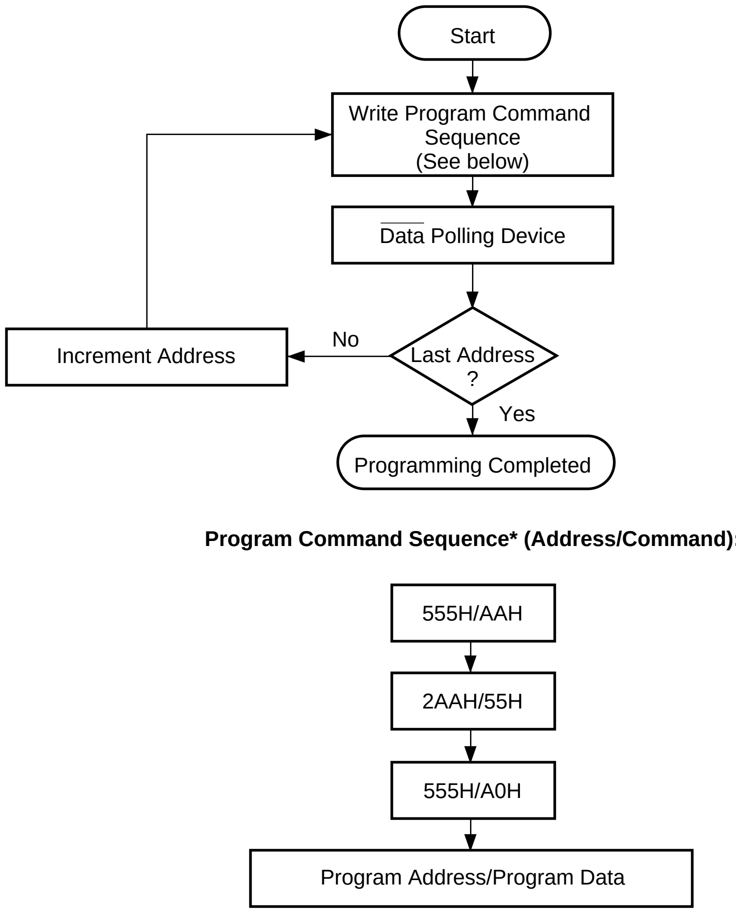


Figure 21 Accelerated Program Operation Timing Diagram

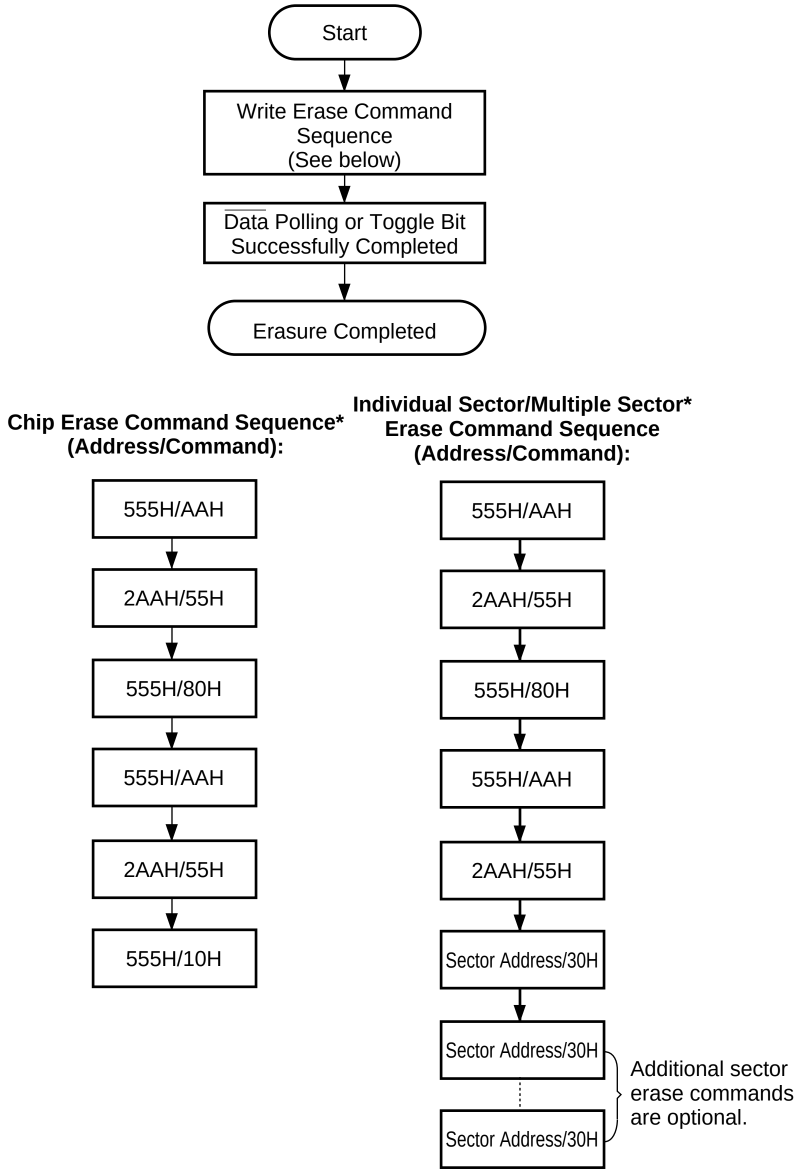
EMBEDDED ALGORITHMS



* : The sequence is applied for × 16 mode.
  The addresses differ from × 8 mode.

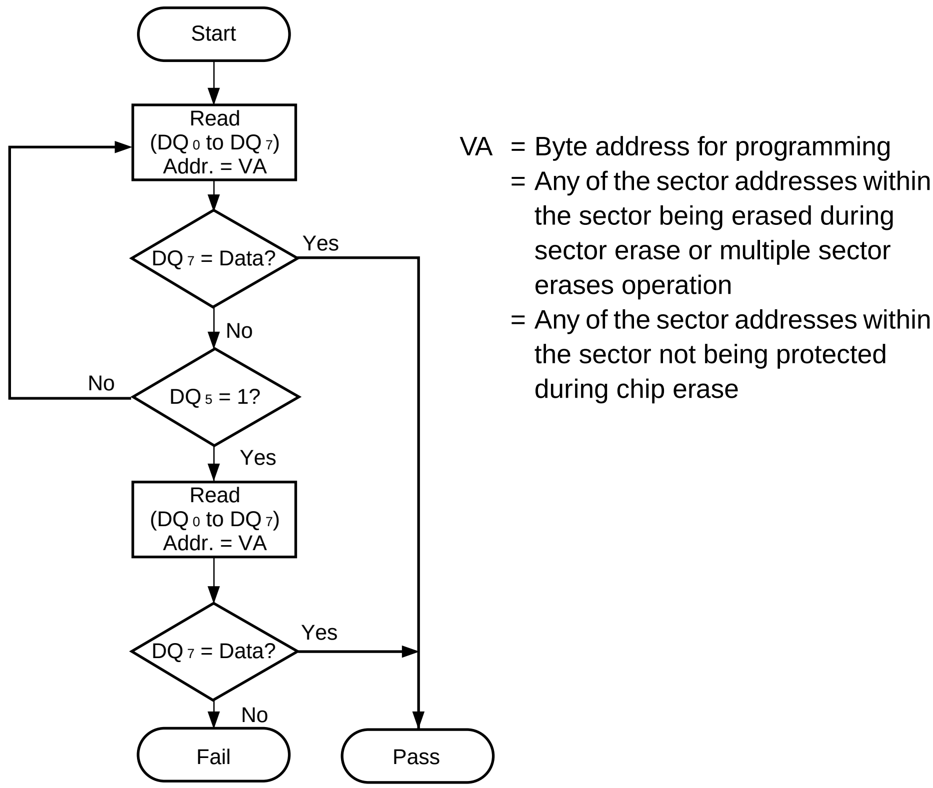
Figure 22 Embedded Program™ Algorithm

EMBEDDED ALGORITHMS



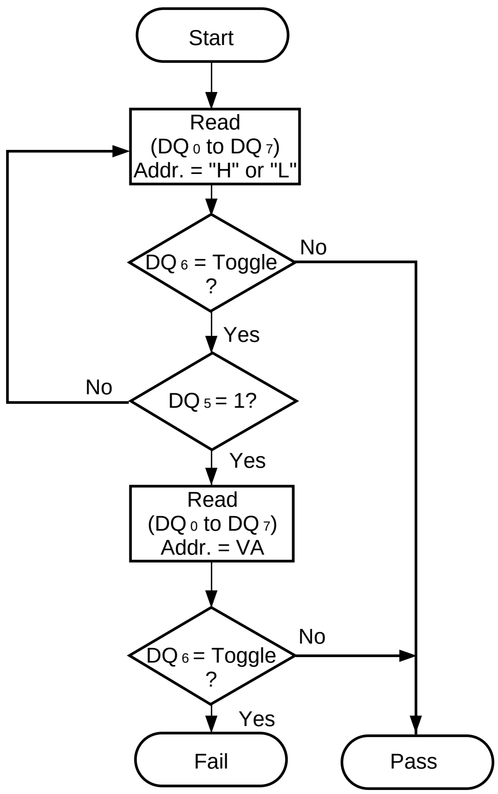
* : The sequence is applied for × 16 mode.
The addresses differ from × 8 mode.

Figure 23 Embedded Erase™ Algorithm



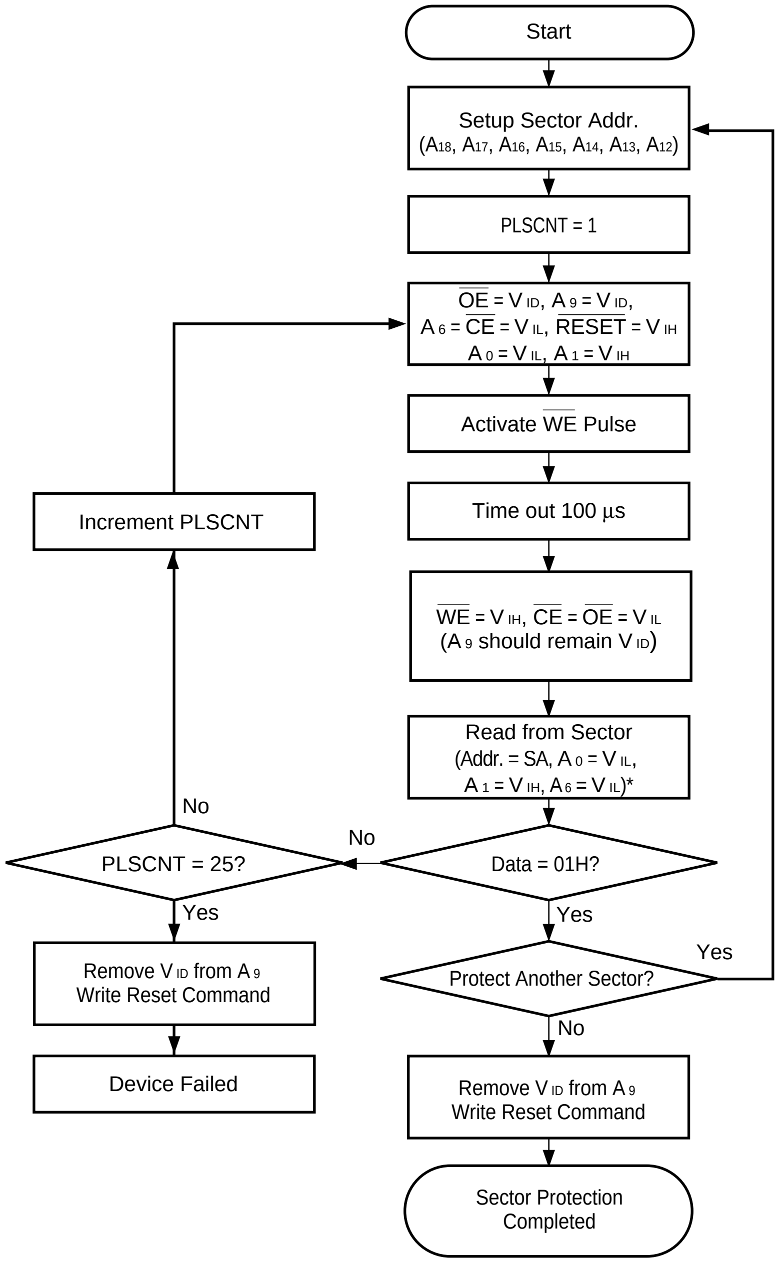
Note: DQ_7 is rechecked even if DQ_5 = “1” because DQ_7 may change simultaneously with DQ_5.

Figure 24 $\overline{\text{Data}}$ Polling Algorithm



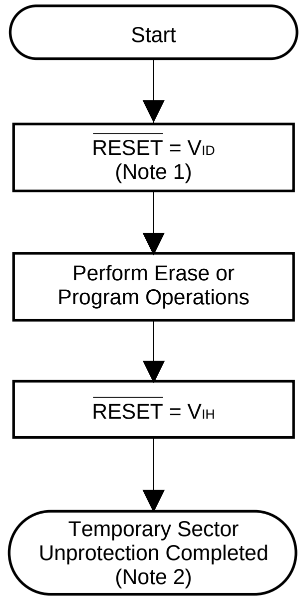
Note: DQ_6 is rechecked even if DQ_5 = “1” because DQ_6 may stop toggling at the same time as DQ_5 changing to “1” .

Figure 25 Toggle Bit Algorithm



* : A_{-1} is V_{IL} on byte mode.

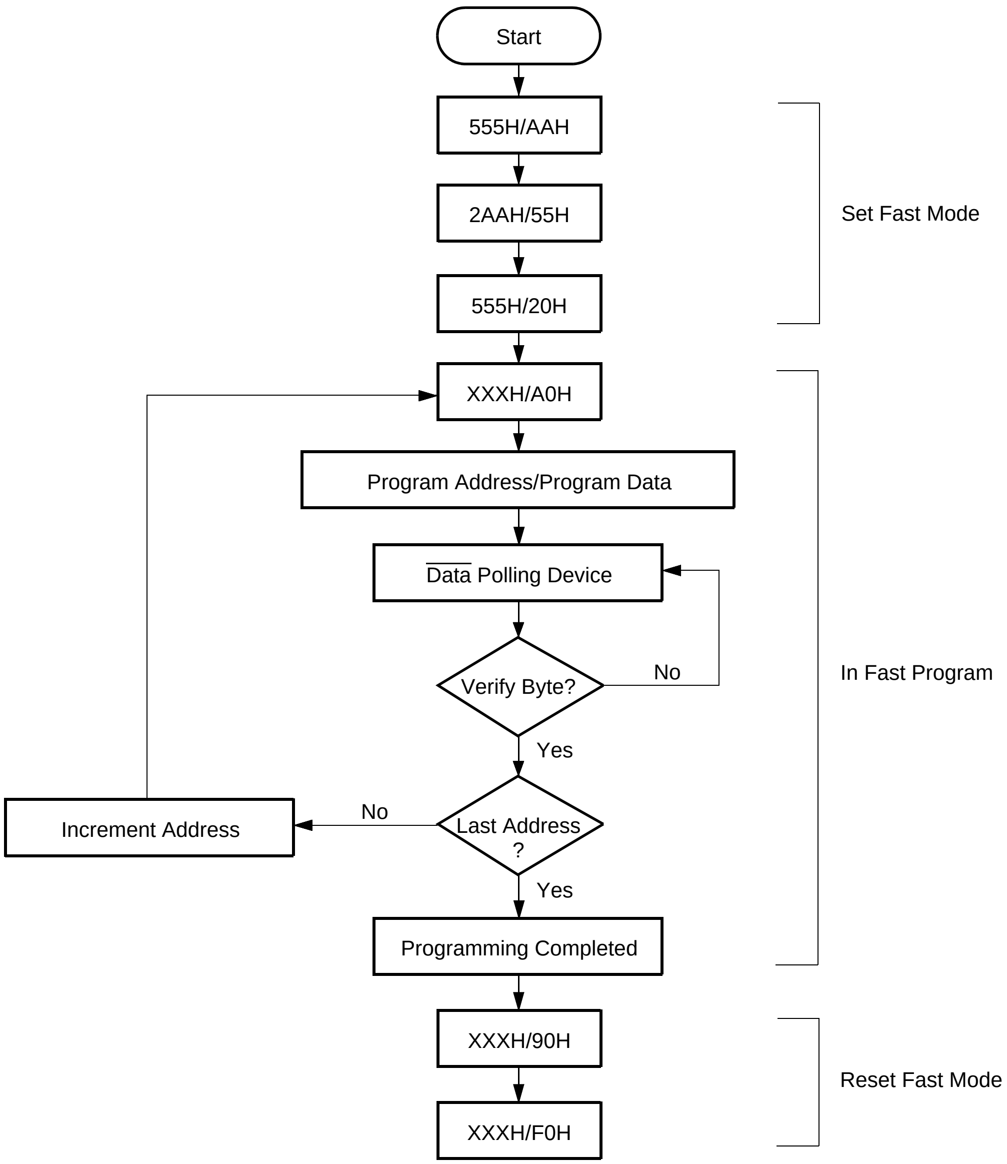
Figure 26 Sector Protection Algorithm



Notes: 1. All protected sectors are unprotected.
2. All previously protected sectors are protected once again.

Figure 27 Temporary Sector Unprotection Algorithm

FAST MODE ALGORITHM



* : The sequence is applied for × 16 mode.
The addresses differ from × 8 mode.

Figure 28 Embedded Program™ Algorithm for Fast Mode

FAST MODE ALGORITHM

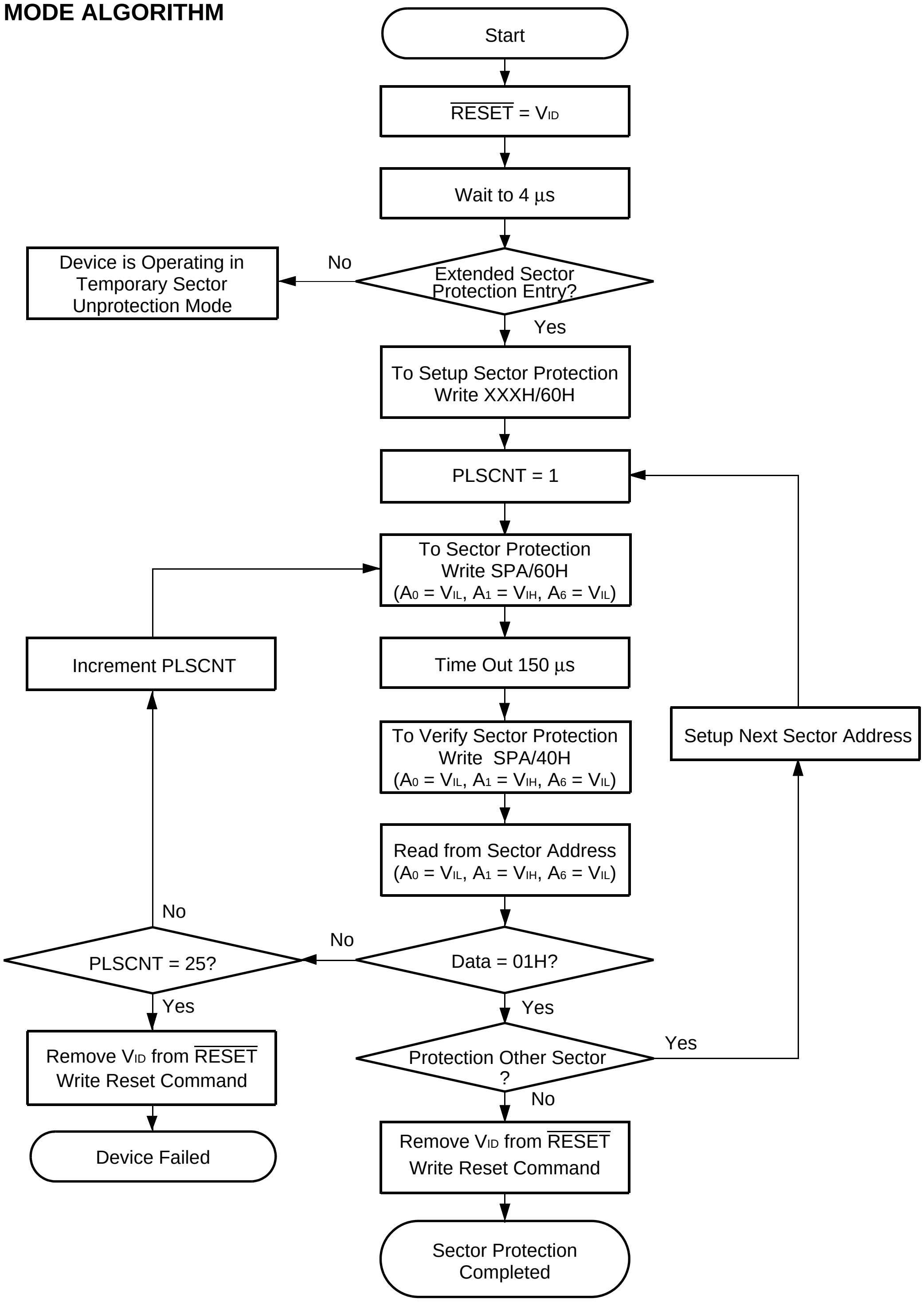


Figure 29 Extended Sector Protection Algorithm

■ ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Unit	Comments
	Min.	Typ.	Max.		
Sector Erase Time	—	1.5	20	sec	Excludes programming time prior to erasure
Word Programming Time	—	14.6	360	µs	Excludes system-level overhead
Byte Programming Time	—	10.6	300	µs	
Chip Programming Time	—	15.4	160	sec	Excludes system-level overhead
Program/Erase Cycle	100,000	—	—	cycles	—

Note:

■ TSOP(I) PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ.	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	7.5	9.5	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	8	10	pF
C_{IN2}	Control Pin Capacitance	$V_{IN} = 0$	8	13	pF

Note: Test conditions T_A = 25°C, f = 1.0 MHz

■ FBGA PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ.	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	7.5	9.5	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	8	10	pF
C_{IN2}	Control Pin Capacitance	$V_{IN} = 0$	8	13	pF

Note: Test conditions T_A = 25°C, f = 1.0 MHz

■ ORDERING INFORMATION

Standard Products

Fujitsu standard products are available in several packages. The order number is formed by a combination of:

MBM29SL160 T D -10 PFTN

PACKAGE TYPE
PFTN = 48-Pin Thin Small Outline Package (TSOP) Standard Pinout
PFTR = 48-Pin Thin Small Outline Package (TSOP) Reverse Pinout
PBT = 48-Ball Fine pitch Ball Grid Array Package (FBGA)

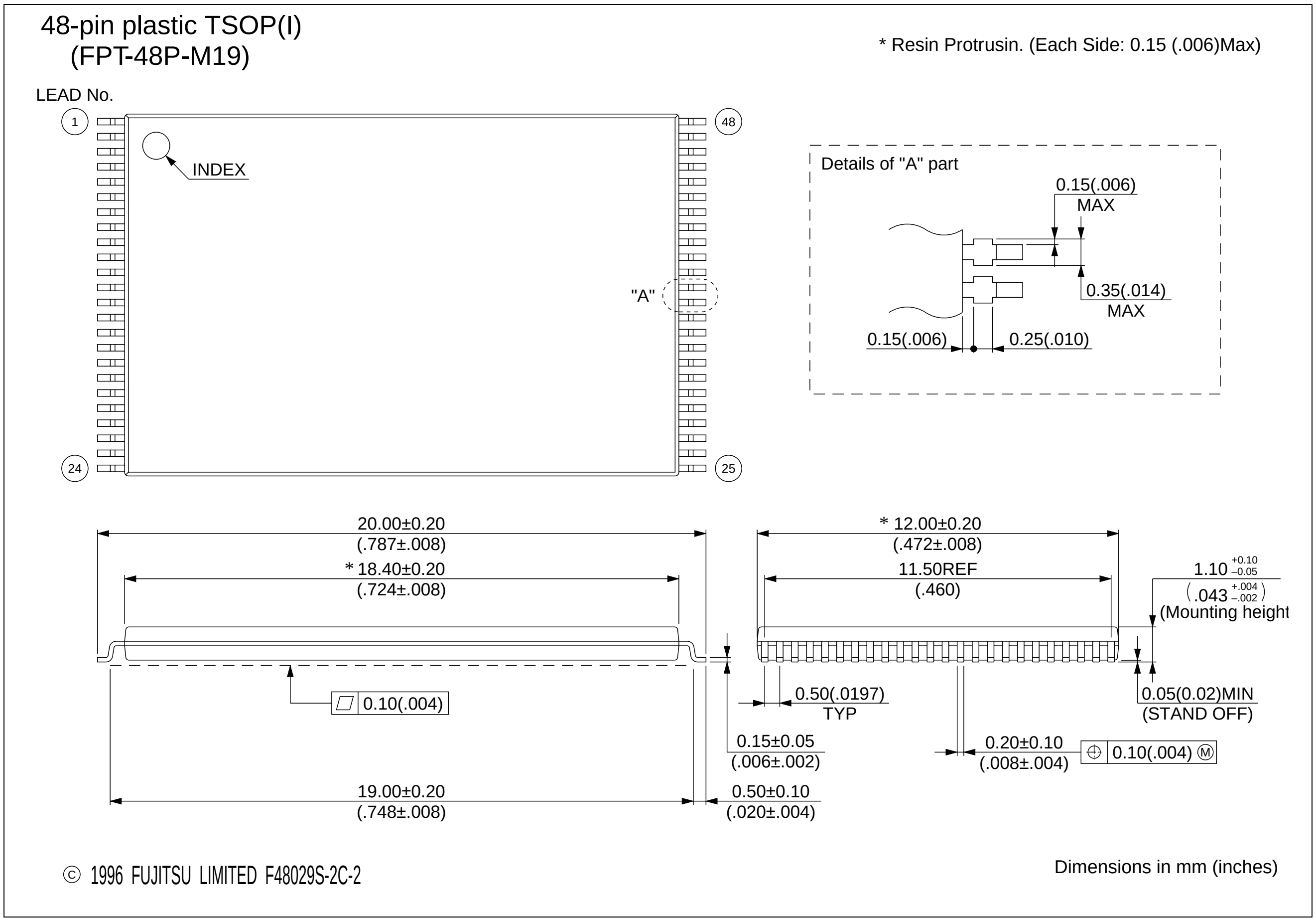
SPEED OPTION
See Product Selector Guide

DEVICE REVISION

BOOT CODE SECTOR ARCHITECTURE
T = Top sector
B = Bottom sector

DEVICE NUMBER/DESCRIPTION
MBM29SL160
16Mega-bit (2M × 8-Bit or 1M × 16-Bit) CMOS Flash Memory
1.8 V-only Read, Program, and Erase

■ PACKAGE DIMENSIONS



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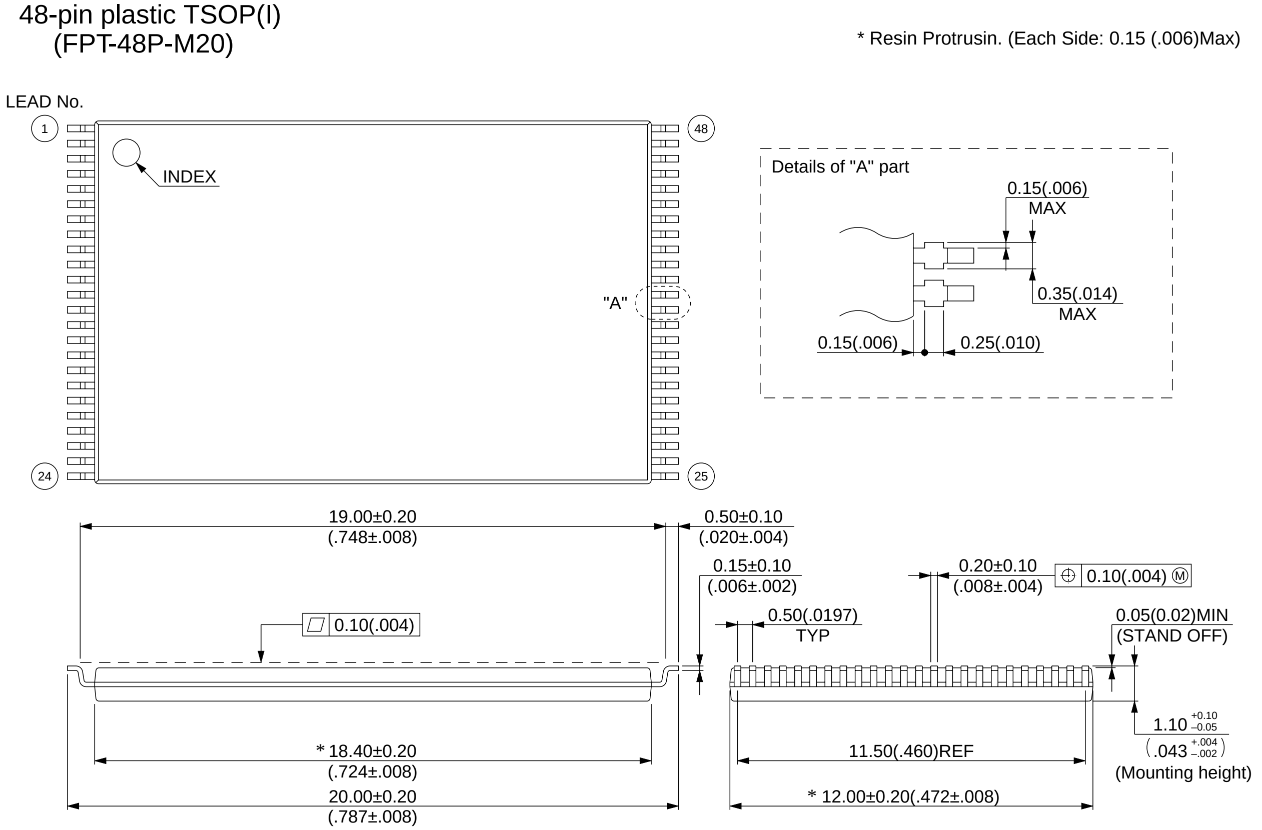
48-pin plastic TSOP(I)
(FPT-48P-M20)



(Continued)

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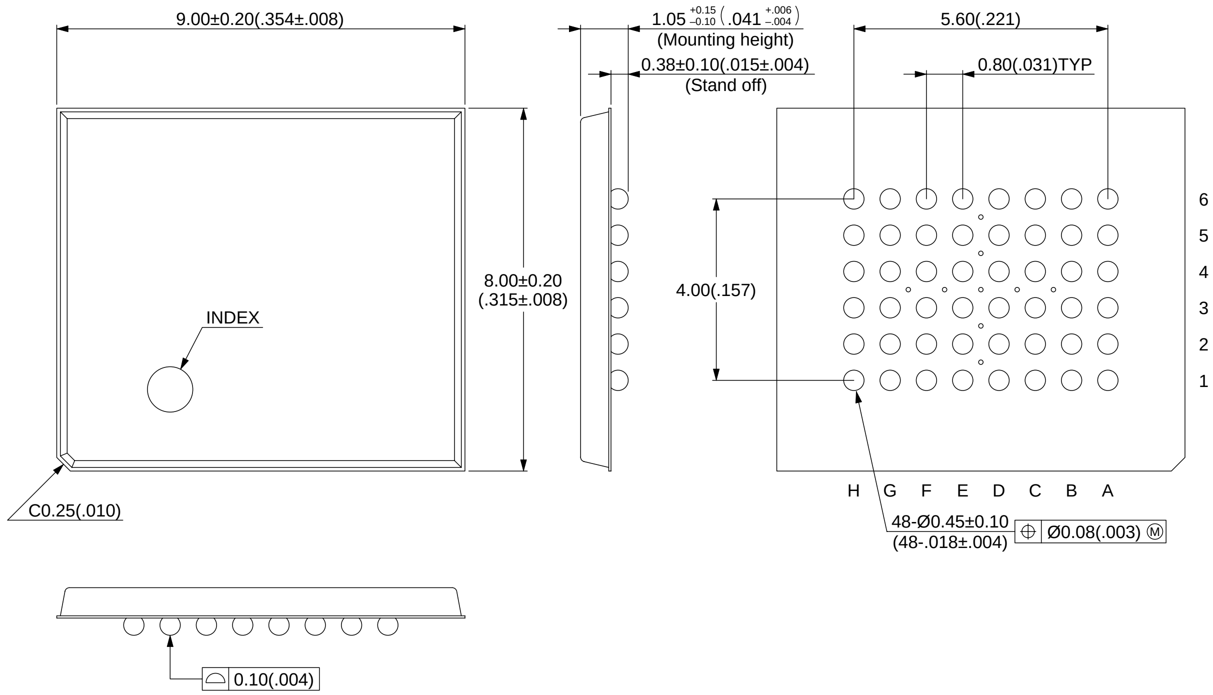
48-pin plastic FBGA
(BGA-48P-M13)

Note: The actual shape of corners may differ from the dimension.



Dimensions in mm (inches)

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F9910

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