



Integrated Device Technology, Inc.

# CMOS STATIC RAM 1 MEG (128K x 8-BIT)

IDT71024S70

### FEATURES:

- 128K x 8 CMOS static RAM
- Equal access and cycle times
  - Commercial: 70ns
- Two Chip Selects plus one Output Enable pin
- Bidirectional inputs and outputs directly TTL-compatible
- Low power consumption via chip deselect
- Available in 300 and 400 mil Plastic SOJ packages

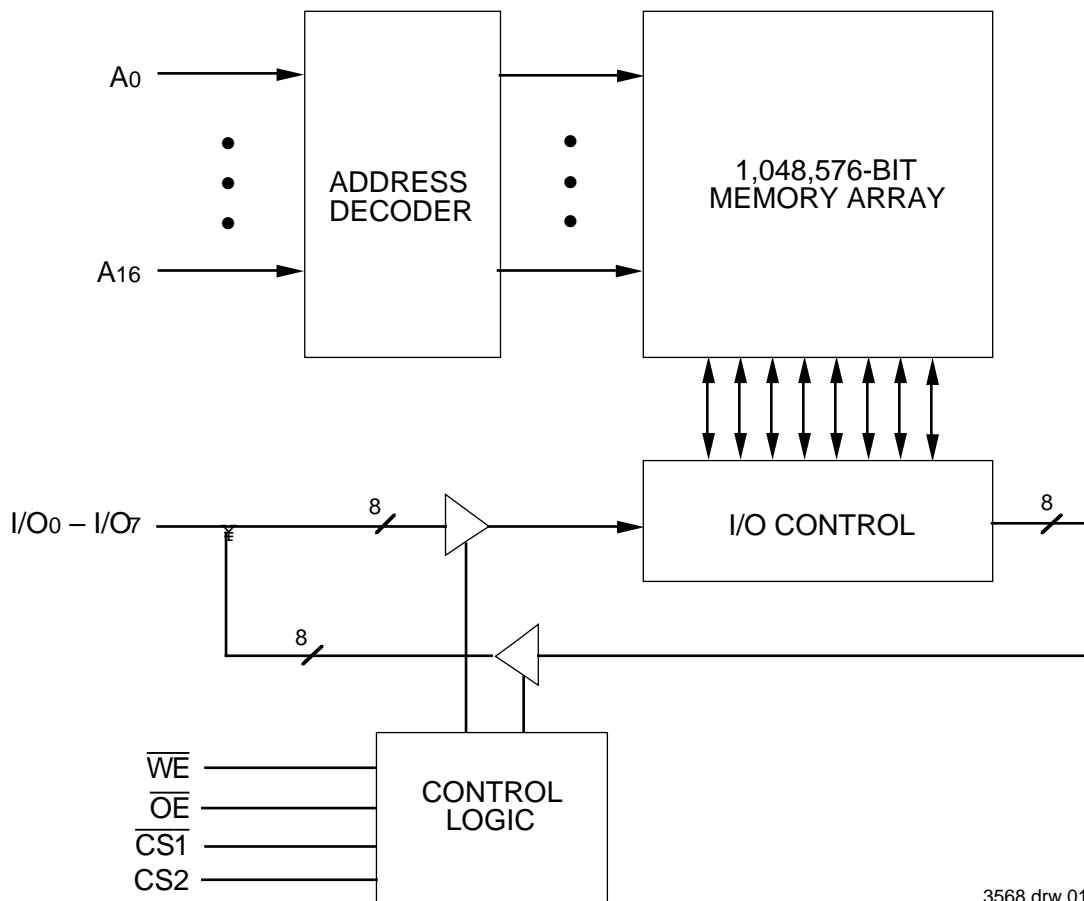
### DESCRIPTION:

The IDT71024 is a 1,048,576-bit medium-speed static RAM organized as 128K x 8. It is fabricated using IDT's high-performance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for your memory needs.

The IDT71024 has an output enable pin which operates as fast as 30ns, with address access times as fast as 70ns available. All bidirectional inputs and outputs of the IDT71024 are TTL-compatible and operation is from a single 5V supply. Fully static asynchronous circuitry is used; no clocks or refreshes are required for operation.

The IDT71024 is packaged in 32-pin 300 mil Plastic SOJ and 32-pin 400 mil Plastic SOJ packages.

### FUNCTIONAL BLOCK DIAGRAM



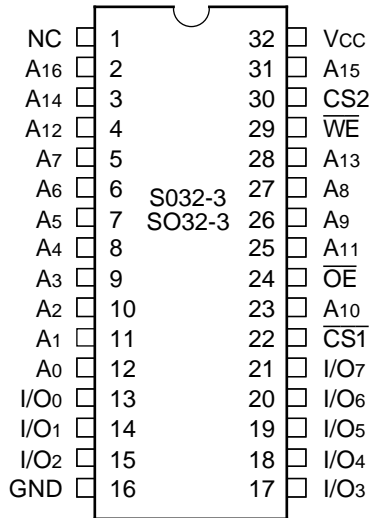
3568 drw 01

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**COMMERCIAL TEMPERATURE RANGE**

**MAY 1996**

## PIN CONFIGURATION



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SOJ  
TOP VIEW

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

| Symbol               | Rating                               | Com'L.       | Unit |
|----------------------|--------------------------------------|--------------|------|
| VTERM <sup>(2)</sup> | Terminal Voltage with Respect to GND | -0.5 to +7.0 | V    |
| TA                   | Operating Temperature                | 0 to +70     | °C   |
| TBIAS                | Temperature Under Bias               | -55 to +125  | °C   |
| TSTG                 | Storage Temperature                  | -55 to +125  | °C   |
| PT                   | Power Dissipation                    | 1.25         | W    |
| IOUT                 | DC Output Current                    | 50           | mA   |

### NOTES:

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- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- VTERM must not exceed VCC + 0.5V.

## TRUTH TABLE<sup>(1,2)</sup>

| INPUTS |                    |                    |    | I/O     | FUNCTION                  |
|--------|--------------------|--------------------|----|---------|---------------------------|
| WE     | CS1                | CS2                | OE |         |                           |
| X      | H                  | X                  | X  | High-Z  | Deselected—Standby (ISB)  |
| X      | VHC <sup>(3)</sup> | X                  | X  | High-Z  | Deselected—Standby (ISB1) |
| X      | X                  | L                  | X  | High-Z  | Deselected—Standby (ISB)  |
| X      | X                  | VLC <sup>(3)</sup> | X  | High-Z  | Deselected—Standby (ISB1) |
| H      | L                  | H                  | H  | High-Z  | Outputs Disabled          |
| H      | L                  | H                  | L  | DATAOUT | Read Data                 |
| L      | L                  | H                  | X  | DATAIN  | Write Data                |

### NOTES:

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- H = VIH, L = VIL, X = Don't care.
- VLC = 0.2V, VHC = VCC - 0.2V.
- Other inputs ≥ VHC or ≤ VLC.

## CAPACITANCE

(TA = +25°C, f = 1.0MHz, SOJ package)

| Symbol | Parameter <sup>(1)</sup> | Conditions | Max. | Unit |
|--------|--------------------------|------------|------|------|
| CIN    | Input Capacitance        | VIN = 3dV  | 8    | pF   |
| CIO    | I/O Capacitance          | VOUT = 3dV | 8    | pF   |

### NOTE:

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- This parameter is guaranteed by device characterization, but is not production tested.

## RECOMMENDED DC OPERATING CONDITIONS

| Symbol | Parameter          | Min.                | Typ. | Max.    | Unit |
|--------|--------------------|---------------------|------|---------|------|
| VCC    | Supply Voltage     | 4.5                 | 5.0  | 5.5     | V    |
| GND    | Supply Voltage     | 0                   | 0    | 0       | V    |
| VIH    | Input High Voltage | 2.2                 | —    | VCC+0.5 | V    |
| VIL    | Input Low Voltage  | -0.5 <sup>(1)</sup> | —    | 0.8     | V    |

### NOTE:

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- VIL (min.) = -1.5V for pulse width less than 10ns, once per cycle.

## DC ELECTRICAL CHARACTERISTICS

VCC = 5.0V ± 10%

| Symbol | Parameter              | Test Condition                                      | IDT71024 |      | Unit |
|--------|------------------------|---|----------|------|------|
|        |                        |   | Min.     | Max. |      |
| ILI    | Input Leakage Current  | VCC = Max., VIN = GND to VCC                        | —        | 5    | μA   |
| ILO    | Output Leakage Current | VCC = Max., CS1 = VIH, CS2 = VIL, VOUT = GND to VCC | —        | 5    | μA   |
| VOL    | Output LOW Voltage     | IOL = 8mA, VCC = Min.                               | —        | 0.4  | V    |
| VOH    | Output HIGH Voltage    | IOH = -4mA, VCC = Min.                              | 2.4      | —    | V    |

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## DC ELECTRICAL CHARACTERISTICS<sup>(1)</sup>

( $V_{CC} = 5.0V \pm 10\%$ ,  $V_{LC} = 0.2V$ ,  $V_{HC} = V_{CC} - 0.2V$ )

| Symbol           | Parameter   | 71024S70 |      | Unit |
|------------------|---|----------|------|------|
|                  |   | Com'l.   | Mil. |      |
| I <sub>CC</sub>  | Dynamic Operating Current, CS2 ≥ V <sub>IH</sub> and CS2 ≥ V <sub>IH</sub> and $\overline{CS1} \leq V_{IL}$ , Outputs Open, V <sub>CC</sub> = Max., f = f <sub>MAX</sub> <sup>(2)</sup>   | 140      | —    | mA   |
| I <sub>SB</sub>  | Standby Power Supply Current (TTL Level) CS1 ≥ V <sub>IH</sub> or CS2 ≤ V <sub>IL</sub> , Outputs Open, V <sub>CC</sub> = Max., f = f <sub>MAX</sub> <sup>(2)</sup>   | 35       | —    | mA   |
| I <sub>SB1</sub> | Full Standby Power Supply Current (CMOS Level) CS1 ≥ V <sub>HC</sub> , or CS2 ≤ V <sub>LC</sub> Outputs Open, V <sub>CC</sub> = Max., f = 0 <sup>(2)</sup> , V <sub>IN</sub> ≤ V <sub>LC</sub> or V <sub>IN</sub> ≥ V <sub>HC</sub> | 10       | —    | mA   |

### NOTES:

1. All values are maximum guaranteed values.

2. f<sub>MAX</sub> = 1/trc (all address inputs are cycling at f<sub>MAX</sub>); f = 0 means no address input lines are changing.

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## AC TEST CONDITIONS

|                               |                     |
|-------------------------------|---------------------|
| Input Pulse Levels            | GND to 3.0V         |
| Input Rise/Fall Times         | 3ns                 |
| Input Timing Reference Levels | 1.5V                |
| Output Reference Levels       | 1.5V                |
| AC Test Load                  | See Figures 1 and 2 |

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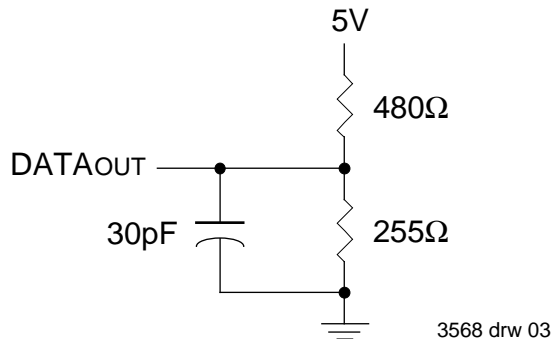
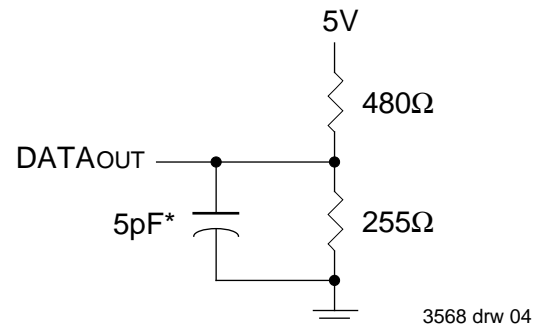


Figure 1. AC Test Load



\*Including jig and scope capacitance.

Figure 2. AC Test Load  
(for t<sub>CLZ</sub>, t<sub>OLZ</sub>, t<sub>CHZ</sub>, t<sub>OHZ</sub>, t<sub>OW</sub>, and t<sub>WHZ</sub>)

**AC ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 5.0V \pm 10\%$ , Commercial Temperature Range)

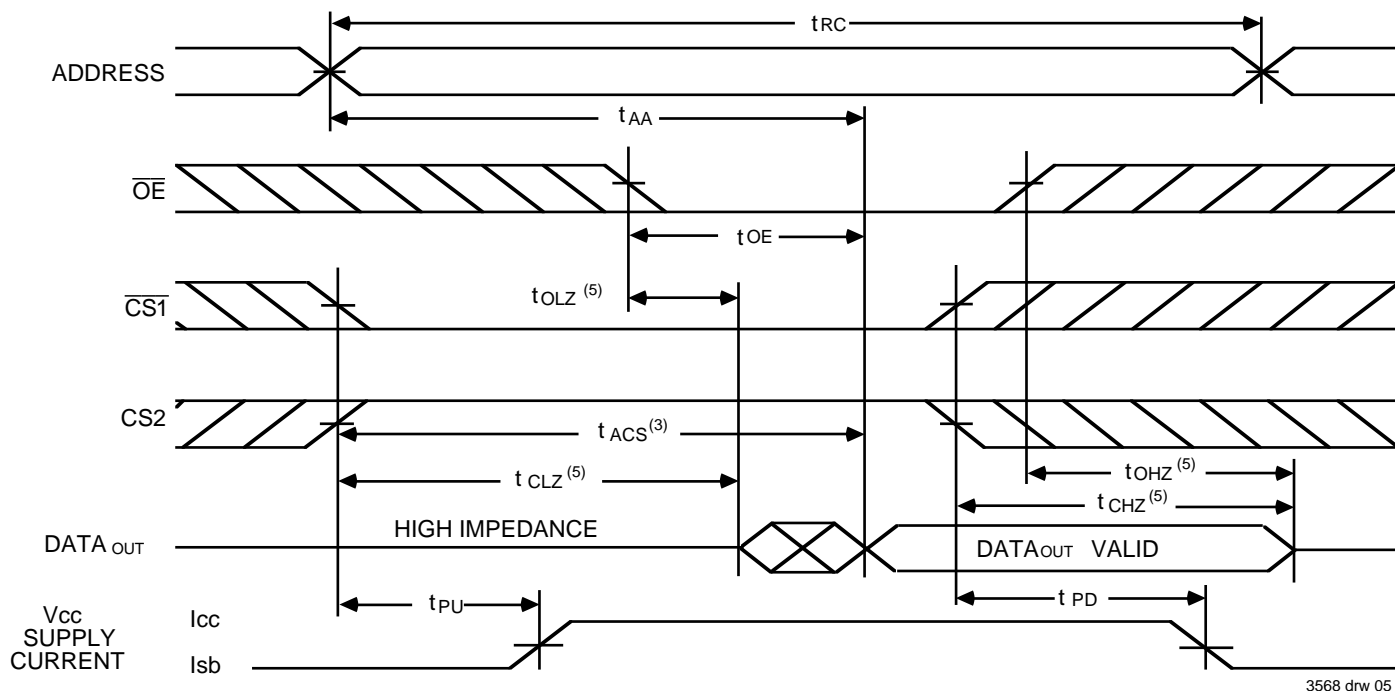
| Symbol                          | Parameter                          | 71024S70 |      | Unit |
|---------------------------------|------------------------------------|----------|------|------|
|                                 |                                    | Min.     | Max. |      |
| <b>Read Cycle</b>               |                                    |          |      |      |
| t <sub>RC</sub>                 | Read Cycle Time                    | 70       | —    | ns   |
| t <sub>AA</sub>                 | Address Access Time                | —        | 70   | ns   |
| t <sub>ACS</sub>                | Chip Select Access Time            | —        | 70   | ns   |
| t <sub>CLZ</sub> <sup>(2)</sup> | Chip Select to Output in Low-Z     | 3        | —    | ns   |
| t <sub>CHZ</sub> <sup>(2)</sup> | Chip Deselect to Output in High-Z  | 0        | 30   | ns   |
| t <sub>OE</sub>                 | Output Enable to Output Valid      | —        | 30   | ns   |
| t <sub>OLZ</sub> <sup>(2)</sup> | Output Enable to Output in Low-Z   | 0        | —    | ns   |
| t <sub>OHZ</sub> <sup>(2)</sup> | Output Disable to Output in High-Z | 0        | 30   | ns   |
| t <sub>OH</sub>                 | Output Hold from Address Change    | 4        | —    | ns   |
| t <sub>PU</sub> <sup>(2)</sup>  | Chip Select to Power-Up Time       | 0        | —    | ns   |
| t <sub>PD</sub> <sup>(2)</sup>  | Chip Deselect to Power-Down Time   | —        | 70   | ns   |
| <b>Write Cycle</b>              |                                    |          |      |      |
| t <sub>WC</sub>                 | Write Cycle Time                   | 70       | —    | ns   |
| t <sub>AW</sub>                 | Address Valid to End-of-Write      | 60       | —    | ns   |
| t <sub>CW</sub>                 | Chip Select to End-of-Write        | 60       | —    | ns   |
| t <sub>AS</sub>                 | Address Set-up Time                | 0        | —    | ns   |
| t <sub>WP</sub>                 | Write Pulse Width                  | 45       | —    | ns   |
| t <sub>WR</sub>                 | Write Recovery Time                | 0        | —    | ns   |
| t <sub>DW</sub>                 | Data Valid to End-of-Write         | 30       | —    | ns   |
| t <sub>DH</sub>                 | Data Hold Time                     | 0        | —    | ns   |
| t <sub>OW</sub> <sup>(2)</sup>  | Output Active from End-of-Write    | 5        | —    | ns   |
| t <sub>WHZ</sub> <sup>(2)</sup> | Write Enable to Output in High-Z   | 0        | 30   | ns   |

**NOTES:**

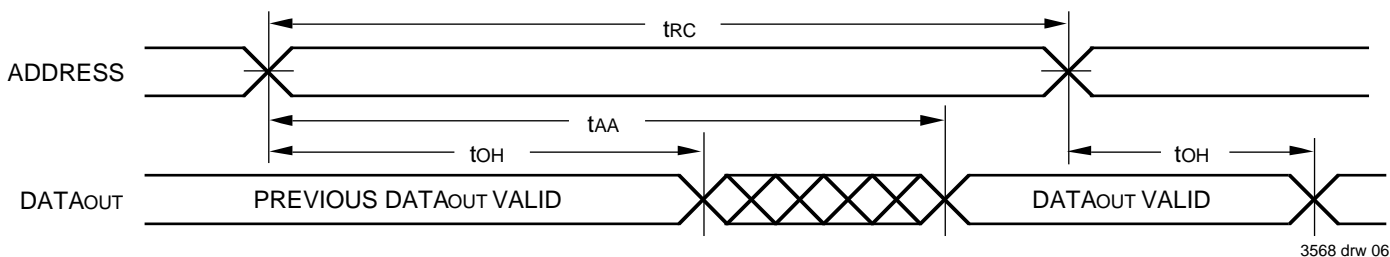
- 0°C to +70°C temperature range only.
- This parameter guaranteed with the AC load (Figure 2) by device characterization, but is not production tested.

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### TIMING WAVEFORM OF READ CYCLE NO. 1<sup>(1)</sup>



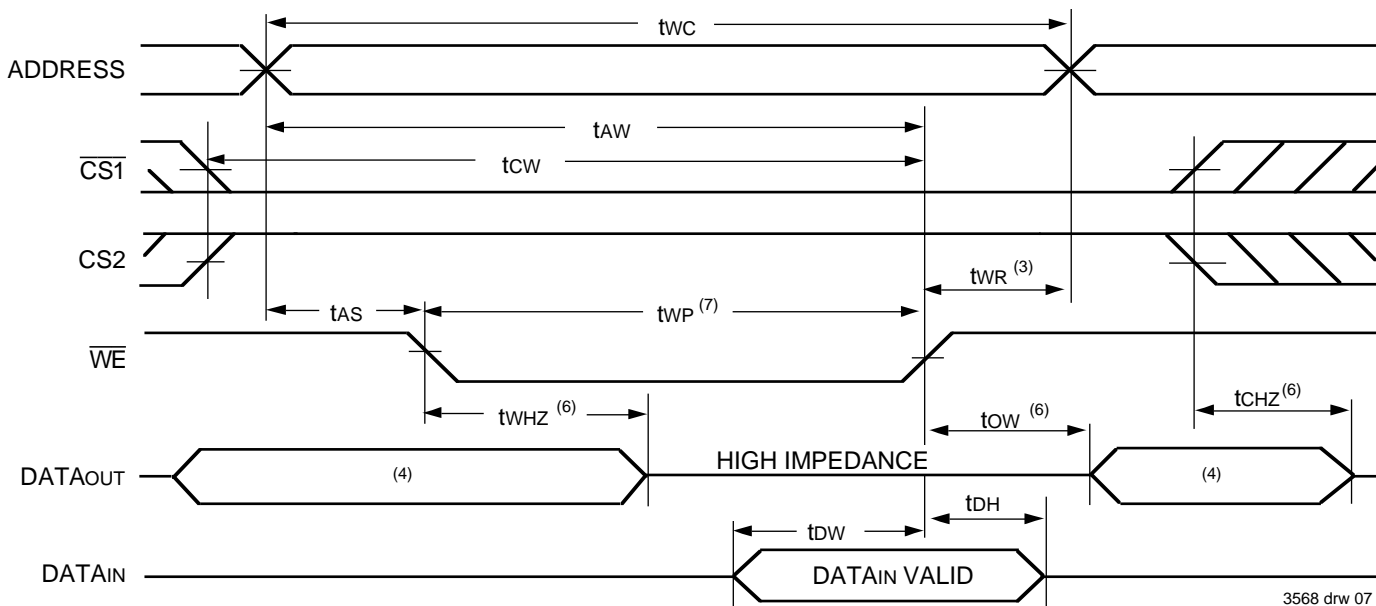
### TIMING WAVEFORM OF READ CYCLE NO. 2<sup>(1, 2, 4)</sup>



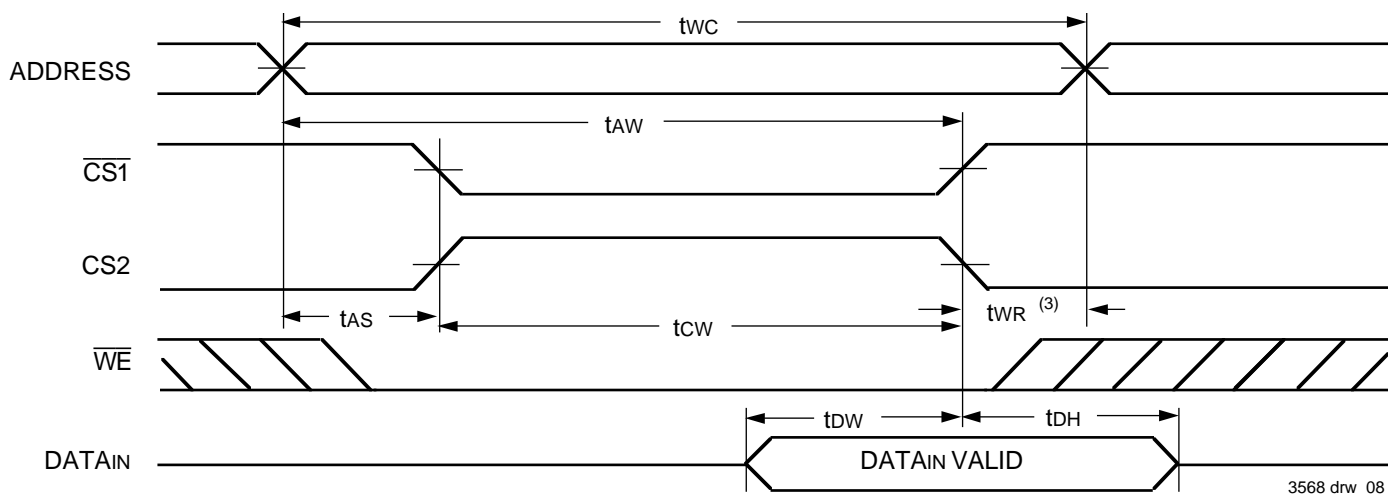
**NOTES:**

1.  $\overline{WE}$  is HIGH for Read Cycle.
2. Device is continuously selected,  $\overline{CS1}$  is LOW, CS2 is HIGH.
3. Address must be valid prior to or coincident with the later of  $\overline{CS1}$  transition LOW and CS2 transition HIGH; otherwise  $t_{AA}$  is the limiting parameter.
4. OE is LOW.
5. Transition is measured  $\pm 200\text{mV}$  from steady state.

**TIMING WAVEFORM OF WRITE CYCLE NO. 1 ( $\overline{WE}$  CONTROLLED TIMING)<sup>(1, 2, 5, 7)</sup>**



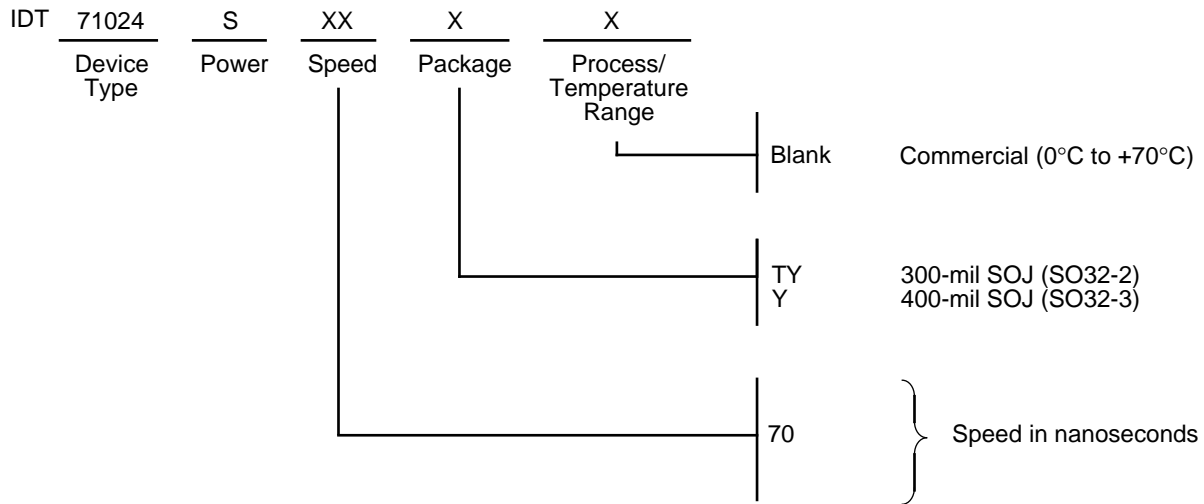
**TIMING WAVEFORM OF WRITE CYCLE NO. 2 ( $\overline{CS1}$  AND CS2 CONTROLLED TIMING)<sup>(1, 2, 5)</sup>**



**NOTES:**

1.  $\overline{WE}$  must be HIGH,  $\overline{CS1}$  must be HIGH, or CS2 must be LOW during all address transitions.
2. A write occurs during the overlap of a LOW  $\overline{CS1}$ , HIGH CS2, and a LOW  $\overline{WE}$ .
3.  $t_{WR}$  is measured from the earlier of either  $\overline{CS1}$  or  $\overline{WE}$  going HIGH or CS2 going LOW to the end of the write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the  $\overline{CS1}$  LOW transition or the CS2 HIGH transition occurs simultaneously with or after the  $\overline{WE}$  LOW transition, the outputs remain in a high impedance state.  $\overline{CS1}$  and CS2 must both be active during the  $t_{CW}$  write period.
6. Transition is measured  $\pm 200mV$  from steady state.
7.  $\overline{OE}$  is continuously HIGH. During a  $\overline{WE}$  controlled write cycle with  $\overline{OE}$  LOW,  $t_{WP}$  must be greater than or equal to  $t_{WHZ} + t_{DW}$  to allow the I/O drivers to turn off and data to be placed on the bus for the required  $t_{DW}$ . If  $\overline{OE}$  is HIGH during a  $\overline{WE}$  controlled write cycle, this requirement does not apply and the minimum write pulse is the specified  $t_{WP}$ .

### ORDERING INFORMATION



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