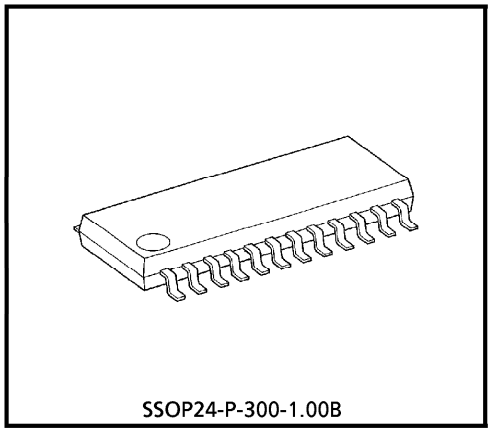
TOSHIBA INTELLIGENT POWER DEVICE SILICON MONOLITHIC POWER MOS INTEGRATED CIRCUIT

TPD2005F

HIGH-SIDE POWER SWITCH ARRAY (8 CHANNELS) for MOTORS, SOLENOIDS, and LAMP DRIVES

The TPD2005F is an 8-channel high-side switch array for vertical power MOS FET output. A monolithic power IC, it can directly drive a power load from a CMOS or TTL logic circuit (such as an MPU). It offers overcurrent and overtemperature protection functions.



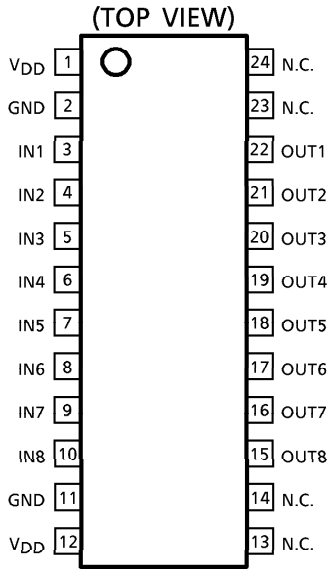
SSOP24-P-300-1.00B

Weight : 0.29 g (typ.)

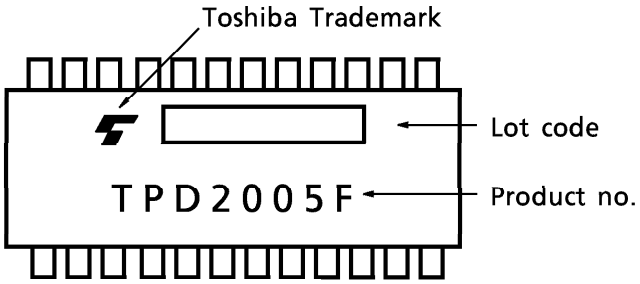
FEATURES

- A high-side switch array incorporating an N-channel power MOS FET (1.2 Ω max.) and an 8-channel charge pump.
- Can directly drive a power load from a microprocessor.
- Built-in protection against overtemperature protection and overcurrent protection.
- 8-channel access enables space-saving design.
- High operating voltage : 40 V
- Low on-resistance : 1.2 Ω max. @V_{DD} = 12 V, I_O = 0.5 A (per channel)
- Supports parallel operation.
- Low operating current : 5 mA max. @V_{DD} = 40 V, V_{IN} = 0 V
- Supplied in an SSOP-24 package (300 mil) in embossed taping.

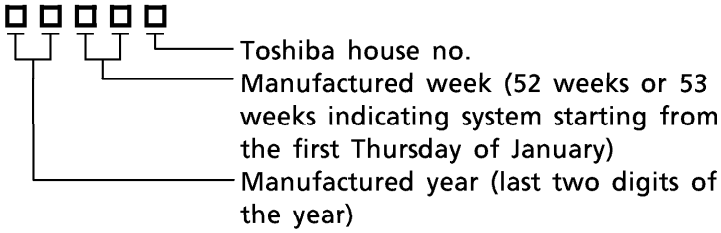
PIN ASSIGNMENT



MARKING



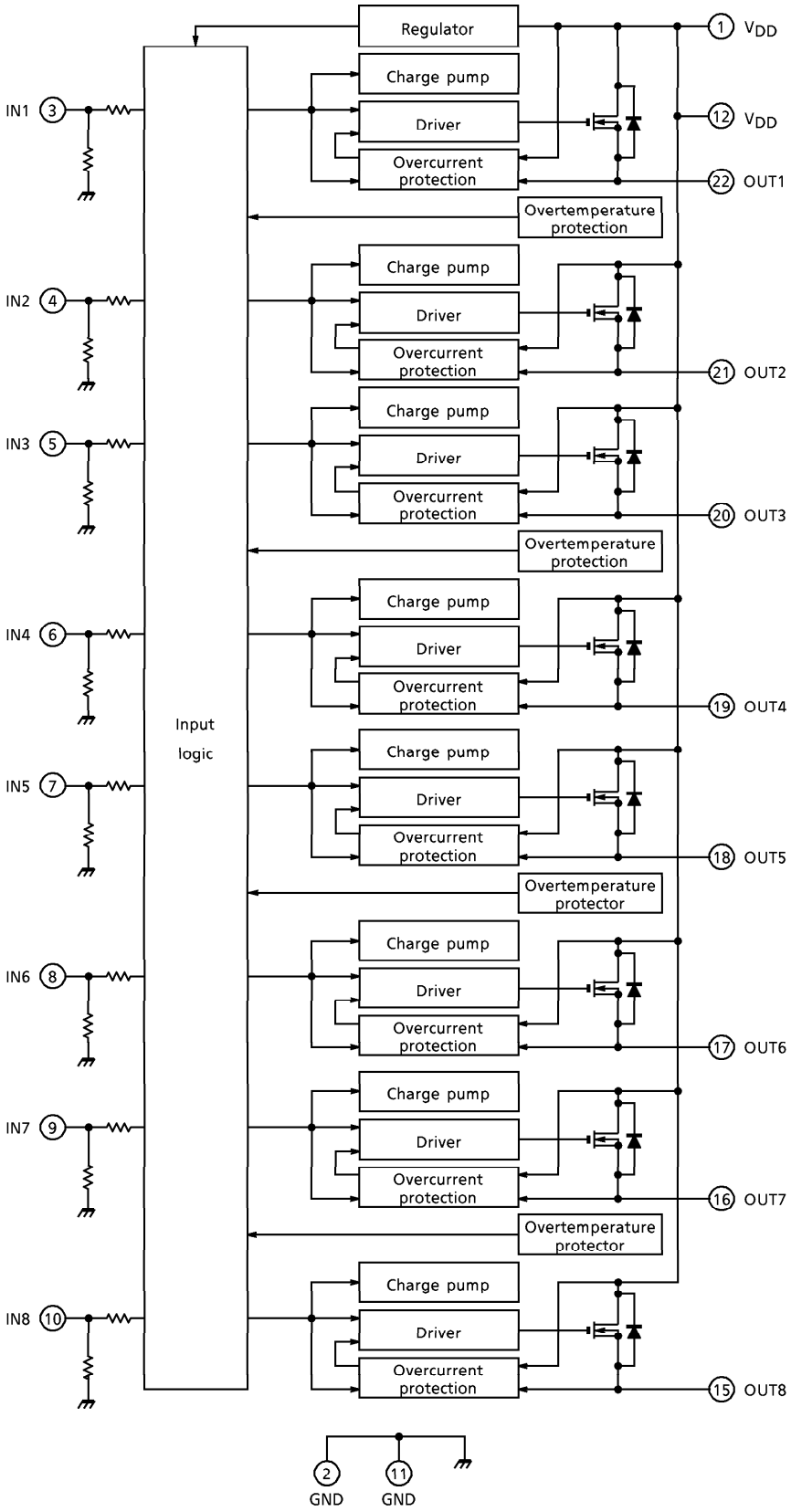
Lot code naming system



This device uses MOS structure, it is sensitive to electrostatics. Please take this into account.

980910EBA2

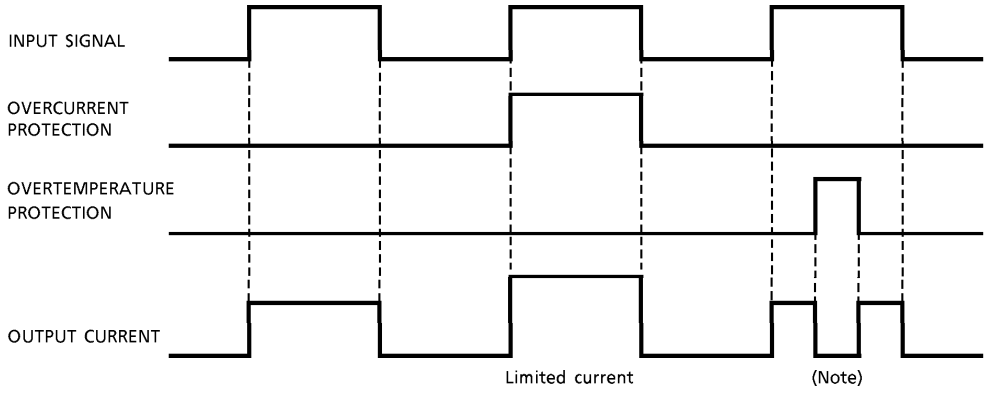
BLOCK DIAGRAM



PIN DESCRIPTION

PIN No.	SYMBOL	DESCRIPTION
1	V_{DD}	Power supply pin; in common with the pin no.12 internally.
2	GND	GND pin; in common with the pin no.11 internally.
3	IN1	Control input pin for channel 1 and built-in pull-down resistor (100 kΩ typ.)
4	IN2	Control input pin for channel 2 and built-in pull-down resistor (100 kΩ typ.)
5	IN3	Control input pin for channel 3 and built-in pull-down resistor (100 kΩ typ.)
6	IN4	Control input pin for channel 4 and built-in pull-down resistor (100 kΩ typ.)
7	IN5	Control input pin for channel 5 and built-in pull-down resistor (100 kΩ typ.)
8	IN6	Control input pin for channel 6 and built-in pull-down resistor (100 kΩ typ.)
9	IN7	Control input pin for channel 7 and built-in pull-down resistor (100 kΩ typ.)
10	IN8	Control input pin for channel 8 and built-in pull-down resistor (100 kΩ typ.)
11	GND	GND pin; in common with the pin no.2 internally.
12	V_{DD}	Power supply pin; in common with the pin no.1 internally.
13	N.C.	—
14	N.C.	—
15	OUT8	Output pin for channel 8
16	OUT7	Output pin for channel 7
17	OUT6	Output pin for channel 6
18	OUT5	Output pin for channel 5
19	OUT4	Output pin for channel 4
20	OUT3	Output pin for channel 3
21	OUT2	Output pin for channel 2
22	OUT1	Output pin for channel 1
23	N.C.	—
24	N.C.	—

TIMING CHART



(Note) : The overheating detector circuits feature hysteresis. After overheating is detected, normal operation is restored only when the junction temperature falls by the hysteresis amount (10°C typ.) in relation to the overheating detection temperature.

TRUTH TABLE

INPUT SIGNAL	OUTPUT SIGNAL	STATE
L	L	Normal
H	H	
L	L	Overcurrent protection
H	Internally limited	
L	L	Overtemperature protection
H	L	

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	45	V
Input Voltage	V_{IN}	−0.5~7	V
Drain-source Voltage	V_{DS}	60	V
Output Current	I_O	Internally Limited	A
Power Dissipation (Operating All Channels, Ta = 25°C)	P_T	0.8	W
		1.5 (Note)	
Single Pulse Avalanche Energy	E_{AS}	10	mJ
Operating Temperature	T_{opr}	−40~85	°C
Junction Temperature	T_j	150	°C
Storage Temperature	T_{stg}	−55~150	°C

THERMAL CHARACTERISTIC

CHARACTERISTIC	SYMBOL	RATING	UNIT
Thermal Resistance Junction to Ambient (Operating All Channels, Ta = 25°C)	$\Sigma R_{th\ (j\text{-}a)}$	156.3	°C / W
		83.4 (Note)	

(Note) : 60 mm × 60 mm × 1.6 t when a device is mounted on a glass epoxy PCB. (DC)

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, V_{DD} = 8~40 V, Ta = 25°C)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Operating Supply Voltage		V_{DD}	—	—	8	—	40	V
Supply Current		I_{DD}	—	V_{DD} = 40 V, V_{IN} = 0 V	—	—	5	mA
Input Voltage	"L" level	V_{IL}	—		—	—	1.5	V
	"H" level	V_{IH}	—		3.5	—	—	
Input Current		I_{IL}	—	V_{DD} = 24 V, V_{IN} = 0 V	− 10	—	10	μA
		I_{IH}	—	V_{DD} = 24 V, V_{IN} = 5V	—	50	200	
Output On Resistance		$R_{DS\ (ON)}$	—	V_{DD} = 12 V, I_O = 0.5 A	—	0.9	1.2	Ω
Output Leakage Current		I_{OL}	—	V_{DD} = 40 V, V_{IN} = 0 V	—	—	100	μA
Overcurrent Protection		I_S	—	—	1	—	3	A
Overtemperature Protection	Temperature	T_{SD}	—	—	—	160	—	°C
	Hysteresis	ΔT_{SD}	—	—	—	10	—	
Switching Time		t_{ON}	1	V_{DD} = 12 V, R_L = 24 Ω	—	11	200	μs
		t_{OFF}			—	4	50	

DESCRIPTION OF PROTECTOR CIRCUIT

(1) Overtemperature Protection

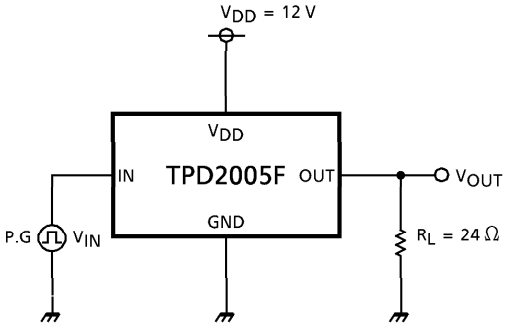
- Four overheating detector circuits are built in. One each for channels 1 and 2 ; channels 3 and 4 ; channels 5 and 6 ; and channels 7 and 8. The circuit logic is that, when any of the four detectors detects overheating, the circuit turns the output of both channels off (for example, channels 1 and 2).
- The overheating detector circuits feature hysteresis. After overheating is detected, normal operation is restored only when the junction temperature falls by the hysteresis amount (10°C typ.) in relation to the overheating detection temperature.

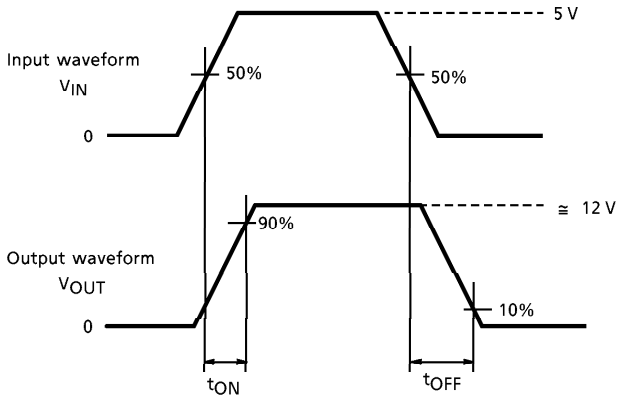
(2) Overcurrent Protection

- When overcurrent is detected, the overcurrent limiter function limits the output current. Normal operation is restored when the load current drops below the overcurrent detection value.

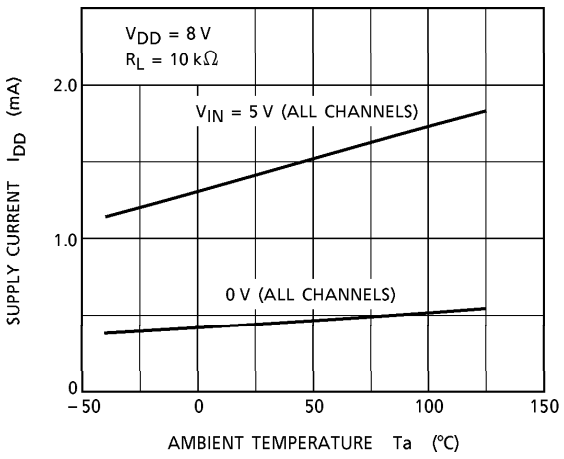
TEST CIRCUIT

Switching Time

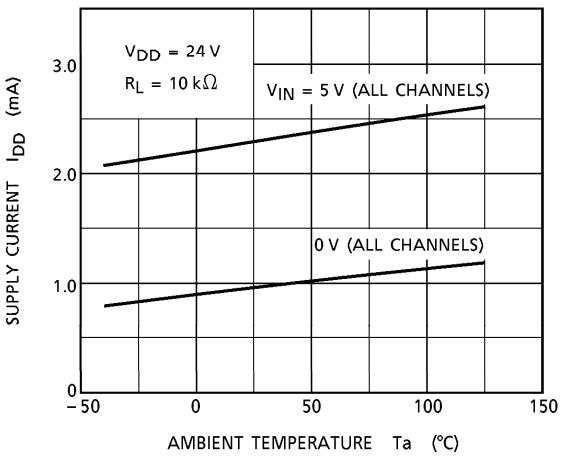




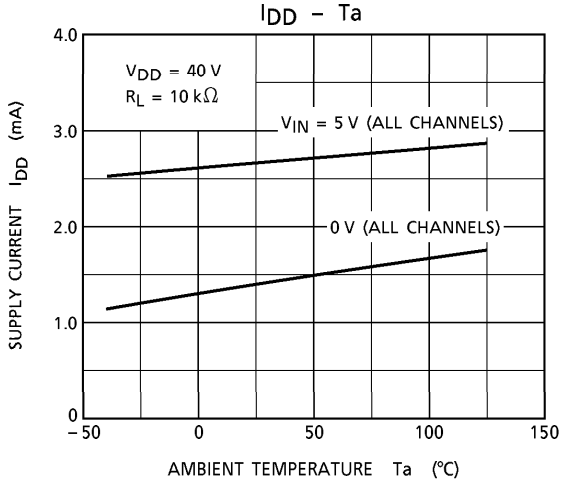
I_{DD} – Ta



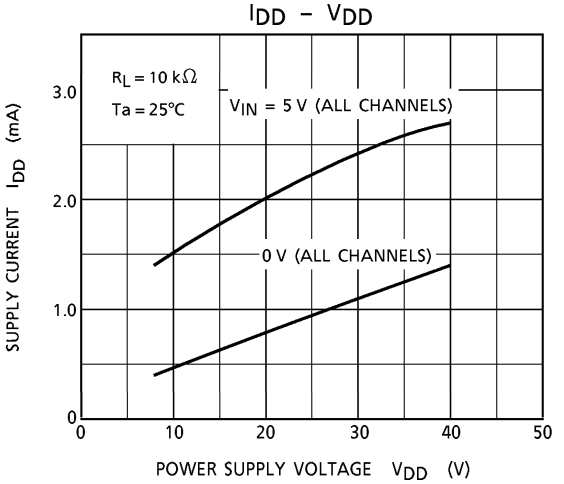
I_{DD} – Ta



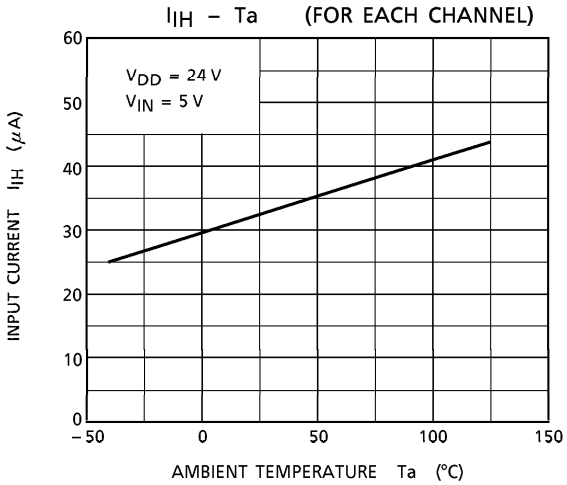
I_{DD} – Ta



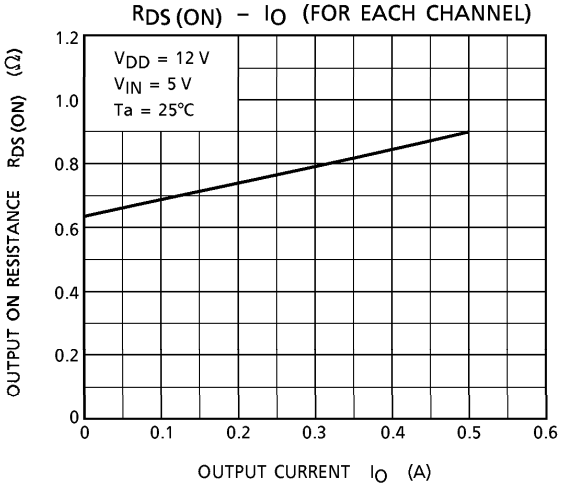
I_{DD} – V_{DD}



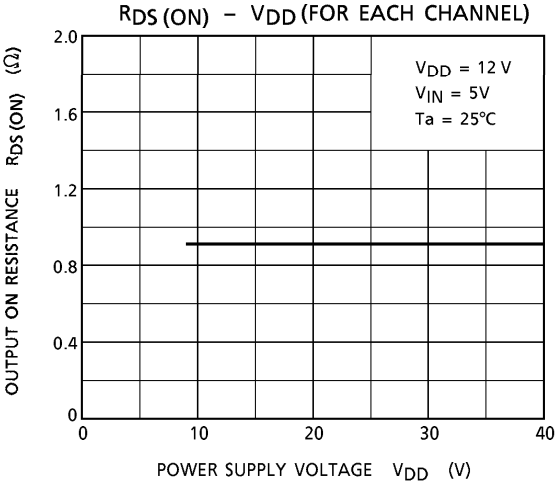
I_{IH} – Ta (FOR EACH CHANNEL)



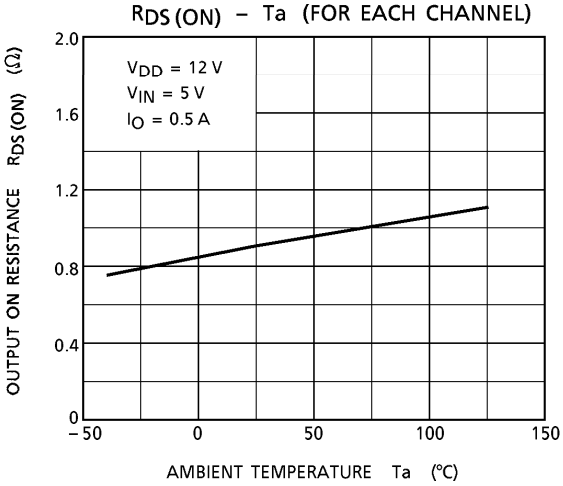
$R_{DS\,(ON)}$ – I_O (FOR EACH CHANNEL)



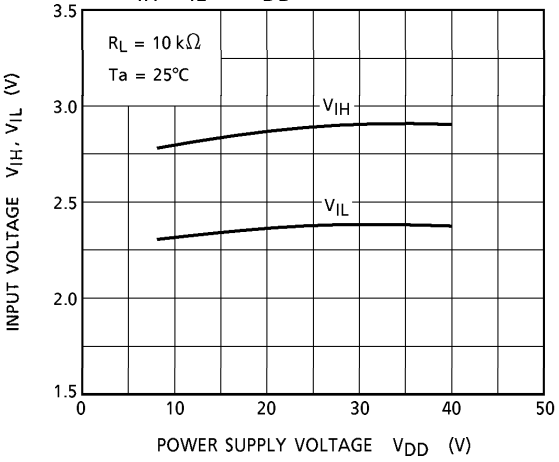
$R_{DS\,(ON)}$ – V_{DD} (FOR EACH CHANNEL)



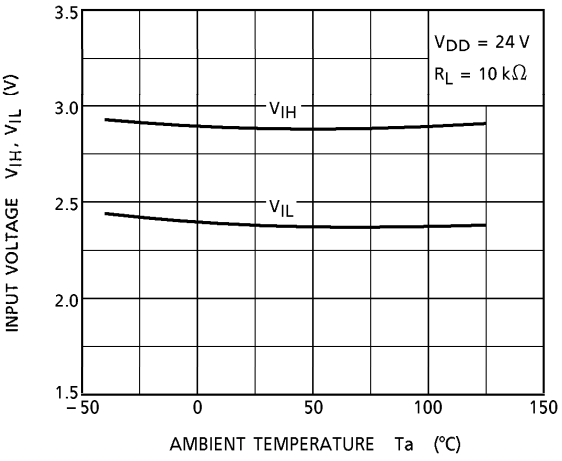
$R_{DS\,(ON)}$ – Ta (FOR EACH CHANNEL)



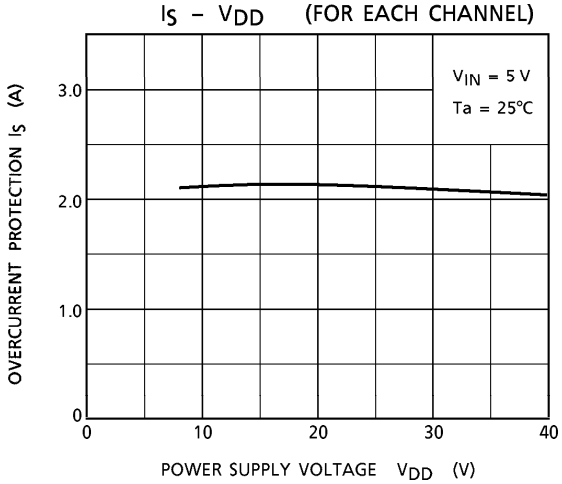
V_{IH}, V_{IL} – V_{DD} (FOR EACH CHANNEL)



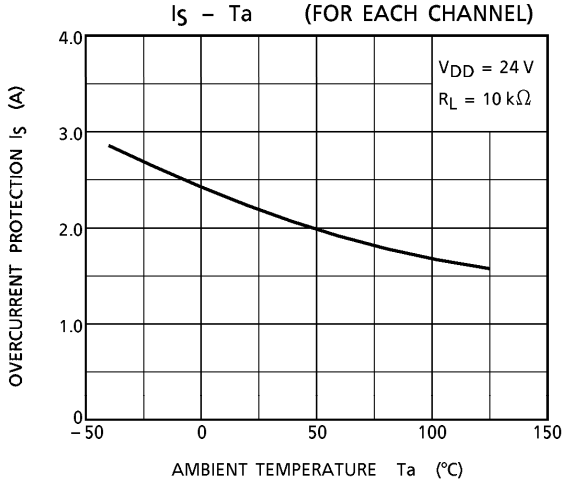
V_{IH}, V_{IL} – Ta (FOR EACH CHANNEL)



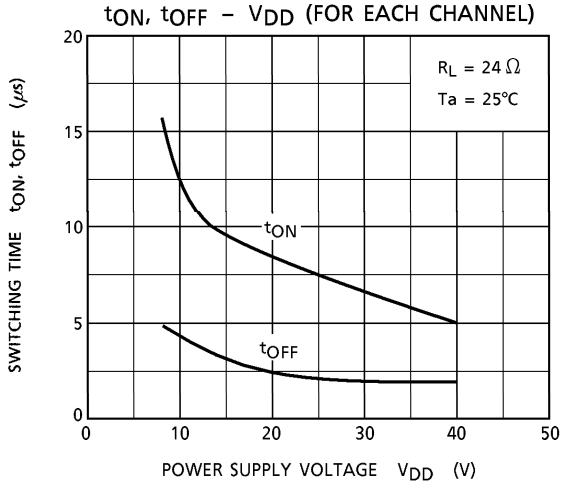
I_S – V_{DD} (FOR EACH CHANNEL)



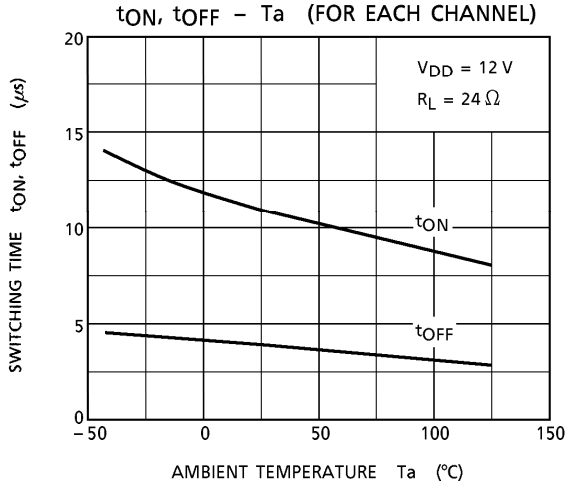
I_S – Ta (FOR EACH CHANNEL)



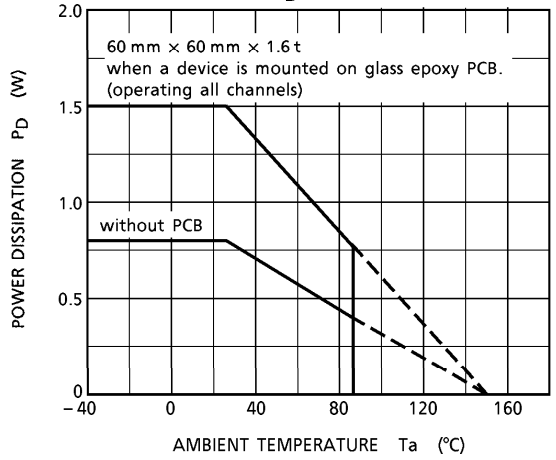
t_{ON}, t_{OFF} – V_{DD} (FOR EACH CHANNEL)



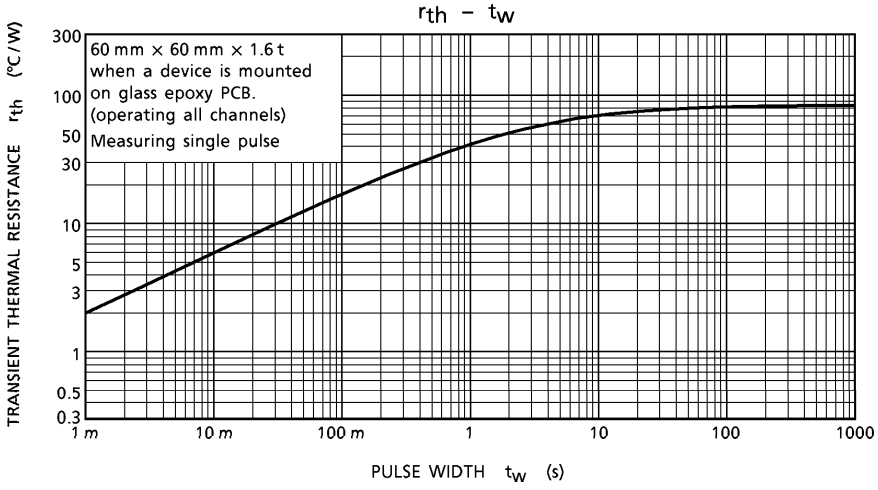
t_{ON}, t_{OFF} – Ta (FOR EACH CHANNEL)



P_D – Ta



r_{th} – t_W



CAUTION ON USAGE

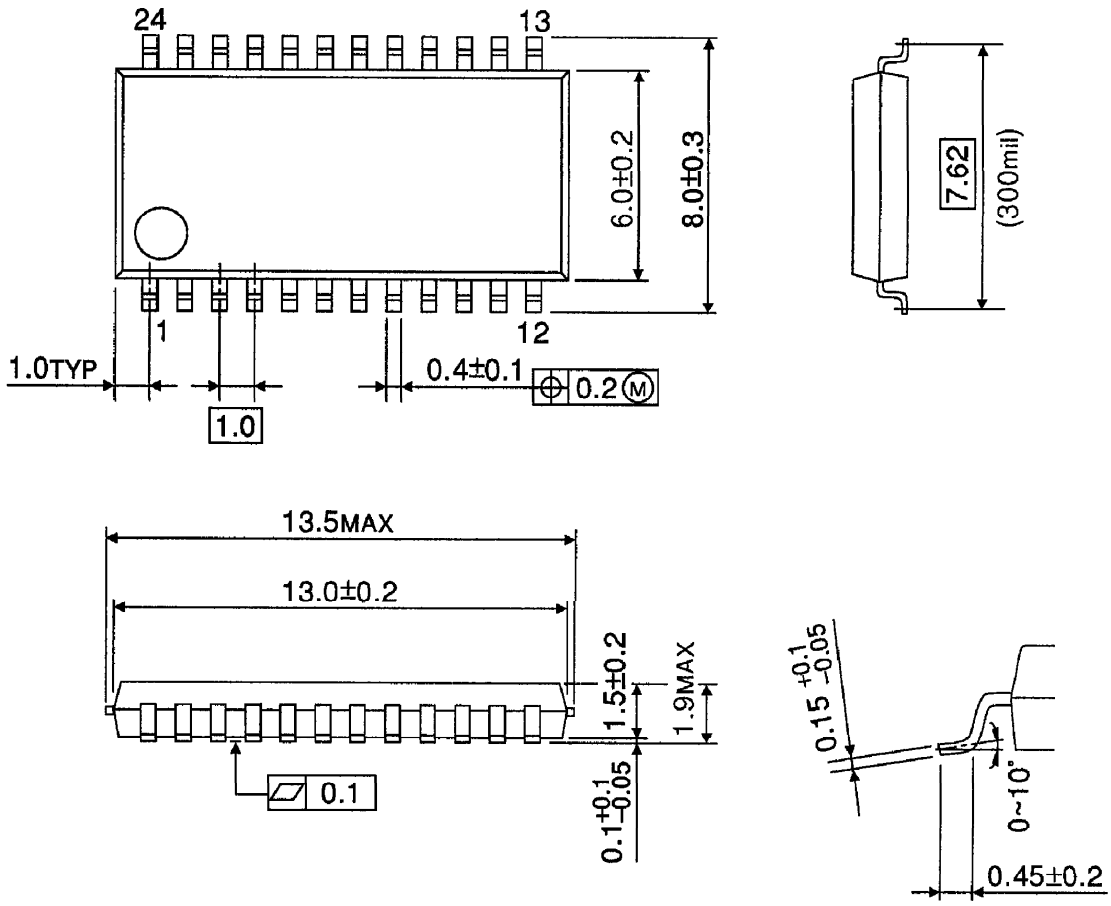
1. As protection against reverse connection of batteries is not provided, take protective measures using external circuits.
2. As a negative bias protector circuit is not built into the output pins, if negative bias is applied to the output pins, be sure to connect a freewheel diode between OUT and GND.

MOISTURE-PROOF PACKING

After the pack is opened, use the devices in a 30°C, 60% RH environment, and within the 48 hours. Embossed-tape packing cannot be baked. Devices so packed must be within their allowable time limits after unpacking, as specified on the packing.
Tape packing quantity: 500 devices / reel (EL) or 2000 devices / reel (EL1)

PACKAGE DIMENSIONS

SSOP24-P-300-1.00B Unit : mm



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