TH71101
315/433MHz
FSK/FM/ASK Receiver

Features

- ❑ Single superhet architecture for low external component count
- ❑ FSK for digital data and FM reception for analog signal transmission
- ❑ FM/FSK demodulation with phase-coincidence demodulator
- ❑ Low current consumption in active mode and very low standby current
- ❑ Switchable LNA gain for improved dynamic range
- ❑ RSSI allows signal strength indication and ASK detection
- ❑ Surface mount package LQFP32

Ordering Information

Part No.	***Temperature Range***	***Package***
TH71101	-40 °C to 85°C	LQFP32

Application Examples

- ❑ General digital and analog 315 MHz or 433 MHz ISM band usage
- ❑ Low-power telemetry
- ❑ Alarm and security systems
- ❑ Keyless car and central locking
- ❑ Pagers

Technical Data Overview

- ❑ Input frequency range: 300 MHz to 450 MHz
- ❑ Power supply range: 2.5 V to 5.5 V at 315 MHz and 2.7 V to 5.5 V at 433 MHz
- ❑ Temperature range: -40 °C to +85 °C
- ❑ Operating current: 6.5 mA at low gain and 8.2 mA at high gain mode
- ❑ Standby current: < 100 nA
- ❑ Sensitivity: -111 dBm [1)] with 40 kHz IF filter BW (incl. SAW front-end filter loss)
- ❑ Sensitivity: -104 dBm [2)] with 150 kHz IF filter BW (incl. SAW front-end filter loss)
- ❑ Range of IF: 455 kHz to 21.4 MHz
- ❑ Maximum input level: –10 dBm at ASK and 0 dBm at FSK
- ❑ Image rejection: > 55 dB (e.g. with SAW front-end filter and at 10.7 MHz IF)
- ❑ Spurious emission: < -70 dBm
- ❑ Input frequency acceptance: ±50 kHz (with AFC option)
- ❑ RSSI range: 70 dB
- ❑ Frequency deviation range: ±5 kHz to ±120 kHz
- ❑ Maximum data rate: 80 kbit/s NRZ
- ❑ Maximum analog modulation frequency: 15 kHz

[1)] at ± 8 kHz FSK deviation, BER = $3{\cdot}10^{-3}$ and phase-coincidence demodulation
[2)] at ± 50 kHz FSK deviation, BER = $3{\cdot}10^{-3}$ and phase-coincidence demodulation

General Description

The TH71101 receiver IC consists of the following building blocks

- PLL synthesizer (PLL SYNTH) for generation of the local oscillator signal LO
- Parts of the PLL SYNTH are the high-frequency VCO1, the feedback divider DIV_16,
  a phase-frequency detector (PFD) with charge pump (CP) and a crystal-based reference oscillator (RO)
- Low-noise amplifier (LNA) for high-sensitivity RF signal reception
- First mixer (MIX1) for down-conversion of the RF signal to the IF
- IF pre amplifier which is a mixer cell (MIX2) that operates as an amplifier
- IF amplifier (IFA) to amplify and limit the IF signal and for RSSI generation
- Phase coincidence demodulator (DEMOD) with third mixer (MIX3) to demodulate the IF signal
- Operational amplifier (OA) for data slicing, filtering and ASK detection
- Bias circuitry for bandgap biasing and circuit shutdown

With the TH71101 receiver chip, various circuit configurations can be arranged in order to meet a number of different customer requirements. For FM/FSK reception the IF tank used in the phase coincidence demodulator can be constituted either by a ceramic resonator or an LC tank (optionally with a varactor diode to create an AFC circuit). In ASK configuration, the RSSI signal is feed to an ASK detector, which is constituted by the operational amplifier.

Demodulation	Type of receiver
FM / FSK	narrow-band RX with ceramic demodulation tank
FM / FSK	wide-band RX with LC demodulation tank
ASK	RX with RSSI-based demodulation

A double-conversion variant, called TH71102, is also available. This receiver IC allows a higher degree of image rejection, achieved in conjunction with an RF frontend filter. Both RXICs have the same die. At the TH71102, the second mixer (MIX2) is used to down-convert the first IF (IF1) to the second IF (IF2). At the TH71101, MIX2 operates as an amplifier.

Efficient RF frontend filtering is realized by using a SAW, ceramic or helix filter in front of the LNA and by adding an LC filter at the LNA output.

Block Diagram

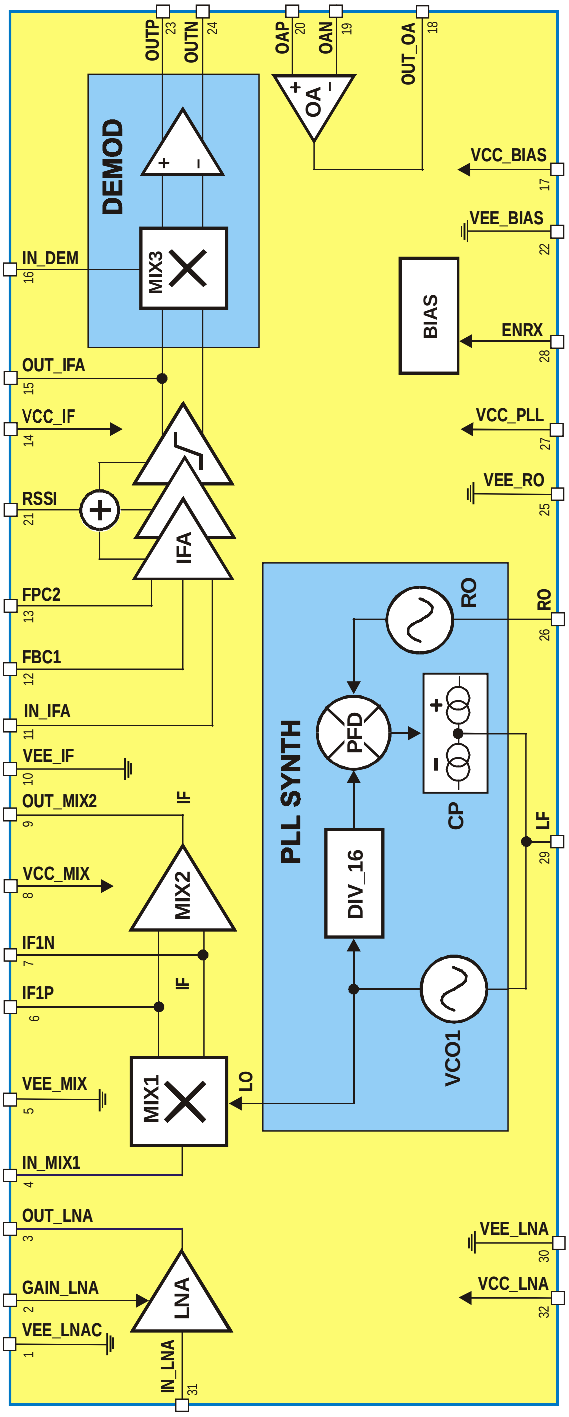


Fig. 1: TH71101 block diagram

Frequency Planning

Frequency planning is straightforward for single-conversion applications because there is only one IF that might be chosen, and then the only possible choice is low-side or high-side injection of the LO signal (which is now the one and only LO signal in the receiver).

The receiver's single-conversion architecture requires careful frequency planning. Besides the desired RF input signal, there are a number of spurious signals that may cause an undesired response at the output. Among them is the image of the RF signal that must be suppressed by the RF front-end filter.

By using the internal PLL synthesizer of the TH71101 with the fixed feedback divider ratio of N = 16 (DIV_16), two types of down-conversion are possible: low-side injection of LO and high-side injection of LO. The following table summarizes some equations that are useful to calculate the crystal reference frequency (REF), the IF and the LO frequency respectively, for a given RF.

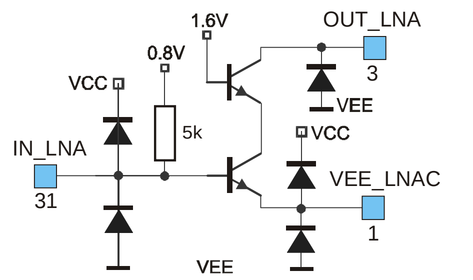
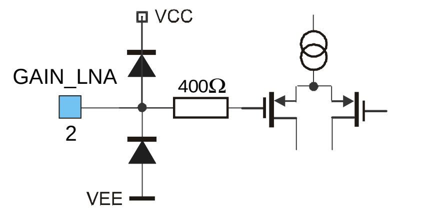
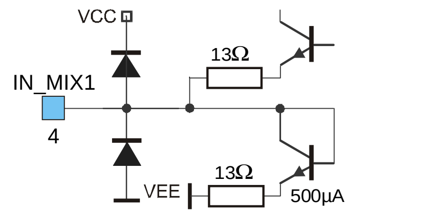
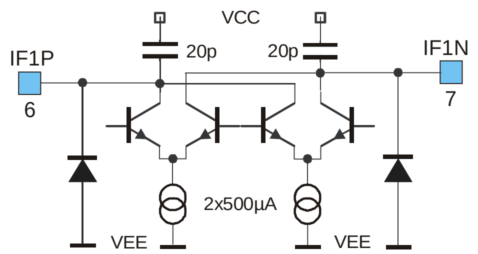
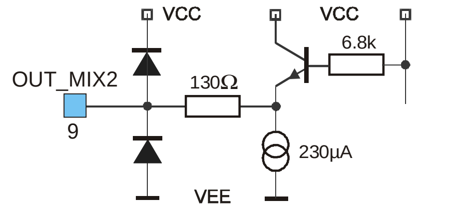
Injection type	low	high
REF	(RF – IF)/16	(RF + IF)/16
LO	16•REF	16•REF
IF	RF – LO	LO – RF
RF image	RF – 2IF	RF + 2IF

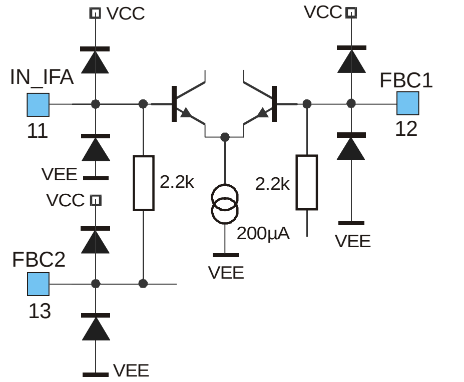
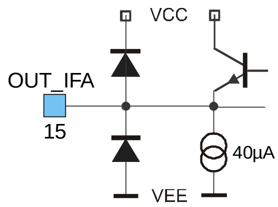
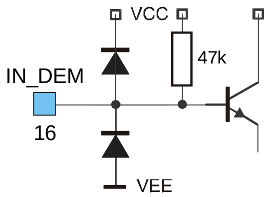
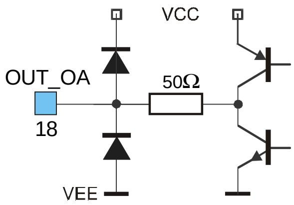
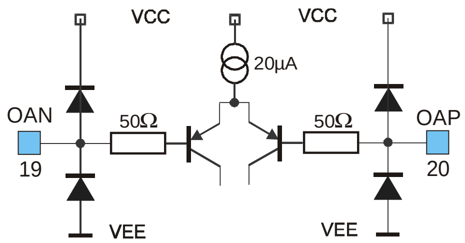
The following table depicts crystal, LO and image signals considering the examples of 315 MHz and 433.6 MHz RF reception at IF = 10.7 MHz.

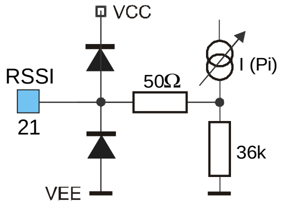
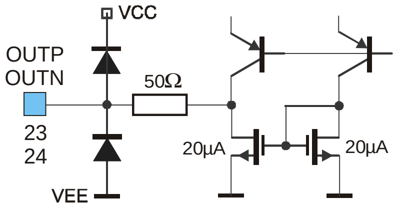
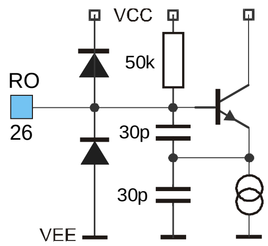
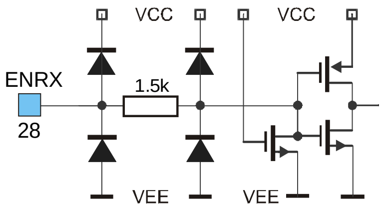
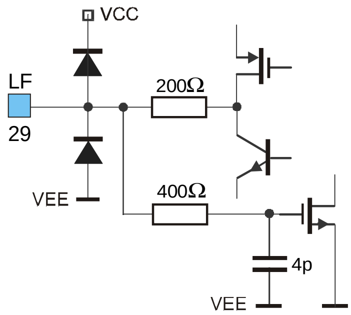
Signal type	RF = 315 MHz	RF = 315 MHz	RF = 433.6 MHz	RF = 433.6 MHz
Injection type	low	**high**	**low**	high
REF / MHz	19.01875	**20.35625**	**26.43125**	27.76875
LO / MHz	304.3	**325.7**	**422.9**	444.3
RF image / MHz	293.6	**336.4**	**412.2**	455.0

The selection of the reference crystal frequency is based on some assumptions. As for example: the image frequency should not be in a radio band where strong interfering signals might occur (because they could represent parasitic receiving signals), the LO signal should be in the range of 300 MHz to 430 MHz (because this is the optimum frequency range of the VCO1). Furthermore the IF should be as high as possible to achieve highest RF image rejection. The columns in bold depict the selected frequency plans to receive at 315 MHz and 433.6 MHz, respectively.

Pin Definition and Description

Pin No.	Name	I/O Type	Functional Schematic	Description
3	OUT_LNA	analog output		LNA open-collector output, to be connected to external LC tank that resonates at RF
31	IN_LNA	analog input		LNA input, approx. 26Ω single-ended
1	VEE_LNAC	ground		ground of LNA core (cascode)
2	GAIN_LNA	analog input		LNA gain control (CMOS input with hysteresis)
4	IN_MIX1	analog input		MIX1 input, approx. 33Ω single-ended
5	VEE_MIX	ground		LNA biasing ground
6	IF1P	analog I/O		open-collector output, to be connected to external LC tank that resonates at first IF
7	IF1N	analog I/O		open-collector output, to be connected to external LC tank that resonates at first IF
8	VCC_MIX	supply		MIX1 and MIX2 positive supply
9	OUT_MIX2	analog output		MIX2 output, approx. 330Ω output impedance
10	VEE_IF	ground		ground for MIX2, IFA and DEMOD

Pin No.	Name	I/O Type	Functional Schematic	Description
11	IN_IFA	analog input		IFA input, approx. 2.2kΩ input impedance
12	FBC1	analog I/O		to be connected to external IFA feedback capacitor
13	FBC2	analog I/O		to be connected to external IFA feedback capacitor
14	VCC_IF	supply		positive supply for IFA, DEMOD
15	OUT_IFA	analog I/O		IFA output and MIX3 input (of DEMOD)
16	IN_DEM	analog input		DEMOD input, to MIX3 core
17	VCC_BIAS	supply		positive supply of general bias system and OA
18	OUT_OA	analog output		OA output, 40uA current drive capability
19	OAN	analog input		negative OA input, input voltage limited to approx. 0.7 V_{pp} between pins OAP and OAN
20	OAP	analog input		negative OA input, input voltage limited to approx. 0.7 V_{pp} between pins OAP and OAN

Pin No.	Name	I/O Type	Functional Schematic	Description
21	RSSI	analog output		RSSI output, for RSSI and ASK detection, approx. 36kΩ output impedance
22	VEE_BIAS	ground		ground for general bias system and OA
23	OUTP	analog output		FSK/FM positive output, output impedance of 100kΩ to 300kΩ
24	OUTN	analog		FSK/FM negative output, output impedance of 100kΩ to 300kΩ
25	VEE_RO	ground		ground of dividers, PFD and RO
26	RO	analog input		RO input, Colpitts type oscillator with internal feed-back capacitors
27	VCC_PLL	supply		positive supply of RO, DIV, PFD and charge pump
28	ENRX	digital input		mode control input (CMOS Input)
29	LF	analog output		charge pump output and VCO1 control input
30	VEE_LNA	ground		LNA biasing ground
32	VCC_LNA	supply		positive supply of LNA biasing

Technical Data

Mode Configurations

ENRX	Mode	Description
0	SBY	standby mode
1	ON	entire chip active

Note: ENRX are pulled down internally

LNA Gain Control

V_{GAIN_LNA}	Mode	Description
< 0.8 V	HIGH GAIN	LNA set to high gain by voltage at GAIN_LNA
> 1.4 V	LOW GAIN	LNA set to low gain by voltage at GAIN_LNA

Note: hysteresis between gain modes to ensure stability

Absolute Maximum Ratings

Parameter	Symbol	Condition / Note	Min	Max	Unit
Supply voltage	V_{cc}		0	7.0	V
Input voltage	V_{IN}		- 0.3	V_{CC}+0.3	V
Input RF level	P_{imax}	no damage		10	dBm
Storage temperature	T_{STG}		-40	+125	°C
Electrostatic discharge	ESD	human body model, MIL STD 833D method 3015.7, all pins except OUT_IFA pin OUT_IFA	-500 -500	+500 +250	V V

Normal Operating Conditions

Parameter	Symbol	Condition	Min	Max	Unit
Supply voltage at 315 MHz	$V_{cc,\ 315}$	$f_i \leq 400$ MHz	2.5	5.5	V
Supply voltage at 433 MHz	$V_{cc,\ 433}$	$f_i > 400$ MHz	2.7	5.5	V
Operating temperature	T_a		-40	+85	ºC
Input frequency	f_i		300	450	MHz
Frequency deviation	Δf	at FM or FSK	±5	±120	kHz
FSK data rate	R_{FSK}	NRZ		40	kbit/s
FM bandwidth	f_m			15	kHz
ASK data rate	R_{ASK}	NRZ		80	kbit/s

DC Characteristics

all parameters under normal operating conditions, unless otherwise stated;
typical values at T_a = 23 °C and V_{cc} = 3 V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Standby current	I_{SBY}	ENRX=0			100	nA
Total supply current at low gain	$I_{cc, low}$	ENRX=1, LNA at LOW GAIN	5.0	6.5	8.0	mA
Total supply current at high gain	$I_{cc, high}$	ENRX=1, LNA at HIGH GAIN	6.5	8.2	10.0	mA
Opamp input offset voltage	V_{offs}		-20		20	mV
Opamp input offset current	I_{offs}	$I_{OAP} - I_{OAN}$	-50		50	nA
Opamp input bias current	I_{bias}	$0.5 * (I_{OAP} + I_{OAN})$	-100		100	nA
RSSI voltage at low input level	$V_{RSSI, low}$	P_i = -65 dBm, LNA at LOW GAIN	0.5	1.0	1.5	V
RSSI voltage at high input level	$V_{RSSI, high}$	P_i = -35 dBm, LNA at LOW GAIN	1.25	1.9	2.45	V

AC System Characteristics

all parameters under normal operating conditions, unless otherwise stated;
all parameters based on test circuits for FSK (Fig. 2), FM (Fig. 4) and ASK (Fig. 5), respectively;
typical values at T_a = 23 °C and V_{cc} = 3 V, RF at 433.6 MHz, second IF at 10.7 MHz

Parameter	Symbol	Condition	Min	Typ	Max	Unit
start-up time – FSK/FM	T_{FSK}	ENRX from 0 to 1, valid data at output			0.9	ms
start-up time – ASK	T_{ASK}	depends on ASK detector time constant, valid data at output			R3•C12 + T_{FSK}	ms
input sensitivity – FSK (narrow band)	$P_{min, n}$	B_{IF2} = 40kHz $\Delta f = \pm 15$kHz (FSK/FM) $BER \leq 3 \cdot 10^{-3}$		-111		dBm
input sensitivity – FSK (wide band)	$P_{min, w}$	B_{IF2} = 150kHz $\Delta f = \pm 50$kHz (FSK/FM) $BER \leq 3 \cdot 10^{-3}$		-104		dBm
input sensitivity – ASK (narrow band)	$P_{minA, n}$	B_{IF2} = 40kHz $BER \leq 3 \cdot 10^{-3}$		-109		dBm
input sensitivity – ASK (wide band)	$P_{minA, w}$	B_{IF2} = 150kHz $BER \leq 3 \cdot 10^{-3}$		-106		dBm
maximum input signal – FSK/FM	$P_{max, FM}$	$BER \leq 3 \cdot 10^{-3}$ LNA at LOW GAIN		0		dBm
maximum input signal – ASK	$P_{max, ASK}$	$BER \leq 3 \cdot 10^{-3}$ LNA at LOW GAIN		-10		dBm
spurious emission	P_{spur}				-70	dBm
image rejection	ΔP_{imag}			55		dB
blocking immunity	ΔP_{block}	$\Delta f_{block} > \pm 2$MHz, note 1		57		dB
VCO gain	K_{VCO}			250		MHz/V
Charge pump current	I_{CP}			60		µA

Notes: 1. desired signal with FSK/FM or ASK modulation, CW blocking signal

Test Circuits

FSK Reception

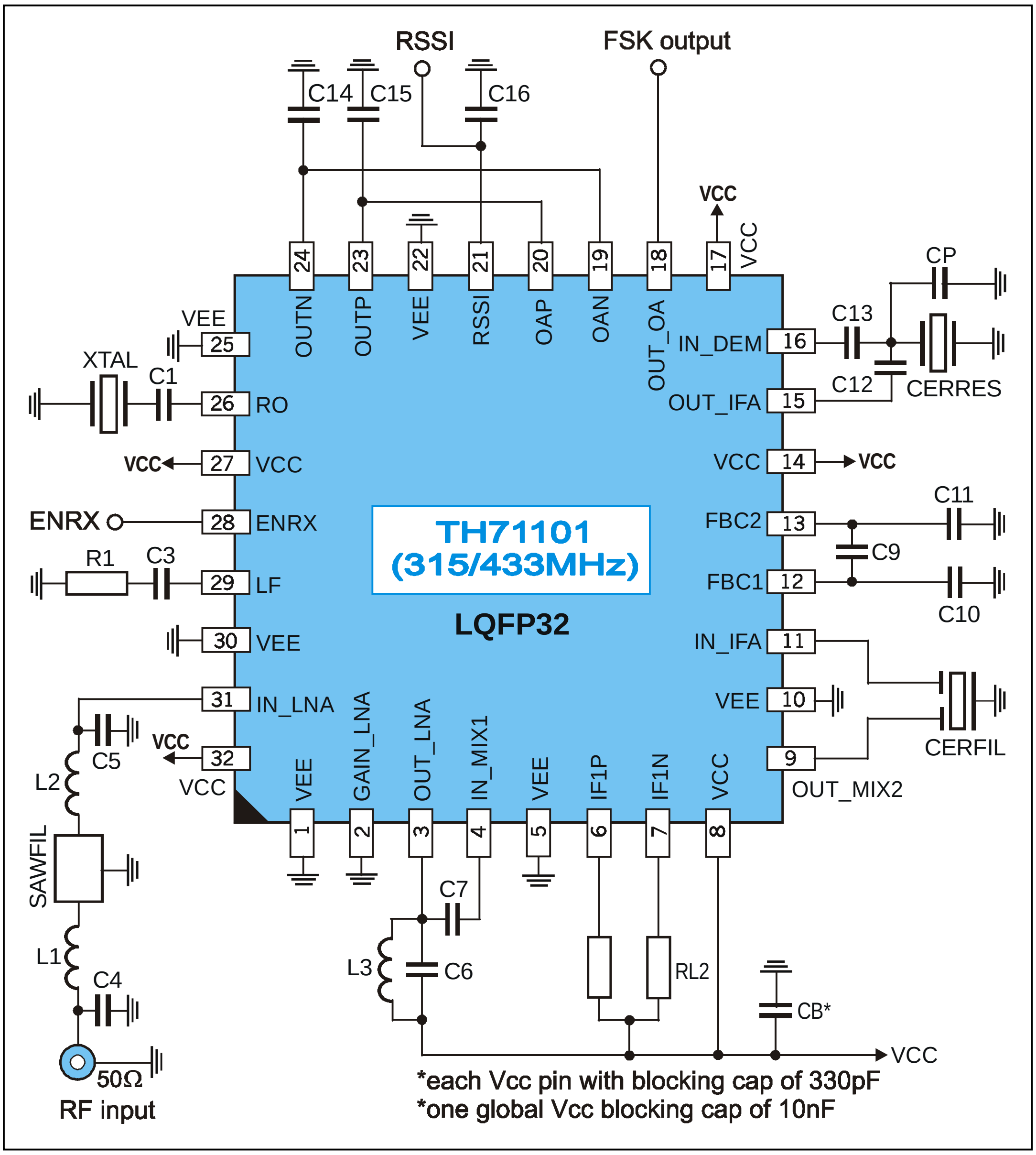


Fig. 2: Test circuit for FSK reception

FSK test circuit component list to Fig. 2

Part	Size	Value / Type	Tolerance	Description
C1	0805	15 pF	±10%	crystal series capacitor
C3	0805	1 nF	±10%	loop filter capacitor
C4	0603	3.3 pF	±5%	capacitor to match to SAW filter input
C5	0603	3.3 pF	±5%	capacitor to match to SAW filter output
C6	0603	4.7 pf	±5%	LNA output tank capacitor
C7	0603	2.2 pf	±5%	MIX1 input matching capacitor
C9	0805	33 nF	±10%	IFA feedback capacitor
C10	0603	1 nF	±10%	IFA feedback capacitor
C11	0603	1 nF	±10%	IFA feedback capacitor
C12	0603	1.5 pF	±5%	DEMOD phase-shift capacitor
C13	0603	680 pF	±10%	DEMOD coupling capacitor
CP	0805	10 – 12 pF	±5%	CERRES parallel capacitor
C14	0805	10 – 47 pF	±5%	demodulator output low-pass capacitor, depending on data rate
C15	0805	10 – 47 pF	±5%	demodulator output low-pass capacitor, depending on data rate
C16	0603	330 pF	±10%	RSSI output low-pass capacitor
R1	0805	10 kΩ	±10%	loop filter resistor
RL1	0805	470 Ω	±5%	MIX1 bias resistor
RL2	0805	470 Ω	±5%	MIX1 bias resistor
L1	0603	33 nH	±5%	inductor to match SAW filter
L2	0603	33 nH	±5%	inductor to match SAW filter
L3	0603	15 nH	±5%	LNA output tank inductor
XTAL	HC49 SMD	**26.43125 MHz @ RF = 433.6 MHz**	±25ppm calibration ±30ppm temp.	fundamental-mode crystal, C_{load} = 10 pF to 15pF, $C_{0,\,max}$ = 7 pF, $R_{m,\,max}$ = 50 Ω
SAWFIL	QCC8C	**B3555 @ RF = 433.6 MHz**	B_{3dB} = 860 kHz ±100 kHz (f_0 = 433.92 MHz)	low-loss SAW filter from EPCOS
CERFIL	Leaded type	SFE10.7MFP @ B_{IF2} = 40 kHz	TBD	ceramic filter from Murata
	SMD type	SFECV10.7MJS-A @ B_{IF2} = 150 kHz	±40 kHz	
CERRES	SMD type	CDACV10.7MG18-A		ceramic demodulator tank from Murata

NIP – not in place, may be used optionally

FSK Circuit with AFC and Ceramic Resonator Tolerance Compensation

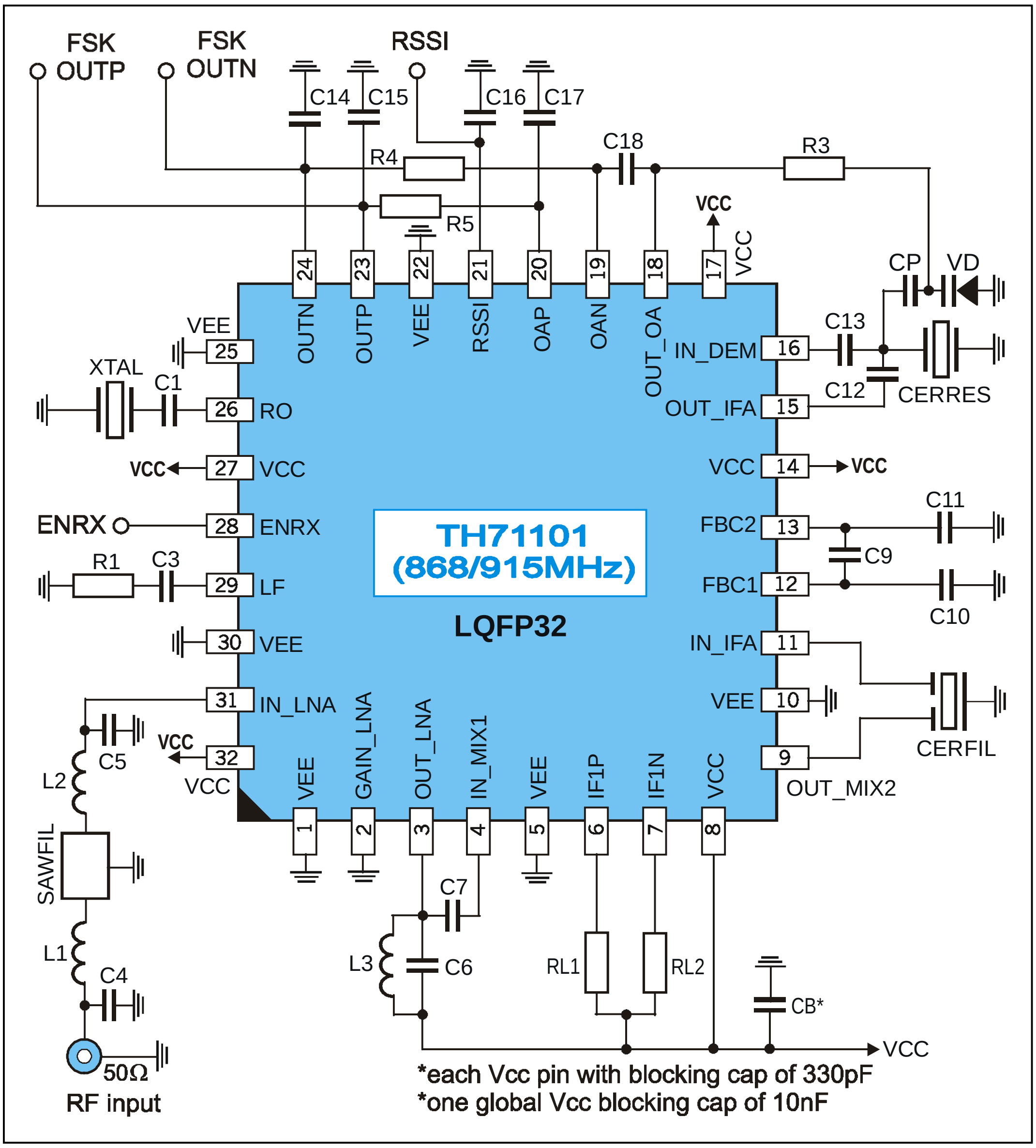


Fig. 3: Test circuit for FSK with AFC and resonator compensation

Circuit Feature

- ❑ Improves input frequency acceptance range up to RF_{nom} ±50 kHz
- ❑ Eliminates calibration tolerances of ceramic resonator
- ❑ Eliminates temperature tolerances of ceramic resonator
- ❑ Non-inverted and inverted CMOS-compatible outputs

FSK test circuit with AFC component list to Fig. 3

Part	Size	Value / Type	Tolerance	Description
C1	0805	15 pF	±10%	crystal series capacitor
C3	0805	1 nF	±10%	loop filter capacitor
C4	0603	3.3 pF	±5%	capacitor to match to SAW filter input
C5	0603	3.3 pF	±5%	capacitor to match to SAW filter output
C6	0603	4.7 pF	±5%	LNA output tank capacitor
C7	0603	2.2 pF	±5%	MIX1 input matching capacitor
C9	0805	33 nF	±10%	IFA feedback capacitor
C10	0603	1 nF	±10%	IFA feedback capacitor
C11	0603	1 nF	±10%	IFA feedback capacitor
C12	0603	1.5 pF	±5%	DEMOD phase-shift capacitor
C13	0603	680 pF	±10%	DEMOD coupling capacitor
CP	0805	27 pF	±5%	ceramic resonator loading capacitor
C14	0805	10 – 47 pF	±5%	demodulator output low-pass capacitor, depending on data rate
C15	0805	10 – 47 pF	±5%	demodulator output low-pass capacitor, depending on data rate
C16	0603	330 pF	±10%	RSSI output low-pass capacitor
C17		33 nF	±10%	integrator capacitor, fixed
C18	0805	33 nF	±10%	integrator capacitor, @ 0.5 to 2 kbit/s NRZ
		10 nF		integrator capacitor, @ 2 to 20 kbit/s NRZ
		1 nF		integrator capacitor, @ 20 to 40 kbit/s NRZ
R1	0805	10 kΩ	±10%	loop filter resistor
R3	0805	100 kΩ	±10%	varactor diode biasing resistor
R4	0805	680 kΩ	±10%	integrator resistor
R5	0805	680 kΩ	±10%	integrator resistor
RL1	0805	470 Ω	±5%	MIX1 bias resistor
RL2	0805	470 Ω	±5%	MIX1 bias resistor
L1	0603	33 nH	±5%	inductor to match SAW filter
L2	0603	33 nH	±5%	inductor to match SAW filter
L3	0603	15 nH	±5%	LNA output tank inductor
VD	SOD-323	BB535		varactor diode from Infineon
XTAL	HC49 SMD	**26.43125 MHz @ RF = 433.6 MHz**	±25ppm calibration ±30ppm temp.	fundamental-mode crystal, C_{load} = 10 pF to 15pF, $C_{0,\,max}$ = 7 pF, $R_{m,\,max}$ = 50 Ω
SAWFIL	QCC8C	**B3555 @ RF = 433.6 MHz**	B_{3dB} = 860 kHz ±100 kHz (f_0 = 433.92 MHz)	low-loss SAW filter from EPCOS
CERFIL	Leaded type	SFE10.7MFP @ B_{IF2} = 40 kHz	TBD	ceramic filter from Murata
	SMD type	SFECV10.7MJS-A @ B_{IF2} = 150 kHz	±40 kHz	
CERRES	SMD type	CDACV10.7MG18-A		ceramic demodulator tank from Murata

NIP – not in place, may be used optionally

FM Reception

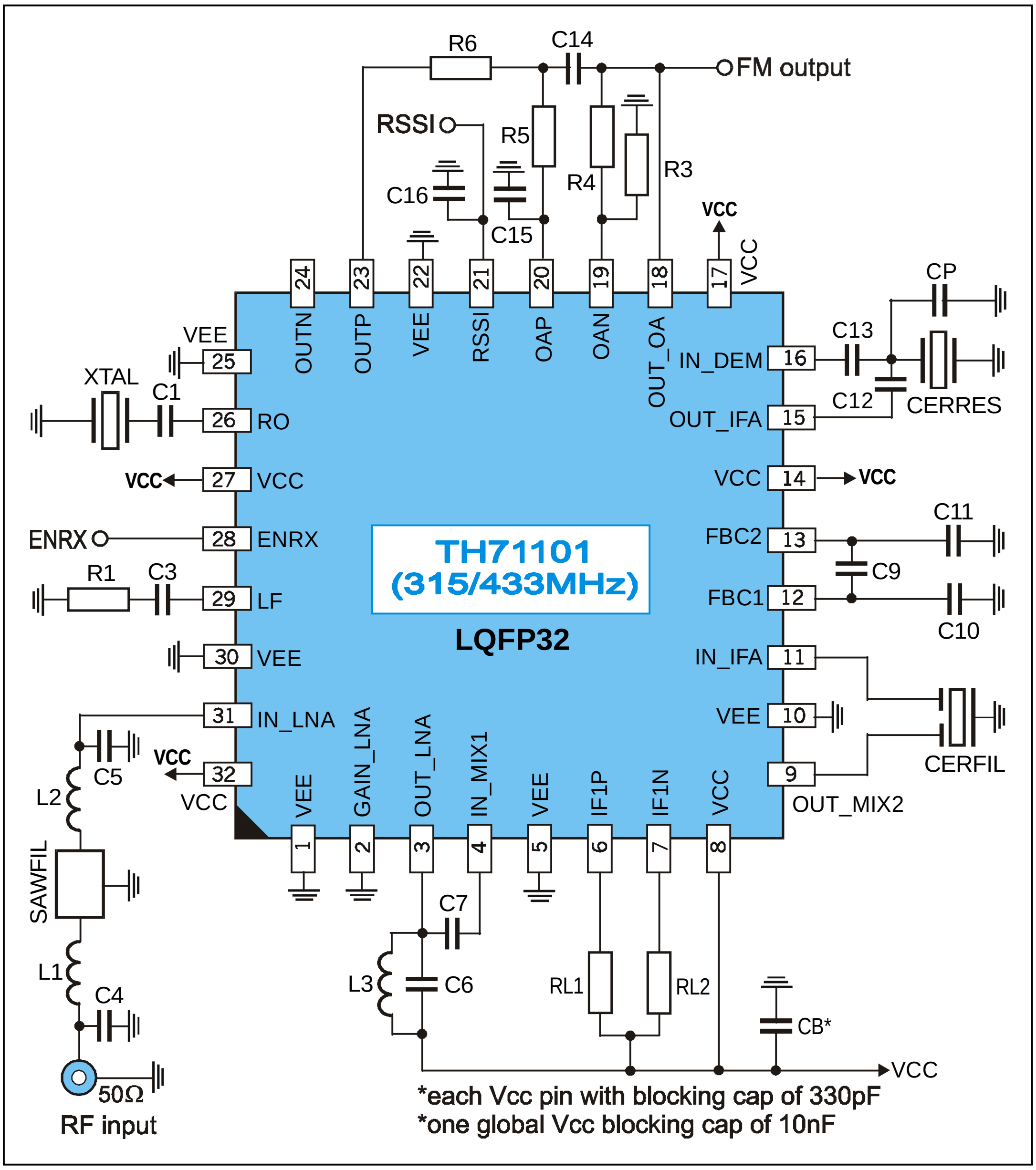


Fig. 4: Test circuit for FM reception

FM test circuit component list to Fig. 4

Part	Size	Value / Type	Tolerance	Description
C1	0805	15 pF	±10%	crystal series capacitor
C3	0805	1 nF	±10%	loop filter capacitor
C4	0603	3.3 pF	±5%	capacitor to match to SAW filter input
C5	0603	3.3 pF	±5%	capacitor to match to SAW filter output
C6	0603	4.7 pF	±5%	LNA output tank capacitor
C7	0603	2.2 pF	±5%	MIX1 input matching capacitor
C9	0805	33 nF	±10%	IFA feedback capacitor
C10	0603	1 nF	±10%	IFA feedback capacitor
C11	0603	1 nF	±10%	IFA feedback capacitor
C12	0603	1.5 pF	±5%	DEMOD phase-shift capacitor
C13	0603	680 pF	±10%	DEMOD coupling capacitor
CP	0805	10 – 12 pF	±5%	CERRES parallel capacitor
C14	0805	100 pF	±5%	sallen-Key low-pass filter capacitor, to set cut-off fre-quency
C15	0805	100 pF	±5%	sallen-Key low-pass filter capacitor, to set cut-off fre-quency
C16	0603	330 pF	±10%	RSSI output low-pass capacitor
R1	0805	10 kΩ	±10%	loop filter resistor
R3	0805	12 kΩ	±5%	sallen-Key filter resistor, to set desired filter characteristic
R4	0805	6.8 kΩ	±5%	sallen-Key filter resistor, to set desired filter characteristic
R5	0805	33 kΩ	±5%	sallen-Key filter resistor, to set cut-off frequency
R6	0805	33 kΩ	±5%	sallen-Key filter resistor, to set cut-off frequency
RL1	0805	470 Ω	±5%	MIX1 bias resistor
RL2	0805	470 Ω	±5%	MIX1 bias resistor
L1	0603	33 nH	±5%	inductor to match SAW filter
L2	0603	33 nH	±5%	inductor to match SAW filter
L3	0603	15 nH	±5%	LNA output tank inductor
XTAL	HC49 SMD	**26.43125 MHz @ RF = 433.6 MHz**	±25ppm calibra-tion ±30ppm temp.	fundamental-mode crystal, C_{load} = 10 pF to 15pF, $C_{0,\ max}$ = 7 pF, $R_{m,\ max}$ = 50 Ω
SAWFIL	QCC8C	**B3555 @ RF = 433.6 MHz**	B_{3dB} = 860 kHz ±100 kHz (f_0 = 433.92 MHz)	low-loss SAW filter from EPCOS
CERFIL	leaded type	SFE10.7MFP @ B_{IF2} = 40 kHz	TBD	ceramic filter from Murata
	SMD type	SFECV10.7MJS-A @ B_{IF2} = 150 kHz	±40 kHz	
CERRES	SMD type	CDACV10.7MG18-A		ceramic demodulator tank from Murata

NIP – not in place, may be used optionally

ASK Reception

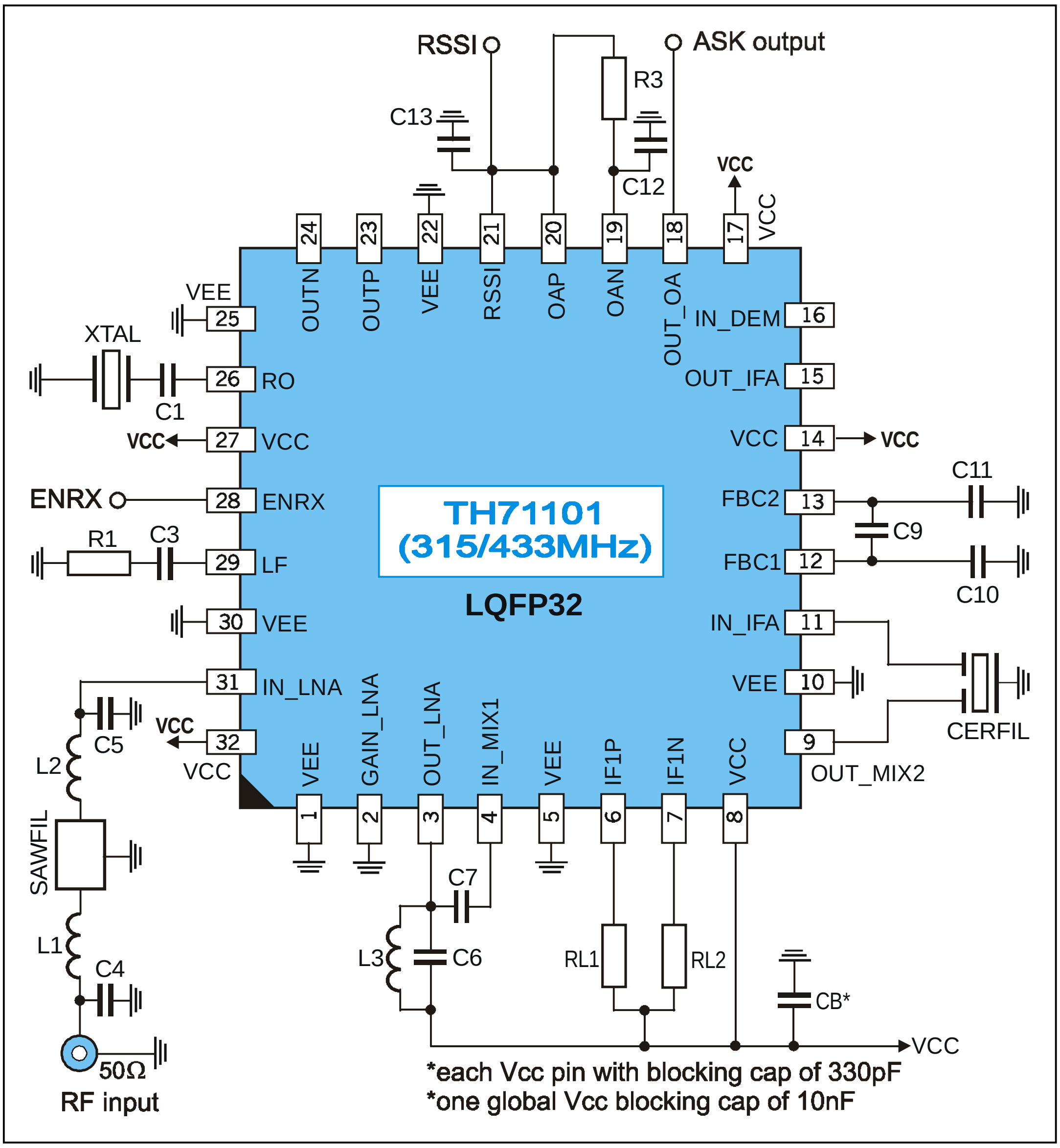


Fig. 5: Test circuit for ASK reception

ASK test circuit component list to Fig. 5

Part	Size	Value / Type	Tolerance	Description
C1	0805	15 pF	±10%	crystal series capacitor
C3	0805	1 nF	±10%	loop filter capacitor
C4	0603	3.3 pF	±5%	capacitor to match to SAW filter input
C5	0603	3.3 pF	±5%	capacitor to match to SAW filter output
C6	0603	4.7 pF	±5%	LNA output tank capacitor
C7	0603	2.2 pF	±5%	MIX1 input matching capacitor
C9	0805	33 nF	±10%	IFA feedback capacitor
C10	0603	1 nF	±10%	IFA feedback capacitor
C11	0603	1 nF	±10%	IFA feedback capacitor
C12	0805	1 nF to 10 nF	±10%	ASK data slicer capacitor, depending on data rate
C13	0603	330 pF	±10%	RSSI output low-pass capacitor
R1	0805	10 kΩ	±10%	loop filter resistor
R3	0603	100 kΩ	±5%	ASK data slicer resistor, depending on data rate
RL1	0805	470 Ω	±5%	MIX1 bias resistor
RL2	0805	470 Ω	±5%	MIX1 bias resistor
L1	0603	33 nH	±5%	inductor to match SAW filter
L2	0603	33 nH	±5%	inductor to match SAW filter
L3	0603	15 nH	±5%	LNA output tank inductor
XTAL	HC49 SMD	**26.43125 MHz @ RF = 433.6 MHz**	±25ppm calibration ±30ppm temp.	fundamental-mode crystal, C_{load} = 10 pF to 15pF, $C_{0,\ max}$ = 7 pF, $R_{m,\ max}$ = 50 Ω
SAWFIL	QCC8C	**B3555 @ RF = 433.6 MHz**	B_{3dB} = 860 kHz ±100 kHz (f_0 = 433.92 MHz)	low-loss SAW filter from EPCOS
CERFIL	leaded type	SFE10.7MFP @ B_{IF2} = 40 kHz	TBD	ceramic filter from Murata
	SMD type	SFECV10.7MJS-A @ B_{IF2} = 150 kHz	±40 kHz	

NIP – not in place, may be used optionally

Package Dimensions

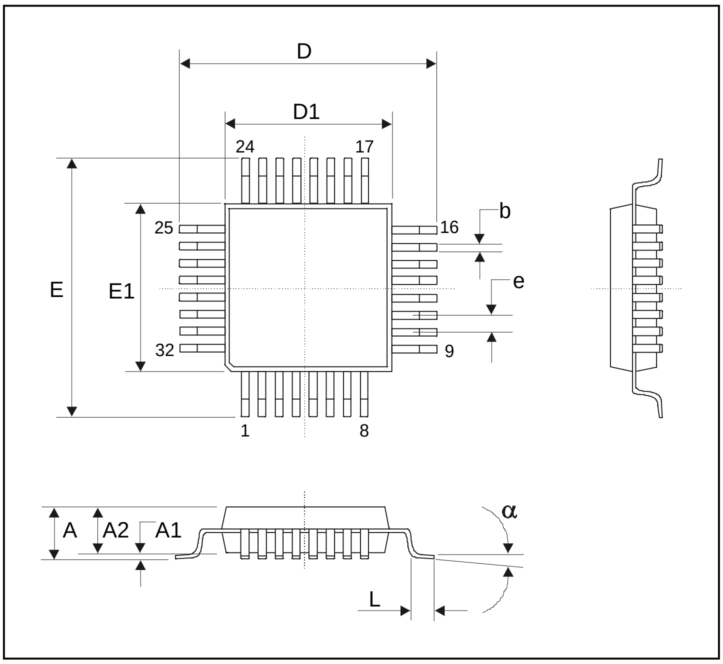


Fig. 6: LQFP32 (Low Quad Flat Package)

All Dimension in mm, coplanarity < 0.1mm									
	E1, D1	**A**	**A1**	**A2**	**e**	**b**	**L**	**E, D**	**α**
min	7.00		0.05	1.35	0.8	0.30	0.45	9.00	0°
max		1.60	0.15	1.45		0.45	0.75		7°
All Dimension in inch, coplanarity < 0.004"									
min	0.276		0.002	0.053	0.031	0.012	0.018	0.354	0°
max		0.630	0.006	0.057		0.018	0.030		7°

Your Notes

Your Notes

Important Notice

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