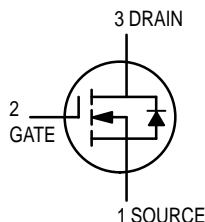


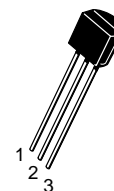
TMOS FET Transistor

N-Channel — Enhancement



VN2222LL

Motorola Preferred Device



CASE 29-04, STYLE 22
TO-92 (TO-226AA)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	60	Vdc
Drain-Gate Voltage ($R_{GS} = 1.0 \text{ M}\Omega$)	V_{DGR}	60	Vdc
Gate-Source Voltage	V_{GS}	± 20	Vdc
— Continuous	V_{GSM}	± 40	Vpk
— Non-repetitive ($t_p \leq 50 \mu\text{s}$)			
Drain Current			mAdc
Continuous	I_D	150	
Pulsed	I_{DM}	1000	
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	400	mW
Derate above 25°C		3.2	mW/ $^\circ\text{C}$
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	312.5	$^\circ\text{C}/\text{W}$
Maximum Lead Temperature for Soldering Purposes, 1/16" from case for 10 seconds	T_L	300	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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OFF CHARACTERISTICS

Drain-Source Breakdown Voltage ($V_{GS} = 0, I_D = 100 \mu\text{Adc}$)	$V_{(BR)DSS}$	60	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 48 \text{ Vdc}, V_{GS} = 0$) ($V_{DS} = 48 \text{ Vdc}, V_{GS} = 0, T_J = 125^\circ\text{C}$)	I_{DSS}	—	10 500	μAdc
Gate-Body Leakage Current, Forward ($V_{GSF} = 30 \text{ Vdc}, V_{DS} = 0$)	I_{GSSF}	—	-100	nAdc

ON CHARACTERISTICS(1)

Gate Threshold Voltage ($V_{DS} = V_{GS}, I_D = 1.0 \text{ mAdc}$)	$V_{GS(th)}$	0.6	2.5	Vdc
Static Drain-Source On-Resistance ($V_{GS} = 10 \text{ Vdc}, I_D = 0.5 \text{ Adc}$) ($V_{GS} = 10 \text{ Vdc}, I_D = 0.5 \text{ Vdc}, T_C = 125^\circ\text{C}$)	$r_{DS(on)}$	—	7.5 13.5	Ω

1. Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

VN2222LL**ELECTRICAL CHARACTERISTICS** ($T_C = 25^\circ\text{C}$ unless otherwise noted) (Continued)

Characteristic	Symbol	Min	Max	Unit
ON CHARACTERISTICS⁽¹⁾ (Continued)				
Drain-Source On-Voltage ($V_{GS} = 5.0\text{ Vdc}$, $I_D = 200\text{ mAdc}$) ($V_{GS} = 10\text{ Vdc}$, $I_D = 500\text{ mAdc}$)	$V_{DS(on)}$	— —	1.5 3.75	Vdc
On-State Drain Current ($V_{GS} = 10\text{ Vdc}$, $V_{DS} \geq 2.0\text{ V}_{DS(on)}$)	$I_{D(on)}$	750	—	mA
Forward Transconductance ($V_{DS} = 10\text{ Vdc}$, $I_D = 500\text{ mAdc}$)	g_{fs}	100	—	μmhos

DYNAMIC CHARACTERISTICS

Input Capacitance	$(V_{DS} = 25\text{ Vdc}, V_{GS} = 0,$ $f = 1.0\text{ MHz})$	C_{iss}	—	60	pF
Output Capacitance		C_{oss}	—	25	
Reverse Transfer Capacitance		C_{rss}	—	5.0	

SWITCHING CHARACTERISTICS⁽¹⁾

Turn-On Delay Time	$(V_{DD} = 15\text{ Vdc}, I_D = 600\text{ mA},$ $R_{gen} = 25\ \Omega, R_L = 23\ \Omega)$	t_{on}	—	10	ns
Turn-Off Delay Time		t_{off}	—	10	

1. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

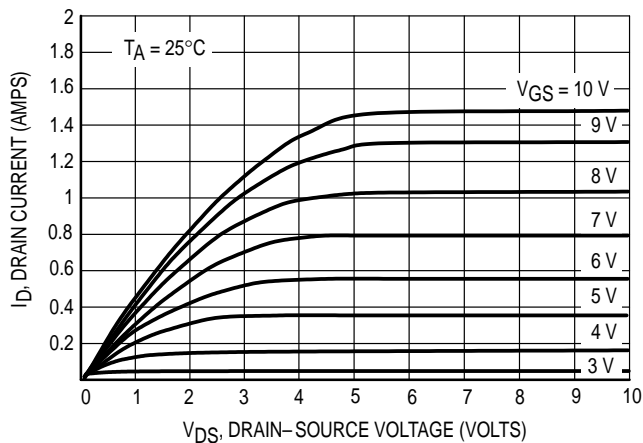


Figure 1. Ohmic Region

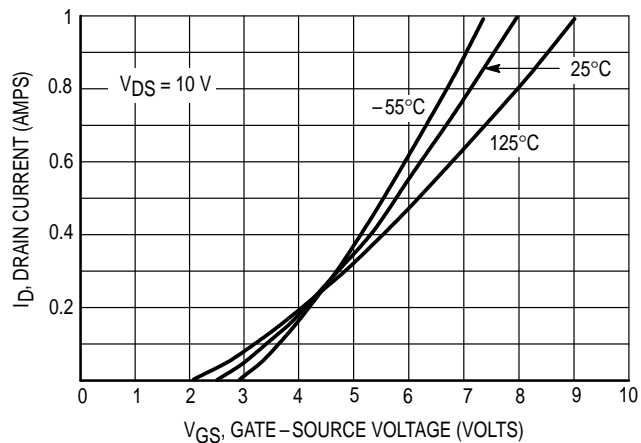


Figure 2. Transfer Characteristics

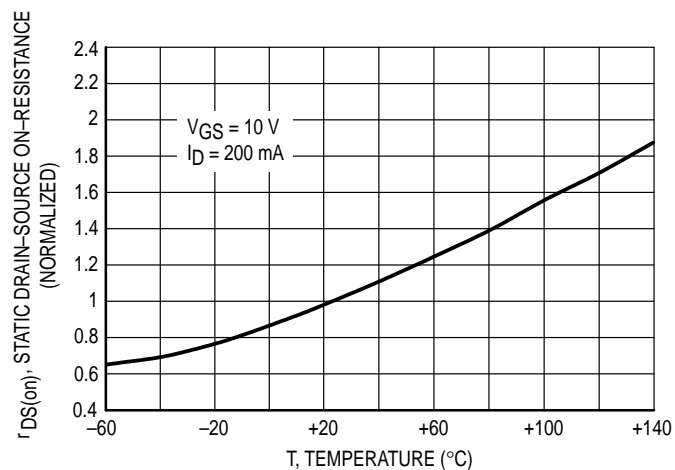


Figure 3. Temperature versus Static Drain-Source On-Resistance

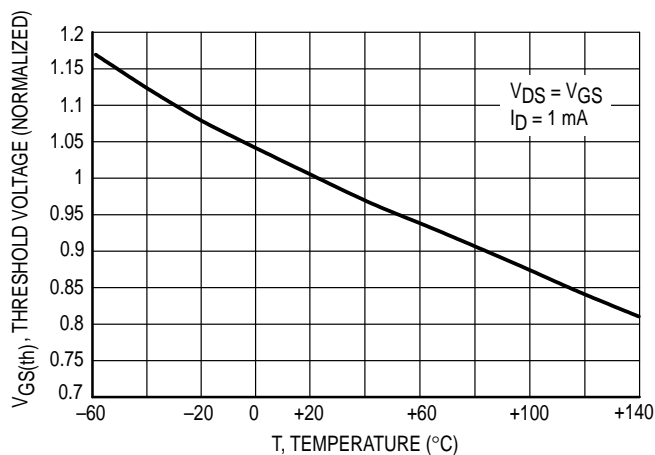
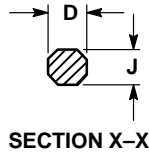
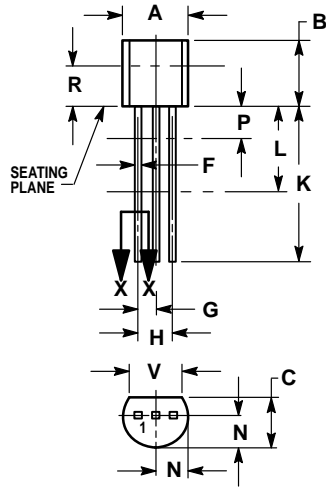


Figure 4. Temperature versus Gate Threshold Voltage

PACKAGE DIMENSIONS



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. DIMENSION F APPLIES BETWEEN P AND L. DIMENSION D AND J APPLY BETWEEN L AND K. MINIMUM. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.022	0.41	0.55
F	0.016	0.019	0.41	0.48
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	—	12.70	—
L	0.250	—	6.35	—
N	0.080	0.105	2.04	2.66
P	—	0.100	—	2.54
R	0.115	—	2.93	—
V	0.135	—	3.43	—

**CASE 029-04
(TO-226AA)
ISSUE AD**

STYLE 22:
PIN 1. SOURCE
2. GATE
3. DRAIN

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