

PRELIMINARY

**10-CHARACTER 3-LINE DOT MATRIX LCD
CONTROLLER DRIVER**

■ GENERAL DESCRIPTION

The NJU6424 is a Dot Matrix LCD controller driver for 10-character 3-line with icon display in single chip.

It contains voltage tripler, bleeder resistance, bias control circuit, CR oscillator, microprocessor interface circuits, instruction decoder controller, character generator ROM/RAM, high voltage operation common and segment drivers.

The voltage tripler and bleeder resistance generates about triple voltage(8V) and bias voltage for LCD driving waveform internally from single power supply (3V). Consequently, high-contrast display can be performed though the simple power supply circuits.

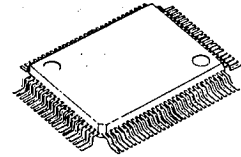
The bias control circuit can change the output current of Voltage follower, therefore COM/SEG driveability can be increased.

The CR oscillator incorporates C and R, therefore no external components for oscillation are required.

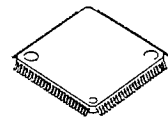
The microprocessor interface circuits which operate by 1MHz, can be connected directly to 4/8bit microprocessor.

The character generator consists of 9,600 bits ROM and 64 bytes RAM.

The 26-common (24 for character, 2 for icon) and 50-segment drivers are operated up to 13.5V, and the icon common driver display up to 100 icons.

■ PACKAGE OUTLINE

NJU6424FC1

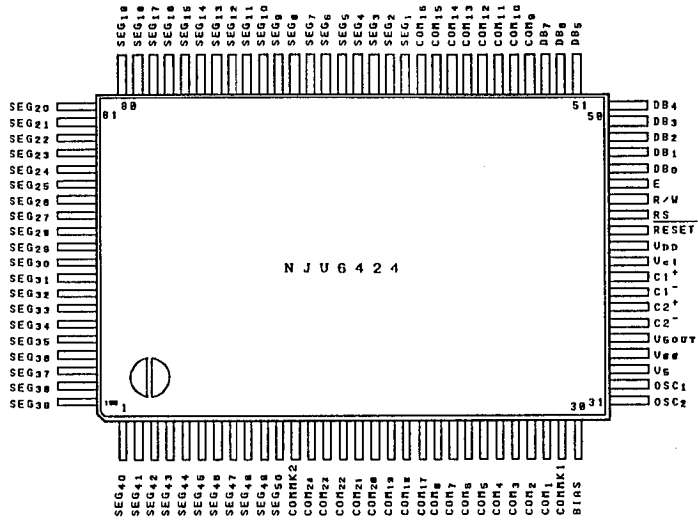


NJU6424FG1

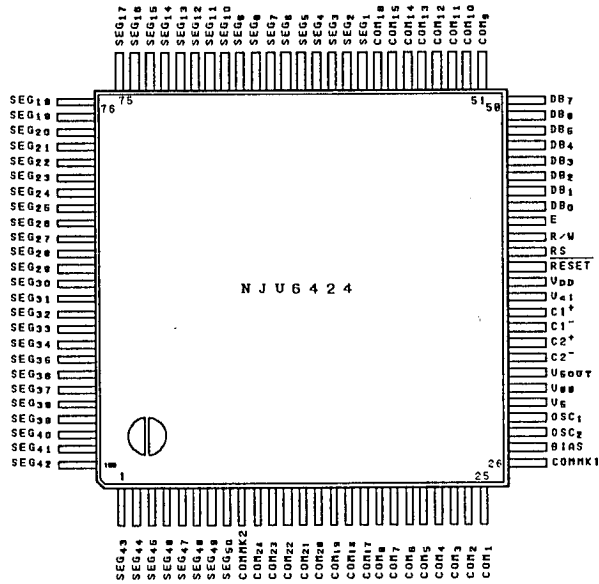
5**■ FEATURES**

- 10-character 3-line Dot Matrix LCD Controller Driver
- Maximum 100 icon Display (COMM1,COMM2)
- 4/8 Bit Microprocessor Direct Interface
- Display Data RAM - 30 x 8 bits : Maximum 10-character 3-line Display
- Character Generator ROM - 9,600 bits : 240 Characters for 5 x 7 Dots
- Character Generator RAM - 32 x 5 bits : 4 Patterns(5 x 7 Dots)
- High Voltage LCD Driver : 26-common / 50-segment
- Useful Instruction Set : Clear Display, Return Home, Display ON/OFF Cont, Cursor ON/OFF Cont, Display Blink, Cursor Shift, Character Shift
- Power On Initialize / Hardware Reset Function
- Voltage Tripler On-chip
- Bleeder Resistance with voltage follower On-chip
- Bias control circuit of voltage follower On-chip
- Oscillation Circuit On-chip
- Low Power Consumption -- (150 μ A TYP.)
- Operating Voltage --- 2.4 to 3.6 V (Except LCD Driving Voltage)
- Package Outline --- Chip / QFP 100 / TQFP 100 / TCP
- C-MOS Technology

■ PIN CONFIGURATION (NJU6424FC1)

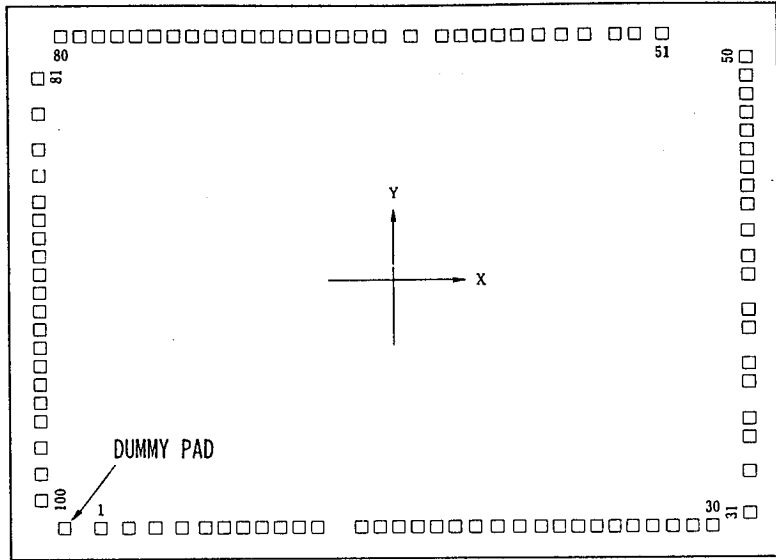


■ PIN CONFIGURATION (NJU6424FG1)



Note) Pin configuration of "FG1" package is different from "FC1" package.

■ PAD LOCATION



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CHIP SIZE : 5.78mm x 4.18mm
CHIP CENTER : X=0 μ m, Y=0 μ m
PAD SIZE : 92 μ m x 92 μ m

■ PAD COORDINATES

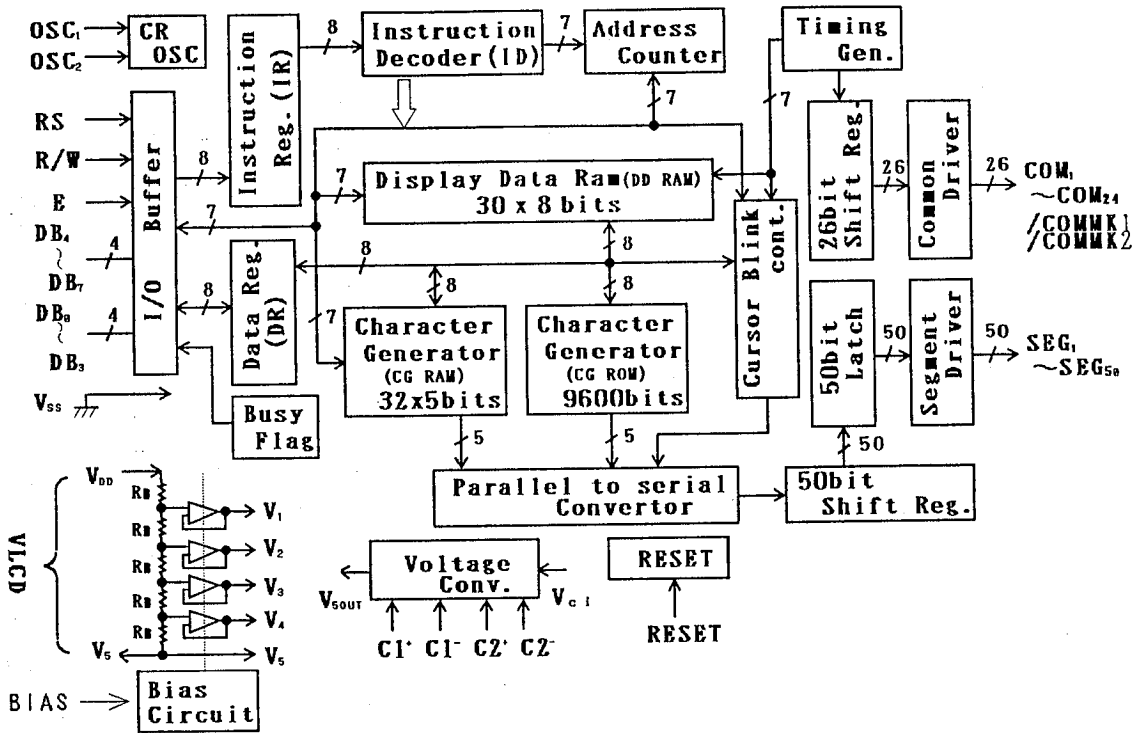
 CHIP SIZE 5.78mm x 4.18mm (CHIP CENTER X=0 μ m, Y=0 μ m)

PAD No	PAD NAME	X=(μ m)	Y=(μ m)
1	SEG ₄₀	-2220	-1895
2	SEG ₄₁	-2000	-1895
3	SEG ₄₂	-1800	-1895
4	SEG ₄₃	-1600	-1895
5	SEG ₄₄	-1420	-1895
6	SEG ₄₅	-1280	-1895
7	SEG ₄₆	-1140	-1895
8	SEG ₄₇	-1000	-1895
9	SEG ₄₈	-860	-1895
10	SEG ₄₉	-720	-1895
11	SEG ₅₀	-580	-1895
12	COMMK2	-254	-1895
13	COM ₂₄	-114	-1895
14	COM ₂₃	26	-1895
15	COM ₂₂	166	-1895
16	COM ₂₁	306	-1895
17	COM ₂₀	446	-1895
18	COM ₁₉	606	-1895
19	COM ₁₈	766	-1895
20	COM ₁₇	926	-1895
21	COM ₈	1086	-1895
22	COM ₇	1226	-1895
23	COM ₆	1366	-1895
24	COM ₅	1506	-1895
25	COM ₄	1646	-1895
26	COM ₃	1786	-1895
27	COM ₂	1946	-1895
28	COM ₁	2106	-1895
29	COMMK1	2266	-1895
30	BIAS	2426	-1895
31	OSC ₂	2688	-1794
32	OSC ₁	2688	-1485
33	V _S	2688	-1220
34	V _{SS}	2688	-1080
35	V _{5OUT}	2688	-801
36	C2 ⁻	2688	-661
37	C2 ⁺	2688	-382
38	C1 ⁻	2688	-242
39	C1 ⁺	2688	38
40	V _{C1}	2688	178
41	V _{DD}	2688	378
42	RESET	2688	578
43	RS	2688	718
44	R/W	2688	858
45	E	2688	998
46	DB ₀	2688	1138
47	DB ₁	2688	1278
48	DB ₂	2688	1418
49	DB ₃	2688	1558
50	DB ₄	2688	1698

PAD No	PAD NAME	X=(μ m)	Y=(μ m)
51	DB ₅	2174	1896
52	DB ₆	1954	1896
53	DB ₇	1784	1896
54	COM ₉	1547	1896
55	COM ₁₀	1367	1896
56	COM ₁₁	1187	1896
57	COM ₁₂	1027	1896
58	COM ₁₃	887	1896
59	COM ₁₄	747	1896
60	COM ₁₅	607	1896
61	COM ₁₆	467	1896
62	SEG ₁	228	1896
63	SEG ₂	-4	1896
64	SEG ₃	-164	1896
65	SEG ₄	-304	1896
66	SEG ₅	-444	1896
67	SEG ₆	-584	1896
68	SEG ₇	-724	1896
69	SEG ₈	-864	1896
70	SEG ₉	-1004	1896
71	SEG ₁₀	-1144	1896
72	SEG ₁₁	-1284	1896
73	SEG ₁₂	-1424	1896
74	SEG ₁₃	-1564	1896
75	SEG ₁₄	-1704	1896
76	SEG ₁₅	-1864	1896
77	SEG ₁₆	-2024	1896
78	SEG ₁₇	-2184	1896
79	SEG ₁₈	-2344	1896
80	SEG ₁₉	-2504	1896
81	SEG ₂₀	-2688	1561
82	SEG ₂₁	-2688	1281
83	SEG ₂₂	-2688	1031
84	SEG ₂₃	-2688	831
85	SEG ₂₄	-2688	631
86	SEG ₂₅	-2688	491
87	SEG ₂₆	-2688	351
88	SEG ₂₇	-2688	211
89	SEG ₂₈	-2688	71
90	SEG ₂₉	-2688	-69
91	SEG ₃₀	-2688	-209
92	SEG ₃₁	-2688	-349
93	SEG ₃₂	-2688	-489
94	SEG ₃₃	-2688	-629
95	SEG ₃₄	-2688	-769
96	SEG ₃₅	-2688	-909
97	SEG ₃₆	-2688	-1049
98	SEG ₃₇	-2688	-1249
99	SEG ₃₈	-2688	-1449
100	SEG ₃₉	-2688	-1649

* The left side PAD of No1 PAD is Dummy PAD (Coordinates X=-2500, Y=-1895), No need Bonding.

■ BLOCK DIAGRAM



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■ TERMINAL DESCRIPTION

PIN NO.		SYMBOL	FUNCTION
FC1 Package	FG1 Package		
41	38	V_{DD}	Power Source (+ 3V)
34	31	V_{SS}	Power Source (0V)
33	30	V_5	LCD Driving Voltage Output
32 31	29 28	OSC_1 OSC_2	Oscillation Frequency Adjust Terminals. Normally Open. (Oscillation C and R are incorporated, Osc Freq.=80kHz) For external clock operation, the clock should be input on OSC_1 .
43	40	RS	Register selection signal input(Pull-up resistance On-chip) "0" : Instruction Register (Writing) Busy Flag, Address Counter (Reading) "1" : Data Register (Writing/Reading)
44	41	R/W	Read/Write selection signal input(Pull-up Resistance On-chip) "0" : Write , "1" : Read
45	42	E	Read/Write activation signal input
50~53	47~50	$DB_4 \sim DB_7$	3-state Data Bus(Upper) to transfer the data between MPU and NJU6424. DB_7 is also used for the Busy Flag reading.
46~49	43~46	$DB_0 \sim DB_3$	3-state Data Bus(Lower) to transfer the data between MPU and NJU6424. These bus are not used in the 4-bit operation.
28~13 54~61	25~10 51~58	COM_1 $\sim COM_{24}$	LCD Common Driving Signal
29 12	26 9	COMMK1 COMMK2	Icon Common Driving Signal
62~100 1~11	59~100 1~8	$SEG_1 \sim$ SEG_{50}	LCD Segment Driving Signal
39,37 38,36	36, 34 35, 33	$C1^+, C2^+$ $C1^-, C2^-$	Step up capacitor connecting terminals Connect the step up capacitors between $C1^+$ and $C1^-$, $C2^+$ and $C2^-$ respectively.
40	37	V_{c1}	Input Terminal for Voltage Tripler (Normally $V_{c1} = V_{DD}$)
35	32	V_{5OUT}	Voltage Tripler Output Terminal
30	27	BIAS	COM/SEG output current adjust terminal To increase output current of the voltage follower, connect a resistance(R_{BIAS}) between this terminal and V_{SS} . Normally Open.
42	39	RESET	Reset Terminal. When the "L" level input over than 1.2ms to this terminal, the system will be reset($f_{OSC}=80kHz$)

FUNCTIONAL DESCRIPTION
(1) Description for each blocks
(1-1) Register

The NJU6424 incorporates two 8-bit registers, an Instruction Register (IR) and a Data Register (DR). The Register (IR) stores instruction codes such as "Clear Display", "Return Home", and address data for Display Data RAM (DD RAM) and Character Generator RAM (CG RAM).

The MPU can write the instruction code and address data to the Register (IR), but it cannot read out from the Register (IR).

The Register (DR) is a temporary stored register, the data stored in the Register (DR) is written into the DD RAM or CG RAM and read out from the DD RAM or CG RAM.

The data in the Register (DR) written by the MPU is transferred automatically to the DD RAM or CG RAM by internal operation.

When the address data for the DD RAM or CG RAM is written into the Register (IR), the addressed data in the DD RAM or CG RAM is transferred to the Register (DR). By the MPU read out the data in the Register (DR), the data transmitting process is performed completely.

After reading the data in the Register (DR) by the MPU, the next address data in the DD RAM or CG RAM is transferred automatically to the Register (DR) to provide for the next MPU reading.

These two registers are selected by the selection signal RS as shown below.

Table 1. shows register operation controlled by RS and R/W signals.

Table 1. Register Operation

RS	R/W	Selected Register	Operation
0	0	IR	Write
0	1		Read busy flag (DB ₇) and address counter (DB ₀ ~DB ₆)
1	0	DR	Write (DR to DD RAM or CG RAM)
1	1		Read (DD or CG RAM to DR)

(1-2) Busy Flag (BF)

When the internal circuits are in the operation mode, the busy flag (BF) is "1", and any instruction reading is inhibited.

The busy flag (BF) is output at DB₇ when RS="0" and R/W="1" as shown in Table 1.

The next instruction should be written after the busy flag (BF) goes to "0".

(1-3) Address Counter (AC)

The address counter (AC) addressing the DD RAM and CG RAM.

When the address setting instruction is written into the Register (IR), the address information is transferred from Register (IR) to the Counter (AC). The selection of either the DD RAM or CG RAM is also determined by this instruction.

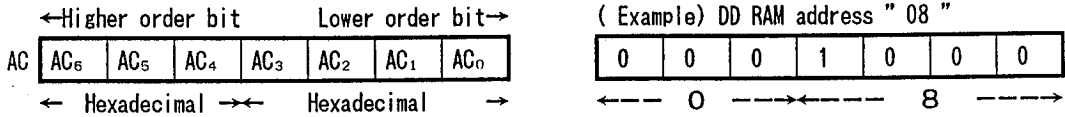
After writing (or reading) the display data to (or from) the DD RAM or CG RAM, the Counter (AC) increments (or decrements) automatically.

The address data in the Counter (AC) is output from DB₆~DB₀ when RS="0" and R/W="1" as shown in Table 1.

(1-4) Display Data RAM (DD RAM)

The display data RAM (DD RAM) consists of 30 x 8 bits stores up to 30-character display data represented in 8-bit code.

The DD RAM address data set in the address counter(AC) is represented in Hexadecimal.



The relation between DD RAM address and display position on the LCD is shown below.

	1	2	3	4	5	6	7	8	9	10	← Display Position
1st Line (COM ₁ to COM ₈)	00	01	02	03	04	05	06	07	08	09	
2nd Line (COM ₉ to COM ₁₆)	0C	0D	0E	0F	10	11	12	13	14	15	← DD RAM Address (Hexadecimal)
3rd Line (COM ₁₇ to COM ₂₄)	40	41	42	43	44	45	46	47	48	49	
	SEG ₁ ~ SEG ₅₀										

Note : The 1st, 2nd and 3rd line address are defined as (00)_H to (09)_H, (0C)_H to (15)_H and (40)_H to (49)_H. Please note that the end of 1st line address and the beginning of 2nd line address are not consecutive.

When the display shift is performed, the DD RAM address changes as follows:

(Left Shift Display)

	1	2	3	4	5	6	7	8	9	10
(00)←	01	02	03	04	05	06	07	08	09	00
(0C)←	0D	0E	0F	10	11	12	13	14	15	0C
(40)←	41	42	43	44	45	46	47	48	49	40

(Right Shift Display)

	1	2	3	4	5	6	7	8	9	10	
	09	00	01	02	03	04	05	06	07	08	→(09)
	15	0C	0D	0E	0F	10	11	12	13	14	→(15)
	49	40	41	42	43	44	45	46	47	48	→(49)

(1-5) Character Generator ROM (CG ROM)

The Character Generator ROM (CG ROM) generates 5 x 7 dots character pattern represented in 8-bit character codes.

The storage capacity is up to 240 kinds of 5 x 7 dots character pattern.

The correspondence between character code and standard character pattern of NJU6424 is shown in Table 2-1.

User-defined character patterns (Custom Font) are also available by mask option.

Table 2-1. CG ROM Character Pattern (ROM version -02)

		Upper 4-bit (Hexadecimal)															
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Lower 4-bit (Hexadecimal)	0	CG RAM (01)	Ⓐ		⓪	ⓐ	ⓑ	Ⓒ	Ⓓ	Ⓔ		—	㊦	㊧	㊨	㊩	Ⓟ
	1	(02)	Ⓑ	!	1	Ⓐ	ⓐ	ⓑ	Ⓒ	Ⓓ	Ⓔ	Ⓝ	㊦	㊧	㊨	㊩	Ⓠ
	2	(03)	Ⓒ	"	2	Ⓑ	ⓑ	Ⓒ	Ⓓ	Ⓔ	Ⓝ	㊦	㊧	㊨	㊩	Ⓡ	Ⓡ
	3	(04)	Ⓓ	#	3	Ⓒ	ⓑ	Ⓒ	Ⓓ	Ⓔ	Ⓝ	㊦	㊧	㊨	㊩	Ⓢ	Ⓢ
	4	(01)	Ⓔ	\$	4	Ⓓ	Ⓒ	Ⓓ	Ⓔ	Ⓝ	㊦	㊦	㊦	㊦	㊦	Ⓣ	Ⓣ
	5	(02)	Ⓝ	%	5	Ⓔ	Ⓒ	Ⓓ	Ⓔ	Ⓝ	㊦	㊦	㊦	㊦	㊦	Ⓤ	Ⓤ
	6	(03)	Ⓝ	&	6	Ⓔ	Ⓒ	Ⓓ	Ⓔ	Ⓝ	㊦	㊦	㊦	㊦	㊦	Ⓥ	Ⓥ
	7	(04)	Ⓝ	'	7	Ⓔ	Ⓒ	Ⓓ	Ⓔ	Ⓝ	㊦	㊦	㊦	㊦	㊦	Ⓦ	Ⓦ
	8	(01)	Ⓝ	(8	Ⓔ	Ⓒ	Ⓓ	Ⓔ	Ⓝ	㊦	㊦	㊦	㊦	㊦	Ⓧ	Ⓧ
	9	(02)	Ⓝ)	9	Ⓔ	Ⓒ	Ⓓ	Ⓔ	Ⓝ	㊦	㊦	㊦	㊦	㊦	Ⓨ	Ⓨ
	A	(03)	Ⓝ	*		Ⓔ	Ⓒ	Ⓓ	Ⓔ	Ⓝ	㊦	㊦	㊦	㊦	㊦	Ⓩ	Ⓩ
	B	(04)	Ⓝ	+		Ⓔ	Ⓒ	Ⓓ	Ⓔ	Ⓝ	㊦	㊦	㊦	㊦	㊦	ⓐ	ⓐ
	C	(01)	Ⓝ	,	<	Ⓔ	Ⓒ	Ⓓ	Ⓔ	Ⓝ	㊦	㊦	㊦	㊦	㊦	ⓑ	ⓑ
	D	(02)	Ⓝ	-	=	Ⓔ	Ⓒ	Ⓓ	Ⓔ	Ⓝ	㊦	㊦	㊦	㊦	㊦	ⓓ	ⓓ
	E	(03)	Ⓝ	.	>	Ⓔ	Ⓒ	Ⓓ	Ⓔ	Ⓝ	㊦	㊦	㊦	㊦	㊦	ⓔ	ⓔ
	F	(04)	Ⓝ	/	?	Ⓔ	Ⓒ	Ⓓ	Ⓔ	Ⓝ	㊦	㊦	㊦	㊦	㊦	ⓕ	ⓕ

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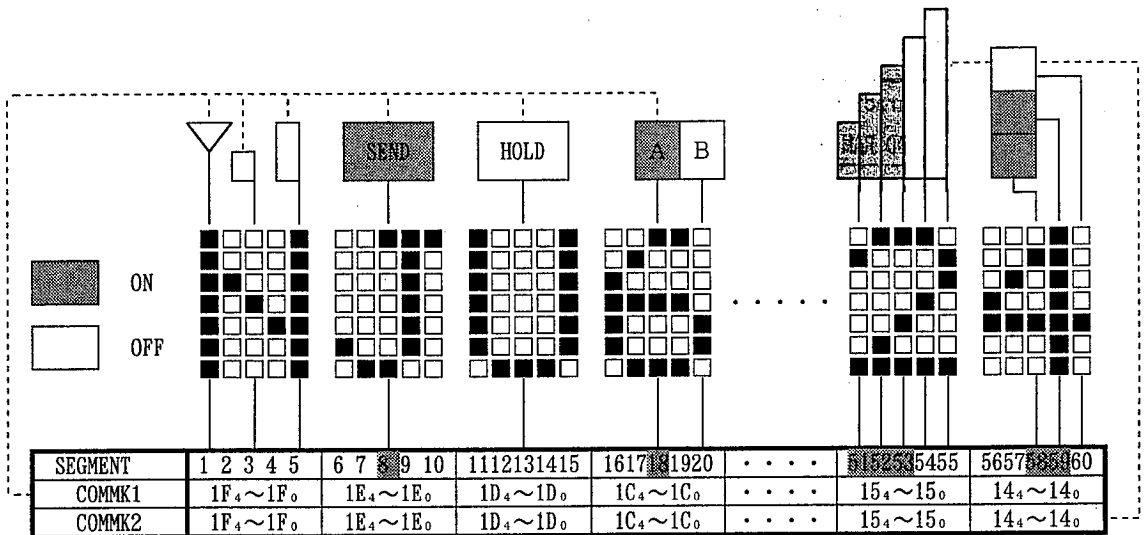
(1-7) Icon Display Function

The NJU6424 can display not only 5 x 7 bits character pattern but also maximum 100 icons.

The icon can display by writing bit "1" to each data bit 0 to 4 in the address (0C)_H to (1F)_H of CG RAM.

The fixed character display code is not affected except CG RAM writing and display ON/OFF instruction.

The relation between CG RAM address and icon display position on the LCD is fixed even if the display shift is executed. The relation is shown below:



NOTE) The 1F₄ corresponds bit 4 of (1F)_H in CG RAM.

< CG RAM vs. SEG terminal for icon display >

	CG RAM		SEG
	address	data	terminal
COMM2	0C	00110	46~50
	0D	11100	41~45
	0E	36~40
	0F	31~35
	10	26~30
	11	21~25
	12	16~20
	13	11~15
COMM1	14	6~10
	15	1~5
	16	46~50
	17	41~45
	18	36~40
	19	31~35
	1A	26~30
	1B	21~25
1C	00100	16~20	
1D	00000	11~15	
1E	00100	6~10	
1F	00000	1~5	

Maximum Character Number and Icon Display Number in CG RAM

Icon Disp. Number	Max. Chara. Number	Note
No Use	4 Chara.	
Up to 40	3 Chara.	(03) _H , (07) _H , (0B) _H and (0F) _H can not use for Character Memory.
Up to 80	2 Chara.	(02) _H , (03) _H , (06) _H , (07) _H , (0A) _H , (0B) _H , (0E) _H and (0F) _H can not use for Character Memory.
Up to 100	1 Chara.	(01) _H , (02) _H , (03) _H , (05) _H , (06) _H , (07) _H , (09) _H , (0A) _H , (0B) _H , (0D) _H , (0E) _H , (0F) _H can not use...

NOTE) When the icon display function using, the system should be initialized by the software initialization because of the CG RAM does not initialize except the software initialization.

(1-8) Timing Generator

The timing generator generates a timing signals for the DD RAM, CG RAM, CG ROM and other internal circuits operation.

RAM read timing for the display and internal operation timing for MPU access are separately generated, so that they may not interfere with each other.

Therefore, when the data write to the DD RAM for example, there will be no undesirable influence, such as flickering, in areas other than the display area.

(1-9) LCD Driver

LCD driver consist of 26-common driver and 50-segment driver.

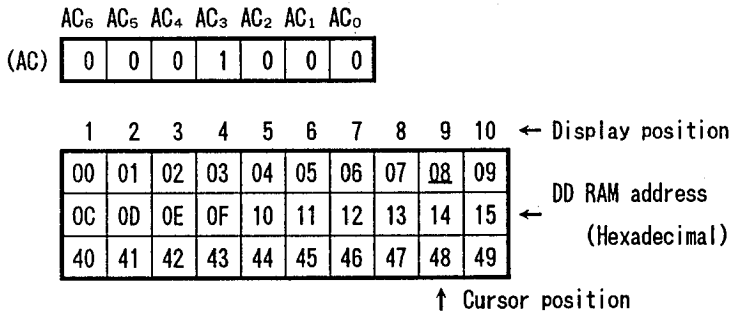
The 50 bits of character pattern data are shifted in the shift-register and latched when the 50 bits shift performed completely. This latched data controls display driver to output LCD driving waveform.

(1-10) Cursor Blinking Control Circuit

This circuits controls cursor On/Off and the cursor position character blinks.

The cursor or blinks appear in the digit residing at the DD RAM address set in the address counter (AC).

When the address counter is (08)_H, a cursor position is shown as follows:



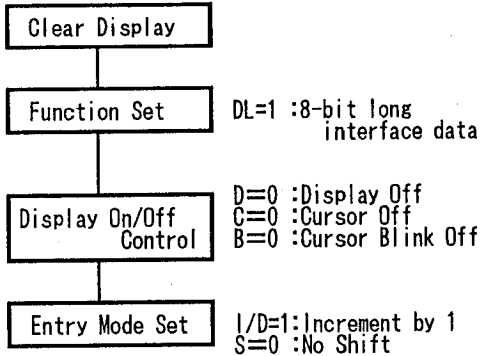
(Note) The cursor or blinks also appear when the address counter (AC) selects the CG RAM. But the displayed cursor and blink are meaningless. If the AC storing the CG RAM address data, the cursor and blink are displayed in the meaningless position.

(2) Power on Initialization by internal circuits

(2-1) Initialization By Internal Reset Circuit

The NJU6424 is automatically initialized by internal power on initialization circuits when the power is turned on. In the internal power on initialization, following instructions are executed. During the internal power on initialization, the busy flag (BF) is "1" and this status is kept 10 ms after V_{DD} rises to 2.4V.

Initialization flow is shown below:

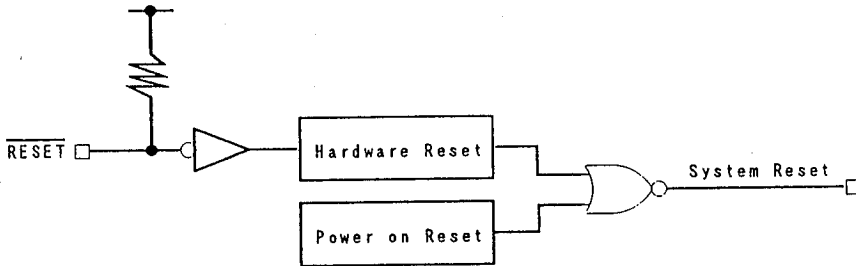


NOTE
If the condition of power supply rise time described in the Electrical Characteristics is not satisfied, the internal Power On Initialization Circuits will not operate and initialization will not be performed. In this case the initialization by MPU software is required.

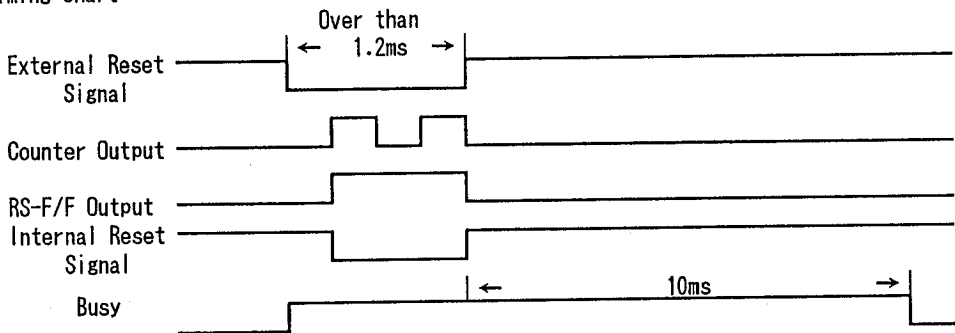
(2-2) Initialization By Hardware

The NJU6424 incorporates $\overline{\text{RESET}}$ terminal to initialize the all system. When the "L" level input over than 1.2ms to the $\overline{\text{RESET}}$ terminal, reset sequence is executed. In this time, busy signal output during 10ms after $\overline{\text{RESET}}$ terminal goes to "H".

• Reset Circuit



• Timing Chart



(3) Instructions

The NJU6424 incorporates two registers, an Instruction Register (IR) and a Data Register (DR). These two registers store control information temporarily to allow interface between NJU6424 and MPU or peripheral IC's operating different cycles. The operation of NJU6424 is determined by this control signal from MPU. The control information includes register selection signals (RS), read/write signals (R/W) and data bus signals (DB_0 to DB_7). Table 4. shows each instruction and its operating time.

Note 1) The execution time mentioned in Table 4. based on f_{cp} or $f_{osc}=80\text{kHz}$.
If the oscillation frequency is changed, the execution time is also changed.

Table 4. Table of Instructions

INSTRUCTIONS	RS	R/W	C DB ₇	O DB ₆	D DB ₅	E DB ₄	DB ₃	DB ₂	DB ₁	DB ₀	DESCRIPTION	EXEC TIME
Maker Testing	0	0	0	0	0	0	0	0	0	0	All "0" code is using for maker testing.	
Clear Display	0	0	0	0	0	0	0	0	0	1	Display clear and sets DD RAM address 0 in AC.	2.0ms
Return Home	0	0	0	0	0	0	0	0	1	*	Sets DD RAM address 0 in AC and returns display being shifted to original position. DD RAM contents remain unchanged	125us
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies shift of display are performed in data read/write. I/D=1:Increment, I/D=0:Decrement S=1:Accompanies display shift	125us
Display On/Off Control	0	0	0	0	0	0	1	D	C	B	Sets of display On/Off(D), cursor On/Off(C) and blink of cursor position character(B).	125us
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves cursor and shifts display without changing DD RAM contents S/C=1 : Display shift S/C=0 : Cursor shift R/L=1 : Shift to the right R/L=0 : Shift to the left	188us
Function Set	0	0	0	0	1	DL	*	*	*	*	Sets interface data length(DL), number of display lines(N) and display character number. Character font is fixed 5 X 7. DL=1 : 8 bits , DL=0 : 4 bits	125us
Set CG RAM Address	0	0	0	1	*	←←←	A _{CG}	→→→			Sets CG RAM address. After this instruction, the data is transferred to/from CG RAM.	125us
Set DD RAM Address	0	0	1	←←←			A _{DD}	→→→			Sets DD RAM address. After this instruction, the data is transferred to/from DD RAM.	125us
Read Busy Flag & Address	0	1	BF	←←←			A _C	→→→			Reads busy flag and AC contents. BF=1 : Internally operating BF=0 : Can accept instruction	0us
Write Data to	1	0	←←	Write Data	(DD RAM)	→→					Writes data into DD or CG RAMs.	125us
CG or DD RAM	1	0	*	*	*	←	Write Data	→				
Read Data from	1	1	←←	Read Data	(DD RAM)	→→					Reads data from DD or CG RAMs.	188us
CG or DD RAM	1	1	*	*	*	←	Read Data	→				
Explanation of Abbreviation	DD RAM : Display data RAM , CG RAM : Character generator RAM A _{CG} : CG RAM address , A _{DD} : DD RAM address, Corresponds to cursor address AC : Address counter used for both of DD and CG RAMs											

* = Don't care

5

(3-1) Description of each instructions

(a) Maker Testing

	RS	R/W	DB ₇	DB ₆	DB ₅	DB ₄	DB ₃	DB ₂	DB ₁	DB ₀
Code	0	0	0	0	0	0	0	0	0	0

All "0" code in 4-bit length is using for device testing mode (only for maker).
Therefore, please avoid all "0" input or no meaning Enable signal input at data "0".
(Especially please pay attention the output condition of Enable signal when the power turns on.)

All "0" code in 8-bit length is operated only for NOP (Not Operating instruction).

(b) Clear Display

	RS	R/W	DB ₇	DB ₆	DB ₅	DB ₄	DB ₃	DB ₂	DB ₁	DB ₀
Code	0	0	0	0	0	0	0	0	0	1

Clear display instruction is executed when the code "1" is written into DB₀.
When this instruction is executed, the space code (20)_H is written into every DD RAM address, the DD RAM address 0 is set into the address counter and entry mode is set increment.

If the cursor or blink are displayed, they are returned to the left end of the 1st line.

The S of entry mode does not change.

Note: The character pattern for character code (20)_H must be blank code in the user-defined character pattern(Custom font).

(c) Return Home

	RS	R/W	DB ₇	DB ₆	DB ₅	DB ₄	DB ₃	DB ₂	DB ₁	DB ₀	
Code	0	0	0	0	0	0	0	0	1	*	* = Don't care

Return home instruction is executed when the code "1" is written into DB₁. When this instruction is executed, the DD RAM address 0 is set into the address counter. Display is returned its original position if shifted, the cursor or blink are returned to the left end of the 1st line if the cursor or blink are on the display.

The DD RAM contents do not change.

(d) Entry Mode Set

	RS	R/W	DB ₇	DB ₆	DB ₅	DB ₄	DB ₃	DB ₂	DB ₁	DB ₀
Code	0	0	0	0	0	0	0	1	I/D	S

Entry mode set instruction which sets the cursor moving direction and display shift On/Off, is executed when the code "1" is written into DB₂ and the codes of (I/D) and (S) are written into DB₁(I/D) and DB₀(S), as shown below.

(I/D) sets the address increment or decrement, and the (S) sets the entire display shift in the DD RAM writing.

I/D	F u n c t i o n
1	Address increment: The address of the DD RAM or CG RAM increment (+1) when the read/write, and the cursor or blink move to the right.
0	Address decrement: The address of the DD RAM or CG RAM decrement (-1) when the read/write, and the cursor or blink move to the left.

S	F u n c t i o n
1	Entire display shift. The shift direction is determined by I/D.: shift to the left at I/D=1 and shift to the right at the I/D=0. The shift is operated only for the character, so that it looks as if the cursor stands still and the display moves. The display does not shift when reading from the DD RAM and writing/reading into/from CG RAM.
0	The display does not shifting.

(e) Display On/Off Control

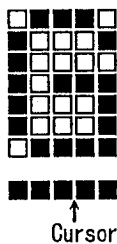
	RS	R/W	DB ₇	DB ₆	DB ₅	DB ₄	DB ₃	DB ₂	DB ₁	DB ₀
Code	0	0	0	0	0	0	1	D	C	B

Display On/Off control instruction which controls the whole display On/Off, the cursor On/Off and the cursor position character blink, is executed when the code "1" is written into DB₃ and the codes of (D), (C) and (B) are written into DB₂(D), DB₁(C) and DB₀(B), as shown below.

D	F u n c t i o n
1	Display On.
0	Display Off. In this mode, the display data remains in the DD RAM so that it is retrieved immediately on the display when the D change to 1.

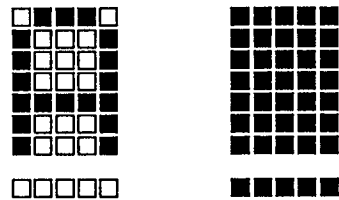
C	F u n c t i o n
1	Cursor On. The cursor is displayed by 5 dots on the 8th line.
0	Cursor Off. Even if the display data write, the I/D etc does not change.

B	F u n c t i o n
1	The cursor position character is blinking. Blinking rate is 520ms at $f_{osc}=80kHz$. The cursor and the blink can be displayed simultaneously.
0	The character does not blink.



Character Font 5 x 7 dots

(1) Cursor display example



Alternating display

(2) Blink display example

(f) Cursor/Display Shift

	RS	R/W	DB ₇	DB ₆	DB ₅	DB ₄	DB ₃	DB ₂	DB ₁	DB ₀	
Code	0	0	0	0	0	1	S/C	R/L	*	*	* = Don't care

The Cursor/Display shift instruction shifts the cursor position or display to the right or left without writing or reading display data. This function is used to correct or search the display. For example the cursor moves to the 2nd line when it passes the 10th digit of the 1st line. Notice that the 1st and 2nd line displays will shift at the same time. When the displayed data is shifted repeatedly, each line moves only horizontally.

For example the 2nd line display does not shift into the 1st line position.

The contents of address counter(AC) does not change by operation of the display shift only.

This instruction is executed when the code "1" is written into DB₄ and the codes of (S/C) and (R/L) are written into DB₃ and DB₂, as shown below.

S/C	R/L	F u n c t i o n
0	0	Shifts the cursor position to the left ((AC) is decremented by 1)
0	1	Shifts the cursor position to the right ((AC) is incremented by 1)
1	0	Shifts the entire display to the left and the cursor follows it.
1	1	Shifts the entire display to the right and the cursor follows it.

(g) Function Set

	RS	R/W	DB ₇	DB ₆	DB ₅	DB ₄	DB ₃	DB ₂	DB ₁	DB ₀	
Code	0	0	0	0	1	DL	*	*	*	*	* = Don't care

Function set instruction which sets the interface data length is executed when the code "1" is written into DB₅ and the code of (DL) is written into DB₄(DL), as shown below (character font is fixed 5 x 7 dots).

(DL) sets the interface data length.

NOTE

This function set instruction must be performed at the head of the program prior to all other existing instructions(except Busy flag/Address read). This function set instruction can not be executed afterwards unless the interface data length change.

DL	F u n c t i o n
1	Set the interface data length to 8 bits (DB ₇ to DB ₀)
0	Set the interface data length to 4 bits (DB ₇ to DB ₄) The data must be sent or received twice in this mode.

(h) Set CG RAM Address

	RS	R/W	DB ₇	DB ₆	DB ₅	DB ₄	DB ₃	DB ₂	DB ₁	DB ₀	
Code	0	0	0	1	*	A	A	A	A	A	* = Don't care
						←Higher order bit			Lower order bit →		

Set CG RAM address set instruction is executed when the code "1" is written into DB₆ and the address is written into DB₄ to DB₀ as shown above.

The address data mentioned by binary code "AAAAA" is written into the address counter (AC) together with the CG RAM addressing condition. After this instruction execution, the data writing/reading is performed into/from the CG RAM.

(i) Set DD RAM Address

	RS	R/W	DB ₇	DB ₆	DB ₅	DB ₄	DB ₃	DB ₂	DB ₁	DB ₀
Code	0	0	1	A	A	A	A	A	A	A
				←Higher order bit				Lower order bit →		

Set DD RAM address instruction is executed when the code "1" is written into DB₇ and the address is written into DB₆ to DB₀ as shown above.

The address data mentioned by binary code "AAAAAA" is written into the address counter (AC) together with the DD RAM addressing condition. After this instruction execution, the data writing/reading is performed into/from the DD RAM.

Note : The "AAAAAA" is addressed (00)_H to (09)_H for the 1st line, the (0C)_H to (15)_H for the 2nd line and the (40)_H to (49)_H for the 3rd line.

(j) Read Busy Flag & Address

	RS	R/W	DB ₇	DB ₆	DB ₅	DB ₄	DB ₃	DB ₂	DB ₁	DB ₀
Code	0	1	BF	A	A	A	A	A	A	A
				←Higher order bit				Lower order bit →		

This instruction reads out the internal status of the NJU6424. When this instruction is executed, the busy flag (BF) which indicate internal operation is read out from DB₇ and the address of the CG RAM or DD RAM is read out from DB₆ to DB₀ (the address for the CG RAM or DD RAM is determined by the previous instruction).

(BF)="1" indicates that internal operation is in progress. The next instruction is inhibited when (BF)="1". Check the (BF) status before the next write operation.

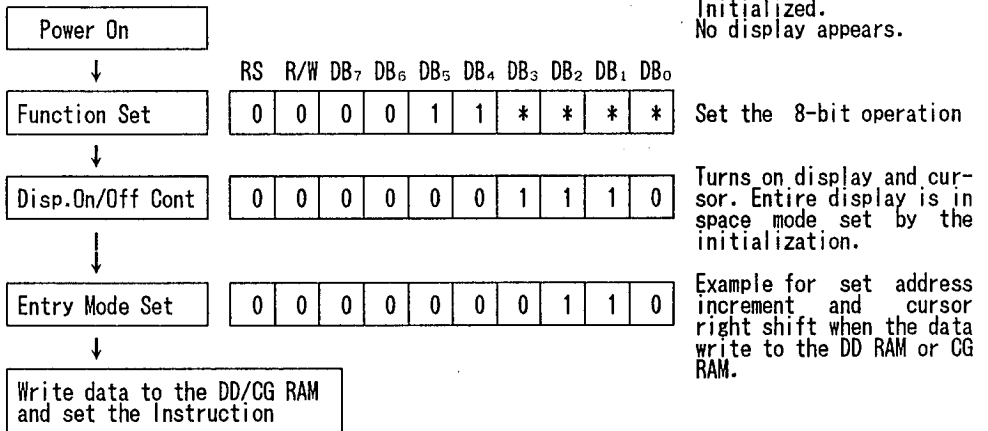
(3-2) Initialization using the internal reset circuits

(a) 8-bit operation (Using internal reset circuits)

At 8-bit operation, the Function set, Display On/Off Control and Entry Set Instruction must be executed before the data input, as shown below.

The DD RAM of the NJU6424 can store up to 30 characters, as explained before, therefore the advertising moving display is available when combined with the display shift operation.

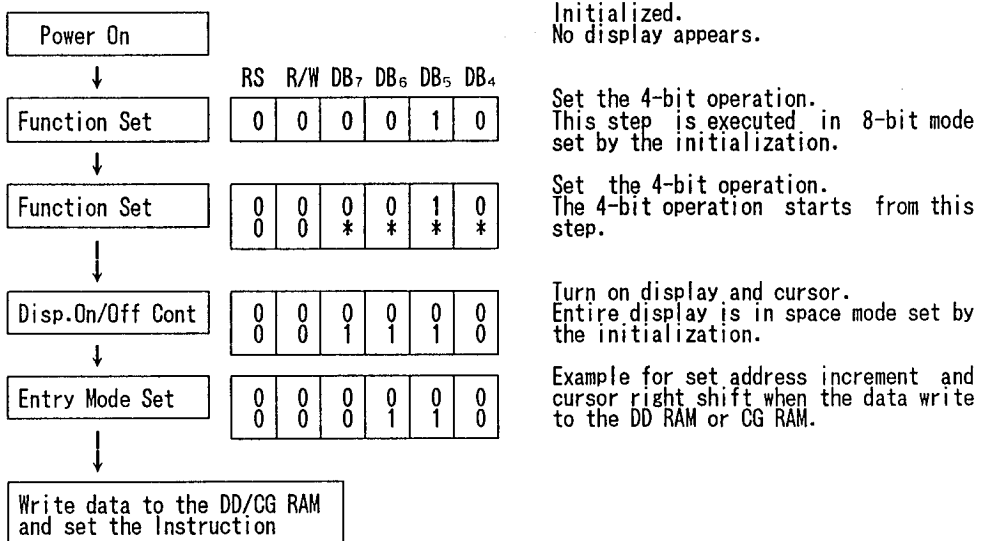
Since the display shift operation changes only display position and the DD RAM contents remain unchanged, display data which are entered first can be output when the return home operation is performed.



(b) 4-bit operation (Using internal reset circuits).

In the 4-bit operation, the function set must be performed by the user programming.

When the power is turned on, 8-bit operation is selected automatically, therefore the first input is performed under 8-bit operation. In this operation, full instruction can not input because of terminals DB₀ to DB₃ are no connection. Therefore, same instruction must be rewritten on the RS, R/W and DB₇ to DB₄, as shown below. Since one operation is completed by the two accesses in the 4-bit operation mode, rewrite is required to set the instruction code in full. 4-bit operation is shown as follows:

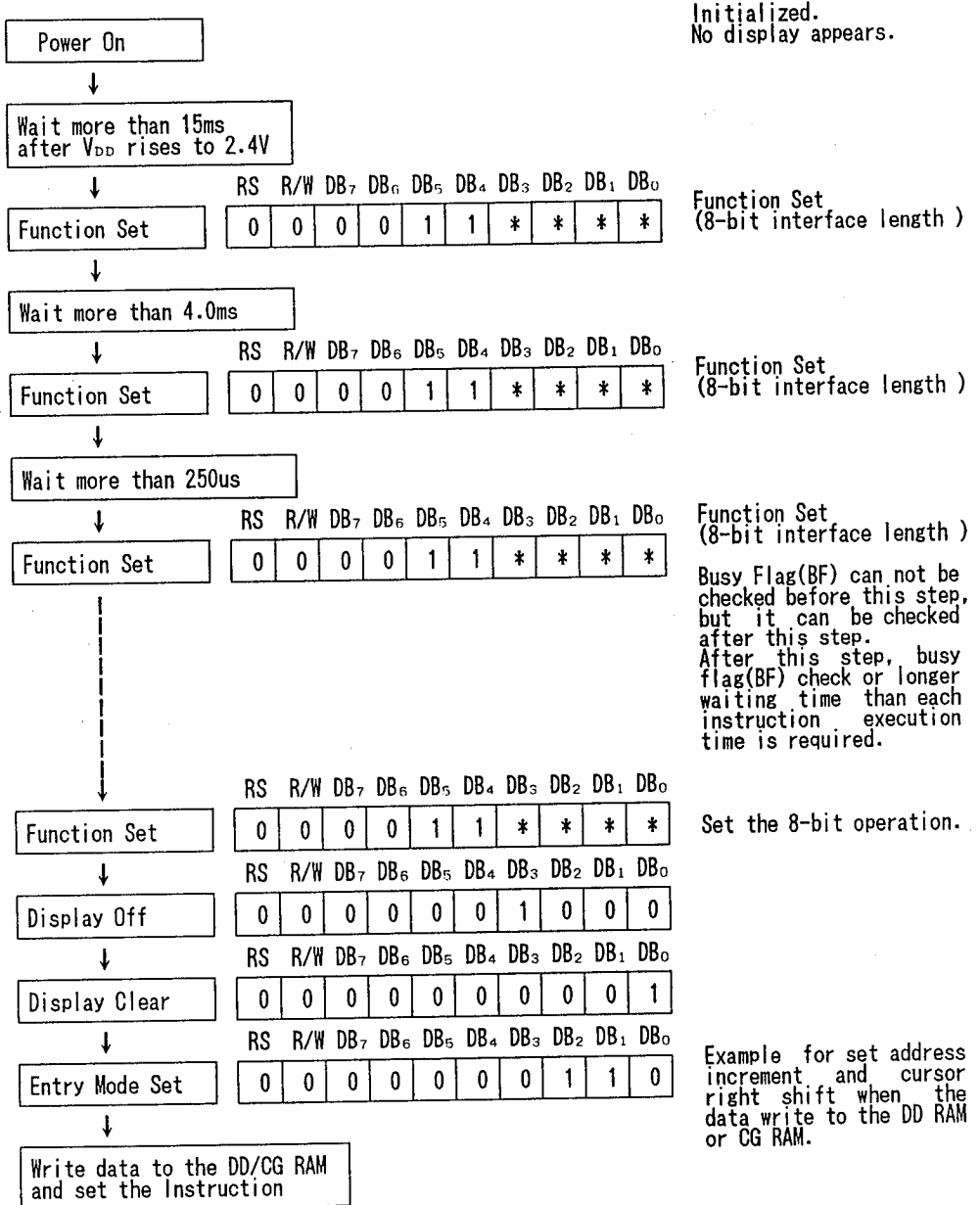


5

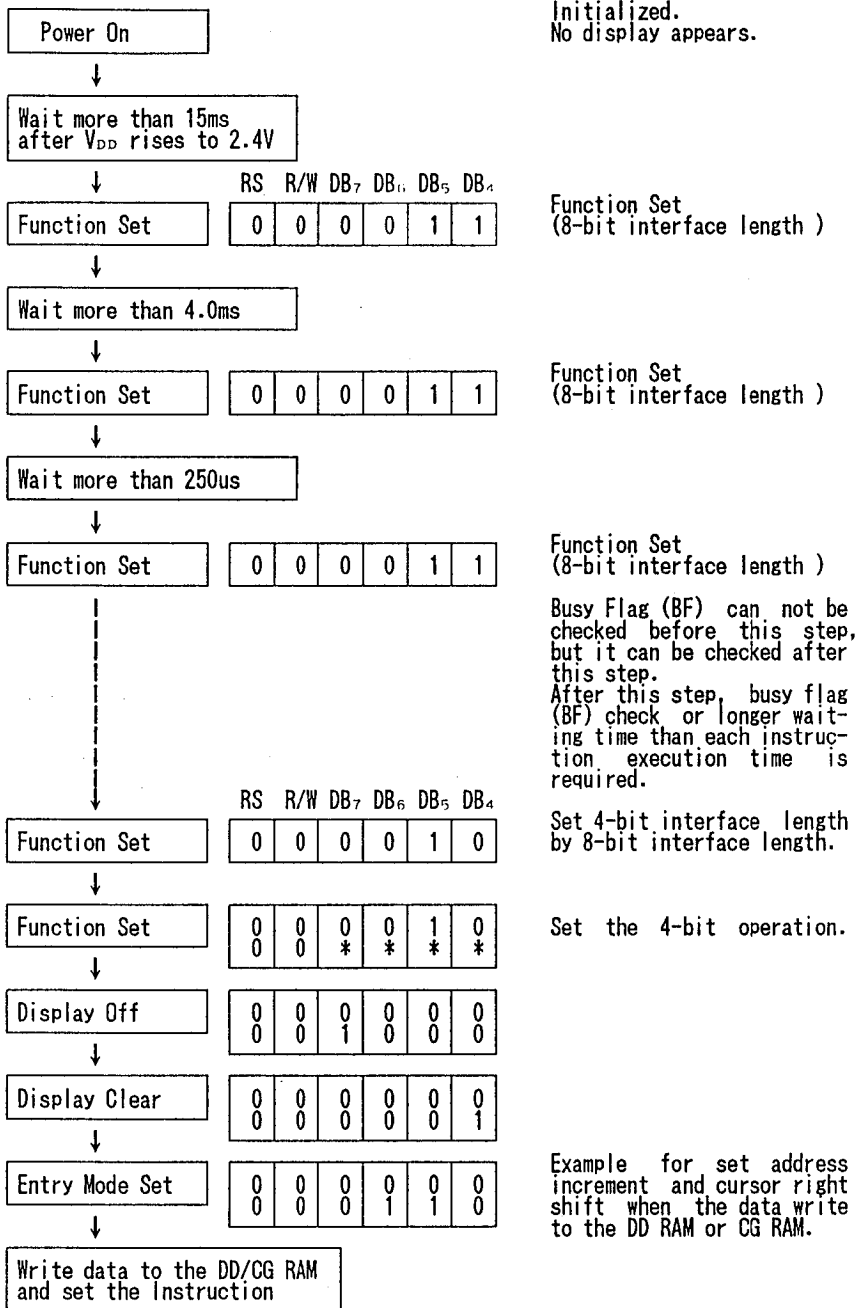
(3-3) Initialization by instruction

If the power supply conditions for the correct operation of the internal reset circuits are not met, the NJU6424 must be initialized by the instruction.

(a) Initialization by Instruction in 8-bit interface length.



(b) Initialization by Instruction in 4-bit interface length



Initialized.
No display appears.

Function Set
(8-bit interface length)

Function Set
(8-bit interface length)

Function Set
(8-bit interface length)

Busy Flag (BF) can not be checked before this step, but it can be checked after this step. After this step, busy flag (BF) check or longer waiting time than each instruction execution time is required.

Set 4-bit interface length by 8-bit interface length.

Set the 4-bit operation.

Example for set address increment and cursor right shift when the data write to the DD RAM or CG RAM.

5

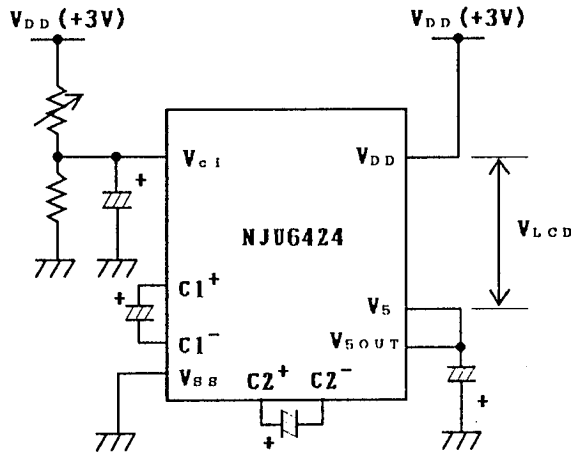
(4) LCD DISPLAY

(4-1) Power Supply for LCD Driving

NJU6424 incorporate voltage tripler to generate LCD driving high voltage and bleeder resistance. The voltage tripler generate about triple voltage from the V_{c1} input voltage (7.8V typ at $I_{out}=1mA$ and $V_{c1}=3V$) and bleeder resistance generate each LCD driving voltage. The bleeder resistance is set 1/5 bias suitable for 1/26 duty ratio and $1M\Omega$ per resistance. Furthermore, the bleeder resistance output the LCD Driving bias level through the voltage follower OP-AMP to get a enough display characteristics with low power consumption.

LCD Driving Voltage vs Duty Ratio

Power supply	Duty Ratio	1/26
	Bias	1/5
V_{LCD}		V_{DD} to V_{5OUT}



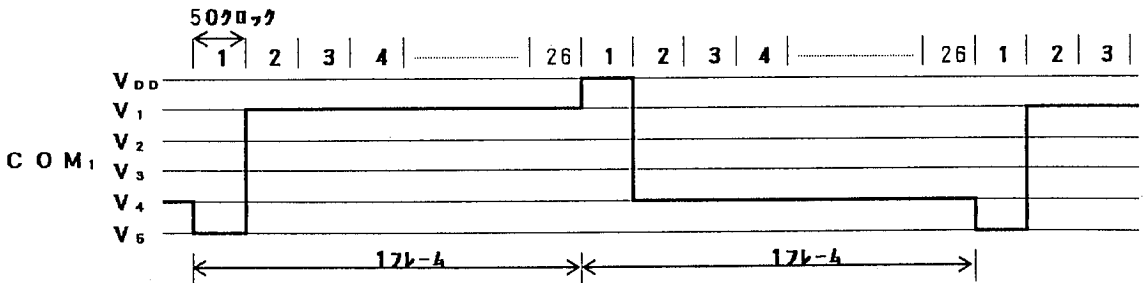
Voltage Tripler used example

(4-2) Relation between oscillation frequency and LCD frame frequency.

As the NJU6424 incorporate oscillation capacitor and resistance for CR oscillation, 80kHz oscillation is available without any external components.

The LCD frame frequency is able to be calculated as follows.

$$1 \text{ frame frequency} = f_{osc} / (50 \times 26) = 61.5 \text{ (Hz)}$$



(5) Interface with MPU

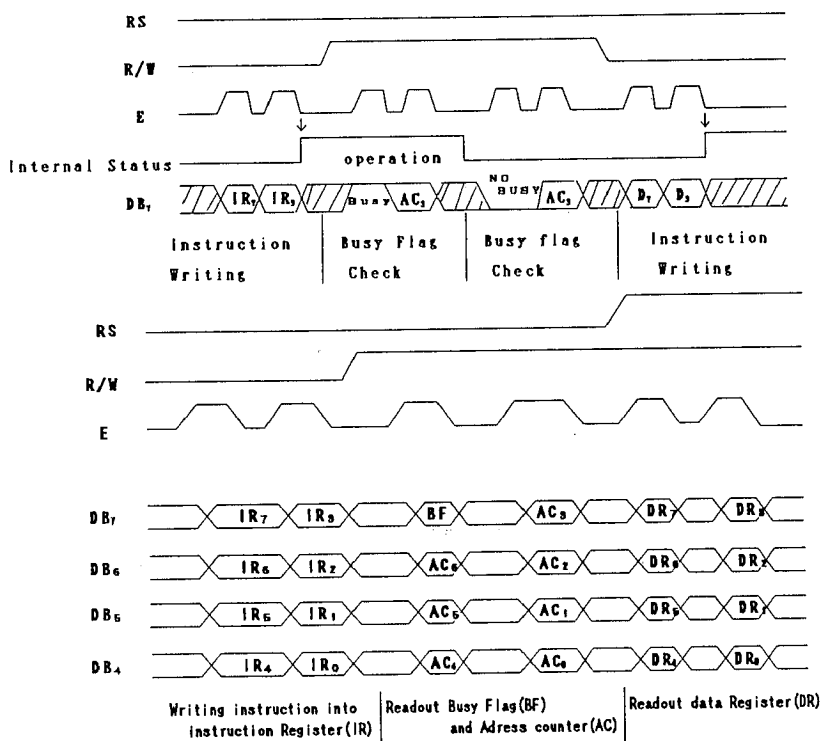
NJU6424 can be interfaced with both of 4/8-bit MPU and the two-time 4-bit or one-time 8-bit data transfer is available.

(5-1) 4-bit MPU interface

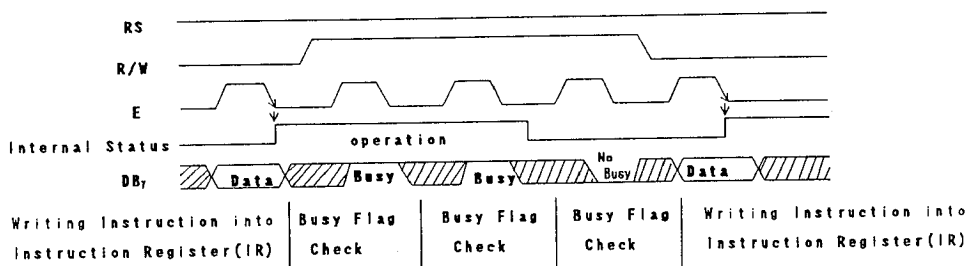
When the interface length is 4-bit, the data transfer is performed by 4 lines connected to DB₄ to DB₇ (DB₀ to DB₃ are not used). The data transfer with the MPU is completed by the two-time 4-bit data transfer.

The data transfer is executed in the sequence of upper 4-bit (the data DB₄ to DB₇ at 8-bit length) and lower 4-bit (the data DB₀ to DB₃ at 8-bit length).

The busy flag check must be executed after two-time 4bit data transfer (1 instruction execution). In this case the data of busy flag and address counter are also output twice.



(5-2) 8-bit MPU interface



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V _{DD}	- 0.3 ~ + 7.0	V
Input Voltage	V _{IN}	- 0.3 ~ V _{DD} +0.3	V
Operating Temperature	T _{opr}	- 30 ~ + 80	°C
Storage Temperature	T _{stg}	- 55 ~ + 125	°C

Note 1) If the LSI are used on condition above the absolute maximum ratings, the LSI may be destroyed. Using the LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electric characteristics conditions will cause malfunction and poor reliability.

Note 2) All voltage values are specified as V_{SS} = 0V

Note 3) The relation : V_{DD} ≥ V_{ci} > V_{SS}, V_{DD} > V_{SS} ≥ V_{5OUT}, V_{SS}=0V must be maintained.

Turn on V_{DD} and V_{ci} at same time or turn on V_{DD} first then turn on V_{ci} must be required. If the turn on sequence does not meet above conditions, latch up will occur.

Note 4) Decoupling capacitor should be connected between V_{ci} and V_{SS} due to the stabilized operation for the voltage Doubler.

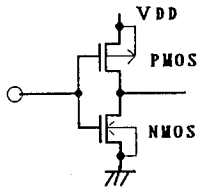
■ ELECTRICAL CHARACTERISTICS

 (V_{DD}=3V±20% , Ta=-20 ~ +75°C)

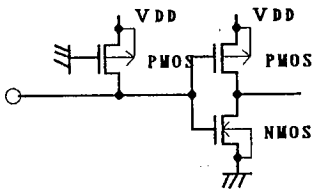
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE	
Operating Voltage	V _{DD}		2.4	3.0	3.6	V		
Input Voltage	V _{IH}		0.8V _{DD}		V _{DD}	V	4	
	V _{IL}				0.2V _{DD}			
Output Voltage	V _{OH}	-I _{OH} =0.205mA	2.0			V	5	
	V _{OL}	I _{OL} =1.6mA			0.5			
Driver On-resist.(COM)	R _{COM}	±I _d =5uA(All common term.)			20	kΩ	8	
Driver On-resist.(SEG)	R _{SEG}	±I _d =5uA(All seg. term.)			30			
Input Leakage Current	I _{LI}	V _{IN} =0 ~ V _{DD}	- 1		1	uA	6	
Pull-up Resistance Current	-I _P	V _{DD} =3V, RS, R/W, RESET, and DB Terminals	10	25	50	uA		
Operating Current	I _{DD}	V _{DD} =3V, f _{OSC} =Internal freq		150	250	uA	7	
Voltage Doubler	Output Volt.	V _{UP}	V _{ci} =3V, I _{OUT} =1mA, Ta=25°C	- 1.6	- 1.8		V	
	Input Volt.	V _{ci}	-	1.8		V _{DD}	V	
	Volt. Effieci	V _{ef}	R _L =∞	95.0	99.9		%	
Voltage Tripler	Output Volt.	V _{UP}	V _{ci} =3V, I _{OUT} =1mA, Ta=25°C	- 4.6	- 4.8		V	
	Input Volt.	V _{ci}	-	1.8		V _{DD}	V	
	Volt. Effieci	V _{ef}	R _L =∞	95.0	99.9		%	
Bleeder resistance	R _B	V _{DD} -V ₅ =3V		1.0		MΩ		
Oscillation Frequency	f _{OSC}	V _{DD} =3V, Ta=25°C	56	80	104	kHz		
LCD Driving Voltage	V _{LCD}	V ₅ Terminal, V _{DD} =3V	V _{DD} -3.0		V _{DD} -13.5	V	10	
V ₅ Terminal Current	I ₅	V _{DD} =V _{ci} =3V			170	uA		

Note 5) Input/Output structure except LCD driver are shown below:

Input Terminal Structure

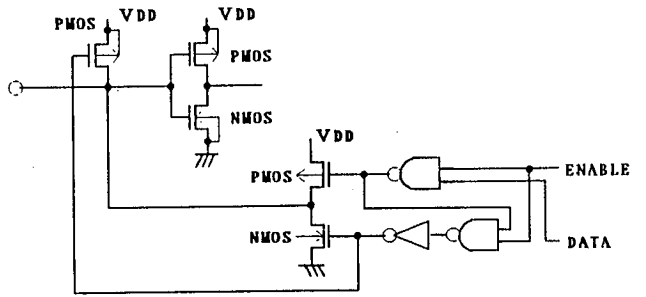


E Terminal



RS, R/W and RESET Terminals

Input/Output Terminal Structure



DB₀ to DB₇ Terminals

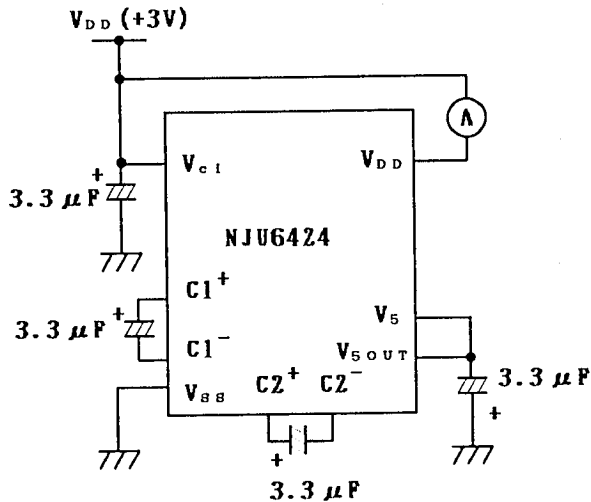
Note 6) Apply to the Input/Output Terminal.

Note 7) Except pull-up resistance current and output driver current.

Note 8) Except Input/output current but including the current flow on bleeder resistance.

If the input level is medium, current consumption will increase due to the penetration current. Therefore, the input level must be fixed to "H" or "L".

Operating Current Measurement Circuit

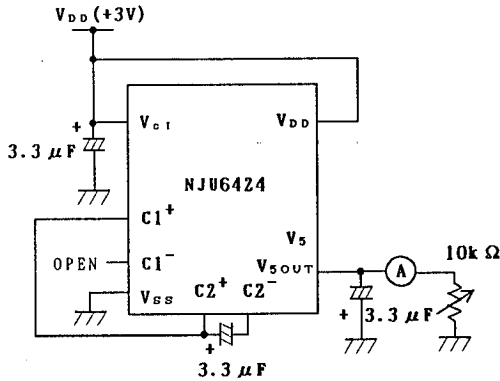


Note 9) R_{COM} and R_{SEG} are the resistance values between power supply terminals (V_{DD} , V_{SOUT}) and each common terminal (COM_1 to COM_{24} , $COMMK1$ and $COMMK2$), and supply voltage (V_{DD} , V_{SOUT}) and each segment terminal (SEG_1 to SEG_{50}) respectively, and measured when the current I_d is flown on every common and segment terminals at a same time.

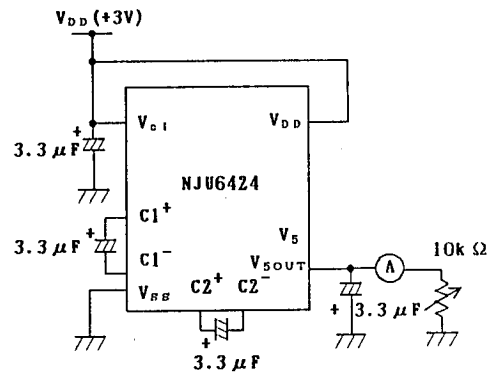
Note 10) R_{COM} or R_{SEG} are able to be decreased by the resistance connected between BIAS and VSS terminal.

Note 11) Apply to the output voltage from each COM and SEG are less than $\pm 0.15V$ against the LCD driving constant voltage (V_{DD} , V_S) at no load condition.

Voltage Doubler Measurement Circuit

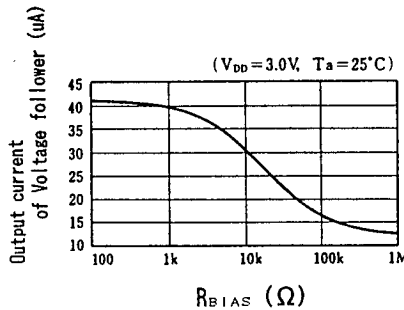
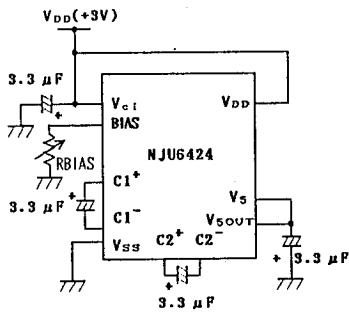


Voltage Tripler Measurement Circuit



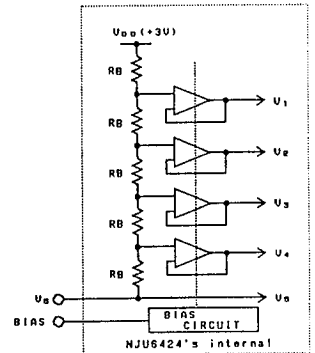
Voltage Doubler/Tripler Internal
Clock Frequency = 10kHz typ.

BIAS Terminal Performance
measurement circuit
(Output current of Voltage Follower)



BIAS Terminal Performance

Internal Bleeder Resistance and Voltage Follower



- Bus timing characteristics ($V_{DD} = 3.0V \pm 20\%$, $V_{SS} = 0V$, $T_a = -20 \sim +75^\circ C$)

Write operation (Write from MPU to NJU6424)

PARAMETER		SYMBOL	MIN	MAX	CONDITION	UNIT
Enable Cycle Time		t_{CYCE}	1		fig.1	us
Enable Pulse Width	"High" level	P_{WEH}	400			ns
Enable Rise Time, Fall Time		t_{ER} , t_{EF}		20		
Set up Time	RS, R/W, E	t_{AS}	40			
Address Hold Time		t_{AH}	10			
Data Set up Time		t_{DSW}	60			
Data Hold Time		t_H	10			

Timing Characteristics (Write operation)

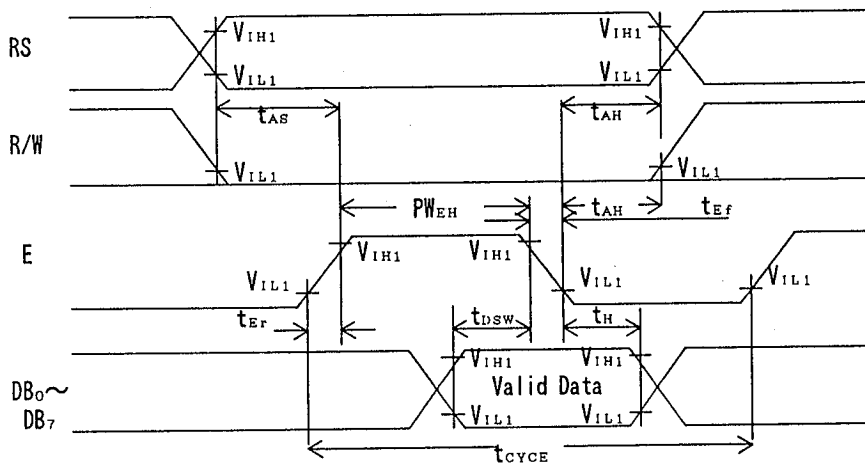


fig. 1

5

Read operation (Read from NJU6424 to MPU)

PARAMETER	SYMBOL	MIN	MAX	CONDITION	UNIT
Enable Cycle Time	t_{CYCE}	1		fig.2	us
Enable Pulse Width "High" level	P_{WEH}	600			ns
Enable Rise Time, Fall Time	$t_{E\uparrow}, t_{E\downarrow}$		20		
Set up Time RS, R/W, E	t_{AS}	40			
Address Hold Time	t_{AH}	10			
Data Delay Time	t_{DDW}		600		
Data Hold Time	t_{DDH}	20			

 $DB_0 \sim DB_7$ Load Condition : $C_L = 100pF$

Timing Characteristics (Read operation)

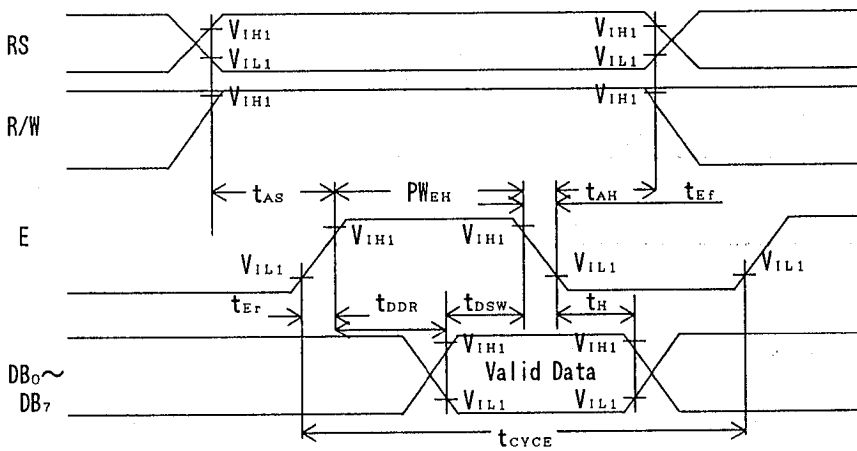
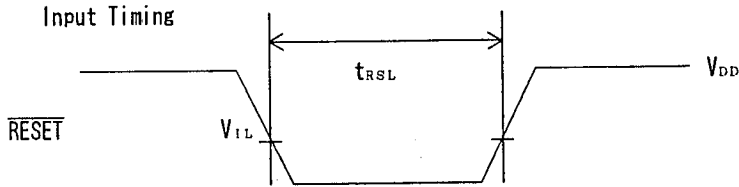


fig. 2

• The Input Condition when using the Hardware Reset Circuit

PARAMETER	SYMBOL	CONDITION	MIN	MAX	UNIT
Reset Input "L" Level Width	t_{RSL}	$f_{OSC}=80kHz$	1.2	-	ms

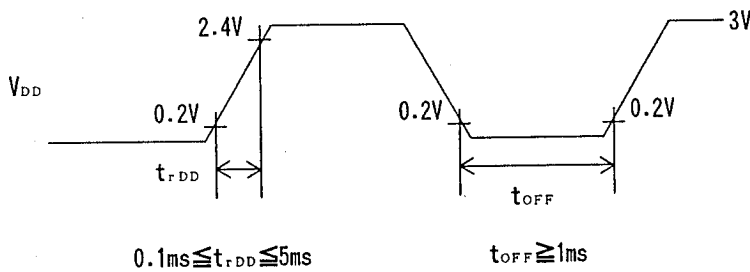


• Power Supply Condition when using the internal initialization circuit
 ($V_{DD} = 3.0V \pm 20\%$, $V_{SS} = 0V$, $T_a = -20 \sim +75^\circ C$)

PARAMETER	SYMBOL	CONDITION	MIN	MAX	UNIT
Power Supply Rise Time	t_{rDD}		0.1	5	ms
Power Supply OFF Time	t_{OFF}		1		

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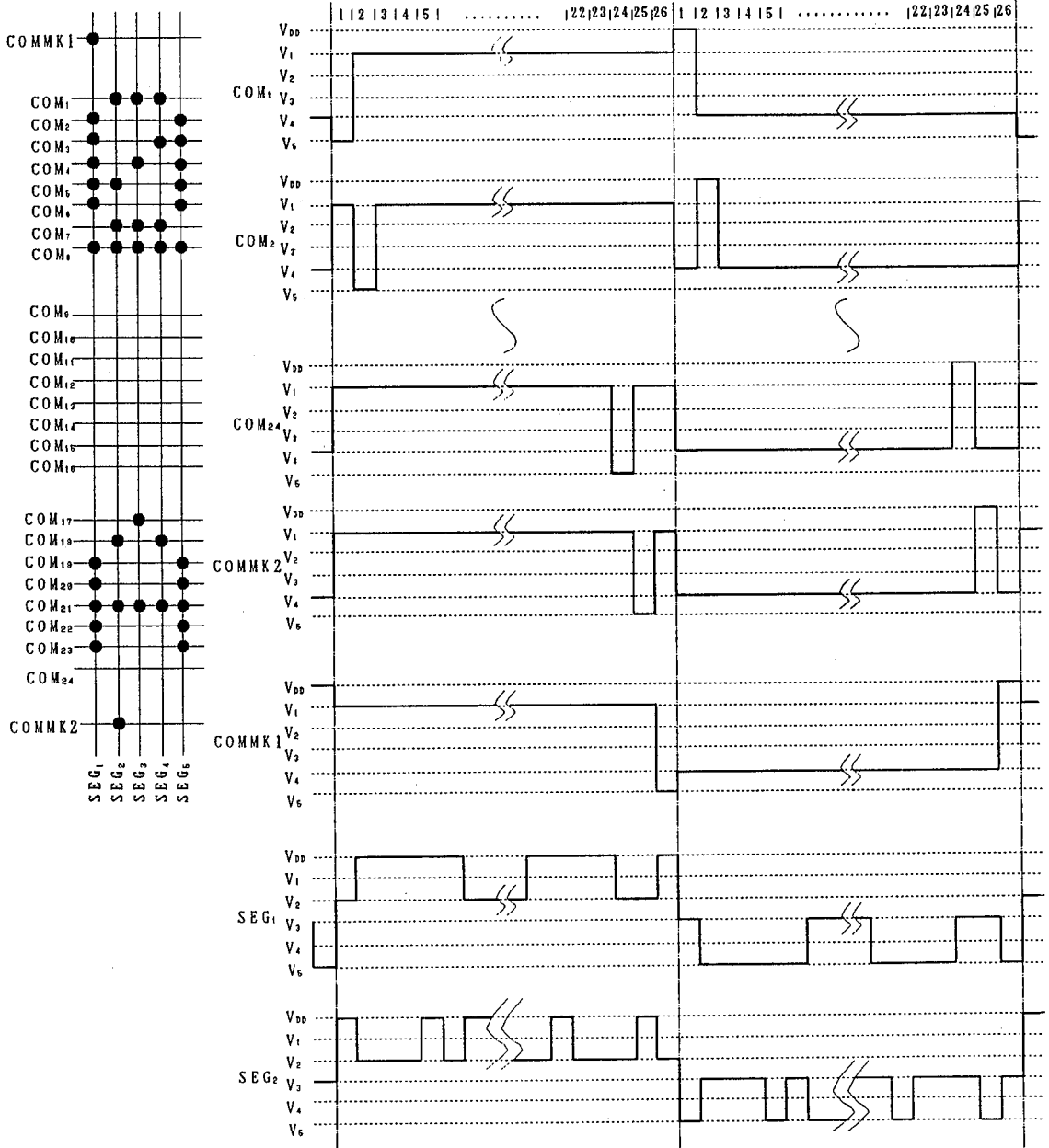
Since the internal initialization circuits will not operate normally unless the above conditions are met, in such a case initialize by instruction.
 (Refer to initialization by the instruction)



t_{OFF} specifies the power off time in a short period off or cyclical on/off.

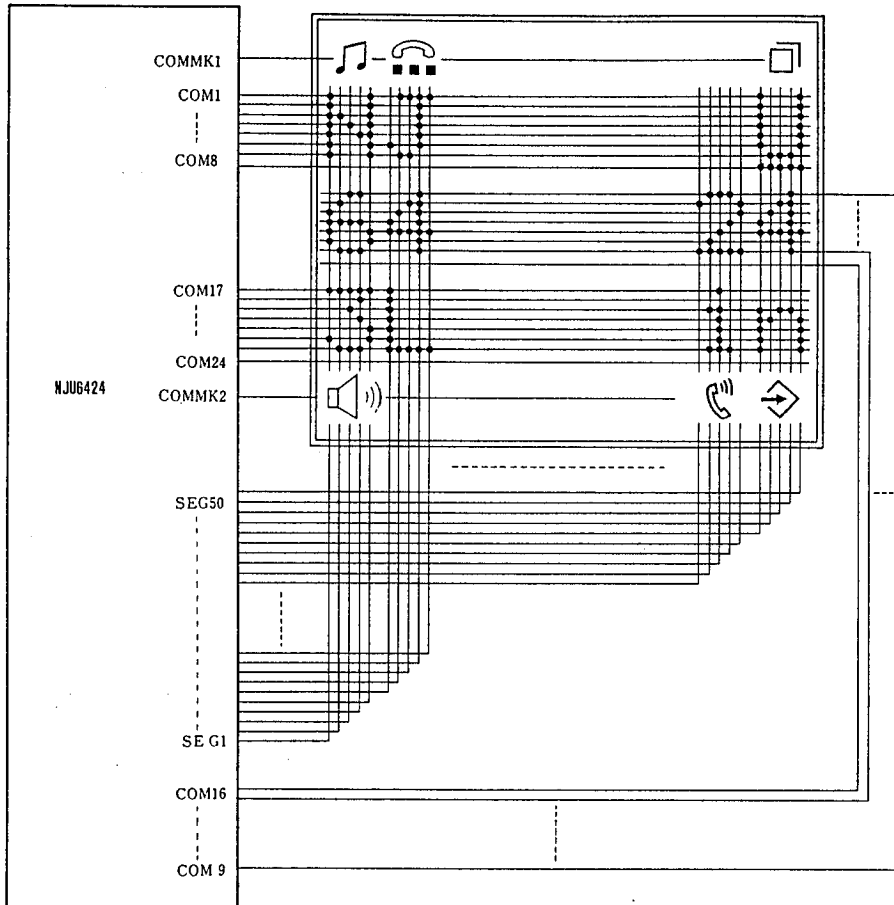
■ LCD DRIVING WAVE FORM

1/26 Duty Driving



APPLICATION CIRCUITS (1)

10-character 3-line WITH ICON Display Example



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MEMO

[CAUTION]

The specifications on this databook are only given for information, without any guarantee as regards either mistakes or omissions. The application circuits in this databook are described only to show representative usages of the product and not intended for the guarantee or permission of any right including the industrial rights.