MSC23837A-xxBS18/DS18

8,388,608-Word × 36-Bit DRAM MODULE : FAST PAGE MODE TYPE

DESCRIPTION

The Oki MSC23837A-xxBS18/DS18 is a fully decoded 8,388,608-word × 36-bit CMOS dynamic random access memory composed of eighteen 16-Mb DRAMs (4M × 4) in SOJ packages mounted with decoupling capacitors on a 72-pin glass epoxy SIMM Package. This module is generally used for memory expansion in parity applications such as workstations.

FEATURES

- 8,388,608-word × 36-bit (ECC) organization
- 72-pin SIMM
  MSC23837A-xxBS18 : Gold tab
  MSC23837A-xxDS18 : Solder tab
- Single 5 V supply ±10% tolerance
- Input : TTL compatible
- Output : TTL compatible, 3-state
- Refresh : 4096 cycles/64 ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{CAS}$ before $\overline{RAS}$ hidden refresh, $\overline{RAS}$-only refresh capability
- Multi-bit test mode capability
- Fast Page Mode capability

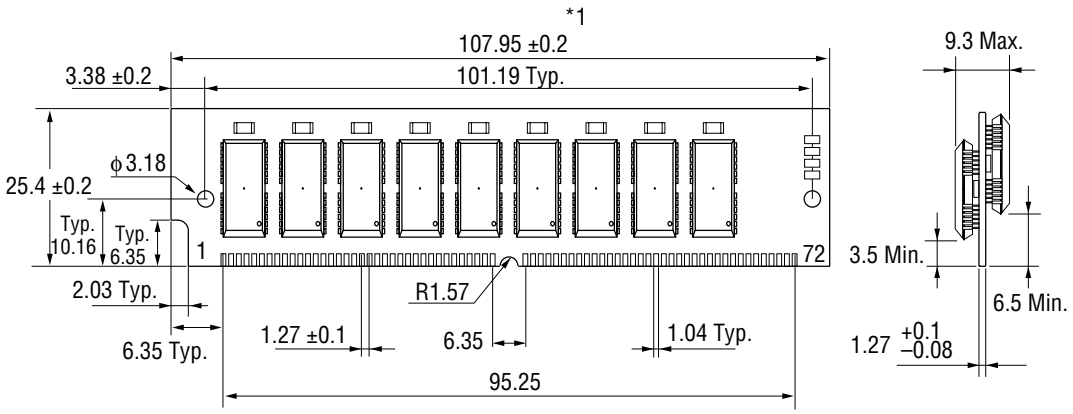
PRODUCT FAMILY

Family	Access Time (Max.)				Cycle Time (Min.)	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}	t_{OEA}		Operating (Max.)	Standby (Max.)
MSC23837A-60BS18/DS18	60 ns	30 ns	15 ns	15 ns	110 ns	5197.5 mW	99 mW
MSC23837A-70BS18/DS18	70 ns	35 ns	20 ns	20 ns	130 ns	4702.5 mW	

PIN CONFIGURATION

MSC23837A-xxBS18/DS18

(Unit : mm)



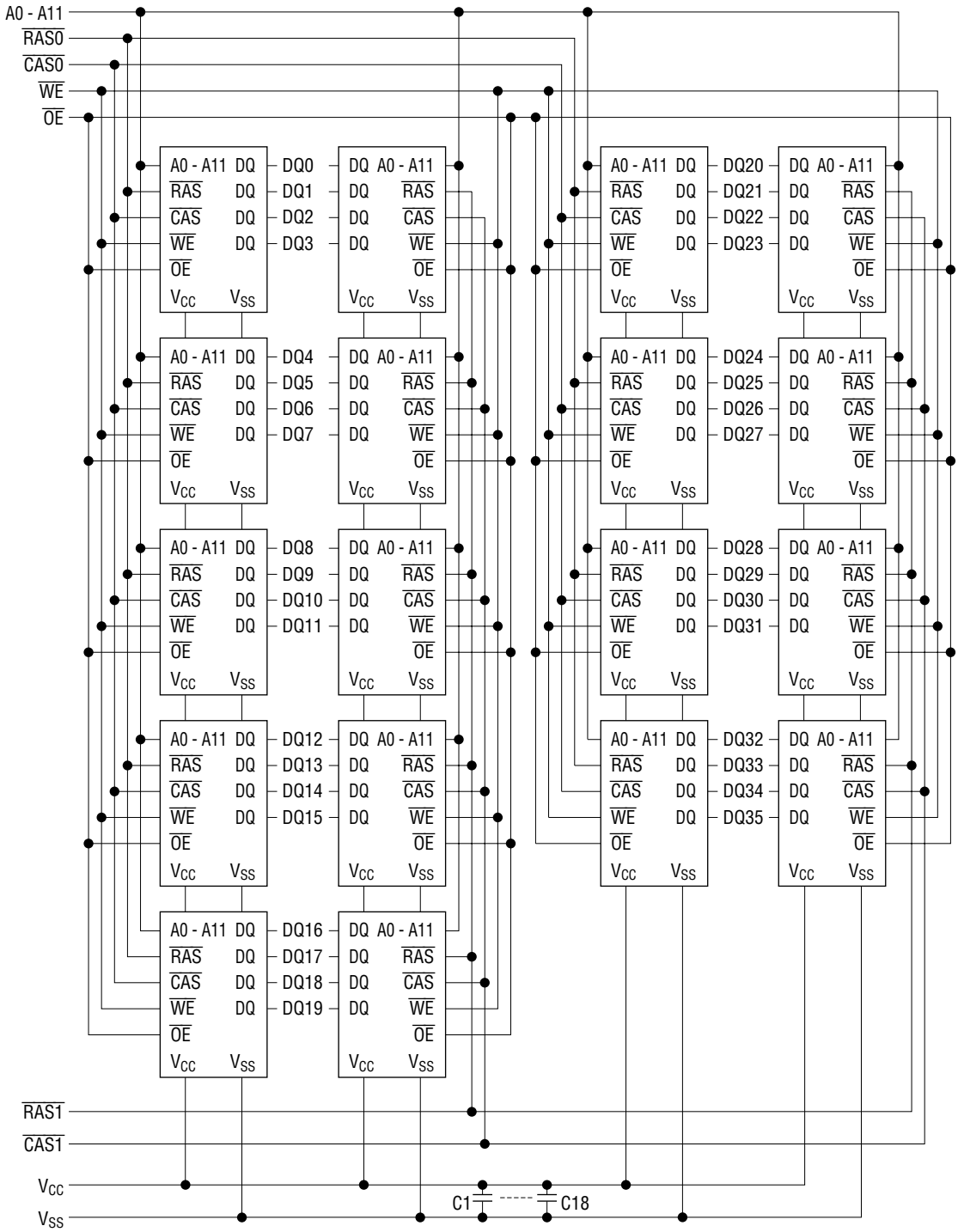
*1 The common size difference of the board width 12.5 mm of its height is specified as ±0.2. The value above 12.5 mm is specified as ±0.5.

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{SS}	16	A4	31	A8	46	DQ21	61	DQ33
2	DQ0	17	A5	32	A9	47	$\overline{WE}$	62	DQ34
3	DQ1	18	A6	33	NC	48	NC	63	DQ35
4	DQ2	19	$\overline{OE}$	34	NC	49	DQ22	64	NC
5	DQ3	20	DQ8	35	DQ17	50	DQ23	65	NC
6	DQ4	21	DQ9	36	DQ18	51	DQ24	66	NC
7	DQ5	22	DQ10	37	DQ19	52	DQ25	67	PD1
8	DQ6	23	DQ11	38	DQ20	53	DQ26	68	PD2
9	DQ7	24	DQ12	39	V_{SS}	54	DQ27	69	PD3
10	V_{CC}	25	DQ13	40	$\overline{CAS0}$	55	DQ28	70	PD4
11	PD5	26	DQ14	41	A10	56	DQ29	71	NC
12	A0	27	DQ15	42	A11	57	DQ30	72	V_{SS}
13	A1	28	A7	43	$\overline{CAS1}$	58	DQ31		
14	A2	29	DQ16	44	$\overline{RAS0}$	59	V_{CC}		
15	A3	30	V_{CC}	45	$\overline{RAS1}$	60	DQ32		

Presence Detect Pins

Pin No.	Pin Name	MSC23837A -60BS18/DS18	MSC23837A -70BS18/DS18
67	PD1	NC	NC
68	PD2	V_{SS}	V_{SS}
69	PD3	NC	V_{SS}
70	PD4	NC	NC
11	PD5	V_{SS}	V_{SS}

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	–1.0 to 7.0	V
Voltage V_{CC} Supply Relative to V_{SS}	V_{CC}	–1.0 to 7.0	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_D	18	W
Operating Temperature	T_{opr}	0 to 70	°C
Storage Temperature	T_{stg}	–40 to 125	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

(Ta = 0°C to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	6.5	V
Input Low Voltage	V_{IL}	–1.0	—	0.8	V

Capacitance

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 - A11)	C_{IN1}	—	122	pF
Input Capacitance ($\overline{RAS0}$, $\overline{RAS1}$, $\overline{CAS0}$, $\overline{CAS1}$)	C_{IN2}	—	73	pF
Input Capacitance ($\overline{WE}$, $\overline{OE}$)	C_{IN3}	—	140	pF
I/O Capacitance (DQ0 - DQ35)	C_{DQ}	—	26	pF

Note : Capacitance measured with Boonton Meter.

DC Characteristics

(V_{CC} = 5 V ±10%, Ta = 0°C to 70°C)

Parameter	Symbol	Condition	MSC23837A -60BS18/DS18		MSC23837A -70BS18/DS18		Unit	Note
			Min.	Max.	Min.	Max.		
Input Leakage Current	I_{LI}	0 V ≤ V_I ≤ 6.5 V; All other pins not under test = 0 V	–180	180	–180	180	µA	
Output Leakage Current	I_{LO}	D_{OUT} disable 0 V ≤ V_O ≤ 5.5 V	–20	20	–20	20	µA	
Output High Voltage	V_{OH}	I_{OH} = –5.0 mA	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	I_{OL} = 4.2 mA	0	0.4	0	0.4	V	
Average Power Supply Current (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = Min.	—	945	—	855	mA	1, 2
Power Supply Current (Standby)	I_{CC2}	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}	—	36	—	36	mA	1
		$\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} –0.2 V	—	18	—	18	mA	1
Average Power Supply Current ($\overline{RAS}$-only Refresh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = Min.	—	945	—	855	mA	1, 2
Average Power Supply Current ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	I_{CC6}	$\overline{RAS}$ cycling, $\overline{CAS}$ before $\overline{RAS}$, t_{RC} = Min.	—	945	—	855	mA	1, 2
Average Power Supply Current (Fast Page Mode)	I_{CC7}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{PC} = Min.	—	855	—	765	mA	1, 3

Notes: 1. I_{CC} Max. is specified as I_{CC} for output open condition.
2. Address can be changed once or less while $\overline{RAS}$=V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$=V_{IH}.

AC Characteristics (1/2)

(V_{CC} = 5 V ±10%, Ta = 0°C to 70°C) Note 1,2,3,11,12

Parameter	Symbol	MSC23837A -60BS18/DS18		MSC23837A -70BS18/DS18		Unit	Note
		Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	110	—	130	—	ns	
Read Modify Write Cycle Time	t_{RWC}	155	—	185	—	ns	
Fast Page Mode Cycle Time	t_{PC}	40	—	45	—	ns	
Fast Page Mode Read Modify Write Cycle Time	t_{PRWC}	85	—	100	—	ns	
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	ns	4, 5, 6
Access Time from $\overline{CAS}$	t_{CAC}	—	15	—	20	ns	4, 5
Access Time from Column Address	t_{AA}	—	30	—	35	ns	4, 6
Access Time from $\overline{CAS}$ Precharge	t_{CPA}	—	35	—	40	ns	4
Access Time from $\overline{OE}$	t_{OEA}	—	15	—	20	ns	4
Output Low Impedance Time from $\overline{CAS}$	t_{CLZ}	0	—	0	—	ns	4
Output Buffer Turn-off Delay Time	t_{OFF}	0	15	0	20	ns	7
$\overline{OE}$ to Data Output Buffer Turn-off Delay Time	t_{OEZ}	0	15	0	20	ns	7
Transition Time	t_T	3	50	3	50	ns	3
Refresh Period	t_{REF}	—	64	—	64	ms	
$\overline{RAS}$ Precharge Time	t_{RP}	40	—	50	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10k	70	10k	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	100k	70	100k	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15	—	20	—	ns	
$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	t_{ROH}	10	—	10	—	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10k	20	10k	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60	—	70	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35	—	40	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	50	ns	5
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	ns	6
Row Address Set-up Time	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	ns	
Column Address Hold Time from $\overline{RAS}$	t_{AR}	50	—	55	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	30	—	35	—	ns	

AC Characteristics (2/2)

(V_{CC} = 5 V ±10%, Ta = 0°C to 70°C) Note 1,2,3,11,12

Parameter	Symbol	MSC23837A -60BS18/DS18		MSC23837A -70BS18/DS18		Unit	Note
		Min.	Max.	Min.	Max.		
Read Command Set-up Time	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time	t_{RCH}	0	—	0	—	ns	8
Read Command Hold Time referenced to $\overline{RAS}$	t_{RRH}	0	—	0	—	ns	8
Write Command Set-up Time	t_{WCS}	0	—	0	—	ns	9
Write Command Hold Time	t_{WCH}	10	—	15	—	ns	
Write Command Hold Time from $\overline{RAS}$	t_{WCR}	45	—	55	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	ns	
$\overline{OE}$ Command Hold Time	t_{OEH}	15	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	15	—	20	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	15	—	20	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	ns	10
Data-in Hold Time	t_{DH}	15	—	15	—	ns	10
Data-in Hold Time from $\overline{RAS}$	t_{DHR}	50	—	55	—	ns	
$\overline{OE}$ to Data-in Delay Time	t_{OED}	15	—	20	—	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	40	—	50	—	ns	9
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	55	—	65	—	ns	9
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	85	—	100	—	ns	9
$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPWD}	60	—	70	—	ns	9
$\overline{CAS}$ Active Delay Time from $\overline{RAS}$ Precharge	t_{RPC}	10	—	10	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}	10	—	10	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}	20	—	20	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$)	t_{WRP}	10	—	10	—	ns	
$\overline{WE}$ Hold Time from $\overline{RAS}$ ($\overline{CAS}$ before $\overline{RAS}$)	t_{WRH}	10	—	10	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Set-up Time (Test Mode)	t_{WTS}	10	—	10	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Hold Time (Test Mode)	t_{WTH}	20	—	20	—	ns	

Notes:

1. A start-up delay of 200 μs is required after power-up followed by a minimum of eight initialization cycles ($\overline{RAS}$-only refresh or $\overline{CAS}$ before $\overline{RAS}$ refresh) before proper device operation is achieved.
   When using the internal refresh counter, a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ initialization cycles is required.

2. AC mesurement assume t_T = 5 ns.

3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring input timing signals. Transition times are measured between V_{IH} and V_{IL}.

4. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.

5. Operation within the t_{RCD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (Max.) limit, access time is controlled by t_{CAC}.

6. Operation within the t_{RAD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RAD} (Max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (Max.) limit, access time is controlled by t_{AA}.

7. t_{OFF} (Max.) and t_{OEZ} (Max.) define the time at which the output achieves an open circuit condition and are not referenced to output voltage levels.

8. t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. t_{WCS}, t_{CWD}, t_{RWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (Min.) the cycle is an early write cycle and the data output pin will remain in a high impedance state throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (Min.), $t_{RWD} \geq t_{RWD}$ (Min.), $t_{AWD} \geq t_{AWD}$ (Min.) and $t_{CPWD} \geq t_{CPWD}$ (Min.), the cycle is a read modify write cycle and the data output pin will contain data read from the selected cell. If neither conditions is satisfied, the data output logic state (at access time) is undefined.

10. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in an $\overline{OE}$ control write cycle or a read modify write cycle.

11. The test mode is initiated by performing a $\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. This mode is latched and remains in effect until the exit cycle is generated.
    The test mode specified in this data sheet is a 4-bit parallel test function. CA0 and CA1 are not used. In a read cycle, if all internal bits are equal, the DQ pin will indicate a high level. If any internal bits are not equal, the DQ pin will indicate a low level. The test mode is cleared and the memory device returned to its normal operating state by performing a $\overline{RAS}$-only refresh cycle or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.
    The 8M × 36 module can be tested as a 2M × 36 module in this test mode.

12. In a test mode read cycle, the access time parameters are delayed by 5 ns. The test mode parameters are obtained by adding 5 ns to the normal read cycle values.

See ADDENDUM E for AC Timing Waveforms