RC5051

Programmable Synchronous DC-DC Controller for Low Voltage Microprocessors

Features

- Programmable output from 1.3V to 3.5V using an integrated 5-bit DAC
- 85% efficiency typical
- Adjustable operation from 80KHz to 1MHz
- Integrated Power Good and Enable functions
- Overvoltage protection
- Overcurrent protection
- Drives N-channel MOSFETs
- 20 pin SOIC package
- Meets Intel Pentium II specifications using minimum number of external components

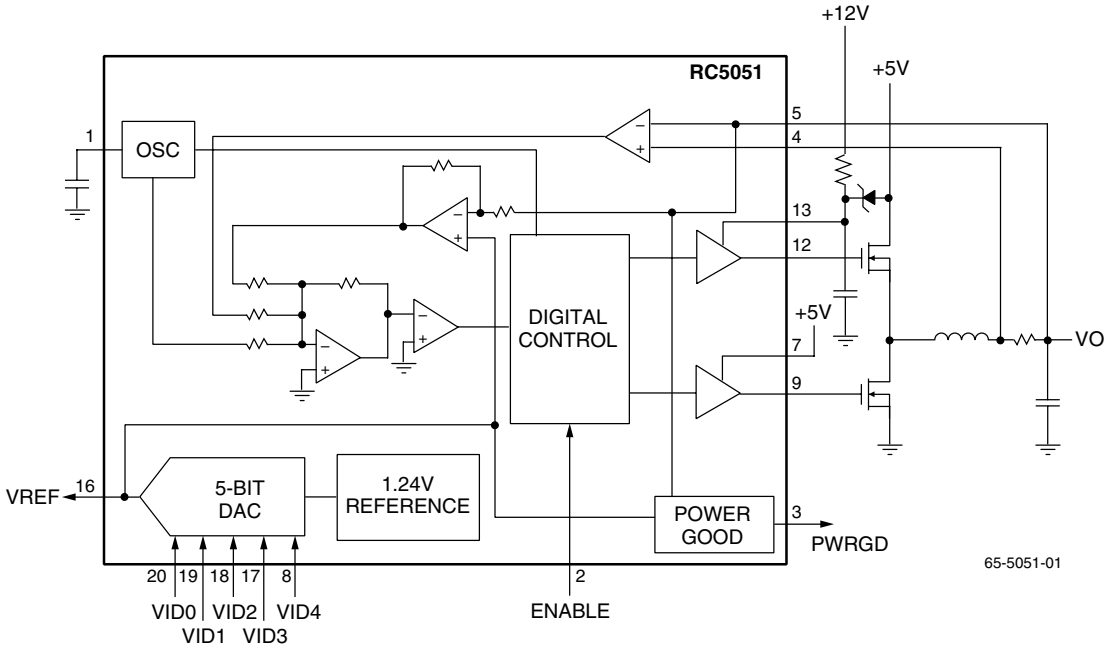
Applications

- Power supply for Pentium® II
- VRM for Pentium II processor
- Programmable step-down power supply

Description

The RC5051 is a synchronous mode DC-DC controller IC which provides an accurate, programmable output voltage for all Pentium II CPU applications. The RC5051 uses a 5-bit D/A converter to program the output voltage from 1.3V to 3.5V. The RC5051 uses a high level of integration to deliver load currents in excess of 19A from a 5V source with minimal external circuitry. Synchronous-mode operation offers optimum efficiency over the entire specified output voltage range, and the internal oscillator can be programmed from 80KHz to 1MHz for additional flexibility in choosing external components. An on-board precision low TC reference achieves tight tolerance voltage regulation without expensive external components. The RC5051 also offers integrated functions including Power Good, Output Enable, over-voltage protection and current limiting.

Block Diagram



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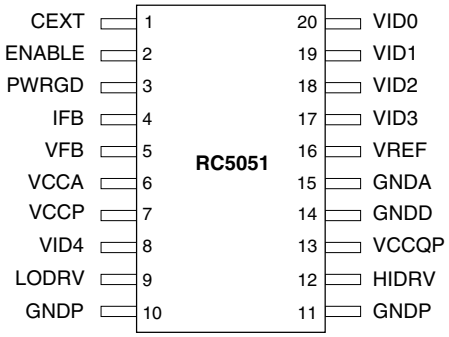
Pin Assignments



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Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	CEXT	**Oscillator Capacitor Connection**. Connecting an external capacitor to this pin sets the internal oscillator frequency. Layout of this pin is critical to system performance. See Application Information for details.
2	ENABLE	**Output Enable**. A logic LOW on this pin will disable the output. An internal pull-up resistor allows for either open collector or TTL compatibility.
3	PWRGD	**Power Good Flag**. An open collector output that will be at logic LOW if the output voltage is not within ±12% of the nominal output voltage setpoint.
4	IFB	**High Side Current Feedback**. Pins 4 and 5 are used as the inputs for the current feedback control loop. Layout of these traces is critical to system performance. See Application Information for details.
5	VFB	**Voltage Feedback**. Pin 5 is used as the input for the voltage feedback control loop and as the low side current feedback input. See Application Information for details regarding correct layout.
6	VCCA	**Analog VCC**. Connect to system 5V supply and decouple with a 0.1µF ceramic capacitor.
7	VCCP	**Power VCC for low side FET driver**. Connect to system 5V supply and place a 1µF ceramic capacitor for decoupling and local charge storage.
8	VID4	**VID4 Input**. A logic 1 on this open collector/TTL input will enable the VID3–VID0 inputs to set the output from 2.1V to 3.5V, and a logic 0 will set the output from 1.3V to 2.05V, as shown in Table 1. Pullup resistors are internal to the controller.
9	LODRV	**Low Side FET Driver**. Connect this pin to the gate of an N-channel MOSFET for synchronous operation. The trace from this pin to the MOSFET gate should be < 0.5".
10, 11	GNDP	**Power Ground**. Return pin for high currents flowing in pins 7 and 13 (VCCP and VCCQP). Connect to a low impedance ground.
12	HIDRV	**High Side FET Driver**. Connect this pin to the gate of an N-channel MOSFET. The trace from this pin to the MOSFET gate should be < 0.5".
13	VCCQP	**Power VCC**. For high side FET driver. VCCQP must be connected to a voltage of at least VCCA + $V_{GS,ON}$ (MOSFET), and place a 1µF ceramic capacitor for decoupling and local charge storage. See Application Information for details
14	GNDD	**Digital Ground**. Return path for digital logic. Connect to a low impedance system ground plane to minimize ground loops.
15	GNDA	**Analog Ground**. Return path for low power analog circuitry. This pin should be connected to a low impedance system ground plane to minimize ground loops.
16	VREF	**Reference Voltage Test point**. This pin provides access to the DAC output and should be decoupled to ground using 0.1µF capacitor. No load should be connected.
17-20	VID0-VID3	**Voltage Identification Code Inputs**. These open collector/TTL compatible inputs will program the output voltage over the ranges specified in Table 1. Pull-up resistors are internal to the controller.

Absolute Maximum Ratings

Supply Voltages, VCCA, VCCP, VCCQP to GND	13V
Supply Voltage VCCQP, Charge Pump (V_{IN}+VCCA)	18V
Voltage Identification Code Inputs, VID4-VID0	13V
Junction Temperature, T_J	150°C
Storage Temperature	-65 to 150°C
Lead Soldering Temperature, 10 seconds	300°C

Operating Conditions

Parameter	Conditions	Min.	Typ.	Max.	Units
Supply Voltage, VCCA, VCCP		4.75	5	5.25	V
Input Logic HIGH		2.0			V
Input Logic LOW				0.8	V
Ambient Operating Temp		0		70	°C
Output Driver Supply, VCCQP		8.5		12	V
PWRGD threshold	Logic High Logic Low	93 88		107 112	%V_{OUT} %V_{OUT}

Electrical Specifications

(V_{CCA} = 5V, V_{OUT} = 2.8V, f_{osc} = 300 KHz, and T_A = +25°C using circuit in Figure 1, unless otherwise noted)
The • denotes specifications which apply over the full operating temperature range.

Parameter	Conditions		Min.	Typ.	Max.	Units
Output Voltage	See Table 1	•	1.3		3.5	V
Output Current				15		A
Initial Voltage Setpoint	I_{LOAD} = 0.8A, V_{OUT} = 2.8V V_{OUT} = 2.0V		2.797 2.000	2.825 2.020	2.853 2.040	V V
Output Temperature Drift	T_A = 0 to 70°C V_{OUT} = 2.8V V_{OUT} = 2.0V	• •		+16 +11		mV mV
Load Regulation	I_{LOAD} = 0.8A to 14.2A	•		-20		mV
Line Regulation	V_{IN} = 4.75V to 5.25V	•		±2		mV
Output Ripple	20MHz BW, I_{LOAD} = 14.2A			±13		mVpk
Total Output Variation Steady State[1]	V_{OUT} = 2.8V V_{OUT} = 2.0V	• •	2.740 1.940		2.900 2.060	V V
Total Output Variation Transient[2]	I_{LOAD} = 0.8 to 14.2A, V_{OUT} = 2.8V V_{OUT} = 2.0V	• •	2.670 1.900		2.930 2.100	V V
Short Circuit Detect Threshold		•	100	120	140	mV
Efficiency	I_{LOAD} = 14.2A, V_{OUT} = 2.8V	•		82		%
Output Driver Rise and Fall Time	See Figure 2			80		nsec
Output Driver Deadtime 1	See Figure 2			5		%/f_{OSC}
Output Driver Deadtime 2	See Figure 2			80		nsec
Turn-on Response Time	I_{LOAD} = 0A to 14.2A				10	msec
Oscillator Range			80		1000	KHz
Oscillator Frequency	C_{EXT} = 100 pF		270	300	330	KHz
Max Duty Cycle			90	95		%

Notes:

1. Steady Date Voltage Regulation includes Initial Voltage Setpoint, Load Regulation, Output Ripple and Output Temperature Drift and is measured at the converter's output capacitors.
2. As measured at the converter's output capacitors. For motherboard applications, the PCB layout should exhibit no more than 0.5mΩ trace resistance between the converter's output capacitors and the CPU.

Table 1. Output Voltage Programming Codes

VID4	VID3	VID2	VID1	VID0	V_{OUT} to CPU
0	1	1	1	1	1.30V
0	1	1	1	0	1.35V
0	1	1	0	1	1.40V
0	1	1	0	0	1.45V
0	1	0	1	1	1.50V
0	1	0	1	0	1.55V
0	1	0	0	1	1.60V
0	1	0	0	0	1.65V
0	0	1	1	1	1.70V
0	0	1	1	0	1.75V
0	0	1	0	1	1.80V
0	0	1	0	0	1.85V
0	0	0	1	1	1.90V
0	0	0	1	0	1.95V
0	0	0	0	1	2.00V
0	0	0	0	0	2.05V
1	1	1	1	1	No CPU
1	1	1	1	0	2.1V
1	1	1	0	1	2.2V
1	1	1	0	0	2.3V
1	1	0	1	1	2.4V
1	1	0	1	0	2.5V
1	1	0	0	1	2.6V
1	1	0	0	0	2.7V
1	0	1	1	1	2.8V
1	0	1	1	0	2.9V
1	0	1	0	1	3.0V
1	0	1	0	0	3.1V
1	0	0	1	1	3.2V
1	0	0	1	0	3.3V
1	0	0	0	1	3.4V
1	0	0	0	0	3.5V

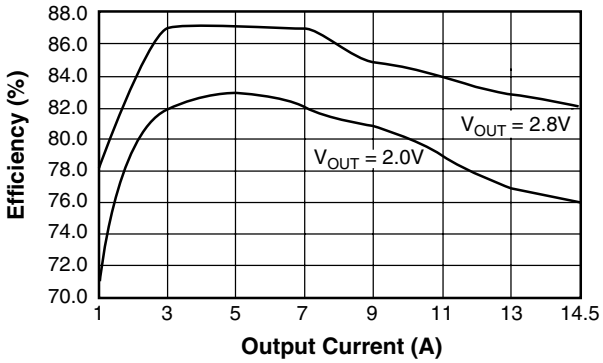
Note:

1. 0 = processor pin is tied to GND.
   1 = processor pin is open.

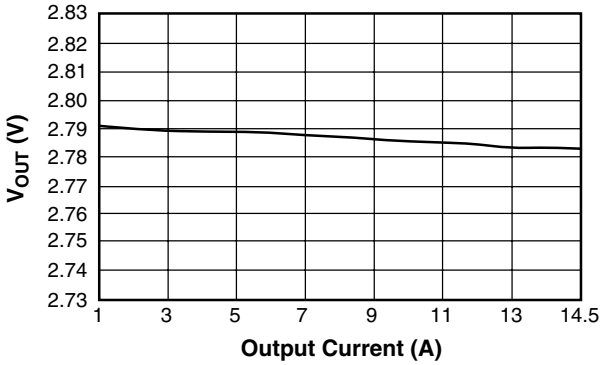
Typical Operating Characteristics

(VCCA, VCCD = 5V, f_{OSC} = 280 KHz, and T_A = +25°C using circuit in Figure 1, unless otherwise noted)

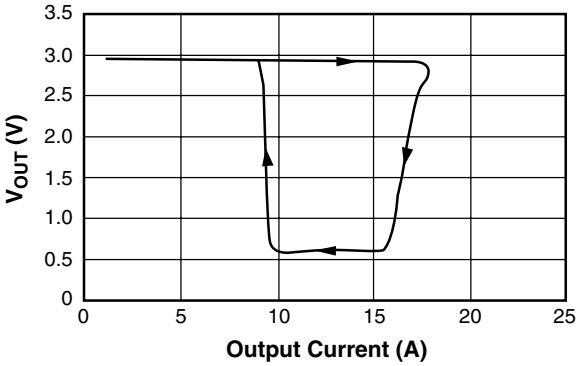
Efficiency vs. Output Current



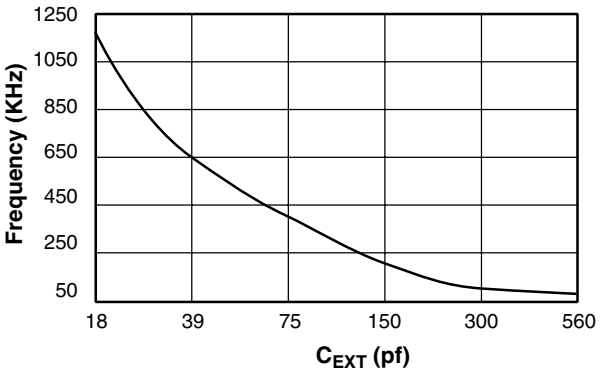
Load Regulation, V_{OUT} = 2.8 V



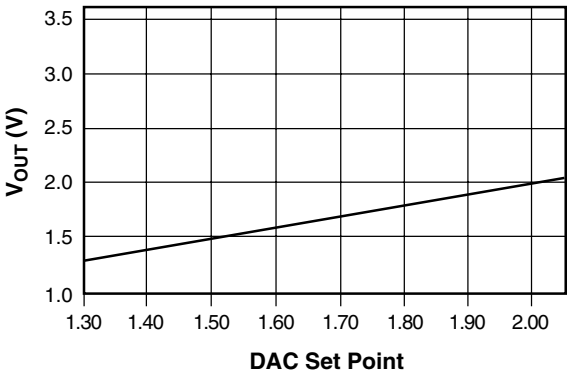
Output Voltage vs. Output Current, R_{SENSE} = 6mΩ



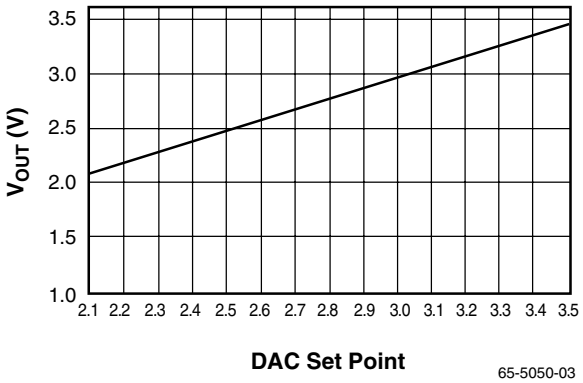
Oscillator Frequency vs. C_{EXT}



Output Programming, VID4 = 0



Output Programming, VID4 = 1



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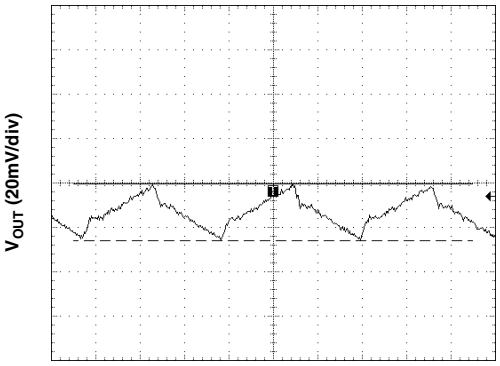
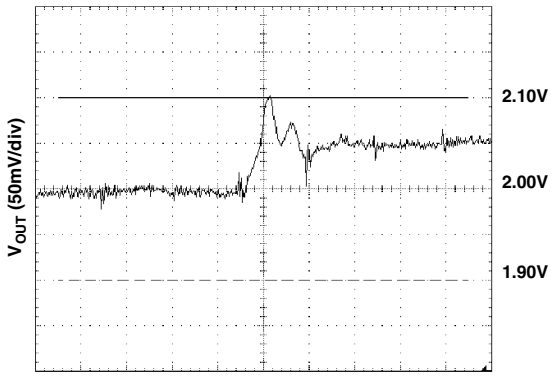
Typical Operating Characteristics (continued)

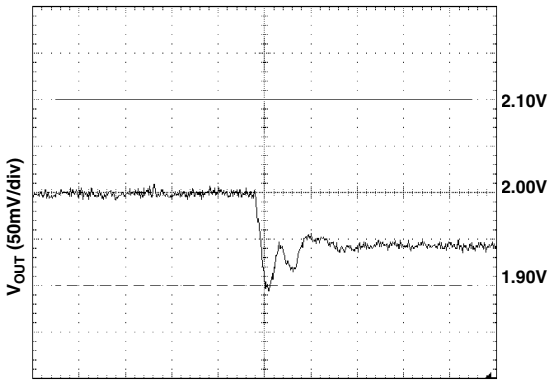
Output Ripple, 2.8V @ 14.2A



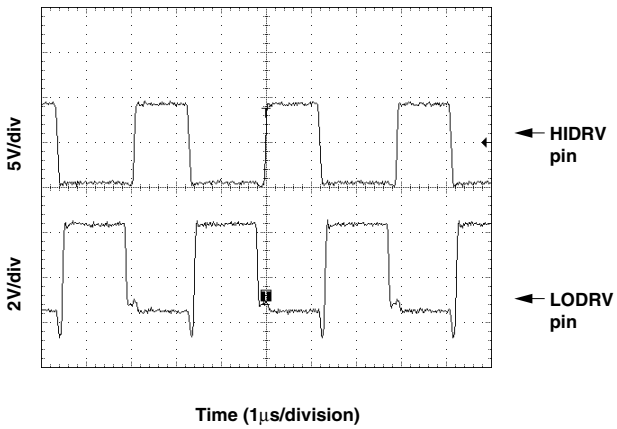
Transient Response, 14.2A to 0.8A



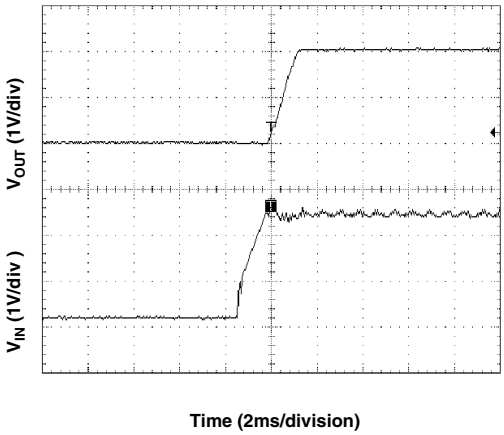
Transient Response, 0.8A to 14.2A



Switching Waveforms, 9A Load



Output Startup, System Power-up



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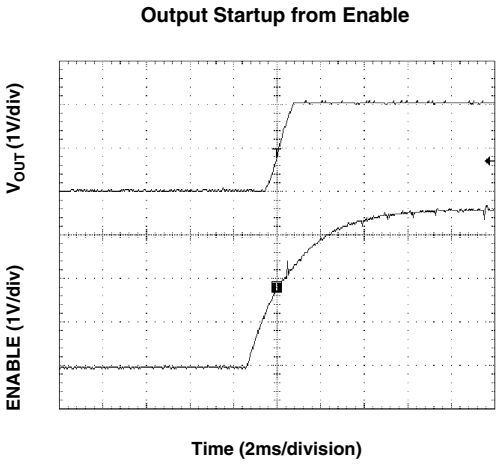
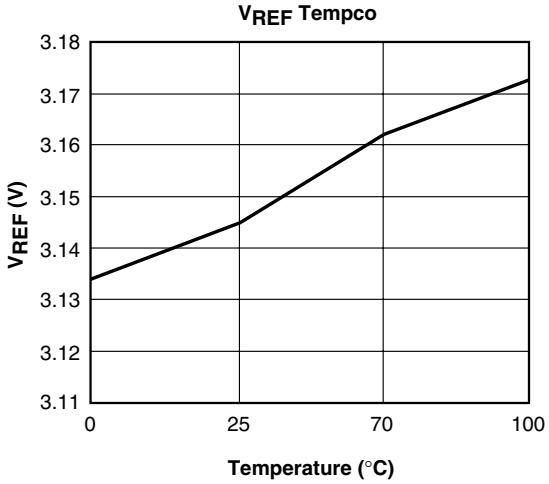
Typical Operating Characteristics (continued)





Application Circuit

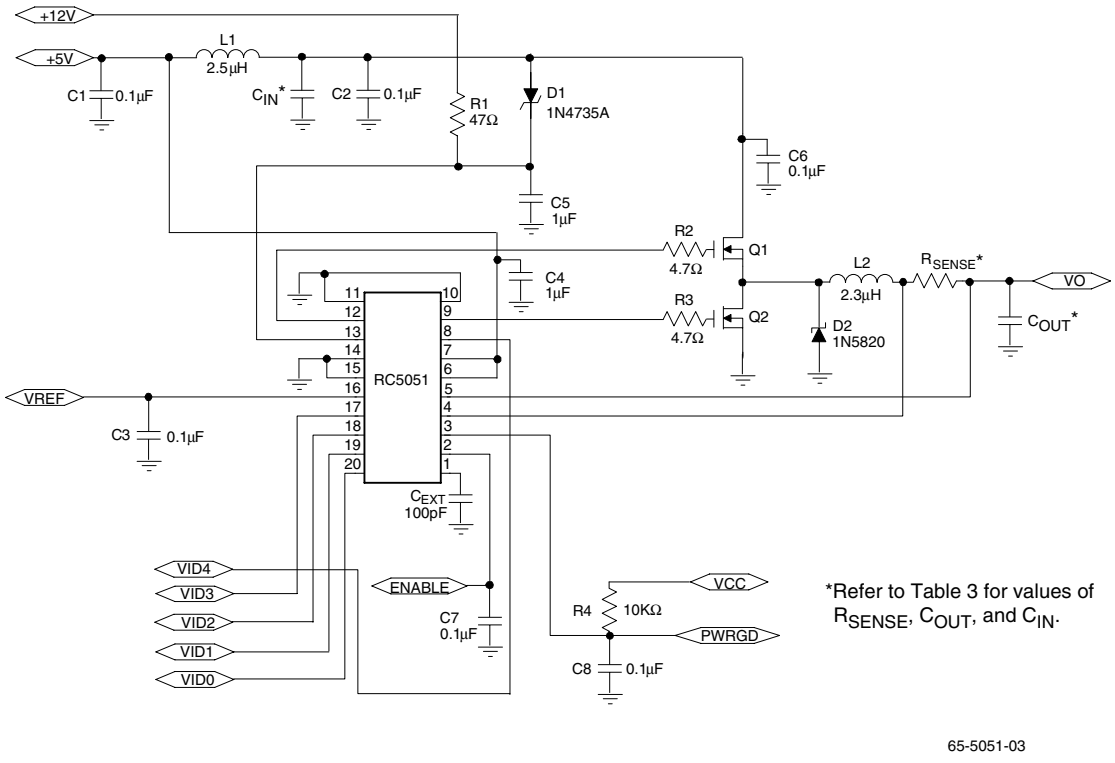


Figure 1. 15A Application Circuit for Pentium II Processors

Table 2. RC5051 Application Bill of Materials for Intel Pentium II Processors

Reference	Manufacturer Part #	Quantity	Description	Requirements/Comments
C1–3, C6–C8	Panasonic ECU-V1H104ZFX	6	100nF, 50V Capacitor	
C4–5	Panasonic ECU-V1C105ZFX	2	1µF, 16V Capacitor	
C_{ext}	Panasonic ECU-V1H101JCG	1	100pF Capacitor	5%, C0G
C_{IN}	Sanyo 10MV1200GX	*	1200µF, 10V Electrolytic	I_{RMS} = 2A
C_{OUT}	Sanyo 6MV1500GX	*	1500µF, 6.3V Electrolytic	ESR < 44mΩ
D1	Motorola 1N4735A	1	6.2V Zener Diode	
D2	Motorola 1N5820	1	3A Schottky Diode	
L1	Skynet 320-6110	1	2.5µH, 11A Inductor	DCR ~ 6mΩ See Note 1.
L2	Any	1	2.3µH, 15A inductor	DCR ~ 3mΩ
Q1–2	Fairchild FDP6030L or FDB6030L	2	N-Channel MOSFET (TO-220 or TO-263)	$R_{DS(ON)}$ = 20mΩ @ V_{GS} = 4.5V See Note 2
R1	Any	1	47Ω	
R2-3	Any	2	4.7Ω	
R4	Any	1	10KΩ	
R_{SENSE}	Fairchild RC10-XX*	1	CuNi Alloy Wire Resistor	
U1	Fairchild RC5051M	1	DC/DC Controller	

* See Table 3.

Notes:

1. Inductor L1 is recommended to isolate the 5V input supply from noise generated by the MOSFET switching, and to comply with Intel dI/dt requirements. L1 may be omitted if desired.
2. For 14.2A designs using the FDP6030L MOSFETs, heatsinks with thermal resistance Θ_{SA} < 20°C/W should be used. For details and a spreadsheet on MOSFET selections, refer to Applications Bulletin AB-8.

Table 3. Recommended Values for CPU-based Applications

Application	Output Current	C_{IN}	C_{OUT}*	C_{OUT} Maximum ESR*	R_{SENSE}
300MHz AMD K6 Motherboard	13A	3 x 1200µF, 10V Sanyo 10MV1200GX	2 x 1500µF, 6.3V Sanyo 6MV1500GX	6.1mΩ	5.8mΩ
300 MHz Intel Pentium Motherboard	14.2A	3 x 1200µF, 10V Sanyo 10MV1200GX	7 x 1500µF, 6.3V Sanyo 6MV1500GX	6.8mΩ	5.2mΩ
400MHz Intel Pentium II Motherboard	12.6A	3 x 1200µF, 10V Sanyo 10MV1200GX	7 x 1500µF, 6.3V Sanyo 6MV1500GX	6.3mΩ	5.8mΩ

* Output capacitance and ESR requirements depend critically on layout and processor type. Consult Application Bulletin AB-14 for details

Test Circuit

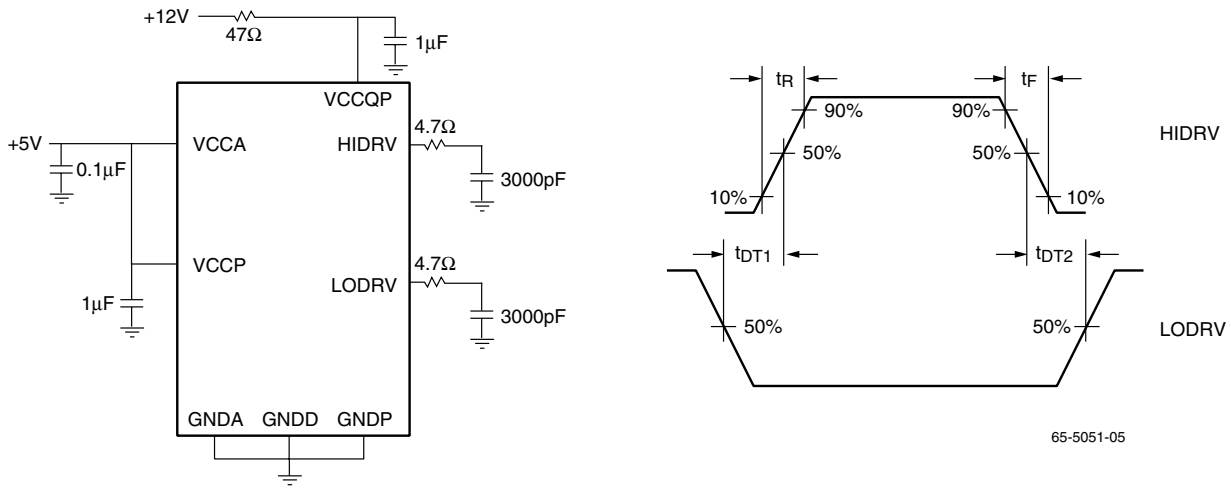


Figure 2. Output Drive Test Circuit and Timing Diagram

Application Information

The RC5051 Controller

The RC5051 is a programmable synchronous DC-DC controller IC. When designed around the appropriate external components, the RC5051 can be configured to deliver more than 19A of output current, as appropriate for the Klamath and Deschutes and other processors. The RC5051 functions as a fixed frequency PWM step down regulator.

Main Control Loop

Refer to the RC5051 Block Diagram on page 1. The RC5051 implements “summing mode control”, which is different from both classical voltage-mode and current-mode control. It provides superior performance to either by allowing a large converter bandwidth over a wide range of output loads.

The control loop of the regulator contains two main sections: the analog control block and the digital control block. The analog section consists of signal conditioning amplifiers feeding into a set of comparators which provide the inputs to the digital control block. The signal conditioning section accepts inputs from the IFB (current feedback) and VFB (voltage feedback) pins and sets up two controlling signal paths. The first, the voltage control path, amplifies the difference between the VFB signal the reference voltage from the DAC and presents the output to one of the summing amplifier inputs. The second, current control path, takes the difference between the IFB and VFB pins and presents the resulting signal to another input of the summing amplifier. These two signals are then summed together with the slope compensation input from the oscillator. This output is then presented to a comparator, which provides the main PWM control signal to the digital control block.

The digital control block takes the analog comparator inputs and the main clock signal from the oscillator to provide the appropriate pulses to the HIDRV and LODRV output pins. These two outputs control the external power MOSFETs. The digital block utilizes high speed Schottky transistor logic, allowing the RC5051 to operate at clock speeds as high as 1MHz.

There are additional comparators in the analog control section whose function is to set the point at which the RC5051 enters its pulse skipping mode during light loads, as well as the point at which the current limit comparator disables the output drive signals to the external power MOSFETs.

High Current Output Drivers

The RC5051 contains two identical high current output drivers that utilize high speed bipolar transistors in a push-pull configuration. The drivers’ power and ground are separated from the chip’s power and ground for switching noise immunity. The HIDRV driver has a power supply pin, VCCQP, which is supplied from an external 12V source through a series resistor or from a charge-pump circuit powered from 5V if 12V is not available. The LODRV driver has a power supply pin, VCCP, which can be supplied from either the 12V or 5V source. The resulting voltages are sufficient to provide the gate to source drive to the external MOSFETs required in order to achieve a low $R_{DS,ON}$.

Internal Voltage Reference

The reference included in the RC5051 is a precision bandgap voltage reference. Its internal resistors are precisely trimmed to provide a near zero temperature coefficient (TC). Based on the reference is the output from an integrated 5-bit DAC. The DAC monitors the 5 voltage identification pins, VID0–VID4. When the VID4 pin is at logic HIGH, the DAC scales the reference voltage from 2.0V to 3.5V in 100mV increments. When VID4 is pulled LOW, the DAC scales the reference from 1.30V to 2.05V in 50mV increments. All VID codes are available, including those below 1.80V. For guaranteed stable operation under all loading conditions, 0.1µF of decoupling capacitance should be connected to the VREF pin. No load should be connected to VREF.

Power Good (PWRGD)

The RC5051 Power Good function is designed in accordance with the Pentium II DC-DC converter specifications and provides a continuous voltage monitor on the VFB pin. The circuit compares the VFB signal to the VREF voltage and outputs an active-low interrupt signal to the CPU should the power supply voltage deviate more than ±12% of its nominal setpoint. The Power Good flag provides no other control function to the RC5051.

Output Enable (ENABLE)

The RC5051 will accept an open collector/TTL signal for controlling the output voltage. The low state disables the output voltage. When disabled, the PWRGD output is in the low state. If an enable is not required in the circuit, this pin may be left open.

Over-Voltage Protection

The RC5051 constantly monitors the output voltage for protection against over voltage conditions. If the voltage at the VFB pin exceeds 20% of the selected program voltage, an over-voltage condition is assumed and the RC5051 disables the output drive signal to the external MOSFETs. The DC-DC converter returns to normal operation after the fault has been removed.

Over-Current Protection

Current sense is implemented in the RC5051 to reduce the duty cycle of the output drive signal to the MOSFETs when an over-current condition is detected. The voltage drop created by the output current flowing across a sense resistor is presented to an internal comparator. When the voltage

developed across the sense resistor exceeds the 120mV comparator threshold voltage, the RC5051 reduces the output duty cycle to help protect the power devices. The DC-DC converter returns to normal operation after the fault has been removed.

Oscillator

The RC5051 oscillator section uses a fixed current capacitor charging configuration. An external capacitor (CEXT) is used to set the oscillator frequency between 80KHz and 1MHz. This scheme allows maximum flexibility in choosing external components.

In general, a higher operating frequency decreases the peak ripple current flowing in the output inductor, thus allowing the use of a smaller inductor value. In addition, operation at higher frequencies decreases the amount of energy storage that must be provided by the bulk output capacitors during load transients due to faster loop response of the controller.

Unfortunately, the efficiency losses due to switching of the MOSFETs increase as the operating frequency is increased. Thus, efficiency is optimized at lower frequencies. An operating frequency of 300KHz is a typical choice which optimizes efficiency and minimizes component size while maintaining excellent regulation and transient performance under all operating conditions.

Design Considerations and Component Selection

Additional information on design and component selection may be found in Fairchild Semiconductor's Application Note 53.

MOSFET Selection

This application requires N-channel Logic Level Enhancement Mode Field Effect Transistors. Desired characteristics are as follows:

- Low Static Drain-Source On-Resistance, $R_{DS,ON}$ < 20mΩ (lower is better)
- Low gate drive voltage, V_{GS} = 4.5V rated
- Power package with low Thermal Resistance
- Drain-Source voltage rating > 15V.

The on-resistance ($R_{DS,ON}$) is the primary parameter for MOSFET selection. The on-resistance determines the power dissipation within the MOSFET and therefore significantly affects the efficiency of the DC-DC Converter. For details and a spreadsheet on MOSFET selection, refer to Applications Bulletin AB-8

MOSFET Gate Bias

The high side MOSFET gate driver can be biased by one of two methods–Charge Pump or 12V Gate Bias. The charge pump method has the advantage of requiring only +5V as an input voltage to the converter, but the 12V method will realize increased efficiency by providing an increased V_{GS} to the high side MOSFETs.

Method 1. Charge Pump (Bootstrap)

Figure 3 shows the use of a charge pump to provide gate bias to the high side MOSFET when +12V is unavailable. Capacitor CP is the charge pump used to boost the voltage of the RC5051 output driver. When the MOSFET Q1 switches off, the source of the MOSFET is at approximately 0V because of the MOSFET Q2. (The Schottky D2 conducts for only a very short time, and is not relevent to this discussion.) CP is charged through the Schottky diode D1 to approximately 4.5V. When the MOSFET Q1 turns on, the voltage at the source of the MOSFET is equal to 5V. The capacitor voltage follows, and hence provides a voltage at VCCQP equal to almost 10V. The Schottky diode D1 is required to provide the charge path when the MOSFET is off, and reverses biases when VCCQP goes to 10V. The charge pump capacitor (CP) needs to be a high Q, high frequency capacitor. A 1µF ceramic capacitor is recommended here.

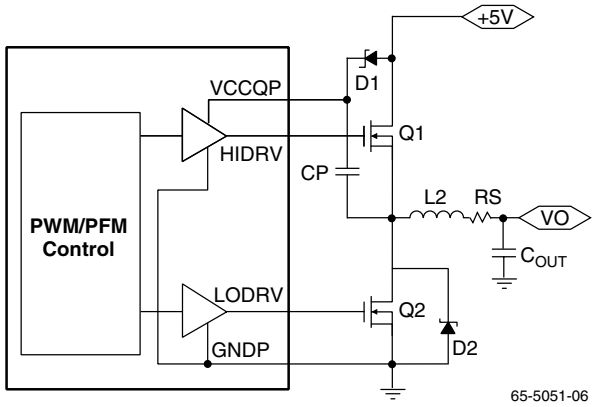


Figure 3. Charge Pump Configuration

Method 2. 12V Gate Bias

Figure 4 illustrates how a 12V source can be used to bias VCCQP. A 47Ω resistor is used to limit the transient current into the VCCQP pin and a 1µF capacitor is used to filter the VCCQP supply. This method provides a higher gate bias voltage (V_{GS}) to the high side MOSFET than the charge pump method, and therefore reduces the $R_{DS,ON}$ and the resulting power loss within the MOSFET. In designs where efficiency is a primary concern, the 12V gate bias method is recommended. A 6.2V Zener diode, D1, is used to clamp the voltage at VCCQP to a maximum of 12V and ensure that the absolute maximum voltage of the IC will not be exceeded.

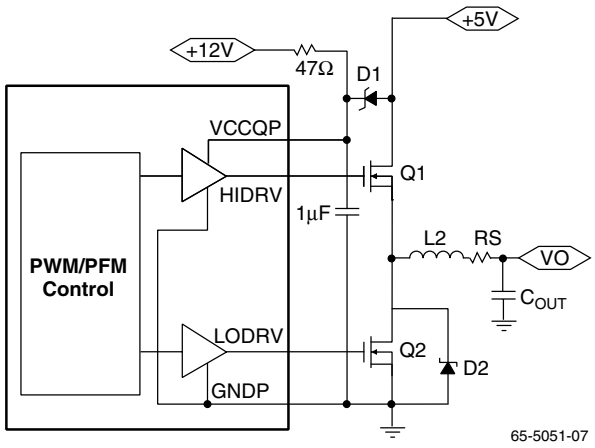


Figure 4. Gate Bias Configuration

Inductor Selection

Choosing the value of the inductor is a tradeoff between allowable ripple voltage and required transient response. The system designer can choose any value within the allowed minimum to maximum range in order to either minimize ripple or maximize transient performance. The first order equation (close approximation) for minimum inductance is:

$$L_{min} = \frac{(V_{in} - V_{out})}{f} \times \frac{V_{out}}{V_{in}} \times \frac{ESR}{V_{ripple}}$$

where:

V_{in} = Input Power Supply
V_{out} = Output Voltage
f = DC/DC converter switching frequency
ESR = Equivalent series resistance of all output capacitors in parallel
V_{ripple} = Maximum peak to peak output ripple voltage budget.

The first order equation for maximum allowed inductance is:

$$L_{max} = 2C_O \times \frac{(V_{in} - V_{out})D_m V_{tb}}{I_{PP}^2}$$

where:

C_o = The total output capacitance
I_{pp} = Maximum to minimum load transient current
V_{tb} = The output voltage tolerance budget allocated to load transient
D_m = Maximum duty cycle for the DC/DC converter (usually 95%).

Some margin should be maintained away from both L_{min} and L_{max}. Adding margin by increasing L almost always adds expense since all the variables are predetermined by system performance except for C_o, which must be increased to increase L. Adding margin by decreasing L can either be done by purchasing capacitors with lower ESR or by increasing the DC/DC converter switching frequency. The RC5051 is capable of running at high switching frequencies and provides significant cost savings for the newer CPU systems that typically run at high supply current.

RC5051 Short Circuit Current Characteristics

The RC5051 short circuit current characteristic includes a hysteresis function that prevents the DC-DC converter from oscillating in the event of a short circuit. Figure 5 shows the typical characteristic of the DC-DC converter circuit with a 6.8 mΩ sense resistor. The converter exhibits a normal load regulation characteristic until the voltage across the resistor exceeds the internal short circuit threshold of 120mV (= 17.5A * 6.8mΩ). At this point, the internal comparator trips and signals the controller to reduce the converter's duty cycle to approximately 20%. This causes a drastic reduction in the output voltage as the load regulation collapses into the short circuit control mode. With a 40mΩ output short, the voltage is reduced to 15A * 40mΩ = 600mV. The output voltage does not return to its nominal value until the output current is reduced to a value within the safe operating range for the DC-DC converter.

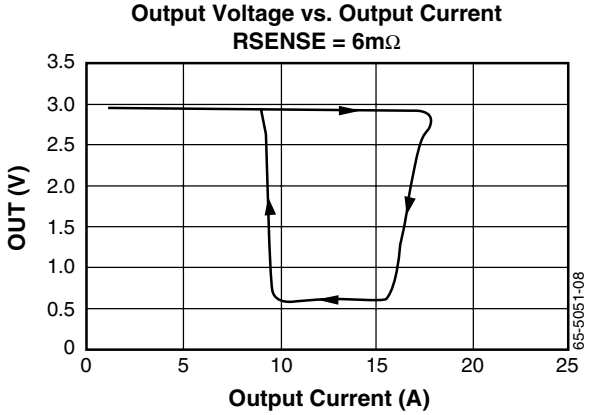


Figure 5. RC5051 Short Circuit Characteristic

Schottky Diode Selection

The application circuit of Figure 1 shows a Schottky diode, D2, which is used as a free-wheeling diode to assure that the body-diode in Q2 does not conduct when the upper MOSFET is turning off and the lower MOSFET is turning on. It is undesirable for this diode to conduct because its high forward voltage drop and long reverse recovery time degrades efficiency, and so the Schottky provides a shunt path for the current. Since this time duration is very short, the selection criterion for the diode is that the forward voltage of the Schottky at the output current should be less than the forward voltage of the MOSFET's body diode.

Output Filter Capacitors

The output bulk capacitors of a converter help determine its output ripple voltage and its transient response. It has already been seen in the section on selecting an inductor that the ESR helps set the minimum inductance, and the capacitance value helps set the maximum inductance. For most converters, however, the number of capacitors required is

determined by the transient response and the output ripple voltage, and these are determined by the ESR and not the capacitance value. That is, in order to achieve the necessary ESR to meet the transient and ripple requirements, the capacitance value required is already very large.

The most commonly used choice for output bulk capacitors is aluminum electrolytics, because of their low cost and low ESR. The only type of aluminum capacitor used should be those that have an ESR rated at 100kHz. Consult Application Bulletin AB-14 for detailed information on output capacitor selection.

The output capacitance should also include a number of small value ceramic capacitors placed as close as possible to the processor; 0.1µF and 0.01µF are recommended values.

Input Filter

The DC-DC converter design may include an input inductor between the system +5V supply and the converter input as shown in Figure 6. This inductor serves to isolate the +5V supply from the noise in the switching portion of the DC-DC converter, and to limit the inrush current into the input capacitors during power up. A value of 2.5µH is recommended.

It is necessary to have some low ESR aluminum electrolytic capacitors at the input to the converter. These capacitors deliver current when the high side MOSFET switches on. Figure 6 shows 3 x 1000µF, but the exact number required will vary with the speed and type of the processor. For the top speed Klamath and Deschutes, the capacitors should be rated to take 7A of ripple current. Capacitor ripple current rating is a function of temperature, and so the manufacturer should be contacted to find out the ripple current rating at the expected operational temperature. For details on the design of an input filter, refer to Applications Bulletin AB-15.

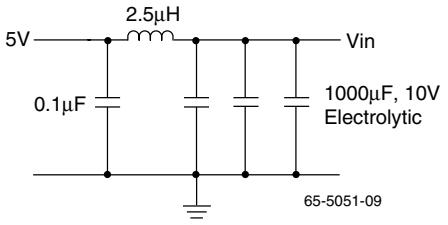


Figure 6. Input Filter

Droop Resistor

Figure 7 shows a converter using a “droop resistor”, R_D. The function of the droop resistor is to improve the transient response of the converter, potentially reducing the number of output capacitors required. In operation, the droop resistor causes the output voltage to be slightly lower at heavy load current than it otherwise would be. When the load transitions from heavy to light current, the output can swing up farther without exceeding limits, because it started from a lower voltage, thus reducing the capacitor requirements.

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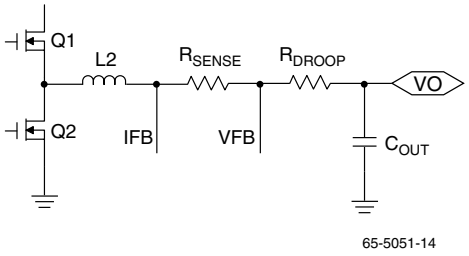


Figure 7. Use of a Droop Resistor

PCB Layout Guidelines

- Placement of the MOSFETs relative to the RC5051 is critical. Place the MOSFETs such that the trace length of the HIDRV and LODRV pins of the RC5051 to the FET gates is minimized. A long lead length on these pins will cause high amounts of ringing due to the inductance of the trace and the gate capacitance of the FET. This noise radiates throughout the board, and, because it is switching at such a high voltage and frequency, it is very difficult to suppress.
- In general, all of the noisy switching lines should be kept away from the quiet analog section of the RC5051. That is, traces that connect to pins 9, 12, and 13 (LODRV, HIDRV and VCCQP) should be kept far away from the traces that connect to pins 1 through 5, and pin 16.
- Place the 0.1µF decoupling capacitors as close to the RC5051 pins as possible. Extra lead length on these reduces their ability to suppress noise.
- Each VCC and GND pin should have its own via to the appropriate plane. This helps provide isolation between pins.
- Surround the CEXT timing capacitor with a ground trace. Be sure to place a ground or power plane underneath the capacitor for further noise isolation, in order to provide additional shielding to the oscillator (pin 1) from the noise on the PCB. In addition, place this capacitor as close to pin 1 as possible.
- Place the MOSFETs, inductor, and Schottky as close together as possible for the same reasons as in the first bullet above. Place the input bulk capacitors as close to the drains of the high side MOSFETs as possible. In addition, placement of a 0.1µF decoupling cap right on the drain of each high side MOSFET helps to suppress some of the high frequency switching noise on the input of the DC-DC converter.
- Place the output bulk capacitors as close to the CPU as possible to optimize their ability to supply instantaneous current to the load in the event of a current transient. Additional space between the output capacitors and the CPU will allow the parasitic resistance of the board traces to degrade the DC-DC converter’s performance under severe load transient conditions, causing higher voltage deviation. For more detailed information regarding capacitor placement, refer to Application Bulletin AB-5.

- The traces that run from the RC5051 IFB (pin 4) and VFB (pin 5) pins should be run together next to each other and Kelvin connected to the sense resistor. Running these lines together rejects some of the common mode noise that is presented to the RC5051 feedback input. Try, as much as possible, to run the noisy switching signals (HIDRV, LODRV & VCCQP) on one layer, but use the inner layers for power and ground only. If the top layer is being used to route all of the noisy switching signals, use the bottom layer to route the analog sensing sign VFB and IFB.
- A PC Board Layout Checklist is available from Fairchild Applications. Ask for Application Bulletin AB-11.

PC Motherboard Sample Layout and Gerber File

A reference design for motherboard implementation of the RC5051 along with the PCAD layout Gerber file and silk screen can be obtained from our marketing department at 650-968-9211 x 7833.

RC5051 Evaluation Board

Fairchild Semiconductor provides an evaluation board to verify the system level performance of the RC5051. It serves as a guide to performance expectations when using the supplied external components and PCB layout. Please call the marketing department at 650-968-9211 x 7833 for an evaluation board.

Additional Information

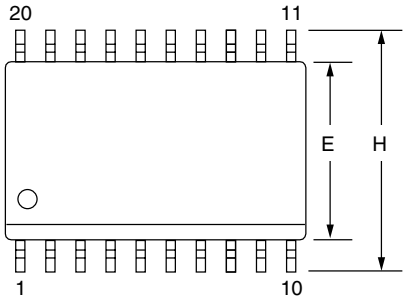
For additional information contact the Fairchild Semiconductor's Analog & Mixed Signal Products Group Marketing Department at 650-968-9211 x 7833.

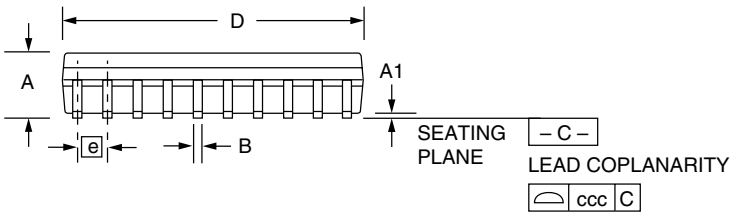
Mechanical Dimensions – 20 Lead SOIC

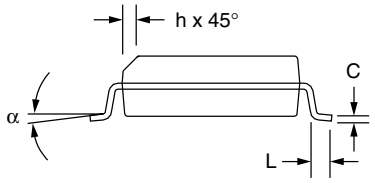
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.093	.104	2.35	2.65	
A1	.004	.012	0.10	0.30	
B	.013	.020	0.33	0.51	
C	.009	.013	0.23	0.32	5
D	.496	.512	12.60	13.00	2
E	.291	.299	7.40	7.60	2
e	.050 BSC		1.27 BSC		
H	.394	.419	10.00	10.65	
h	.010	.029	0.25	0.75	
L	.016	.050	0.40	1.27	3
N	20		20		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Ordering Information

Product Number	Package
RC5051M	20 pin SOIC

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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