

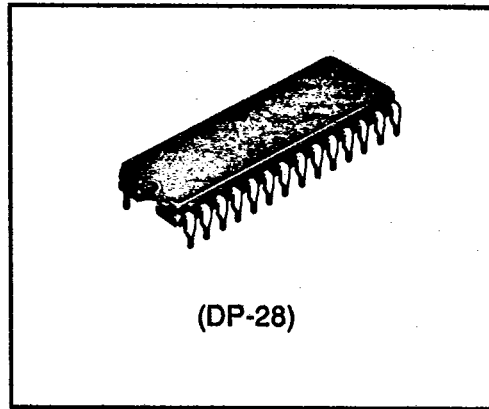
# HD44007A

T-77-17

Sync Signal Generator for TV Cameras (NTSC, PAL/SECAM)

## Functions

- Four times chroma sub-carrier oscillator frequency
- (B-Y) and (R-Y) chroma sub-carrier output circuit
- Active filter genlock phase detector
- Horizontal programmable logic array
- Vertical programmable logic array
- Horizontal/vertical programmable logic array



## Ordering Information

Type No.	Package
HD44007A	DP-28



HD44007A

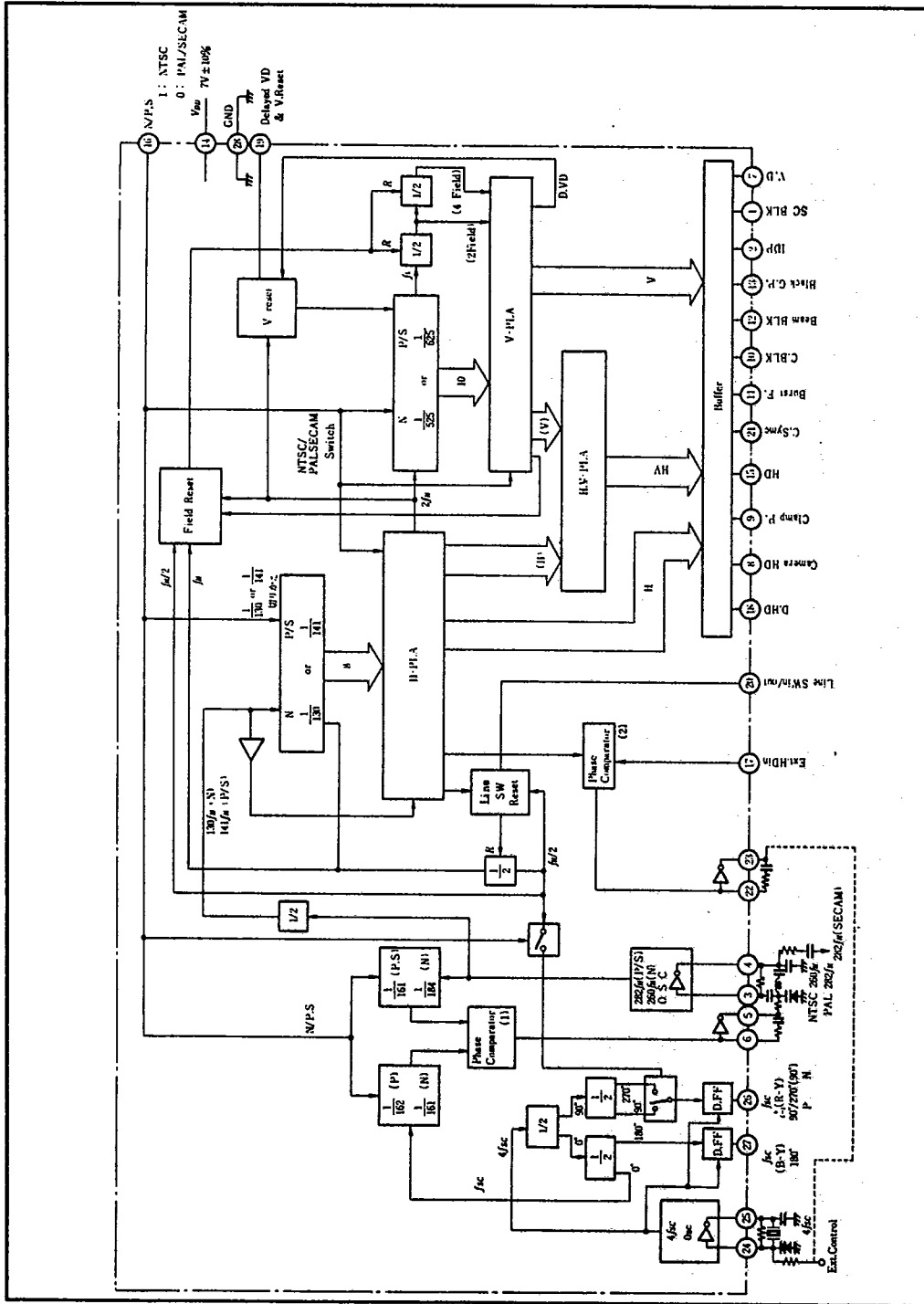
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## Pin Description

Pin No.	Function	Note	Max Output Current
1	SC. BLK	Identification pulse for SECAM	+250 $\mu$ A
2	ID. P	Identification pulse for SECAM	+250 $\mu$ A
3	260 $f_H$ /282 $f_H$ osc	In	
4	260 $f_H$ /282 $f_H$ osc	Out	
5	Filter	Out	
6	Filter	In	
7	VD		$\pm$ 250 $\mu$ A
8	Camera HD		$\pm$ 500 $\mu$ A
9	Clamp P		$\pm$ 500 $\mu$ A
10	Composite BLK		$\pm$ 500 $\mu$ A
11	Burst flag P		$\pm$ 100 $\mu$ A
12	Beam BLK		$\pm$ 500 $\mu$ A
13	Black gate P		$\pm$ 500 $\mu$ A
14	V <sub>DD</sub>	6.3 V to 7.0 V, typ 7.7 V	
15	HD		$\pm$ 500 $\mu$ A
16	Selector input	High level for NTSC, low level for PAL and SECAM	
17	External HD in	H genlock input	
18	Delayed HD		$\pm$ 500 $\mu$ A
19	Delayed VD in/out	In/out, output: V <sub>OH</sub> $\geq$ 0.8 V <sub>DD</sub> , V <sub>OL</sub> = 0.5 V <sub>DD</sub> , input threshold 0.25 V <sub>DD</sub>	-500 $\mu$ A
20	Line SW in/out	In/out, pull-up resistor built-in	+250 $\mu$ A
21	Composite Sync		
22	Filter	In	
23	Filter	Out	
24	4 $f_{SC}$ osc	In	
25	4 $f_{SC}$ osc	Out	
26	SC (90°/270°)	For NTSC, 90° only (high level at pin 16)	$\pm$ 100 $\mu$ A
27	SC (180°)		$\pm$ 100 $\mu$ A
28	GND		



Block Diagram



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Operations

Interleave (external HS input, pin 17 and phase comparator 2 are not used.) See figures 1 and 2.

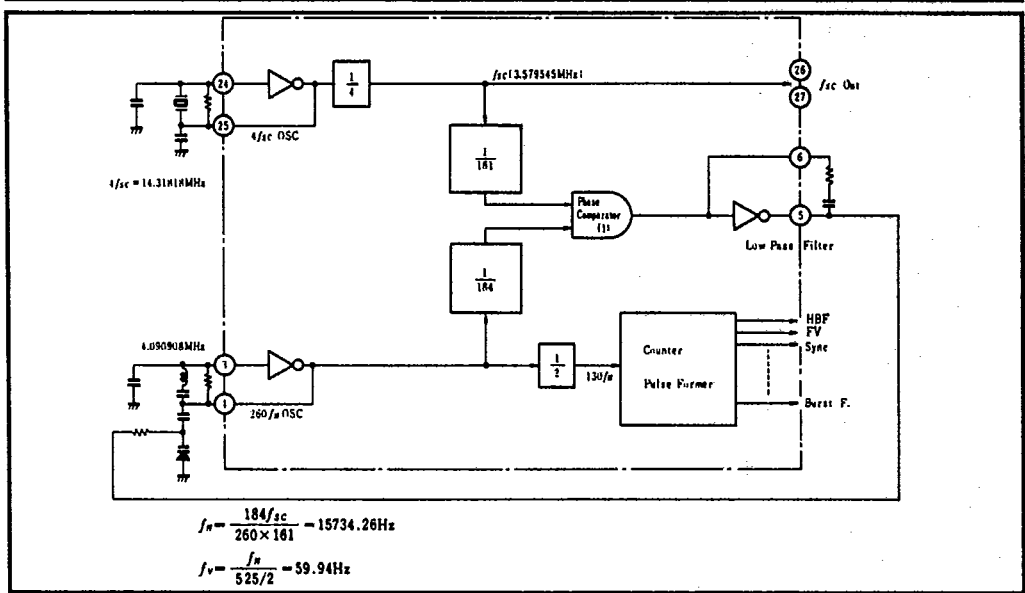


Figure 1 NTSC

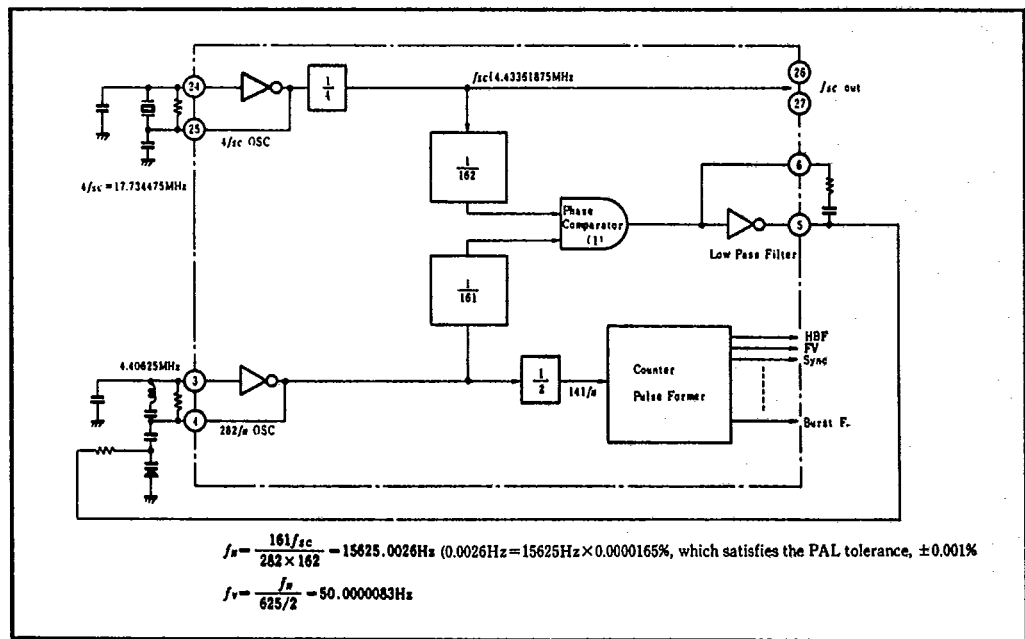


Figure 2 PAL, SECAM



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**Genlock**

In genlock mode, the operating principles of NTSC and PAL/SECAM are the same, so only NTSC is described below. See figure 3. Phase comparator 1 is not used. See figure 4.

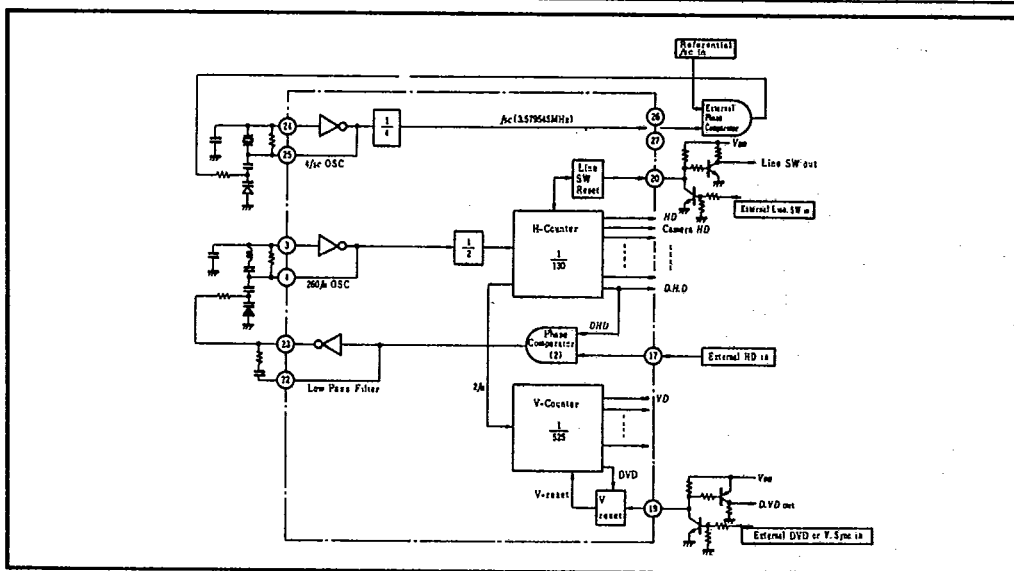
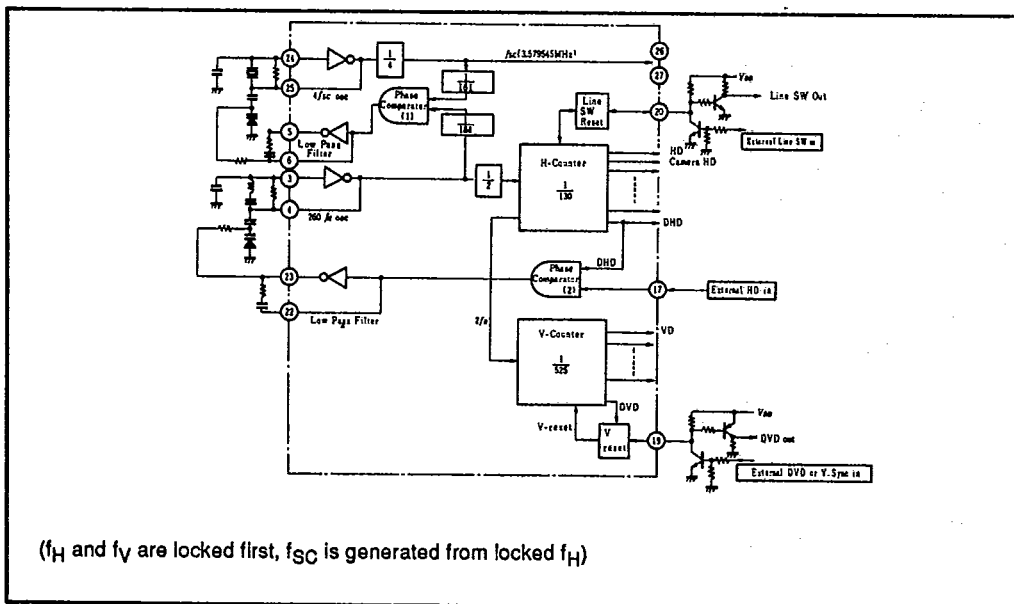


Figure 3 Genlock in Color Cameras



( $f_H$  and  $f_V$  are locked first,  $f_{SC}$  is generated from locked  $f_H$ )

Figure 4 Genlock in B/W Cameras



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**Special Input/Output Terminals**

Pin 20 is for line SW input and output (figure 5). Figure 6 shows the internal circuit and IC operation. The LC oscillator uses a CMOS inverter and crystal oscillator. There is no internal DC

feedback resistor, so an external resistor for feedback should be connected, as in figure 7.

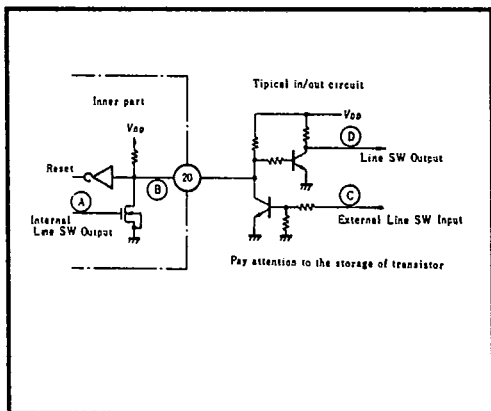


Figure 5 Pin 20 (Line SW In/Out)

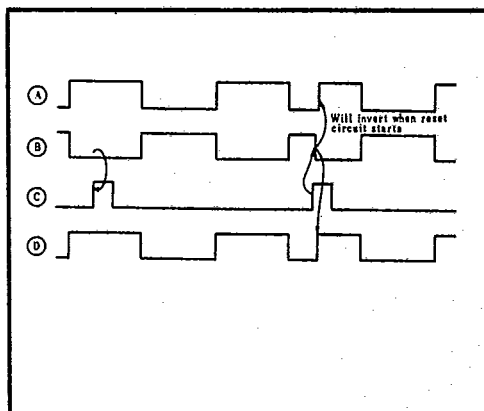


Figure 6 Internal Circuit and IC Operation

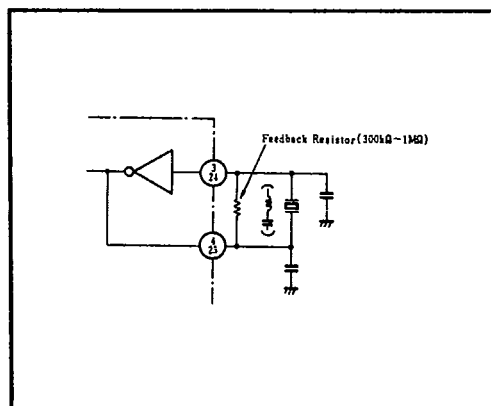


Figure 7 Pins 3, 4 and 24, 25 ( $260 f_H/282 f_H$  osc,  $4 f_{SC}$  osc)



Pin 19 is for VD output and V reset input. Figure 8 shows the internal circuit and IC operation. Output impedance is 500 Ω to 2 kΩ when pin 19 output is  $V_{DD}/2$ .

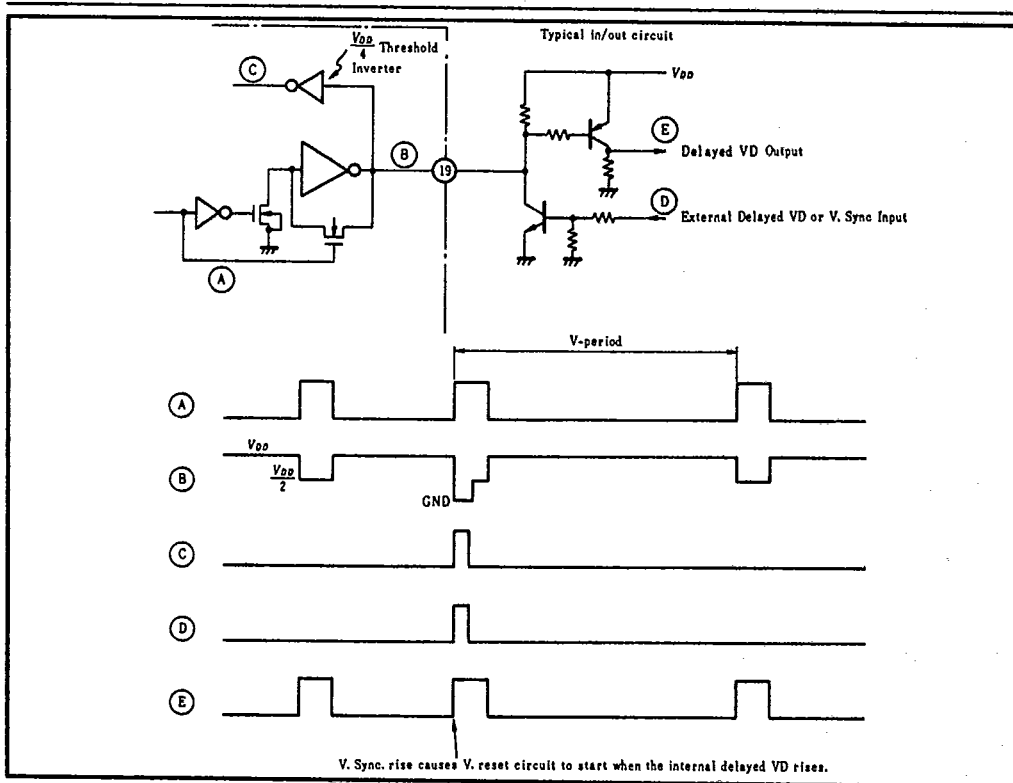


Figure 8 Pin 19, Delayed VD In/Out



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**Absolute Maximum Ratings** (Ta = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V <sub>DD</sub>	10	V
Input Voltage	V <sub>IN</sub>	-0.3 to V <sub>DD</sub> + 0.3	V
Power Dissipation (Ta = 85°C)	P <sub>T</sub>	450	mW
Operating Temperature	T <sub>opr</sub>	-30 to +85	°C
Storage Temperature	T <sub>stg</sub>	-55 to +125	°C

**Electrical Characteristics** (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Operating Supply Voltage	V <sub>DD</sub>	6.3	7.0	7.7	V	
Supply Current	I <sub>DD</sub>	—	—	40	mA	Output pins open, under oscillation
Input Voltage	V <sub>IH</sub>	0.8 V <sub>p-p</sub>	—	V <sub>DD</sub> + 0.3	V	Pins 16, 17, and 20
	V <sub>IL</sub>	-0.3	—	0.2 V <sub>DD</sub>	V	
Input Threshold Voltage	V <sub>IH</sub>	0.2 V <sub>DD</sub>	0.25 V <sub>DD</sub>	0.3 V <sub>DD</sub>	V	Pin 19
Output Voltage	V <sub>OH</sub>	0.8 V <sub>DD</sub>	—	—	V	Pins 11, 26, and 27, I <sub>OH</sub> = -100 μA
		0.8 V <sub>DD</sub>	—	—	V	Pins 1, 2, and 7, I <sub>OH</sub> = -250 μA
		0.8 V <sub>DD</sub>	—	—	V	Pins 8, 9, 10, 12, 13, 15, 18, 19 and 21, I <sub>OH</sub> = -500 μA
Output Voltage	V <sub>OL</sub>	—	—	0.2 V <sub>DD</sub>	V	Pins 11, 26, and 27, I <sub>OL</sub> = 100 μA
		—	—	0.2 V <sub>DD</sub>	V	Pins 1, 2, 7, and 20, I <sub>OL</sub> = 250 μA
		—	—	0.2 V <sub>DD</sub>	V	Pins 8, 9, 10, 12, 13, 15, 18, and 21, I <sub>OL</sub> = 500 μA
		0.4 V <sub>DD</sub>	0.5 V <sub>DD</sub>	0.6 V <sub>DD</sub>	V	Pin 19, open
Output Impedance	Z <sub>out</sub>	500	1000	2000	Ω	Low output level at pin 19
Pull-Up Resistance	I <sub>R</sub>	-200	-100	-50	μA	High output level at pin 20, pin 20 grounded





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**Electrical Characteristics (cont)**

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Maximum Clock Pulse Frequency	$f_{C \max}$	20	—	—	MHz	$V_{DD} = 6.3 \text{ V}$ , 20 MHz crystal resonator between pins 24 and 25, output at pins 26 and 27 (20/4 = 5 MHz output)
Maximum Divider Operating Frequency	$f_{D \max}$	5.0	—	—	MHz	$V_{DD} = 6.3 \text{ V}$ , LC between pins 3 and 4, normal oscillation frequency at output terminal
Pin 26 Output Phase Angle (NTSC)	$\phi_N$	88	90	92	deg	Pin 26 output phase referred to 180° (= pin 27 output phase), pin 16: $V_{DD}$ , $V_{DD} = 6.3\text{--}7.7 \text{ V}$
Pin 26 Output Phase Angle (PAL 1)	$\phi_{P1}$	88	90	92	deg	Pin 26 output phase referred to 180° (= pin 27 output phase), pin 16: GND, high level line output
Pin 26 Output Phase Angle (PAL 2)	$\phi_{P2}$	268	270	272	deg	Pin 26 output phase referred to 180° (= pin 27 output phase), pin 16: GND, low level line output









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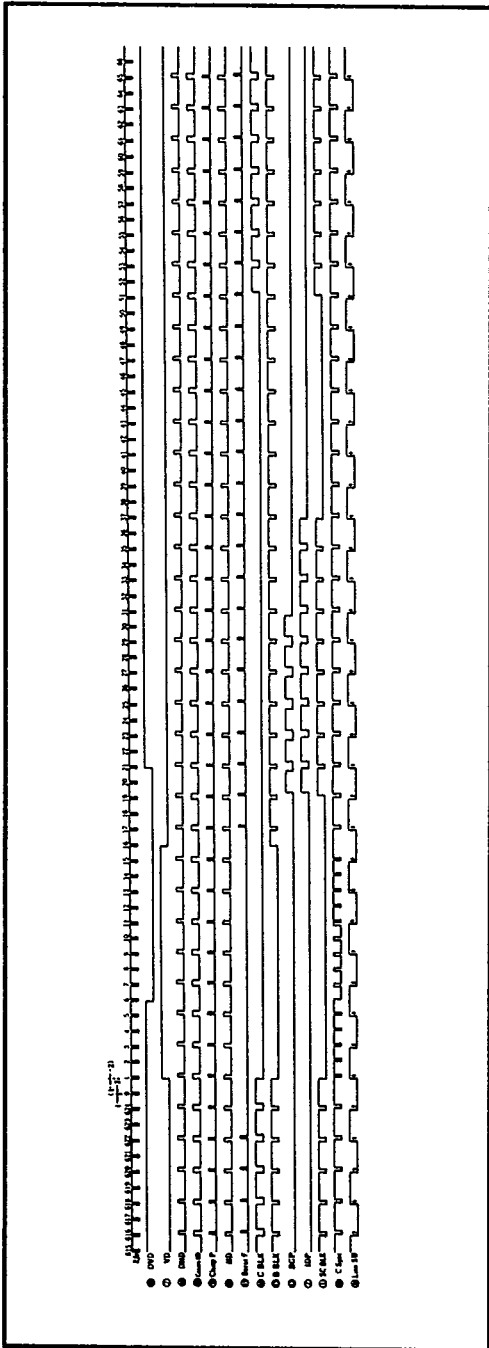


Figure 14 Timing Chart 5

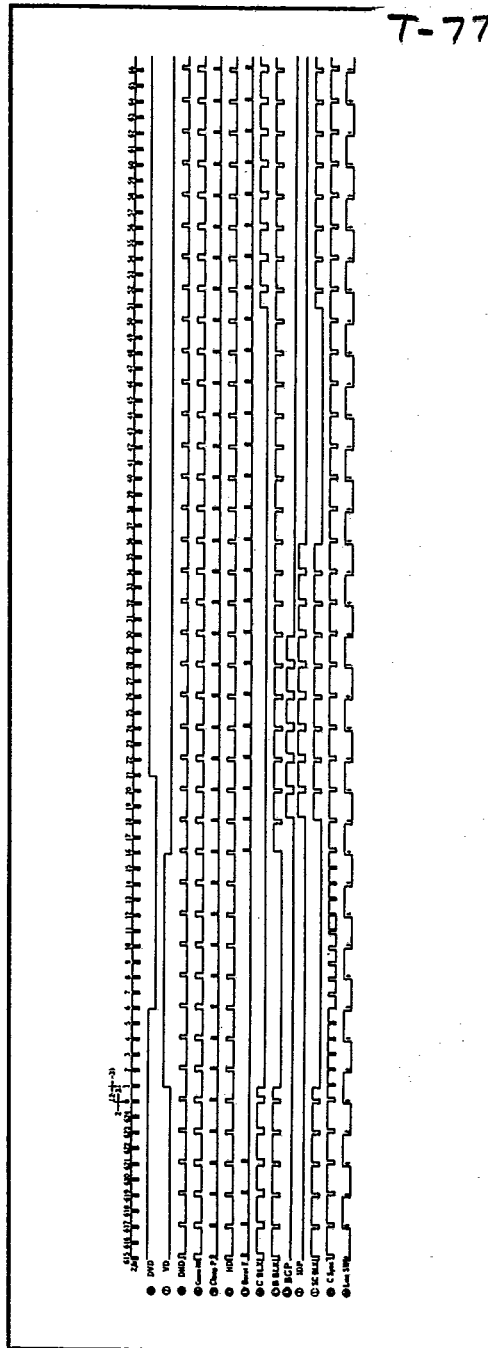


Figure 15 Timing Chart 6



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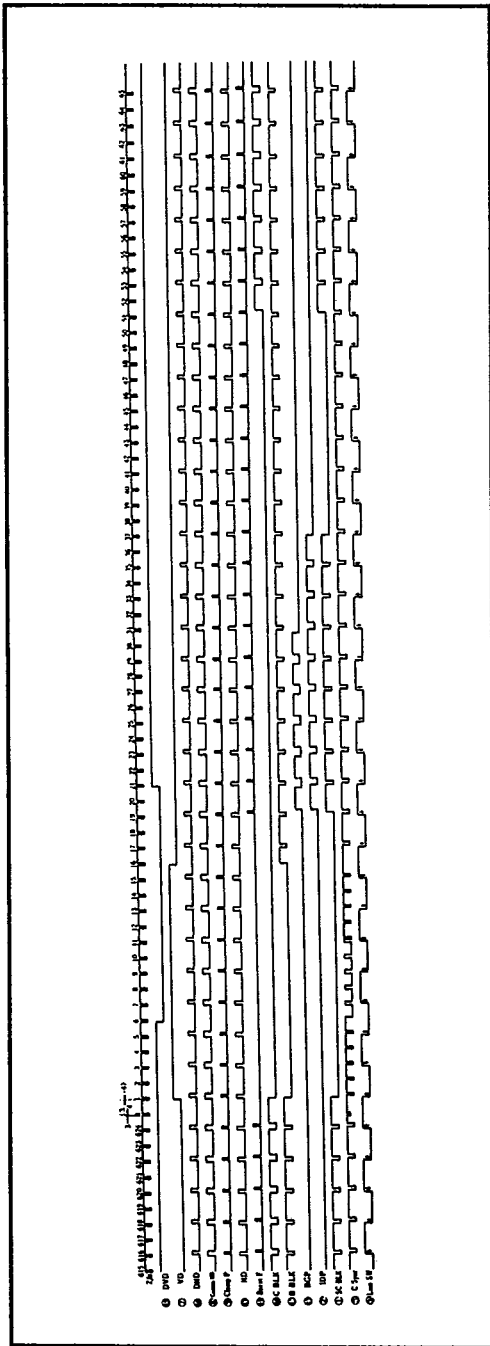


Figure 16 Timing Chart 7

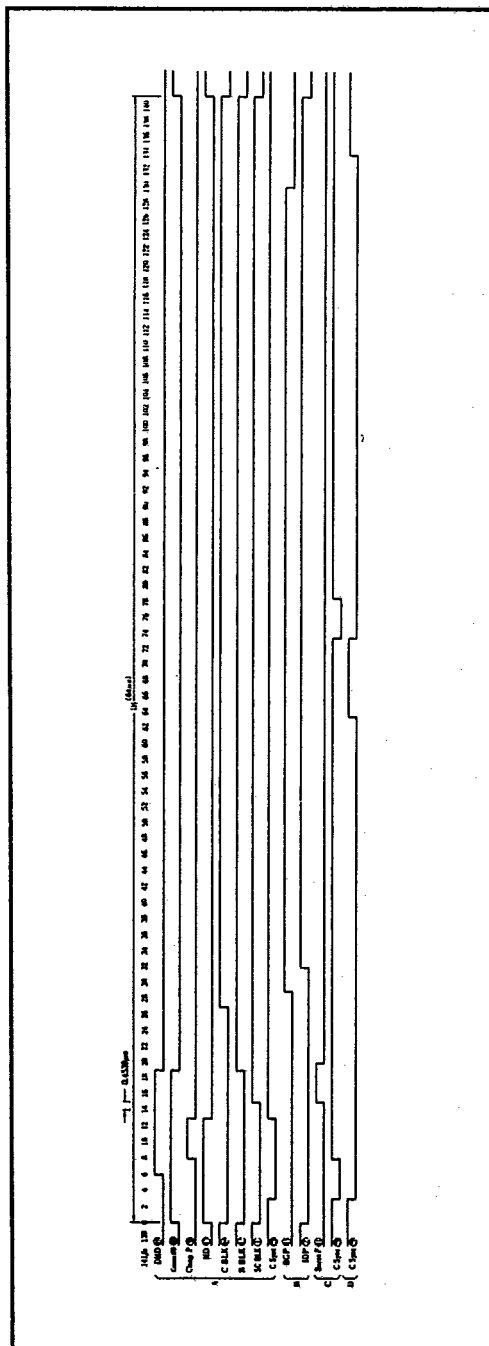


Figure 17 Timing Chart 8

