

## Post Amplifier for Optical Fiber Communication Receiver

### Description

The CXB1810FN achieves 2R optical fiber communication receiver functions (Reshaping and Regenerating) on a single chip.

This IC is equipped with a signal detection function, and outputs at TTL level.

### Features

- Auto-offset canceler circuit
- Signal interruption alarm output
- Single 3.3V or 5.0V power supply

### Applications

SONET/SDH

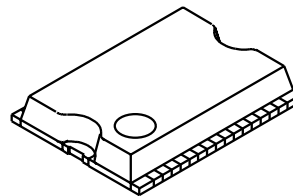
### Absolute Maximum Ratings

• Supply voltage	$V_{CC} - V_{EE}$	-0.3 to +6.0	V
• Input voltage difference	$ V_D - V_{DN} $	2.5	V
• ECL/TTL output current (Continuous)		50	mA
	(Surge)	70	mA
• Storage temperature	$T_j$	-65 to +150	°C

### Recommended Operating Conditions

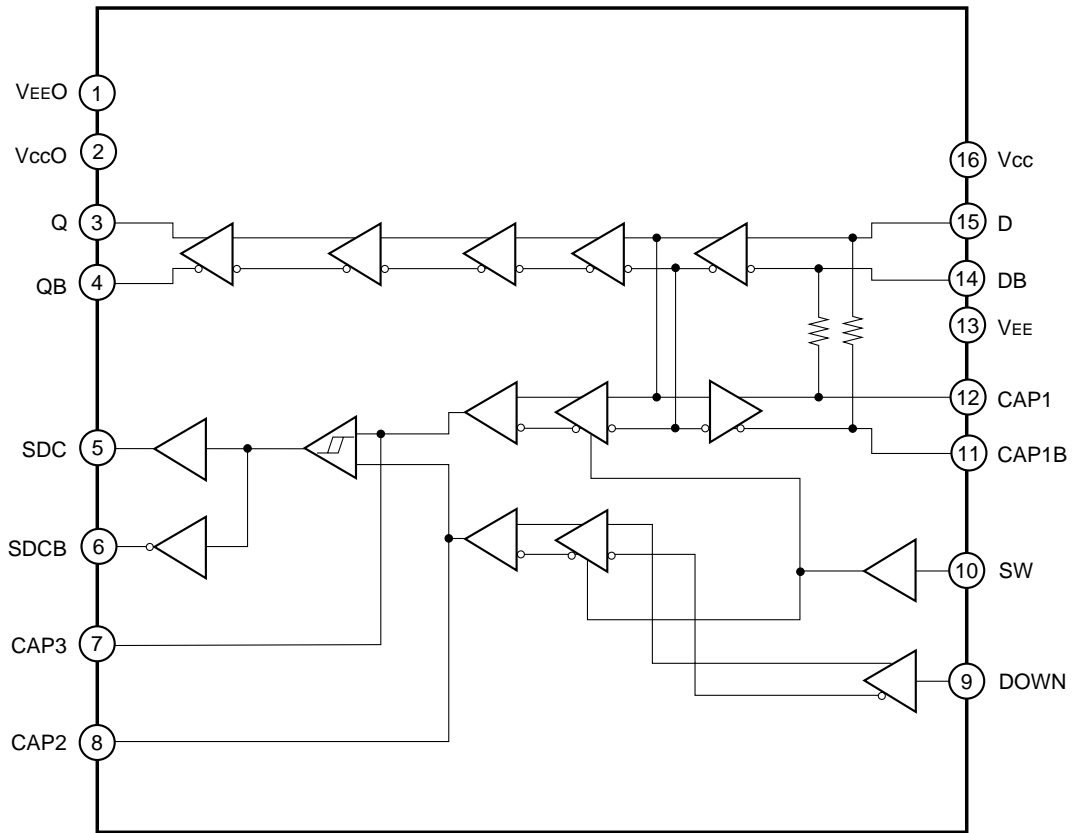
• Supply voltage	$V_{CC} - V_{EE}$	3.14 to 5.25	V
• Termination voltage (for Q/QB)	$V_{t1}$	$V_{CC} - 1.8$ to $V_{CC} - 2.2$	V
• Termination resistance (for Q/QB)	$R_t$	46 to 56	$\Omega$
• Operating temperature	$T_a$	-40 to +85	°C

16 pin HSOF (plastic)

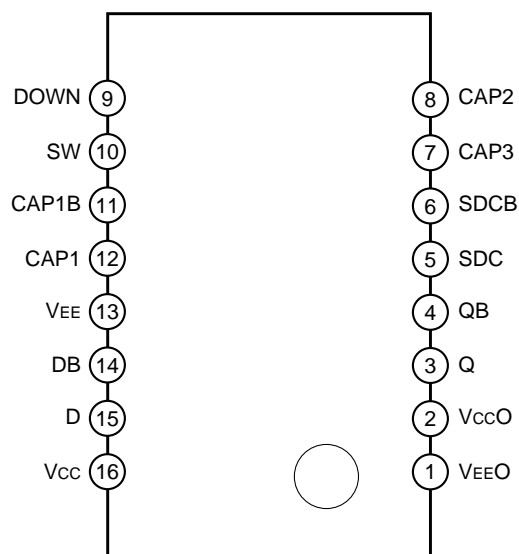


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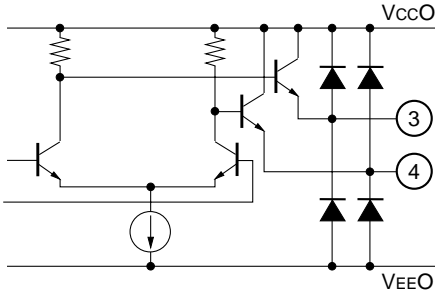
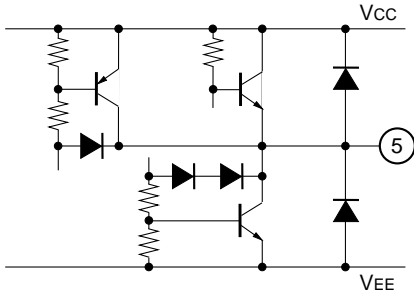
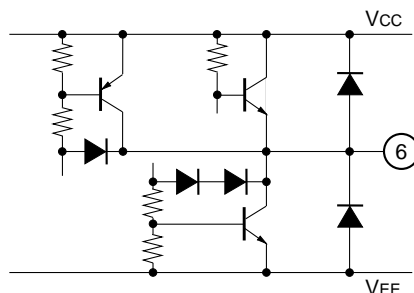
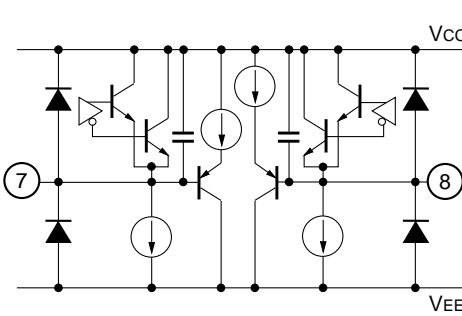
Block Diagram



Pin Configuration



Pin Description

Pin No.	Symbol	Typical pin voltage (V)		Equivalent circuit	Description
		DC	AC		
1	V <sub>EE</sub> O	0			Ground for data output circuit.
2	V <sub>CC</sub> O	3.3 or 5.0			Positive power supply for data output circuit.
3 4	Q QB		1.7 to 2.4 or 3.4 to 4.1		Data outputs.
5	SDC		0.2 to 2.9 or 0.2 to 4.7		Signal detection output (TTL). The SDC output is driven to low level while signal interruption is detected.
6	SDCB		0.2 to 2.9 or 0.2 to 4.7		Signal detection output (TTL). The SDCB output is driven to high level while signal interruption is detected.
7 8	CAP3 CAP2		1.3 to 1.8 or 3.0 to 3.5		Connect a peak hold capacitor for the signal detection circuit. 470pF (typ.)

Pin No.	Symbol	Typical pin voltage (V)		Equivalent circuit	Description
		DC	AC		
9	DOWN	2.4 or 4.1			Connect a resistor between this pin and the Vcc pin to decrease the signal detection level from the default value.
10	SW				Switches the maximum identification voltage amplitude. This pin is set to 50mVp-p (single ended) when open or high level, or to 15mVp-p (single ended) when low level. Setting to low level is recommended when using a resistor of 510Ω or less between the Vcc and DOWN pins.
11 12	CAP1B CAP1	2.2 or 3.9			Connect an external capacitor between these pins. 0.022μF (typ.)
14 15	DB D				Data inputs.
13	V <sub>EE</sub>	0			Ground.
16	V <sub>CC</sub>	3.3 or 5.0			Positive power supply.

**Electrical Characteristics**

**DC Characteristics**

( $V_{CC} = 3.14$  to  $5.25V$ ,  $T_a = -40$  to  $+85^{\circ}C$ , unless otherwise specified)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Q/QB high output voltage	VOH1	$51\Omega$ terminated to $V_{CC} - 2V$	$V_{CC} - 1100$		$V_{CC} - 650$	mV
Q/QB low output voltage	VOL1	$51\Omega$ terminated to $V_{CC} - 2V$	$V_{CC} - 1800$		$V_{CC} - 1300$	mV
Q/QB output amplitude	Vp	$51\Omega$ terminated to $V_{CC} - 2V$	500		1000	mVp-p
SDC/SDCB high output voltage	VOHT	$I_{OH} = -0.2mA$	2.4			V
SDC/SDCB low output voltage	VOLT	$I_{OL} = 2.1mA$			0.5	V
SW high input voltage	VIHT		$V_{CC} - 0.3$		$V_{CC}$	V
SW low input voltage	VILT		$V_{EE}$		$V_{EE} + 0.3$	V
Maximum input voltage amplitude	Vmax	During single-phase input	1000			mVp-p
D/DB input resistance	Rin		33	50	69	$\Omega$
Supply current	ICC	All outputs open		40	55	mA

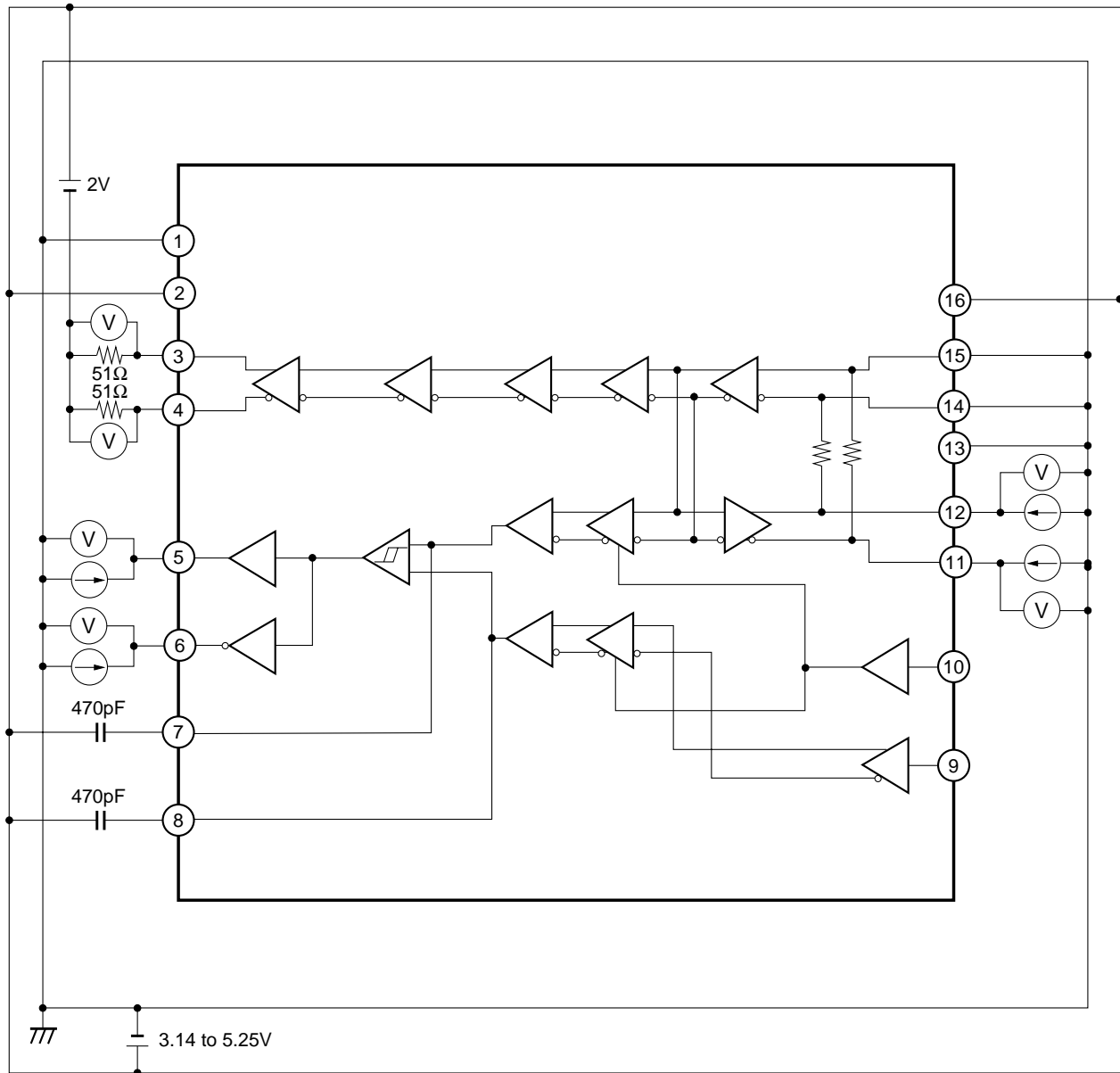
**AC Characteristics**

( $V_{CC} = 3.14$  to  $5.25V$ ,  $T_a = -40$  to  $+85^{\circ}C$ , unless otherwise specified)

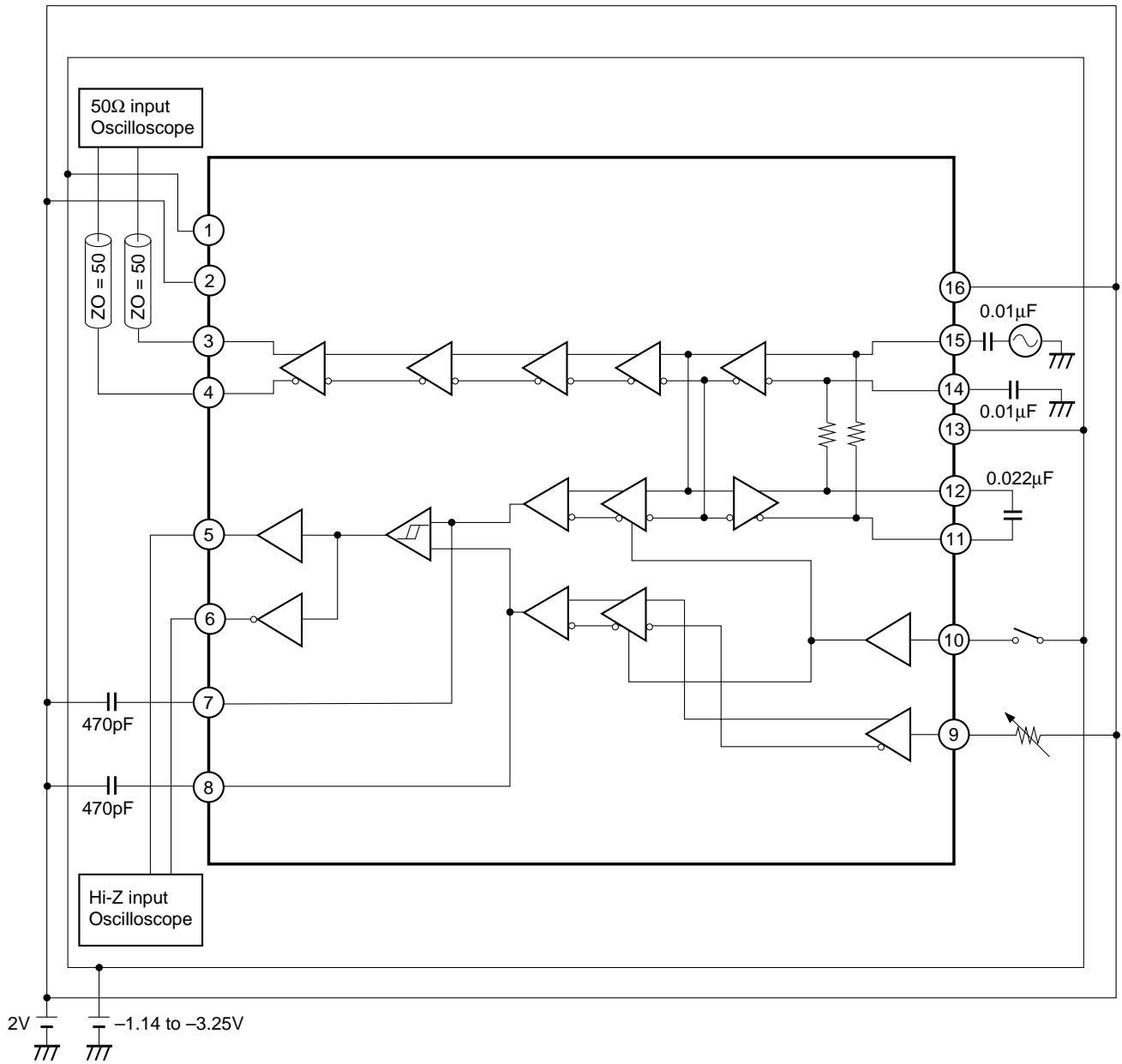
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Limiting amplifier gain	GL		45			dB
Signal detection threshold voltage	Vth	During single ended input		34		mVp-p
Signal detection hysteresis width	$\Delta P$		3	6	8	dB
Signal detection response assert time*1	Tas		0		100	$\mu s$
Signal detection response deassert time*1	Tdas		2.3		100	$\mu s$
Q/QB rise time (20 to 80%)	TR	$51\Omega$ terminated to $V_{CC} - 2V$		130		ps
Q/QB fall time (20 to 80%)	TF	$51\Omega$ terminated to $V_{CC} - 2V$		110		ps

\*1 Data = PN23 - 1 pattern, 100mVp-p single ended,  $R_d = open$ ,  $CAP2/CAP3 = 470pF$

DC Electrical Characteristics Measurement Circuit



AC Electrical Characteristics Measurement Circuit







Notes on Operation

1. Limiting amplifier block

The limiting amplifier block is equipped with an auto-offset canceler circuit. When external capacitors C1 and C2 are connected as shown in Fig. 1, the DC bias is set automatically in this block.

External capacitor C1 and internal resistor R1 determine the input low cut-off frequency  $f_2$  as shown in Fig. 2. Similarly, external capacitor C2 and internal resistor R2 determine the high cut-off frequency for DC feedback. Since a peak may occur in the low frequency area of the gain characteristics depending on the  $f_1/f_2$  combination, set the C1 and C2 values so as to avoid the occurrence of this peak. The typical values of R1, R2, C1 and C2 are indicated below.

Also, when a single ended input is used, provide AC grounding by connecting Pin 14 to a capacitor which has the same capacitance as capacitor C1.

R1 (internal): 50Ω	} f2: 318kHz	R2 (internal): 10kΩ	} f1: 723Hz
C1 (external): 0.01μF		C2 (external): 0.022μF	

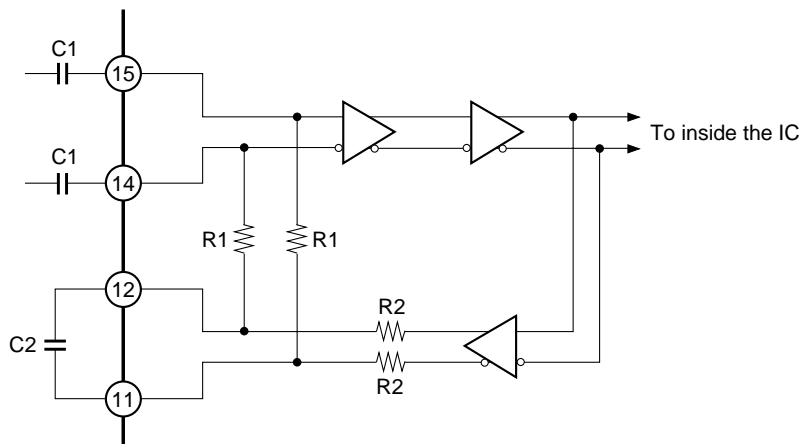


Fig. 1

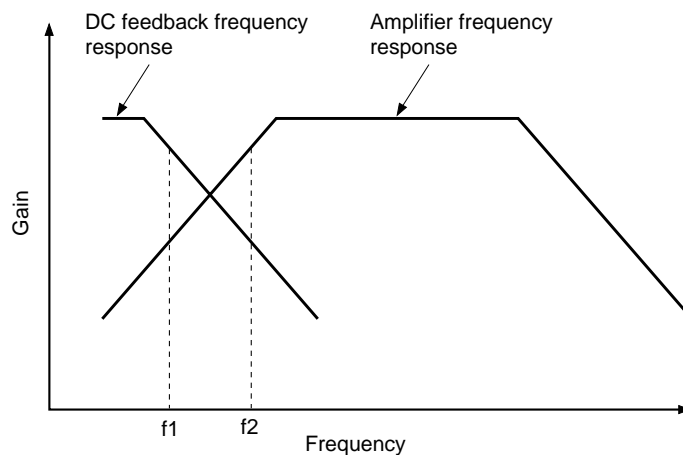


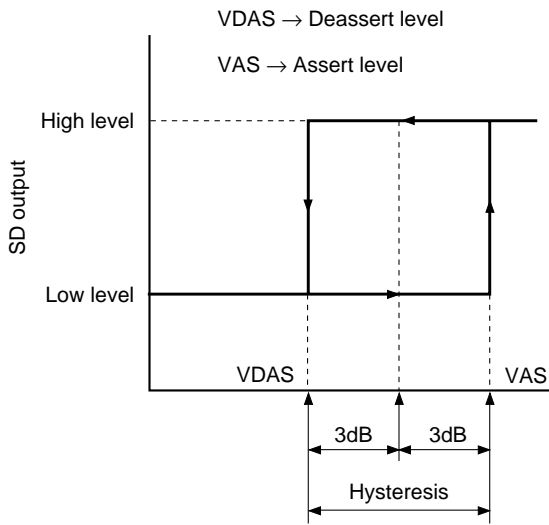
Fig. 2

**2. Alarm block**

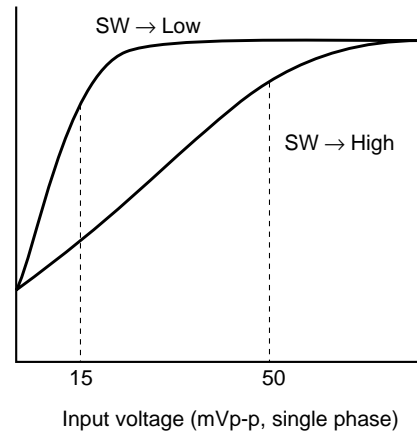
In this block, the input signal amplitude is detected and the signal interruption alarm is output when the amplitude becomes lower than the set alarm level. The alarm level setting can be adjusted by connecting an external resistor  $R_d$  between the DOWN and  $V_{CC}$  pins.

Also, this IC can set the maximum identification voltage amplitude to two levels. The maximum identification voltage amplitude is set to 50mVp-p (single ended) when the SW pin is open or high level, or to 15mVp-p (single ended) when the SW pin is low level.

Figs. 15 and 16 show the relation of  $R_d$  and the alarm assert/deassert level. Setting the SW pin to low level is recommended when  $R_d$  is 510Ω or less.

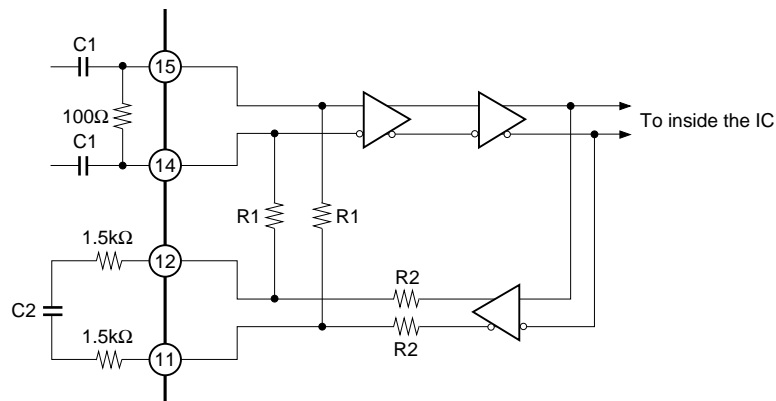


**Fig. 3**



**Fig. 4**

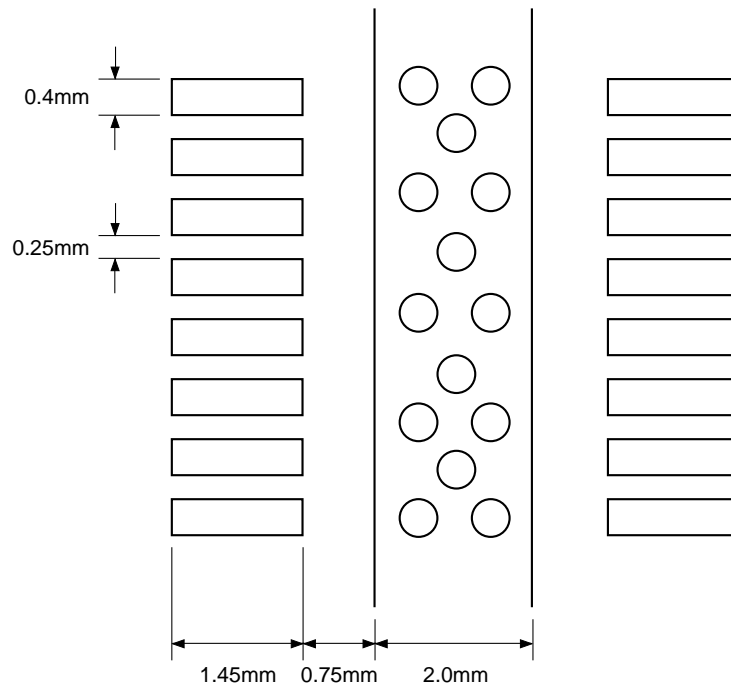
In addition, the SD response deassert time is guaranteed only under the conditions noted in the AC Electrical Characteristics item, but the response becomes delayed as the input signal amplitude becomes larger. This is because the input resistor  $R_1$  shown in Fig. 1 is small at 50Ω, so the charge accumulated in  $C_2$  is relatively large and the discharge time for this charge accounts for most of the SD response deassert time. The SD response deassert time can be shortened by using the external circuit shown in Fig. 5 or by shorting the CAP1 and CAP1B pins. However, care should be taken as the auto-offset canceler circuit does not operate in this case causing the reception sensitivity to deteriorate. Fig. 14 shows the relation between the SD response deassert time and the electrical input amplitude when using the connection shown in Fig. 5.



**Fig. 5**

### 3. Substrate layout

The exposed metal portions on the rear surface of the package used for the CXB1810FN are electrically connected to the silicon substrate. Superior thermal radiation characteristics can be obtained by connecting the rear surface of the package and these exposed metal portions to the ground surface on the PCB. Providing lands directly below the package as shown in the figure below and connecting as many thermal vias as possible to the inner layer ground surface is recommended.



### 4. Other

- Be careful when handling this IC as its electrostatic discharge strength is weak.
- Be sure to connect all power supply pins ( $V_{CCO}$ ,  $V_{CC}$ ) and ground pins ( $V_{EE0}$ ,  $V_{EE}$ ) to power supplies or grounds, respectively. For example, if only  $V_{CCO}$  is left open and power is supplied to the other pin, the IC may malfunction.

Example of Representative Characteristics

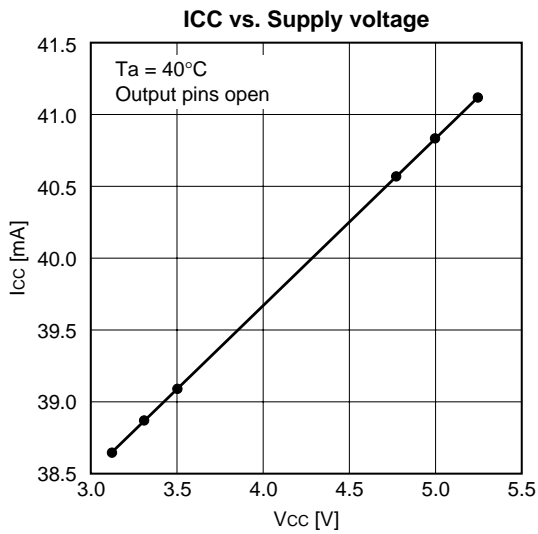


Fig. 6

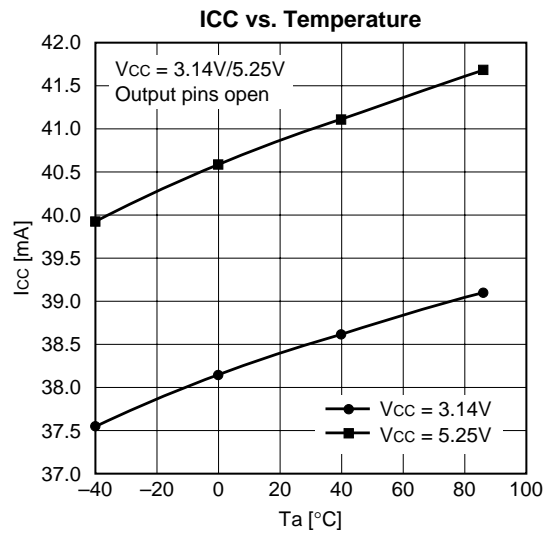


Fig. 7

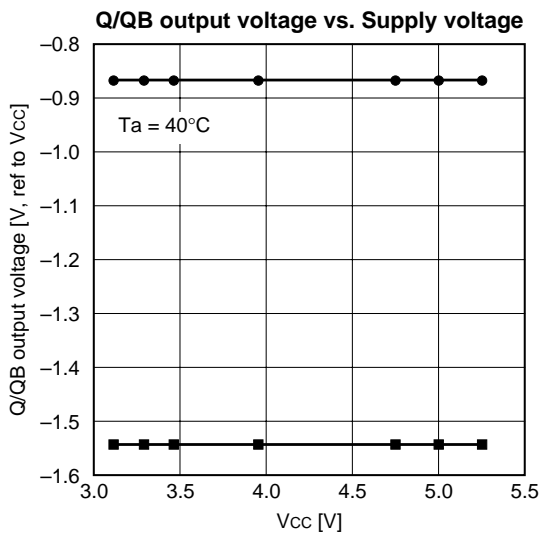


Fig. 8

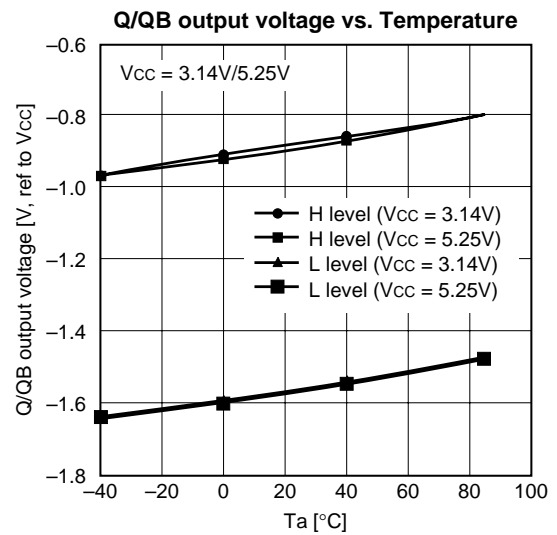


Fig. 9

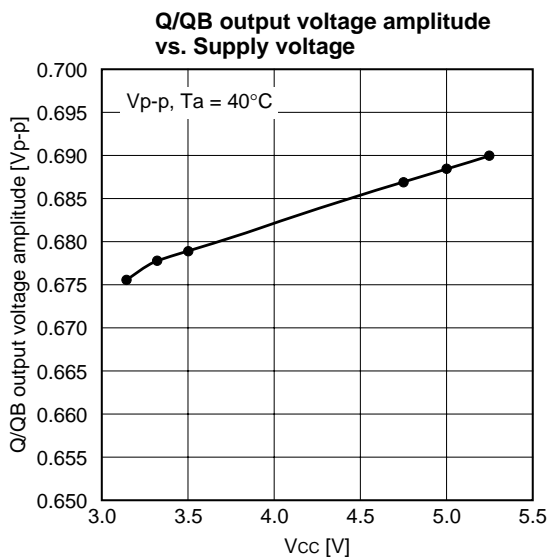


Fig. 10

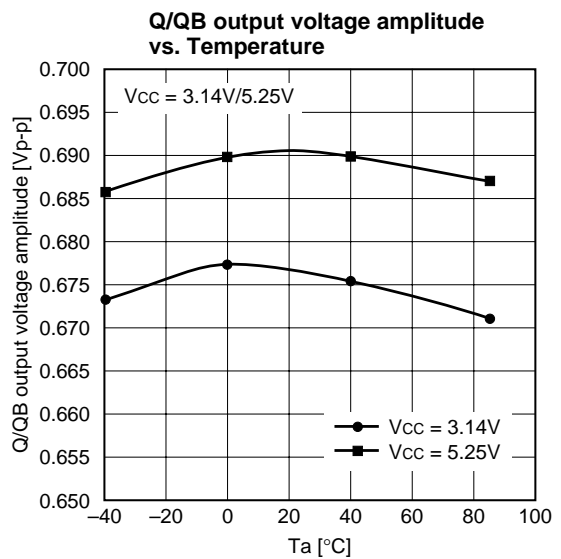


Fig. 11

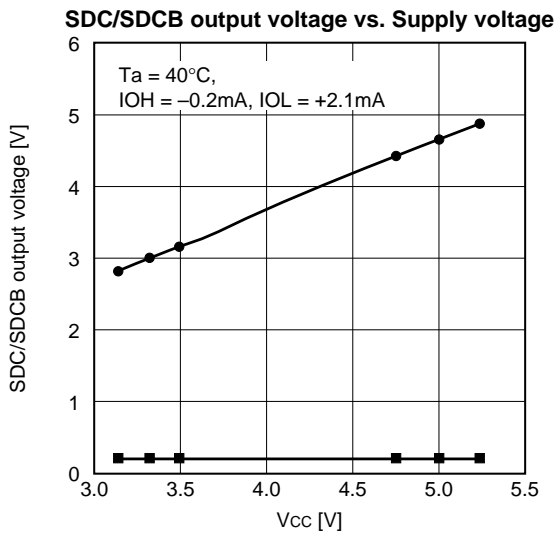


Fig. 12

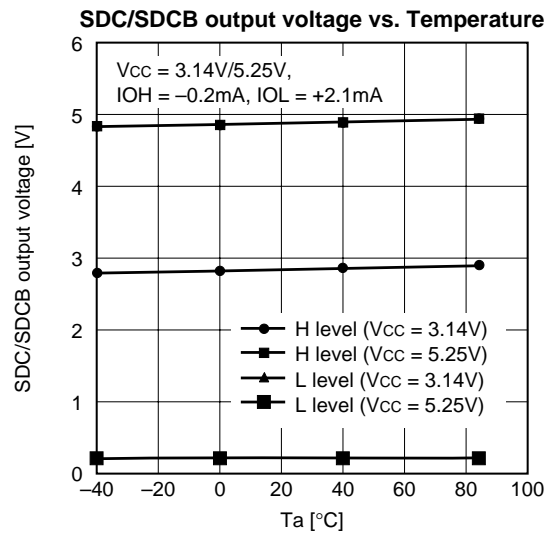


Fig. 13

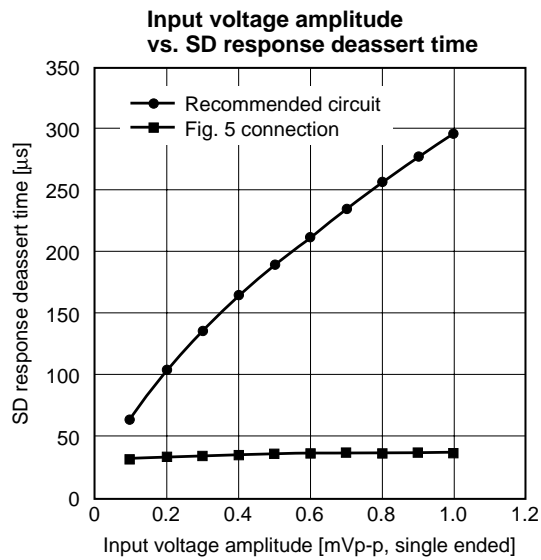


Fig. 14

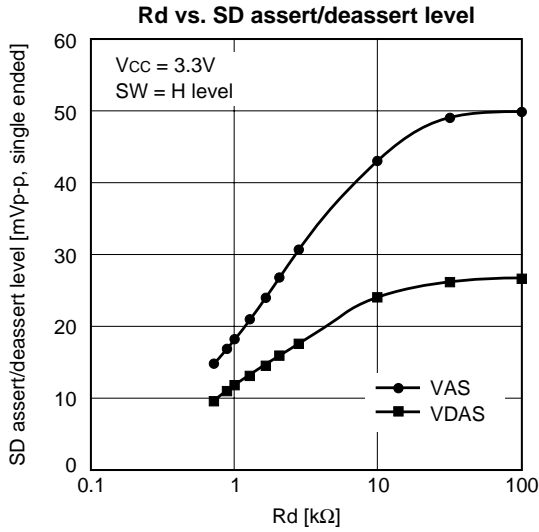


Fig. 15

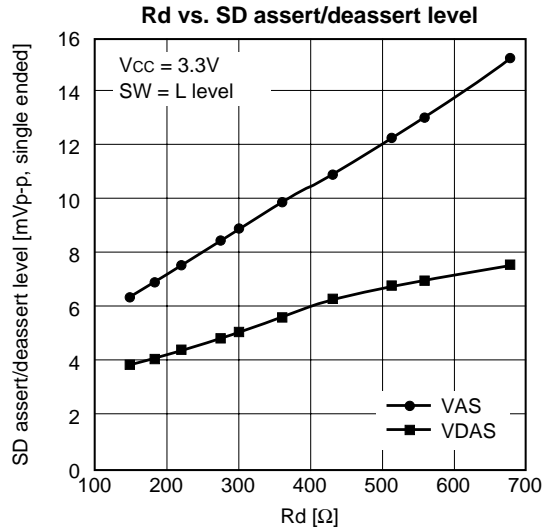


Fig. 16

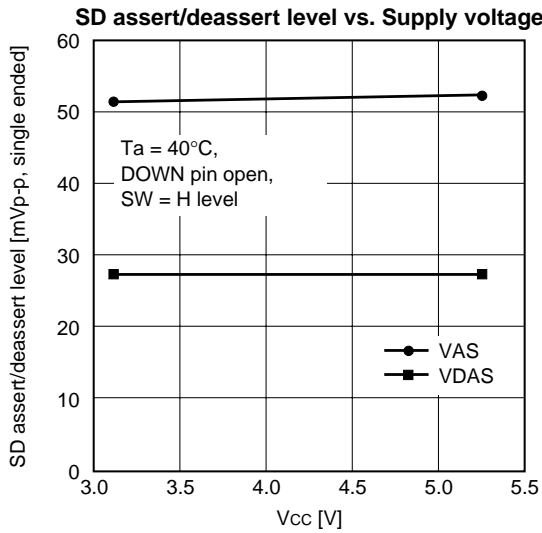


Fig. 17

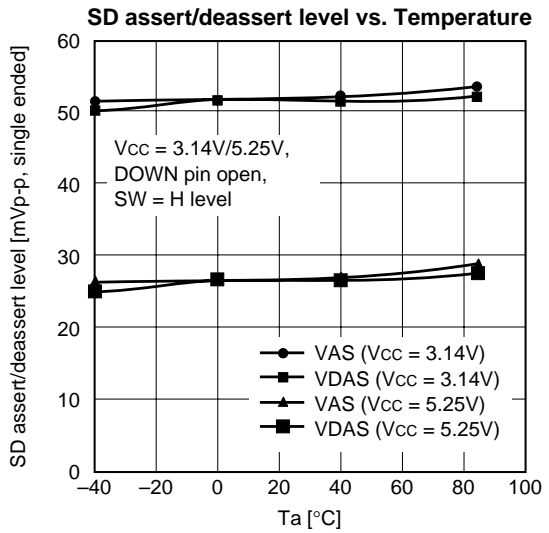


Fig. 18

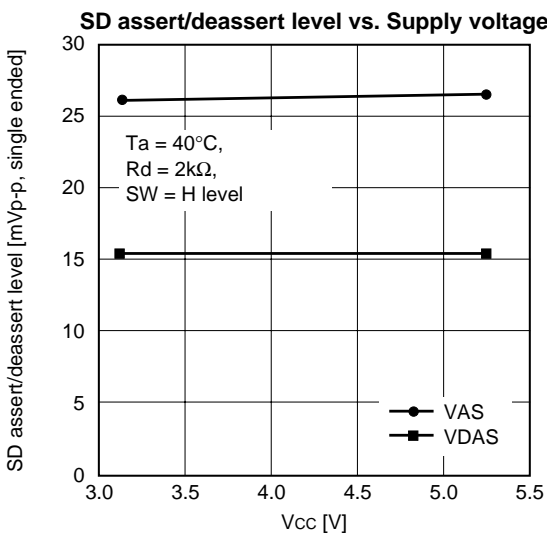


Fig. 19

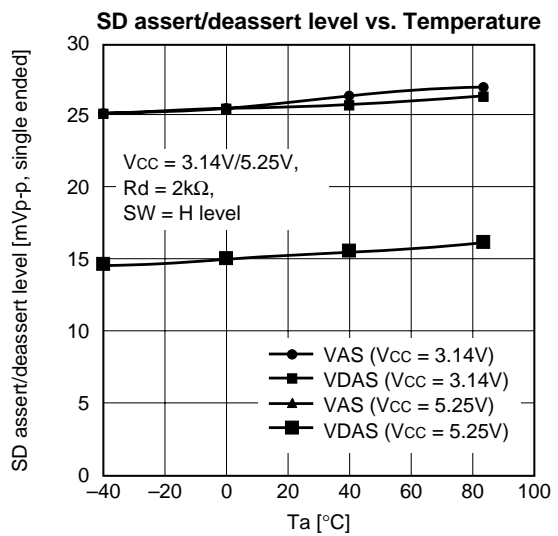


Fig. 20

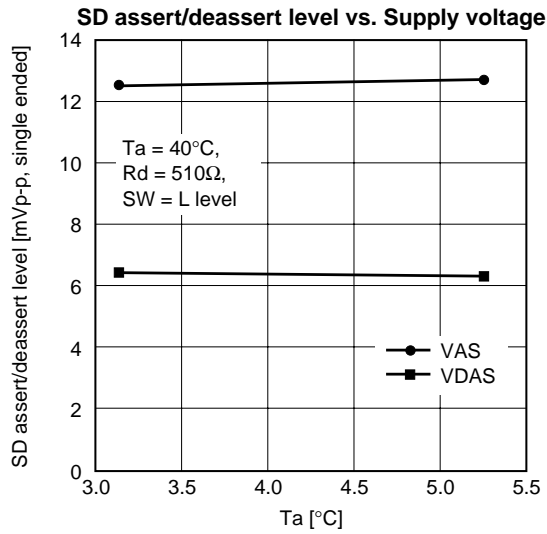


Fig. 21

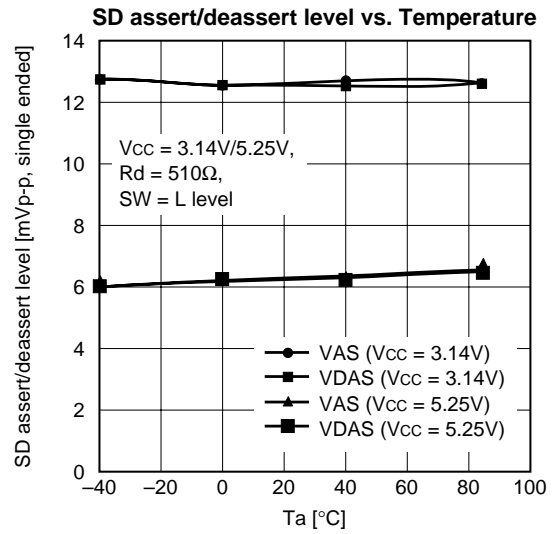


Fig. 22

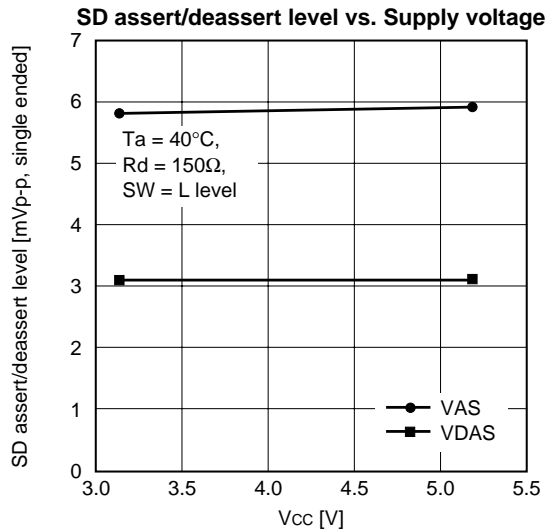


Fig. 23

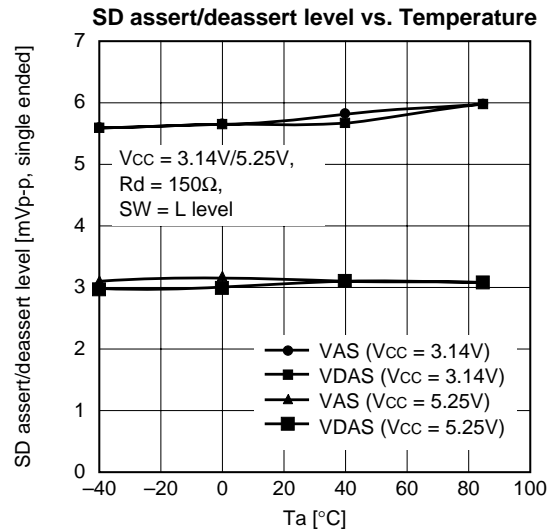


Fig. 24

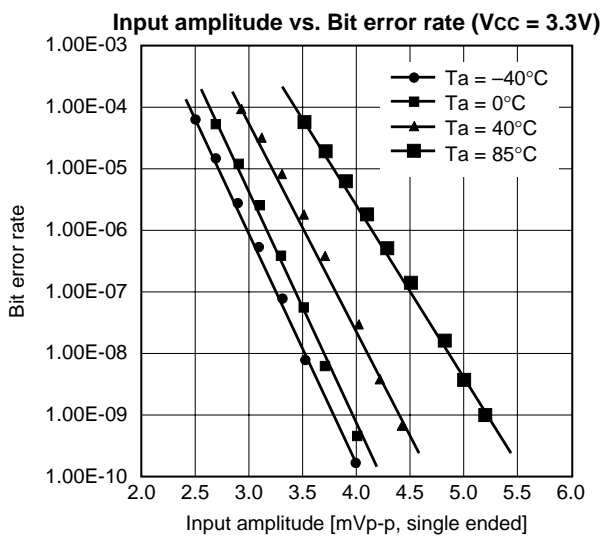


Fig. 25

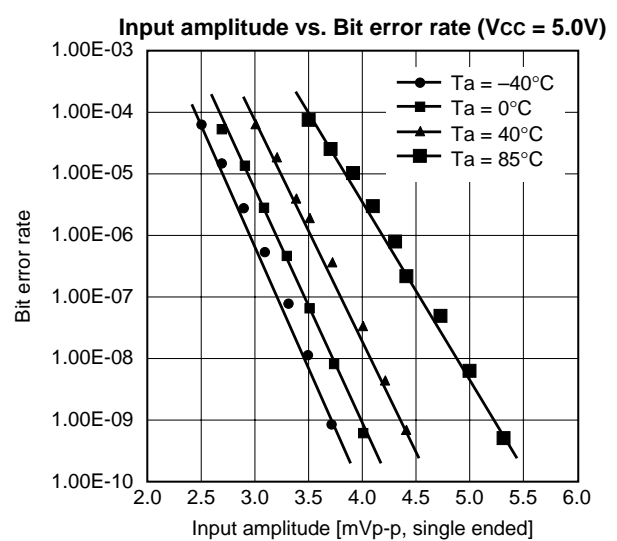
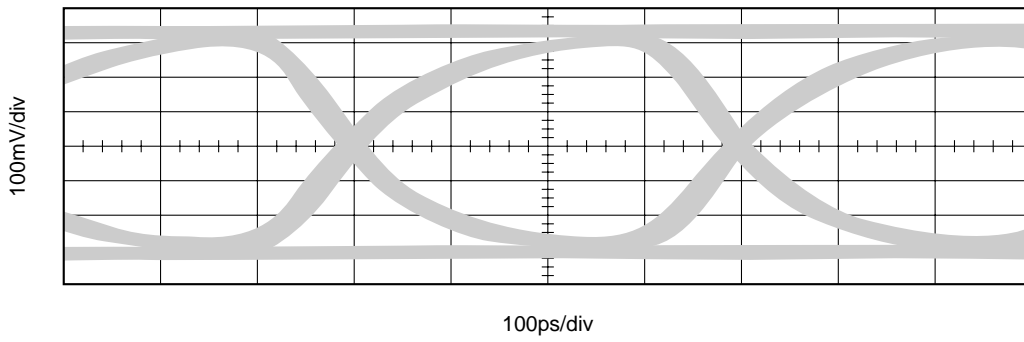
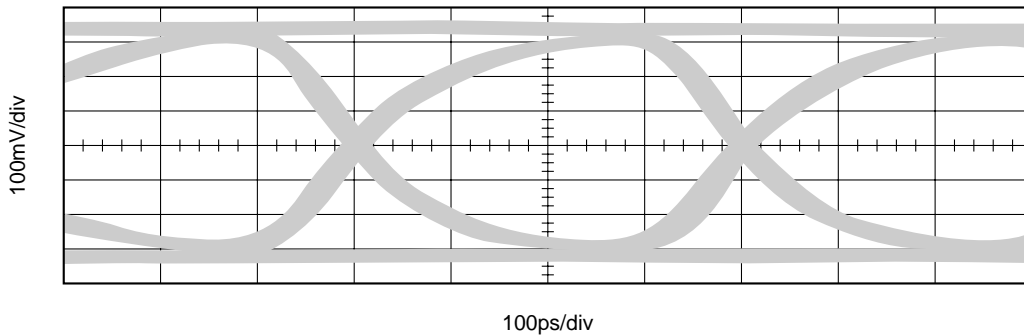


Fig. 26



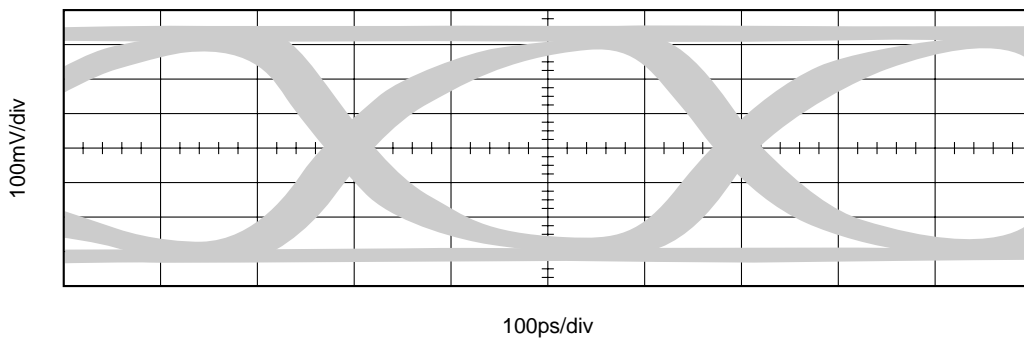
Q output waveform  
 $V_{CC} = 3.3V$ ,  $T_a = 40^\circ C$   
 $D = 100mVp-p$   
 (single ended)  
 PN23 pattern

**Fig. 27**



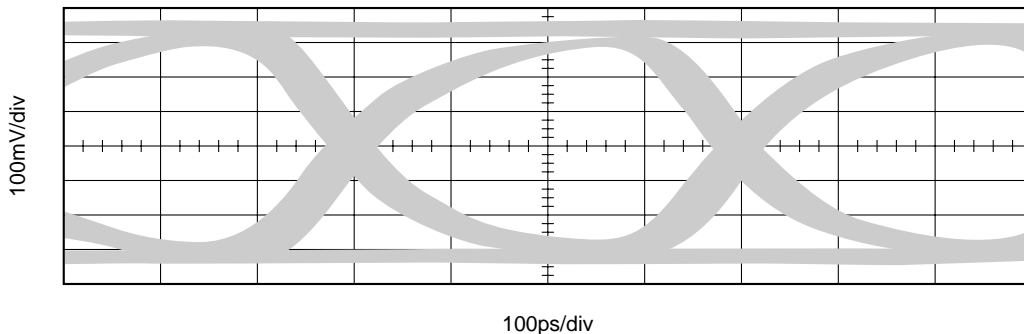
Q output waveform  
 $V_{CC} = 5.0V$ ,  $T_a = 40^\circ C$   
 $D = 100mVp-p$   
 (single ended)  
 PN23 pattern

**Fig. 28**



Q output waveform  
 $V_{CC} = 3.3V$ ,  $T_a = 40^\circ C$   
 $D = 10mVp-p$   
 (single ended)  
 PN23 pattern

**Fig. 29**



Q output waveform  
 $V_{CC} = 5.0V$ ,  $T_a = 40^\circ C$   
 $D = 10mVp-p$   
 (single ended)  
 PN23 pattern

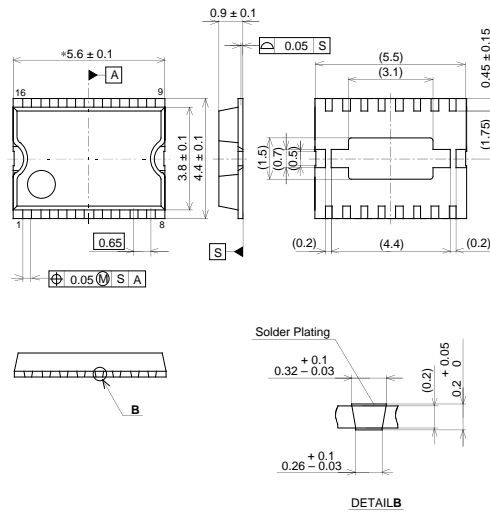
**Fig. 30**



Package Outline

Unit: mm

HSOF 16PIN(PLASTIC)



NOTE: Dimension "\*" does not include mold protrusion.

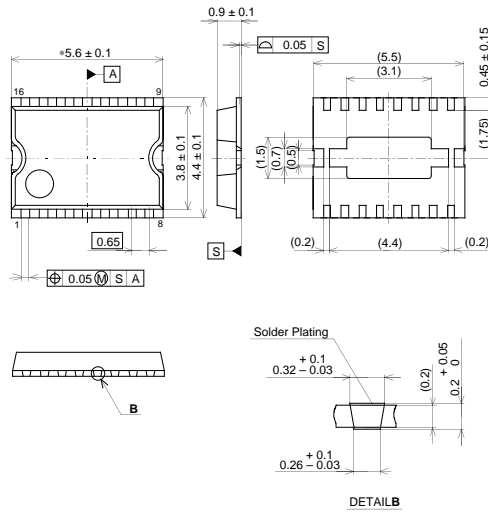
PACKAGE STRUCTURE

SONY CODE	HSOF-16P-02
EIAJ CODE	_____
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.06g

Kokubu & SCT Ass'y

HSOF 16PIN(PLASTIC)



NOTE: Dimension "\*" does not include mold protrusion.

PACKAGE STRUCTURE

SONY CODE	HSOF-16P-02
EIAJ CODE	_____
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.06g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18μm