SONY

CXB1596AR

10-bit Transceiver

Description

The CXB1596AR is a transceiver IC with a built-in PLL for Fibre Channel and Gigabit Ethernet. For a receiver 1.0625/1.25Gbaud serial data is received and output as 10-bit parallel data; for a transmitter 10-bit parallel data is received and output as 1.0625/1.25Gbaud serial data.

Features

- Transmitter and receiver in a single chip
- ANSI X3T11 Fibre Channel compatible (FC_0) at 1.0625Gbaud
- IEEE802.3z Gigabit Ethernet compatible at 1.25Gbaud
- Conforms to 10-bit interface specification
- TTL/ECL compatible
- PLL for clock generation and clock & data recovery
- Byte synchronization detector (positive character of Comma)
- Frequency autolock function
- Low power consumption (620mW typ.)
- 64-pin plastic LQFP package (10mm × 10mm)

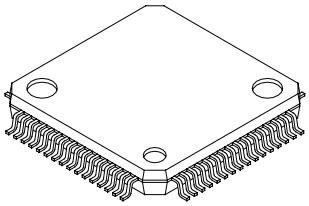
Applications

- 1.0625Gbaud Fibre Channel Interface
- 1.25Gbaud Gigabit Ethernet Interface
- Work Station/Server/HDD Interface
- High-speed data communications
- Switched networks

Structure

Bipolar silicon monolithic IC

64 pin LQFP (Plastic)



Absolute Maximum Ratings

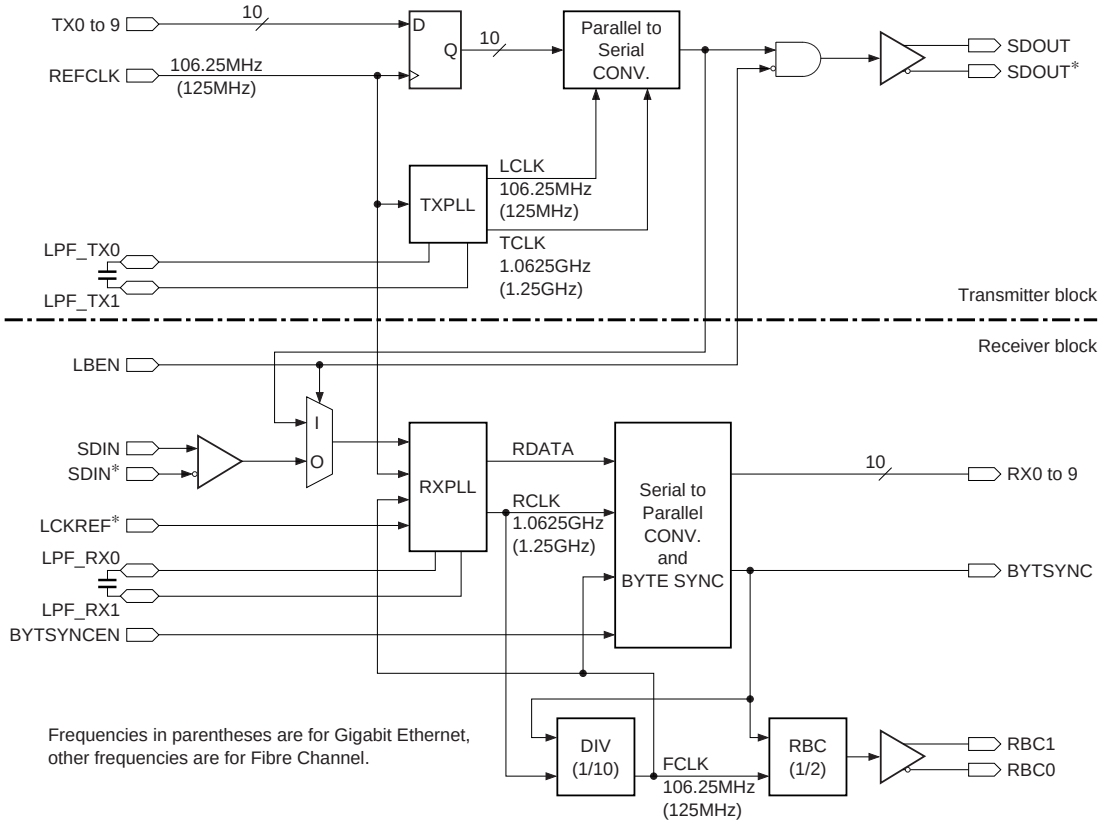
• Supply voltage	V_{CC}	–0.3 to +4	V
• TTL DC input voltage	V_{I}_T	–0.5 to +5.5	V
• ECL DC input voltage	V_{I}_E	V_{CC} – 2 to V_{CC}	V
• ECL differential input voltage amplitude	V_{IS}_E	–4 to +4	V
• TTL high level output current	I_{OH}_T	–20 to 0	mA
• TTL low level output current	I_{OL}_T	0 to 20	mA
• ECL output current	I_{O}_E	–30 to 0	mA
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	880	mW

Recommended Operating Conditions

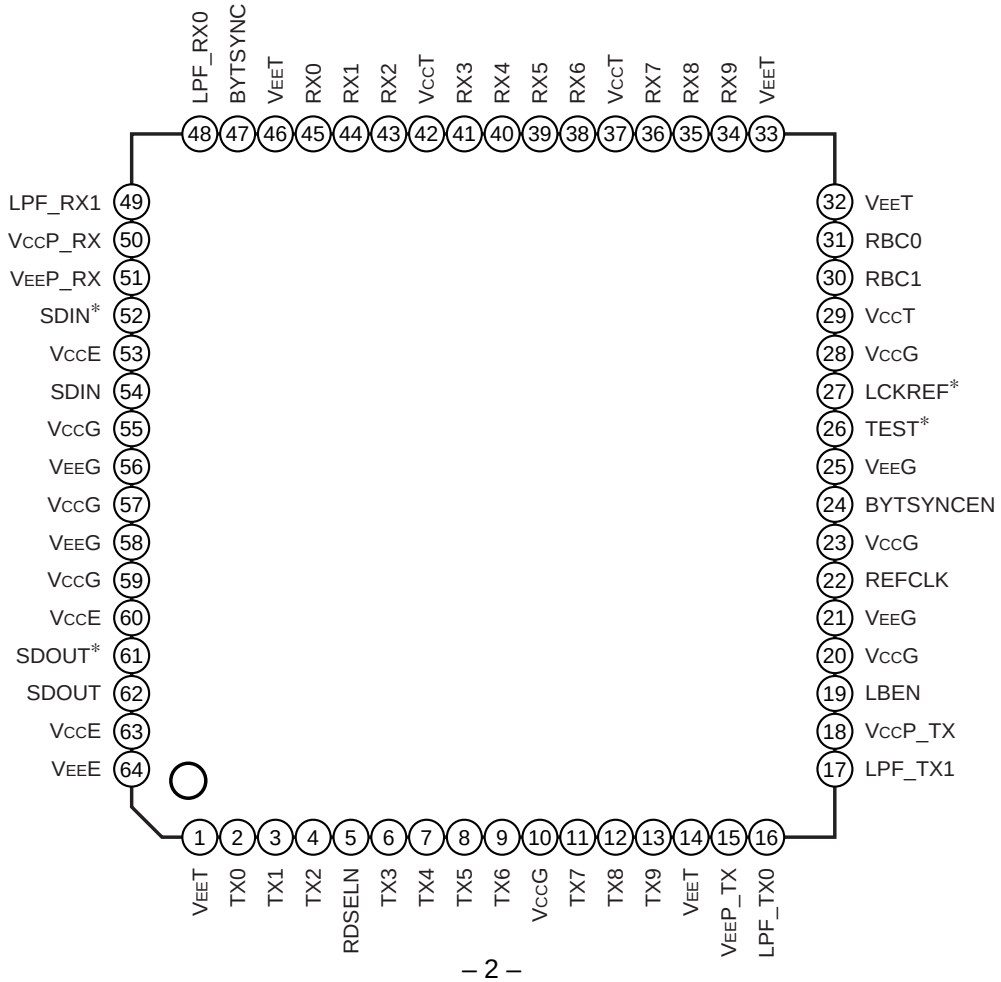
• Supply voltage	V_{CC}	3.135 to 3.465 (3.3V Typ.)	V
• PECL AC coupling differential output load resistance	R_L	(to V_{CC} –2V) 50	Ω
		(to V_{EE}) 150	Ω
• Ambient temperature	Ta	0 to +70	°C

E99212-PS

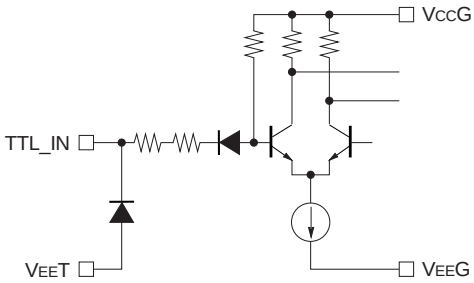
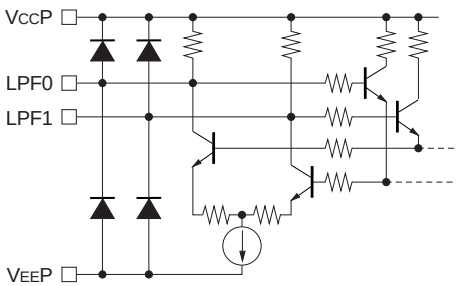
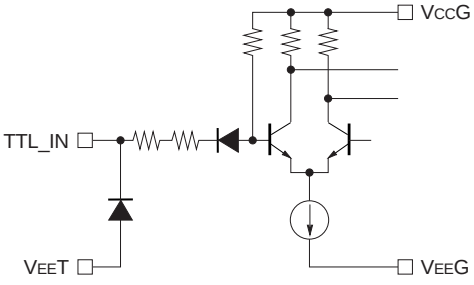
Block Diagram

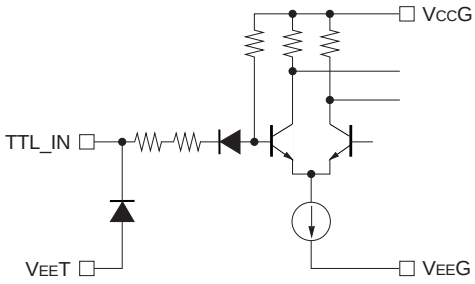
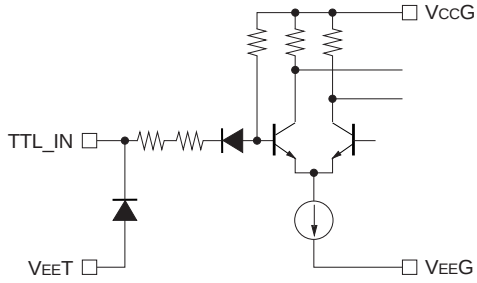
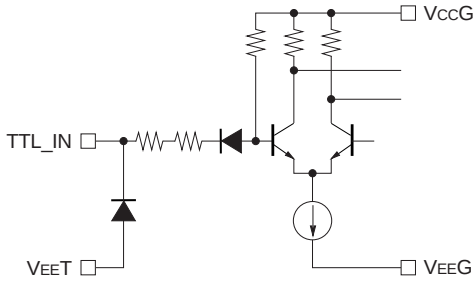
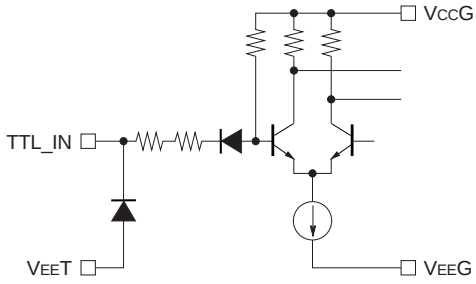


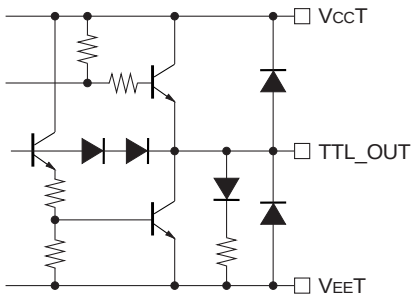
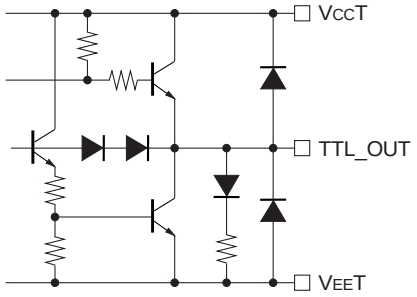
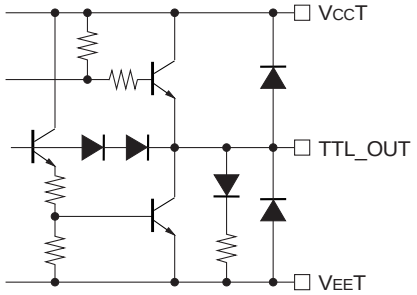
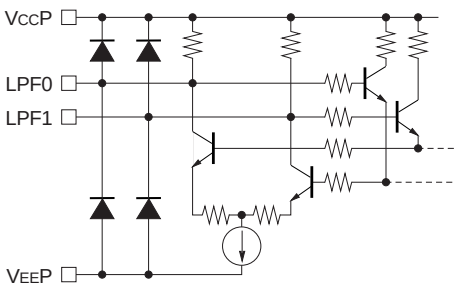
Pin Configuration (Top View)

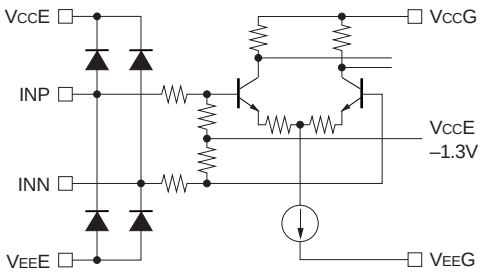
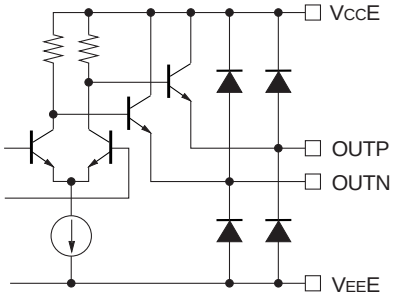


Pin Description

Pin No.	Symbol	Type	Typical pin voltage	Equivalent circuit	Description
1, 14, 32, 33, 46	$V_{EE}T$	Power supply	0V		Negative power supply for TTL output.
2 to 4, 6 to 9, 11 to 13	TX0 to TX9	TTL input	TTL level		Parallel data inputs. Input data is converted to serial data in order from TX0.
5	RDSELN	Test input	TTL High level		Test input. Set to TTL high level or leave open.
10, 20, 23, 28, 55, 57, 59	$V_{CC}G$	Power supply	3.3V		Positive power supply for internal circuits.
15	$V_{EE}P\_TX$	Power supply	0V		Negative power supply for TXPLL.
16 17	LPF_TX0 LPF_TX1	External part connection pin	—		External loop filter connection for TX.
18	$V_{CC}P\_TX$	Power supply	3.3V		Positive power supply for TXPLL.
19	LBEN	TTL input	TTL level		Loop back enable. When high, the TX serial output is serially input to the RX side inside the IC. When low, both transmit and receive are enabled.

Pin No.	Symbol	Type	Typical pin voltage	Equivalent circuit	Description
21, 25, 56, 58	$V_{EE}G$	Power supply	0V		Negative power supply for internal circuits.
22	REFCLK	TTL input	TTL level		External reference clock input.
24	BYTSYNCEN	TTL input	TTL level		Byte synchronization enable. When high, the Comma detection circuit is enabled to perform byte synchronization.
26	TEST*	Test input	TTL High level		Test input. Set to TTL high level or leave open.
27	LCKREF*	TTL input	TTL level		Forced reference clock lock. When low, the PLL is forcibly locked to the external reference clock (REFCLK). Normally set to high: autolock mode.
29, 37, 42	$V_{CC}T$	Power supply	3.3V		Positive power supply for TTL output.

Pin No.	Symbol	Type	Typical pin voltage	Equivalent circuit	Description
30 31	RBC1 RBC0	TTL output	TTL level		Receive side byte clocks recovered from the serial data. RBC1 and RBC0 output clocks which are 180 degrees out of phase.
34 to 36, 38 to 41, 43 to 45	RX0 to RX9	TTL output	TTL level		Parallel data outputs. Serial data is converted to parallel data in order starting from RX0 and ending with RX9.
47	BYTSYNC	TTL output	TTL level		Byte synchronization detection signal. This pin outputs high for a 1 byte period when the Comma signal is detected.
48 49	LPF_RX0 LPF_RX1	External part connection pin	—		External loop filter connection for RX.
50	VCCP_RX	Power supply	3.3V		Positive power supply for RXPLL.
51	VEEP_RX	Power supply	0V		Negative power supply for RXPLL.

Pin No.	Symbol	Type	Typical pin voltage	Equivalent circuit	Description
52 54	SDIN* SDIN	ECL input	PECL level		Serial data inputs.
53, 60, 63	VCCE	Power supply	3.3V		Positive power supply for ECL output.
61 62	SDOUT* SDOUT	ECL output	PECL level		Serial data outputs.
64	VEEE	Power supply	0V		Negative power supply for ECL output.

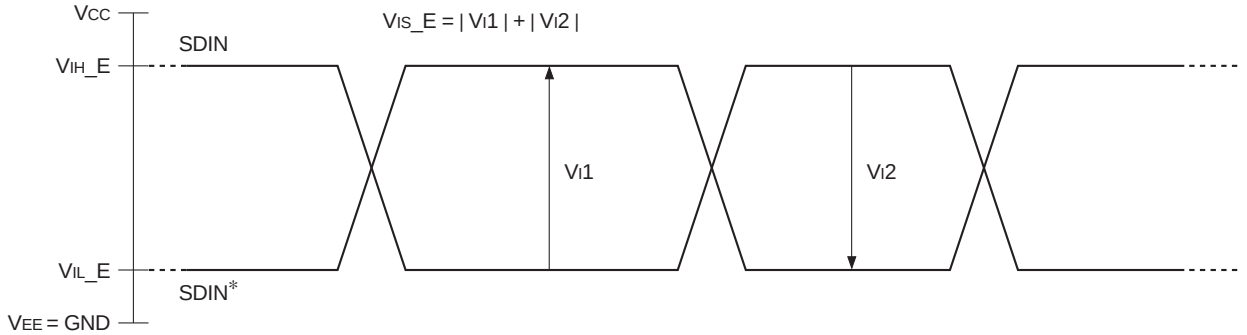
Electrical Characteristics

DC Characteristics

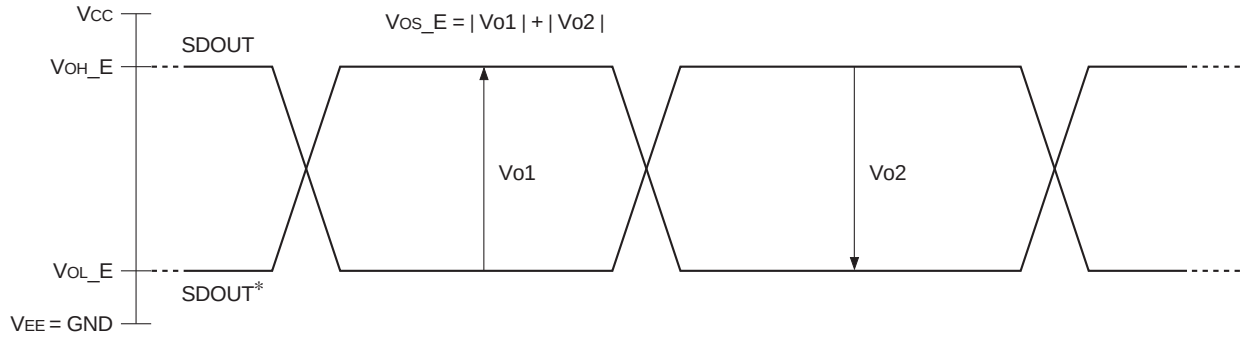
(V_{CC} = 3.135 to 3.465V, Ta = 0 to 70°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
TTL high level input voltage	V_{IH}_T		2		5.5	V
TTL low level input voltage	V_{IL}_T		0		0.8	V
TTL high level input current	I_{IH}_T	V_{IN} = V_{CC}			20	µA
TTL low level input current	I_{IL}_T	V_{IN} = 0V	–400			µA
TTL high level output voltage	V_{OH}_T	I_{OH} = –0.4mA	2.2			V
TTL low level output voltage	V_{OL}_T	I_{OL} = 2mA			0.5	V
ECL high level input voltage	V_{IH}_E		V_{CC} – 1.17		V_{CC} – 0.88	V
ECL low level input voltage	V_{IL}_E		V_{CC} – 1.81		V_{CC} – 1.48	V
ECL differential input voltage amplitude	V_{IS}_E*1	AC coupling input, peak-to-peak	200		2000	mV
ECL differential output voltage amplitude	V_{OS}_E*2	Peak-to-peak	1200		2000	mV
Current consumption	I_{CC}	Output pins open		188	255	mA
Power consumption	P_D	Output pins open		620	870	mW

*1 ECL differential input voltage amplitude



*2 ECL differential output voltage amplitude



AC Characteristics (V_{CC} = 3.135 to 3.465V, Ta = 0 to 70°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
TX TTL input rise time	Tir_Tx	0.8 to 2.0V	0.7		4.8	ns
TX TTL input fall time	Tif_Tx	2.0 to 0.8V	0.7		4.8	ns
REFCLK input rise time	Tir_REF	0.8 to 2.0V	0.7		2.4	ns
REFCLK input fall time	Tif_REF	2.0 to 0.8V	0.7		2.4	ns
TTL output rise time	Tor_T	0.8 to 2.0V, CL = 10pF			3.5	ns
TTL output fall time	Tof_T	2.0 to 0.8V, CL = 10pF			3.5	ns
ECL output rise time	Tor_E	20 to 80%, CL = 2pF			400	ps
ECL output fall time	Tof_E	80 to 20%, CL = 2pF			400	ps
Operating transfer rate	Br		1.052		1.262	Gbps
REFCLK frequency	F_REF		105.2		126.2	MHz
REFCLK frequency tolerance	Ftol_REF		–100		100	ppm
TXPLL/RXPLL frequency pull-in time	Tfa	Loop damping capacitance = 0.01µF			500	µs
RXPLL bit synchronization time	Tbs	Loop damping capacitance = 0.01µF			2500	bit
TX serial output jitter Random	RJ	TX output data K28.7		6.2		ps
TX serial output jitter Deterministic	DJ	TX output data ±K28.5		24	60	ps

Description of Operation

1. Transmitter block

The input 10-bit parallel data (TX0 to TX9) is latched by the external reference clock (REFCLK), converted from parallel to serial (Parallel to Serial CONV.), and output as serial data (SDOUT/SDOUT*).

The TXPLL multiplies REFCLK by 10 times to generate TCLK, and then frequency-divides this by 1/10 to generate LCLK. Parallel/serial conversion uses these TCLK and LCLK as the clocks. [See P10 "Timing Charts 1) Transmitter block".]

2. Receiver block

The RXPLL recovers RCLK from the input serial data (SDIN/SDIN*), uses this RCLK to retime the serial data and outputs it as RDATA. The DIV (divider) frequency-divides RCLK by 1/10 to generate FCLK, and RDATA is converted from serial to parallel (Serial to Parallel CONV.) using these two clocks (RCLK and FCLK). At the same time the byte synchronization signal (Comma detect word) is detected during Serial to Parallel CONV., and 10-bit parallel data (RX0 to RX9) and the sync signal (BYTSYNC) are output. FCLK is initialized and the 10-bit parallel data is byte synchronized using this sync signal. RBC differentially outputs the clocks (RBC1 and RBC0) obtained by 1/20 frequency-dividing TCLK for loading the 10-bit parallel data. [See P11 "Timing Charts 2) Receiver block".]

a. Input serial data amplitude detection

   The serial data input block has the amplitude detection and amplitude control circuits. When the differential amplitude of the input signal is 100mVp-p or less, the input signal is cut and the output is fixed to high level. All parallel output data (RX0 to RX9) are high.

b. Frequency autolock

   If LCKREF* is set high while recovering RCLK with the RXPLL, autolock mode results. In autolock mode, RCLK is locked to 10 times REFCLK when the input serial data is no signal, or to the clock component of the serial data when serial data is input.

   When LCKREF* is set low, RCLK is forcibly locked to 10 times REFCLK.

c. Byte synchronization

   When BYTSYNCEN is set high, Comma data within the input serial data is detected, and the detection signal and byte synchronized 10-bit parallel data are output. At this time RBC1 and RBC0 are also initialized and output.

   When BYTSYNCEN is set low, the 10-bit parallel data is output in the arbitrary order and the RBC1 and RBC0 edges also rise at the arbitrary position.

d. Differential clock output (RBC1 and RBC0)

   RBC1 and RBC0 output at the positive phase when byte synchronization is synchronized properly and Comma data is detected one time or more. RBC1 and RBC0 are extended when byte synchronization is asynchronous and Comma data is detected one time.

e. Loop back

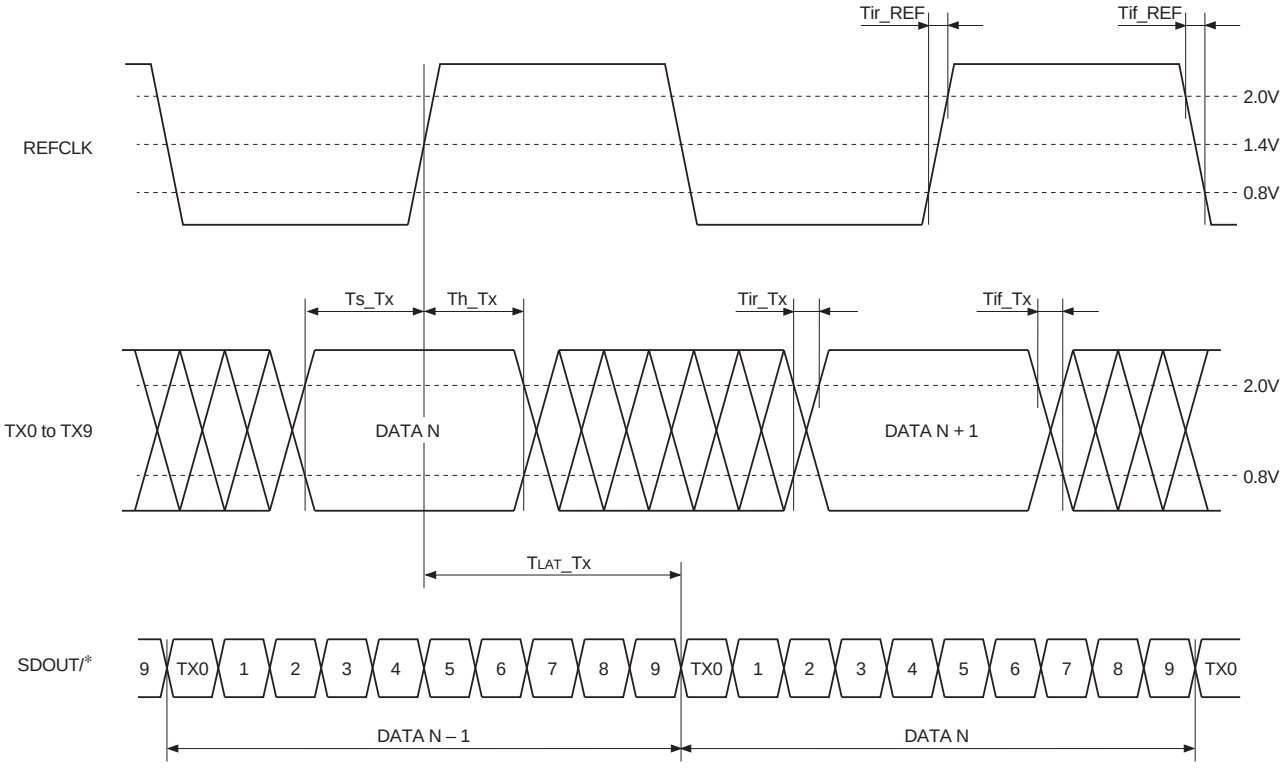
   When LBEN is set high, the serial data is looped back internally. Set LBEN low to perform transmit and receive.

Timing Charts

1) Transmitter block

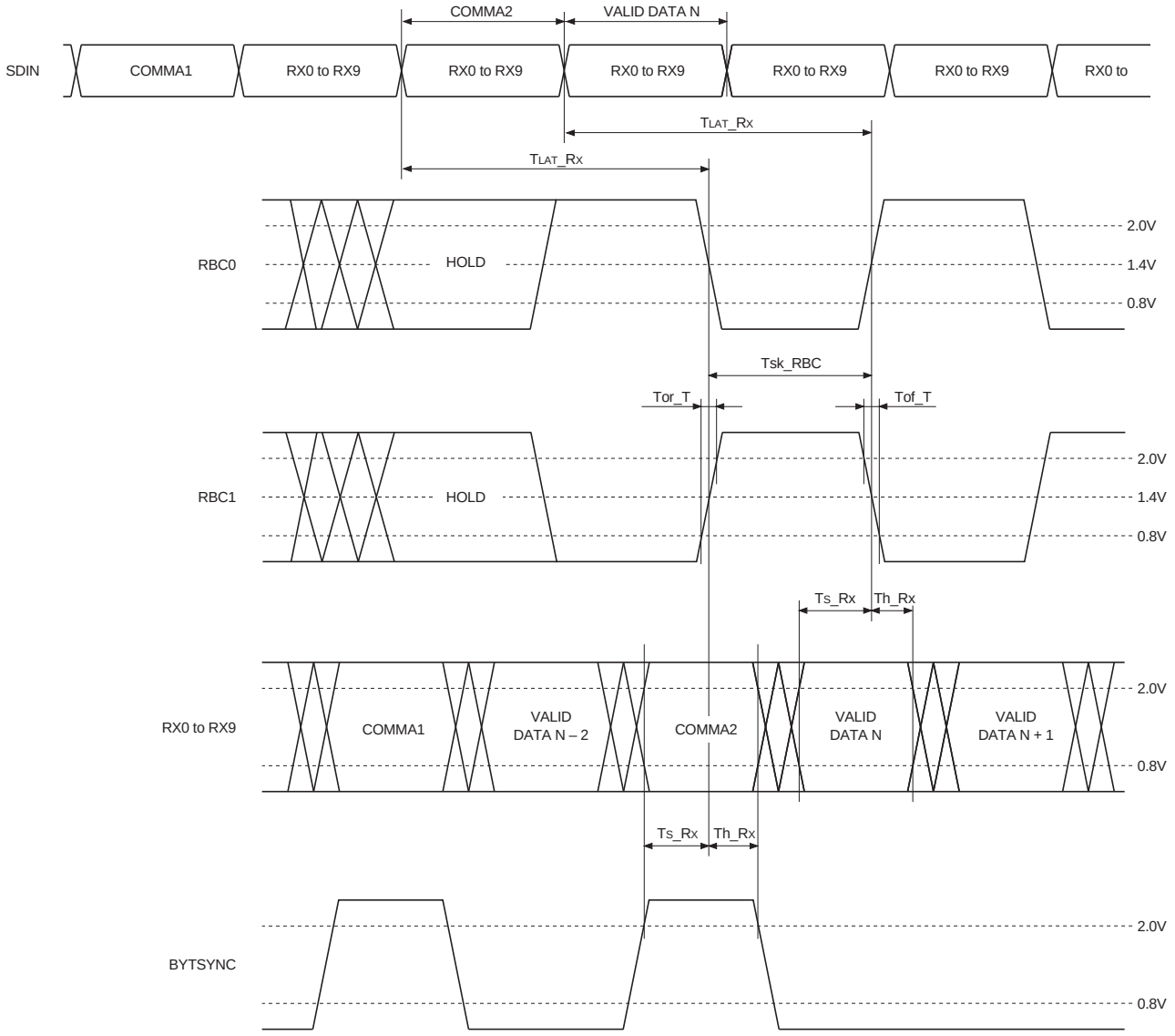
(V_{CC} = 3.3V, Ta = 25°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
TX setup time	Ts_Tx		2.0			ns
TX hold time	Th_Tx		1.5			ns
Latency time	T_{LAT}_Tx	1.0625GHz		4.7		ns
REFCLK input rise time	Tir_REF	0.8 to 2.0V	0.7		2.4	ns
REFCLK input fall time	Tif_REF	2.0 to 0.8V	0.7		2.4	ns
TX TTL input rise time	Tir_Tx	0.8 to 2.0V	0.7		4.8	ns
TX TTL input fall time	Tif_Tx	2.0 to 0.8V	0.7		4.8	ns

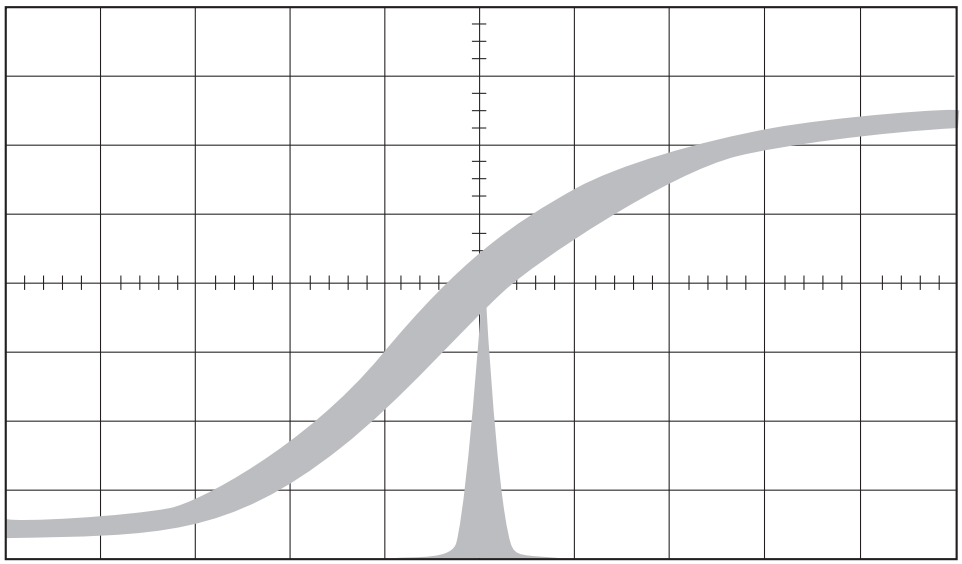


2) Receiver block (V_{CC} = 3.3V, Ta = 25°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
RX setup time	Ts_Rx	1.0625GHz	3.0			ns
		1.25GHz	2.5			ns
RX hold time	Th_Rx	1.0625GHz	1.5			ns
		1.25GHz	1.0			ns
Skew between RBC0 and RBC1	T_{SK}_RBC	1.0625GHz	8.91	9.41	9.91	ns
Latency time	T_{LAT}_Rx	1.0625GHz		18.0		ns
TTL output rise time	Tor_T	0.8 to 2.0V, CL = 10pF			3.5	ns
TTL output fall time	Tof_T	2.0 to 0.8V, CL = 10pF			3.5	ns

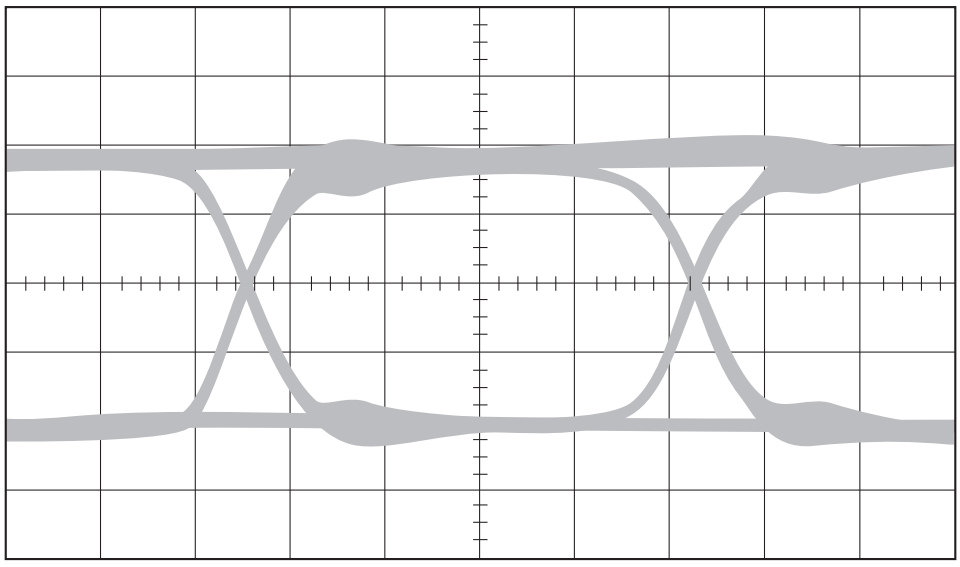


Example of Representative Characteristics



Random jitter 6.7ps (RMS)
X: 50ps/div
Y: 100mV/div
1.0625GHz mode

a) TX random jitter (SDOUT)

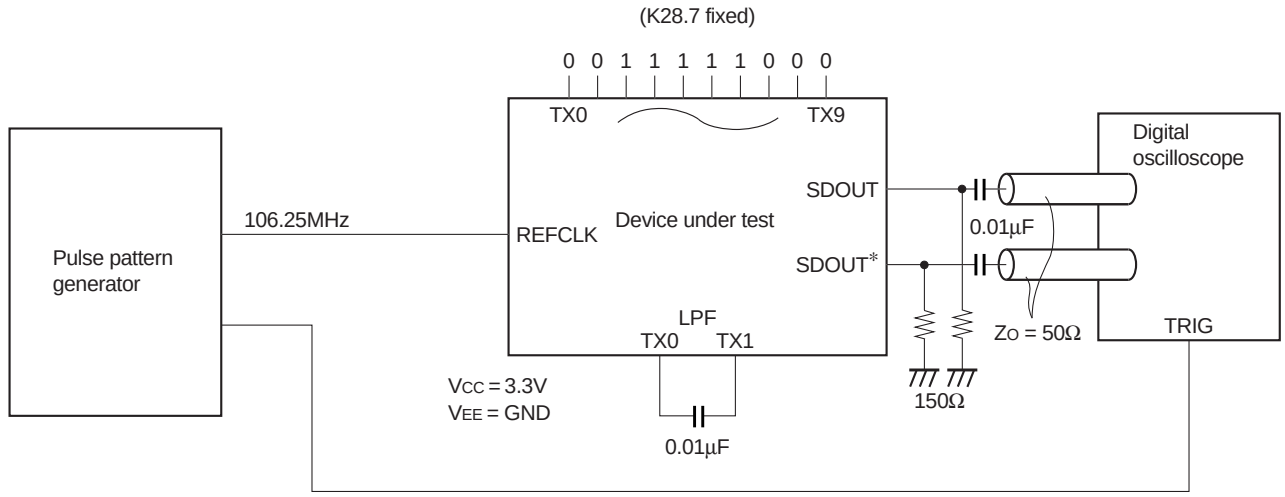


X: 200ps/div
Y: 200mV/div
1.0625GHz mode

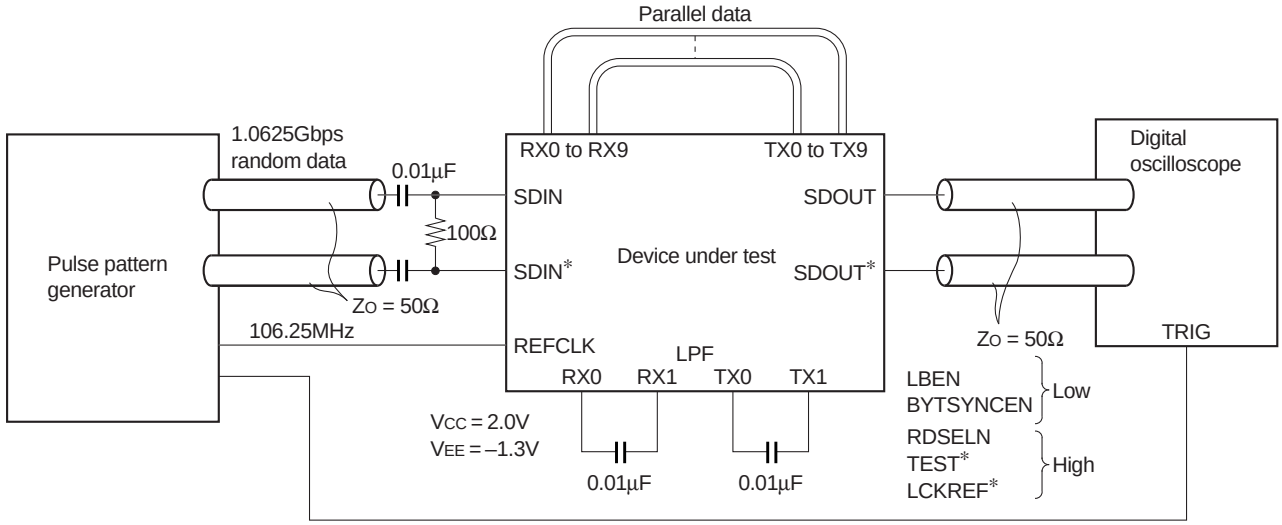
b) TX eye pattern (SDOUT)

Electrical Characteristics Measurement Circuit

a) TX random jitter



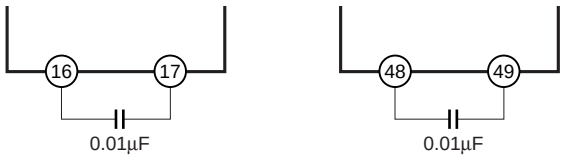
b) TX eye pattern



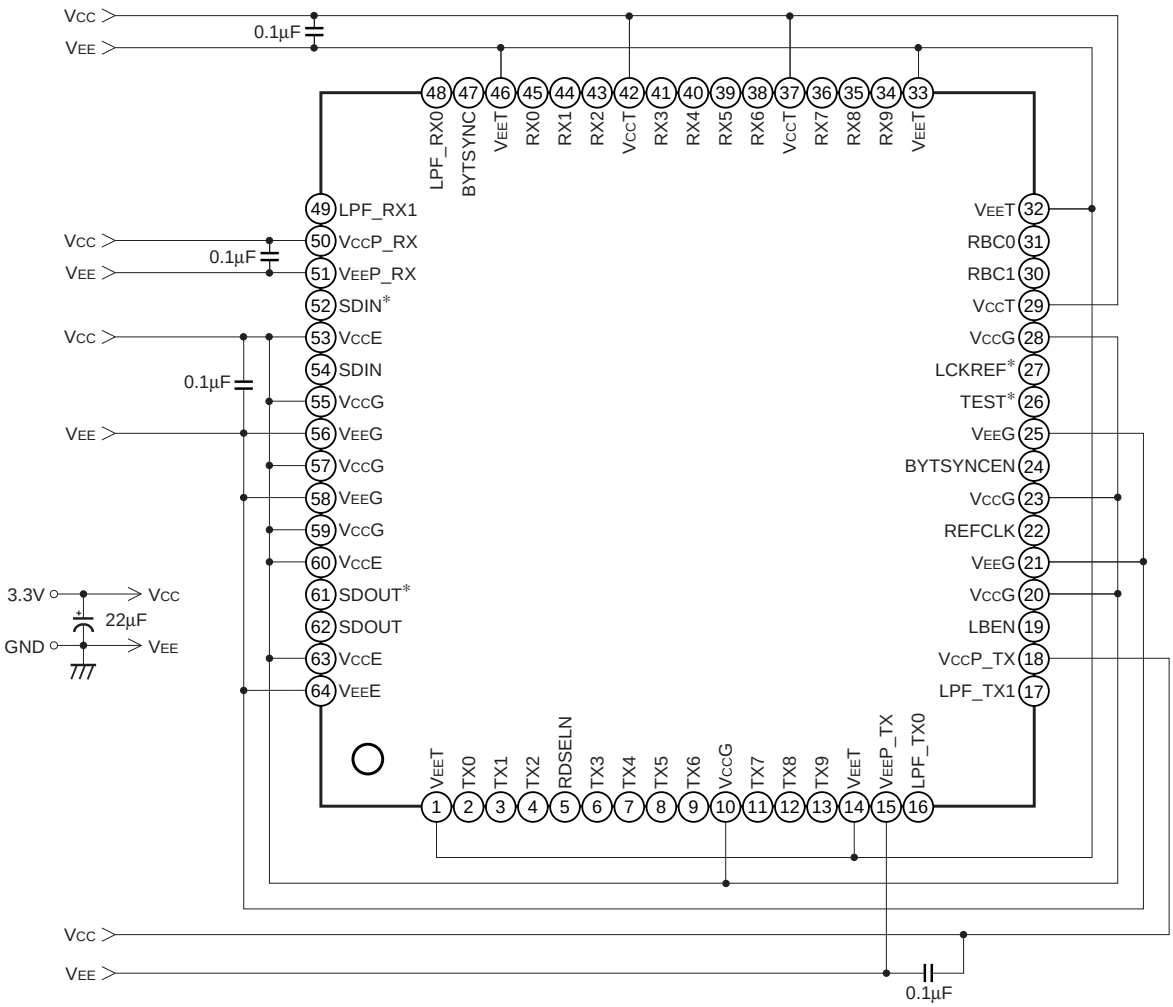
Notes on Operation

1. External loop filters

Connect 0.01µF capacitors as close to the two sets of external loop filter pins as possible.

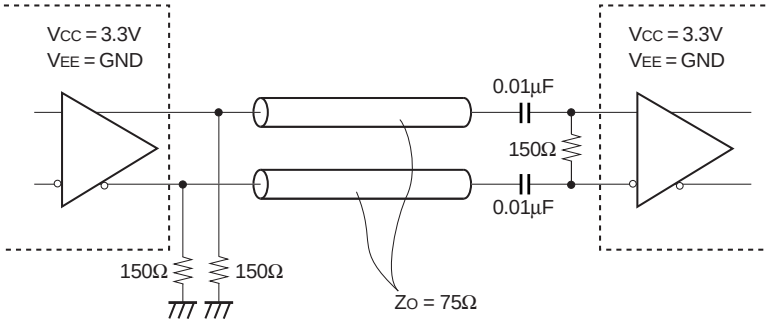


2. Example of power supply circuit



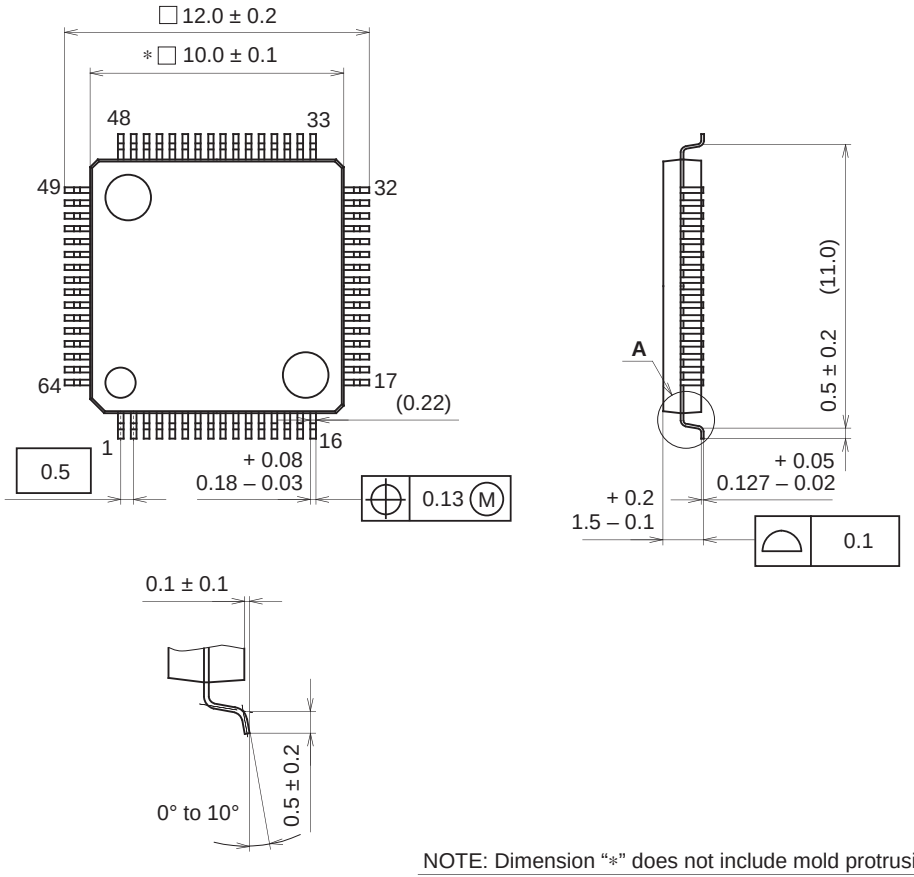
22µF is an electrolytic capacitor, and should be located as close to the power supply as possible.
0.1µF are ceramic capacitors, and should be located as close to the IC power supply pins as possible.

3. Serial data I/O



Package Outline Unit: mm

64PIN LQFP (PLASTIC)



NOTE: Dimension "*" does not include mold protrusion.

DETAIL **A**

SONY CODE	LQFP-64P-L01
EIAJ CODE	LQFP064-P-1010
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.3g

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).