PRODUCT PREVIEW

87C196LB
CHMOS 16-BIT MICROCONTROLLER

Automotive

- **20 MHz operation†**
- **24 Kbytes of on-chip OTPROM**
- **768 bytes of on-chip register RAM**
- **Register-to-register architecture**
- **Peripheral transaction server (PTS) with high-speed, microcoded interrupt service routines**
- **Integrated, industry-standard J1850 communication protocol**
- **Six-channel/10-bit A/D with sample and hold**
- **High-speed event processor array**
  - **— Six capture/compare channels**
  - **— Two compare-only channels**
  - **— Two 16-bit software timers**
- **Full-duplex serial I/O port with dedicated baud-rate generator**
- **Enhanced full-duplex, synchronous serial I/O port (SSIO)**
- **Programmable 8- or 16-bit external bus**
- **Optional clock doubler with programmable clock output signal**
- **SFR register that indicates the source of the last reset**
- **Design enhancements for EMI reduction**
- **Oscillator failure detection circuitry**
- **Watchdog timer (WDT)**
- **–40° C to +125° C ambient temperature**
- **52-pin PLCC package**

† 16 MHz standard; 20 MHz is speed premium

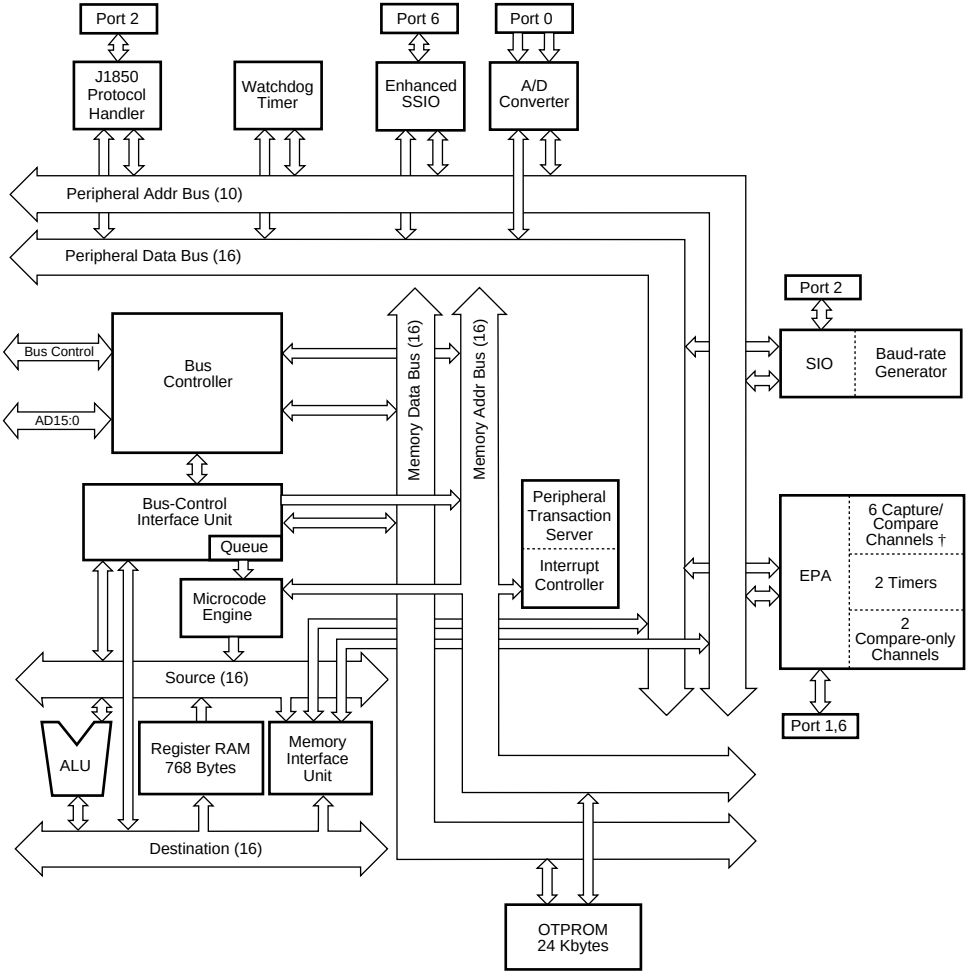
NOTE

This datasheet contains information on products in the design phase of development. The specifications are subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

The 87C196LB is a high-performance 16-bit microcontroller with integrated support for the J1850 communication protocol. The 87C196LB is composed of a high-speed core with the following peripherals: an asynchronous/synchronous serial I/O port (8096 compatible) with a dedicated 16-bit baud-rate generator; an additional synchronous serial I/O port with full duplex master/slave transceivers; a six-channel A/D converter with sample and hold; a flexible timer/counter structure with prescaler, cascading, and quadrature capabilities; six modularized, multiplexed high-speed I/O for capture and compare (called event processor array) with 200 ns resolution and double buffered inputs; and a sophisticated prioritized interrupt structure with programmable peripheral transaction server (PTS). The clock doubler circuitry and oscillator output signal enable a 4 MHz resonator to achieve the same internal clock speed as a more costly 8 MHz resonator in previous applications. This same circuitry can drive other devices where a separate resonator was required in the past. Another cost-savings feature is the fact that the I/O ports are driven low at reset, avoiding the need for pull-up resistors.

Preliminary Information

February 1996 **Order Number:** 272807-000



† Two additional capture/compare channels (EPA6 and EPA7) are available as software timers. They are not connected to package pins.

A3416-01

Figure 1. 87C196LB Block Diagram

1.0 NOMENCLATURE OVERVIEW

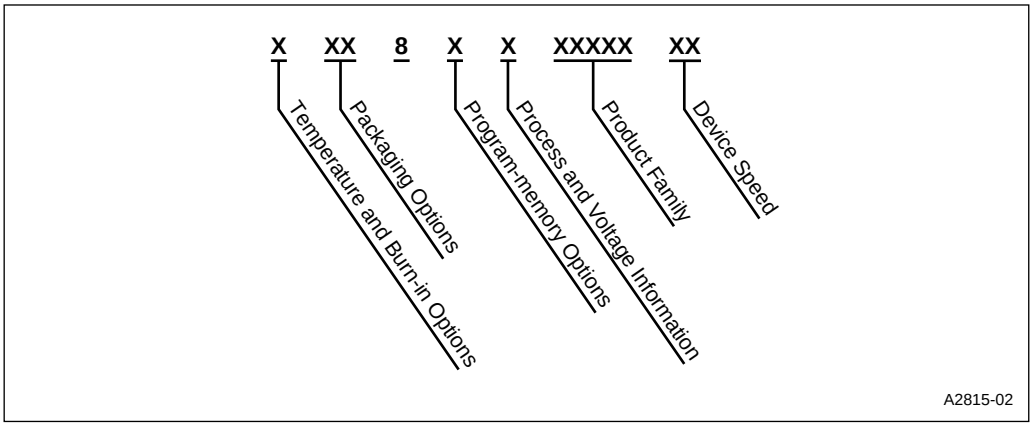


Figure 2. Product Nomenclature

Table 1. Description of Product Nomenclature

Parameter	Options	Description
Temperature and Burn-in Options	A	Automotive operating temperature range (–40° C to 125° C ambient) with Intel standard burn-in.
Packaging Options	N	PLCC
Program-memory Options	7	OTPROM
Process Information	C	CHMOS
Product Family	196L*x*	8XC196L*x* family of products
Device Speed	no mark 20	16 MHz 20 MHz

2.0 PINOUT

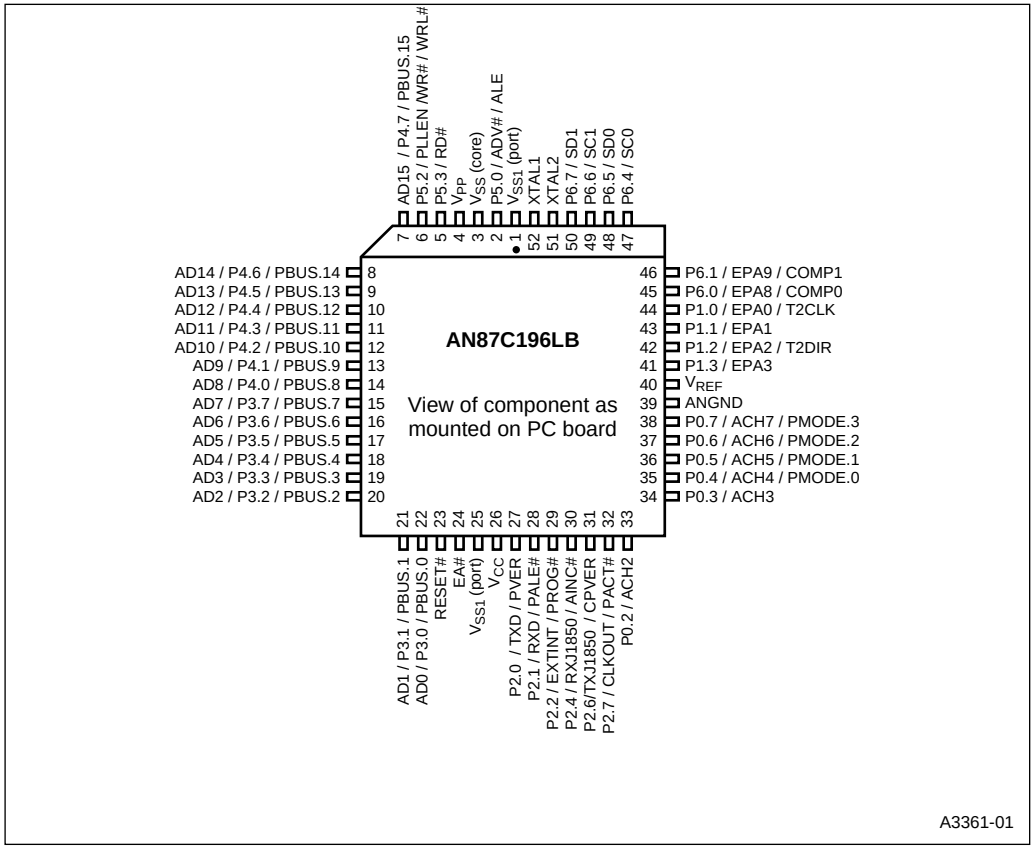


Figure 3. 87C196LB 52-pin Package

Table 2. 87C196LB 52-pin Package Pin Assignments

Pin	Name	Pin	Name	Pin	Name
1	V_{SS1} (port)	19	AD3 / P3.3 / PBUS.3	37	P0.6 / ACH6 / PMODE.2
2	P5.0 / ADV# / ALE	20	AD2 / P3.2 / PBUS.2	38	P0.7 / ACH7 / PMODE.3
3	V_{SS} (core)	21	AD1 / P3.1 / PBUS.1	39	ANGND
4	V_{PP}	22	AD0 / P3.0 / PBUS.0	40	V_{REF}
5	P5.3 / RD#	23	RESET#	41	P1.3 / EPA3
6	P5.2 / PLLEN / WR# / WRL#	24	EA#	42	P1.2 / EPA2 / T2DIR
7	AD15 / P4.7 / PBUS.15	25	V_{SS1} (port)	43	P1.1 / EPA1
8	AD14 / P4.6 / PBUS.14	26	V_{CC}	44	P1.0 / EPA0 / T2CLK
9	AD13 / P4.5 / PBUS.13	27	P2.0 / TXD / PVER	45	P6.0 / EPA8 / COMP0
10	AD12 / P4.4 / PBUS.12	28	P2.1 / RXD / PALE#	46	P6.1 / EPA9 / COMP1
11	AD11 / P4.3 / PBUS.11	29	P2.2 / EXTINT / PROG#	47	P6.4 / SC0
12	AD10 / P4.2 / PBUS.10	30	P2.4 / RXJ1850 / AINC#	48	P6.5 / SD0
13	AD9 / P4.1 / PBUS.9	31	P2.6 / TXJ1850 / CPVER	49	P6.6 / SC1
14	AD8 / P4.0 / PBUS.8	32	P2.7 / CLKOUT / PACT#	50	P6.7 / SD1
15	AD7 / P3.7 / PBUS.7	33	P0.2 / ACH2	51	XTAL2
16	AD6 / P3.6 / PBUS.6	34	P0.3 / ACH3	52	XTAL1
17	AD5 / P3.5 / PBUS.5	35	P0.4 / ACH4 / PMODE.0		
18	AD4 / P3.4 / PBUS.4	36	P0.5 / ACH5 / PMODE.1		

Table 3. Pin Assignment Arranged by Functional Categories

Addr & Data	
Name	**Pin**
AD0	22
AD1	21
AD2	20
AD3	19
AD4	18
AD5	17
AD6	16
AD7	15
AD8	14
AD9	13
AD10	12
AD11	11
AD12	10
AD13	9
AD14	8
AD15	7

Input/Output	
Name	**Pin**
P0.2 / ACH2	33
P0.3 / ACH3	34
P0.4 / ACH4	35
P0.5 / ACH5	36
P0.6 / ACH6	37
P0.7 / ACH7	38
P1.0 / EPA0 / T2CLK	44
P1.1 / EPA1	43
P1.2 / EPA2 / T2DIR	42
P1.3 / EPA3	41
P2.0 / TXD	27

Input/Output (Cont'd)	
Name	**Pin**
P2.1 / RXD	28
P2.2	29
P2.4 / RXJ1850	30
P2.6 / TXJ1850	31
P2.7	32
P3.0	22
P3.1	21
P3.2	20
P3.3	19
P3.4	18
P3.5	17
P3.6	16
P3.7	15
P4.0	14
P4.1	13
P4.2	12
P4.3	11
P4.4	10
P4.5	9
P4.6	8
P4.7	7
P5.0	2
P5.2	6
P5.3	5
P6.0 / EPA8 / COMP0	45
P6.1 / EPA9 / COMP1	46
P6.4 / SC0	47
P6.5 / SD0	48
P6.6 / SC1	49
P6.7 / SD1	50

Program Control	
Name	**Pin**
AINC#	30
CPVER	31
PACT#	32
PALE#	28
PBUS.0	22
PBUS.1	21
PBUS.2	20
PBUS.3	19
PBUS.4	18
PBUS.5	17
PBUS.6	16
PBUS.7	15
PBUS.8	14
PBUS.9	13
PBUS.10	12
PBUS.11	11
PBUS.12	10
PBUS.13	9
PBUS.14	8
PBUS.15	7
PMODE.0	35
PMODE.1	36
PMODE.2	37
PMODE.3	38
PROG#	29
PVER	27

Processor Control	
Name	**Pin**
EA#	24
EXTINT	29
PLLEN	6
RESET#	23
XTAL1	52
XTAL2	51

Bus Cont & Status	
Name	**Pin**
ADV# / ALE	2
CLKOUT	32
RD#	5
WR# / WRL#	6

Power & Ground	
Name	**Pin**
ANGND	39
V_{CC}	26
V_{PP}	4
V_{REF}	40
V_{SS} (core)	3
V_{SS1} (port)	1, 25

3.0 SIGNALS

Table 4. Signal Descriptions

Name	Type	Description
ACH7:2	I	Analog Channels These signals are analog inputs to the A/D converter. The A/D inputs share package pins with port 0. These pins may individually be used as analog inputs (ACH*x*) or digital inputs (P0.*y*). While it is possible for the pins to function simultaneously as analog and digital inputs, this is not recommended because reading port 0 while a conversion is in process can produce unreliable conversion results. The ANGND and V_{REF} pins must be connected for the A/D converter and port 0 to function. ACH7:2 share package pins with the following signals: ACH2/P0.2, ACH3/P0.3, ACH4/P0.4/PMODE.0, ACH5/P0.5/PMODE.1, ACH6/P0.6/PMODE.2, and ACH7/P0.7/PMODE.3.
AD15:0	I/O	Address/Data Lines These pins provide a multiplexed address and data bus. During the address phase of the bus cycle, address bits 0–15 are presented on the bus and can be latched using ALE or ADV#. During the data phase, 8- or 16-bit data is transferred. AD7:0 share package pins with P3.7:0 and PBUS.7:0; AD15:8 share package pins with P4.7:0 and PBUS.15:8.
ADV#	O	Address Valid This active-low output signal is asserted only during external memory accesses. ADV# indicates that valid address information is available on the system address/data bus. The signal remains low while a valid bus cycle is in progress and is returned high as soon as the bus cycle completes. An external latch can use this signal to demultiplex the address from the address/data bus. A decoder can also use this signal to generate chip selects for external memory. ADV# shares a package pin with P5.0 and ALE.
AINC#	I	Auto Increment During slave programming, this active-low input enables the auto-increment feature. (Auto increment allows reading or writing of sequential OTPROM locations, without requiring address transactions across the PBUS for each read or write.) AINC# is sampled after each location is programmed or dumped. If AINC# is asserted, the address is incremented and the next data word is programmed or dumped. AINC# shares package pins with P2.4 and RXJ1850.
ALE	O	Address Latch Enable This active-high output signal is asserted only during external memory cycles. ALE signals the start of an external bus cycle and indicates that valid address information is available on the system address/data bus. An external latch can use this signal to demultiplex the address from the address/data bus. ALE shares a package pin with P5.0 and ADV#.

Table 4. Signal Descriptions (Continued)

Name	Type	Description
ANGND	GND	Analog Ground ANGND must be connected for A/D converter and port 0 operation. ANGND and V_{SS} should be nominally at the same potential.
CLKOUT	O	Output Output of the internal clock generator. You can select one of three frequencies: f, f/2, or f/4. CLKOUT has a 50% duty cycle. CLKOUT shares a package pin with P2.7 and PACT#.
COMP1:0	O	Event Processor Array (EPA) Compare Pins These signals are the outputs of the EPA compare-only channels. COMP1:0 share package pins with the following signals: COMP0/P6.0/EPA8 and COMP1/P6.1/EPA9.
CPVER	O	Cumulative Program Verification During slave programming, a high signal indicates that all locations programmed correctly, while a low signal indicates that an error occurred during one of the programming operations. CPVER shares a package pin with P2.6, TXJ1850, and ONCE#.
EA#	I	External Access This input determines whether memory accesses to special-purpose and program memory partitions are directed to internal or external memory. These accesses are directed to internal memory if EA# is held high and to external memory if EA# is held low. For an access to any other memory location, the value of EA# is irrelevant. EA# also controls entry into the programming modes. If EA# is at V_{PP} voltage (typically +12.5 V) on the rising edge of RESET#, the microcontroller enters a programming mode. **NOTE:** Systems with EA# tied inactive have idle time between external bus cycles. When the address/data bus is idle, you can use ports 3 and 4 for I/O. Systems with EA# tied active cannot use ports 3 and 4 as standard I/O; when EA# is active, these ports will function only as the address/data bus. When EA# is active, a read or write to P3_REG, P4_REG, P3_PIN, or P4_PIN accesses the corresponding location (1FFCH, 1FFDH, 1FFEH, or 1FFFH) in external memory. EA# is sampled and latched only on the rising edge of RESET#. Changing the level of EA# after reset has no effect.
EPA9:8 EPA3:0	I/O	Event Processor Array (EPA) Capture/Compare Channels High-speed input/output signals for the EPA capture/compare channels. The EPA signals share package pins with the following signals: EPA0/P1.0/T2CLK, EPA1/P1.1, EPA2/P1.2/T2DIR, EPA3/P1.3, EPA8/P6.0/COMP0, and EPA9/P6.1/COMP1. EPA7:6 do not connect to package pins. They cannot be used to capture an event, but they can function as software timers. EPA5:4 are not implemented.

Table 4. Signal Descriptions (Continued)

Name	Type	Description
EXTINT	I	External Interrupt In normal operating mode, a rising edge on EXTINT sets the EXTINT interrupt pending bit. EXTINT is sampled during phase 2. The minimum high time is one state time. In powerdown mode, asserting the EXTINT signal for at least 50 ns causes the device to resume normal operation. The interrupt need not be enabled. If the EXTINT interrupt is enabled, the CPU executes the interrupt service routine. Otherwise, the CPU executes the instruction that immediately follows the command that invoked the power-saving mode. In idle mode, asserting any enabled interrupt causes the device to resume normal operation. EXTINT shares a package pin with P2.2 and PROG#.
P0.7:2	I	Port 0 This is a high-impedance, input-only port. Port 0 pins should **not** be left floating. The port 0 signals share package pins with the A/D inputs. These pins may individually be used as analog inputs (ACH*x*) or digital inputs (P0.*y*). While it is possible for the pins to function simultaneously as analog and digital inputs, this is not recommended because reading port 0 while a conversion is in process can produce unreliable conversion results. ANGND and V_{REF} must be connected for port 0 to function. P0.3:2 share package pins with ACH3:2 and P0.7:4 share package pins with ACH7:4 and PMODE.3:0.
P1.3:0	I/O	Port 1 This is a standard bidirectional port that shares package pins with individually selectable special-function signals. Port 1 shares package pins with the following signals: P1.0/EPA0/T2CLK, P1.1/EPA1, P1.2/EPA2/T2DIR, P1.3/EPA3.
P2.7:6 P2.4 P2.2:0	I/O	Port 2 This is a standard bidirectional port that shares package pins with individually selectable special-function signals. Port 2 shares package pins with the following signals: P2.0/TXD/PVER, P2.1/RXD/PALE#, P2.2/EXTINT/PROG#, P2.4/AINC#/RXJ1850, P2.6/TXJ1850/ONCE#/CPVER, P2.7/OSCOUT/PACT#.
P3.7:0	I/O	Port 3 This is a memory-mapped, 8-bit, bidirectional port with programmable open-drain or complementary output modes. The pins are shared with the multiplexed address/data bus, which has complementary drivers.. P3.7:0 share package pins with AD7:0 and PBUS.7:0.
P4.7:0	I/O	Port 4 This is a memory-mapped, 8-bit, bidirectional port with open-drain or complementary output modes. The pins are shared with the multiplexed address/data bus, which has complementary drivers. P4.7:0 share package pins with AD15:8 and PBUS.15:8.

Table 4. Signal Descriptions (Continued)

Name	Type	Description
P5.3:2 P5.0	I/O	Port 5 This is a memory-mapped, bidirectional port. Port 5 shares package pins with the following signals: P5.0/ADV#/ALE, P5.2/WR#/WRL#/PLLEN, and P5.3/RD#. P5.1 and P5.7:4 are not implemented.
P6.7:4 P6.1:0	O	Port 6 This is a standard bidirectional port. Port 6 shares package pins with the following signals: P6.0/EPA8/COMP0, P6.1/EPA9/COMP1, P6.4/SC0, P6.5/SD0, P6.6/SC1, and P6.7/SD1.
PACT#	O	Programming Active During auto programming or ROM-dump, a low signal indicates that programming or dumping is in progress, while a high signal indicates that the operation is complete. PACT# is multiplexed with P2.7 and OSCOUT.
PALE#	I	Programming ALE During slave programming, a falling edge causes the device to read a command and address from the PBUS. PALE# is multiplexed with P2.1 and RXD.
PBUS.15:0	I/O	Address/Command/Data Bus During slave programming, ports 3 and 4 serve as a bidirectional port with open-drain outputs to pass commands, addresses, and data to or from the device. Slave programming requires external pull-up resistors. During auto programming and ROM-dump, ports 3 and 4 serve as a regular system bus to access external memory. P4.6 and P4.7 are left unconnected; P1.1 and P1.2 serve as the upper address lines. **Slave programming:** PBUS.7:0 share package pins with AD7:0 and P3.7:0. PBUS.15:8 share package pins with AD15:8 and P4.7:0. **Auto programming:** PBUS.15:8 share package pins with AD15:8 and P4.7:0; PBUS.7:0 share package pins with AD7:0 and P3.7:0.
PLLEN	I	Phase-locked Loop Enable This active-high input pin enables the on-chip clock multiplier.
PMODE.3:0	I	Programming Mode Select Determines the programming mode. PMODE is sampled after a device reset and must be static while the microcontroller is operating. PMODE.3:0 are multiplexed with P0.7:4 and ACH7:4.

Table 4. Signal Descriptions (Continued)

Name	Type	Description
PROG#	I	Programming Start During programming, a falling edge latches data on the PBUS and begins programming, while a rising edge ends programming. The current location is programmed with the same data as long as PROG# remains asserted, so the data on the PBUS must remain stable while PROG# is active. During a word dump, a falling edge causes the contents of an OTPROM location to be output on the PBUS, while a rising edge ends the data transfer. PROG# is multiplexed with P2.2 and EXTINT.
PVER	O	Program Verification During slave or auto programming, PVER is updated after each programming pulse. A high output signal indicates successful programming of a location, while a low signal indicates a detected error. PVER is multiplexed with P2.0 and TXD.
RD#	O	Read Read-signal output to external memory. RD# is asserted only during external memory reads. RD# shares a package pin with P5.3.
RESET#	I/O	Reset A level-sensitive reset input to and open-drain system reset output from the microcontroller. Either a falling edge on RESET# or an internal reset turns on a pull-down transistor connected to the RESET# pin for 16 state times. In the powerdown and idle modes, asserting RESET# causes the chip to reset and return to normal operating mode. After a device reset, the first instruction fetch is from 2080H.
RXJ1850	I	Receive This signal carries messages from an off-chip, J1850 transceiver to the integrated J1850 module. RXJ1850 shares a package pin with P2.4 and AINC#.
RXD	I/O	Receive Serial Data In modes 1, 2, and 3, RXD receives serial port input data. In mode 0, it functions as either an input or an open-drain output for data. RXD shares a package pin with P2.1 and PALE#.
SC1:0	I/O	Clock Pins for SSIO0 and 1 For handshaking mode, configure SC1:0 as open-drain outputs. This pin carries a signal only during receptions and transmissions. When the SSIO port is idle, the pin remains either high (with handshaking) or low (without handshaking). SC0 shares a package pin with P6.4, and SC1 shares a package pin with P6.6.
SD1:0	I/O	Data Pins for SSIO0 and 1 These pins are the data I/O pins for SSIO0 and 1. SD0 shares a package pin with P6.5, and SD1 shares a package pin with P6.7.

Table 4. Signal Descriptions (Continued)

Name	Type	Description
T2CLK	I	Timer 2 External Clock External clock for timer 2. Timer 2 increments (or decrements) on both rising and falling edges of T2CLK. It is also used in conjunction with T2DIR for quadrature counting mode. T2CLK shares a package pin with P1.0 and EPA0.
T2DIR	I	Timer 2 External Direction External direction (up/down) for timer 2. Timer 2 increments when T2DIR is high and decrements when it is low. It is also used in conjunction with T2CLK for quadrature counting mode. T2DIR shares a package pin with P1.2 and EPA2.
TXJ1850	O	Transmit This signal carries messages from the integrated J1850 module to an off-chip J1850 transceiver. TXJ1850 must not be driven high during reset and should only be used as an output. TXJ1850 shares a package pin with P2.6, ONCE#, and CPVER.
TXD	O	Transmit Serial Data In serial I/O modes 1, 2, and 3, TXD transmits serial port output data. In mode 0, it is the serial clock output. TXD shares a package pin with P2.0 and PVER.
V_{CC}	PWR	Digital Supply Voltage Connect each V_{CC} pin to the digital supply voltage.
V_{PP}	PWR	Programming Voltage V_{PP} causes the device to exit powerdown mode when it is driven low for at least 50 ns. Use this method to exit powerdown only when using an external clock source because it enables the internal phase clocks, but not the internal oscillator. If you do not plan to use the powerdown feature, connect V_{PP} to V_{CC}.
V_{REF}	PWR	Reference Voltage for the A/D Converter This pin supplies operating voltage to the A/D converter.
V_{SS}, V_{SS1}	GND	Digital Circuit Ground (Core Ground, Port Ground) These pins supply ground for the digital circuitry. Connect each V_{SS} and V_{SS1} pin to ground through the lowest possible impedance path. V_{SS} pins are connected to the core ground region of the microcontroller, while V_{SS1} pins are connected to the port ground region. (ANGND is connected to the analog ground region.) Separating the ground regions provides noise isolation.

Table 4. Signal Descriptions (Continued)

Name	Type	Description
WR#	O	Write† This active-low output indicates that an external write is occurring. This signal is asserted only during external memory writes. Forcing WR# high while RESET# is low, causes the device to enter PLL-bypass mode. When the device is in PLL-bypass mode, the internal phase clocks operate at one-half the frequency of the frequency on XTAL1. WR# shares a package pin with P5.2, WRL#, and PLLEN. † The chip configuration register 0 (CCR0) determines whether this pin functions as WR# or WRL#. CCR0.2 = 1 selects WR#; CCR0.2 = 0 selects WRL#.
WRL#	O	Write Low† During 16-bit bus cycles, this active-low output signal is asserted for low-byte writes and word writes to external memory. During 8-bit bus cycles, WRL# is asserted for all write operations. WRL# shares package pin with P5.2, WR#, and PLLEN. † The chip configuration register 0 (CCR0) determines whether this pin functions as WR# or WRL#. CCR0.2 = 1 selects WR#; CCR0.2 = 0 selects WRL#.
XTAL1	I	Input Crystal/Resonator or External Clock Input Input to the on-chip oscillator and the internal clock generators. The internal clock generators provide the peripheral clocks, CPU clock, and CLKOUT signal. When using an external clock source instead of the on-chip oscillator, connect the clock input to XTAL1. The external clock signal must meet the V_{IH} specification for XTAL1.
XTAL2	O	Inverted Output for the Crystal/Resonator Output of the on-chip oscillator inverter. Leave XTAL2 floating when the design uses an external clock source instead of the on-chip oscillator.

4.0 ADDRESS MAP

Table 5. Address Map

Hex Address Range	Description	Addressing Modes
FFFF 8000	External device (memory or I/O) connected to address/data bus	Indirect or indexed
7FFF 2080	Program memory (internal nonvolatile or external memory); see Note 1	Indirect or indexed
207F 2000	Special-purpose memory (internal nonvolatile or external memory)	Indirect or indexed
1FFF 1FE0	Memory-mapped SFRs	Indirect or indexed
1FDF 1F00	Peripheral SFRs	Indirect, indexed, or windowed direct
1EFF 0300	External device (memory or I/O) connected to address/data bus; (future SFR expansion; see Note 2)	Indirect or indexed
02FF 0100	Upper register file (general-purpose register RAM)	Indirect, indexed, or windowed direct
00FF 0000	Lower register file (register RAM, stack pointer, and CPU SFRs)	Direct, indirect, or indexed

NOTES:
1. After a reset, the microcontroller fetches its first instruction from 2080H.
2. The content or function of these locations may change in future microcontroller revisions, in which case a program that relies on a location in this range might not function properly.

5.0 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –60°C to +150° C
Voltage from V_{PP} or EA# to V_{SS} or ANGND... –0.5V to +13.0 V
Voltage from any other pin to V_{SS} or ANGND ...–0.5V to +7.0V
Power Dissipation ..... 0.5 W

OPERATING CONDITIONS†

T_A (Ambient Temperature Under Bias).....–40°C to +125°C
V_{CC} (Digital Supply Voltage) ..... 4.50V to 5.50V
V_{REF} (Analog Supply Voltage).....4.50V to 5.50V
F_{XTAL1} (Input Frequency):
- PLL in 2x mode.....4 MHz to 10 MHz
- PLL in 1x mode.....8 MHz to 20 MHz

Notes
1. ANGND and V_{SS} should be nominally at the same potential.
2. V_{REF} should not exceed V_{CC} by more than 0.5V.

NOTICE: This document contains information on products in the design phase of development. Do not finalize a design with this information. Revised information will be published when the product is available. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

†***WARNING****: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

5.1 DC Characteristics

Table 6. DC Characteristics at V_{CC} = 4.5V to 5.5V

Symbol	Parameter	Min	Typical	Max	Units	Test Conditions (Note 4)
I_{CC}	V_{CC} supply current (–40° C to +125° C ambient)		50	TBD	mA	F_{XTAL1} = 20 MHz, $V_{CC} = V_{PP} = V_{REF}$ = 5.5V (While device is in reset)
I_{CC1}	Active mode supply current (typical)		50		mA	
I_{REF}	A/D reference supply current		2	TBD	mA	
I_{IDLE}	Idle mode current		15	TBD	mA	F_{XTAL1} = 20 MHz, $V_{CC} = V_{PP} = V_{REF}$ = 5.5V
I_{PD}	Powerdown mode current		50	TBD	µA	$V_{CC} = V_{PP} = V_{REF}$ = 5.5V (Note 6)
V_{IL}	Input low voltage (all pins)	– 0.5V		0.3 V_{CC}	V	
V_{IH}	Input high voltage (all pins)	0.7 V_{CC}		V_{CC} + 0.5	V	(Note 7)
V_{OL}	Output low voltage (outputs configured as complementary)			0.3 0.45 1.5	V V V	I_{OL} = 200 µA (Notes 3, 5) I_{OL} = 3.2 mA I_{OL} = 7.0 mA
V_{OH}	Output high voltage (outputs configured as complementary)	V_{CC} – 0.3 V_{CC} – 0.7 V_{CC} – 1.5			V V V	I_{OH} = – 200 µA (Notes 3, 5) I_{OH} = – 3.2 mA I_{OH} = – 7.0 mA
I_{LI}	Input leakage current (standard inputs)			± 8	µA	$V_{SS} \le V_{IN} \le V_{CC}$ (Note 2)
I_{LI1}	Input leakage current (port 0—A/D inputs)			± 1	µA	$V_{SS} \le V_{IN} \le V_{REF}$
I_{IH}	Input high current (NMI pin, bond PAO only)			+175	µA	$V_{SS} \le V_{IN} \le V_{CC}$
V_{OL2}	Output low voltage in reset			1	V	I_{OL} = 6 µA (Notes 1, 8)

NOTES:
1. All bidirectional pins except P5.1/INST and P2.7/CLKOUT which are excluded because they are not weakly pulled low in reset. Bidirectional pins include ports 1–6.
2. Standard input pins include XTAL1, EA#, RESET#, and ports 1–6 when configured as inputs.
3. All bidirectional pins when configured as complementary outputs.
4. Device is static and should operate below 1 Hz, but is only tested down to 4 MHz with the PLL enabled. With the PLL bypassed, the device is only tested down to 8MHz.
5. Maximum I_{OL}or I_{OH} currents per pin will be characterized and published at a later date. Target values are ± 10 mA.
6. Typicals are based on a limited number of samples and are not guaranteed. The values listed are at room temperature and $V_{REF} = V_{CC}$ = 5.5V.
7. V_{IH} max for port 0 is V_{REF} + 0.5V.
8. This specification is not tested in production and is based upon theoretical estimates and/or product characterization.

Table 6. DC Characteristics at V_{CC} = 4.5V to 5.5V (Continued)

Symbol	Parameter	Min	Typical	Max	Units	Test Conditions (Note 4)
I_{OL2}	Output low current in reset	TBD TBD TBD		TBD TBD TBD	µA µA µA	V_{OL2} = TBD V_{OL2} = TBD V_{OL2} = TBD
R_{RST}	Reset pullup resistor	6K		65K	Ω	
V_{OL3}	Output low voltage in reset (RESET# pin only)			0.3 0.5 0.8	V V V	I_{OL3} = 4 mA (Note 8) I_{OL3} = 6 mA I_{OL3} = 10 mA
V_{OL4}	Output low voltage in reset (P2.6 only)			1	V	I_{OL4} = TBD
C_S	Pin capacitance (any pin to V_{SS})			10	pF	F_{TEST} = 1.0 MHz
R_{WPU}	Weak pullup resistance (approximate)		150K		Ω	(Note 6)

NOTES:
1. All bidirectional pins except P5.1/INST and P2.7/CLKOUT which are excluded because they are not weakly pulled low in reset. Bidirectional pins include ports 1–6.
2. Standard input pins include XTAL1, EA#, RESET#, and ports 1–6 when configured as inputs.
3. All bidirectional pins when configured as complementary outputs.
4. Device is static and should operate below 1 Hz, but is only tested down to 4 MHz with the PLL enabled. With the PLL bypassed, the device is only tested down to 8MHz.
5. Maximum I_{OL} or I_{OH} currents per pin will be characterized and published at a later date. Target values are ± 10 mA.
6. Typicals are based on a limited number of samples and are not guaranteed. The values listed are at room temperature and $V_{REF} = V_{CC} = 5.5V$.
7. V_{IH} max for port 0 is V_{REF} + 0.5V.
8. This specification is not tested in production and is based upon theoretical estimates and/or product characterization.

5.2 AC Characteristics (Over Specified Operating Conditions)

Test Conditions: Capacitive load on all pins = 100 pF, rise and fall times = 10 ns, F_{XTAL1} = 8MHz with PLL enabled in clock-doubler mode.

Table 7. AC Characteristics

Symbol	Parameter	Min	Max	Units
The 87C196LB will meet these specifications				
F_{XTAL1}	Frequency on XTAL1, PLL in 1x mode	8.0	20.0	MHz(1)
	Frequency on XTAL1, PLL in 2x mode	4.0	10.0	
f	Operating frequency, f = F_{XTAL1}; PLL in 1x mode	8.0	20.0	MHz
	Operating frequency, f = $2F_{XTAL1}$; PLL in 2x mode			
t	Period t = 1/f	50	125	ns
T_{XHCH}	XTAL1 High to CLKOUT High or Low	20	110	ns(2)
T_{CLCL}	CLKOUT Cycle Time	2t		ns
T_{CHCL}	CLKOUT High Period	t – 10	t + 15	ns
T_{CLLH}	CLKOUT Falling to ALE Rising	– 10	15	ns
T_{LLCH}	ALE Falling to CLKOUT Rising	– 20	15	ns
T_{LHLH}	ALE Cycle Time	4t		ns
T_{LHLL}	ALE High Period	t – 10	t + 10	ns
T_{AVLL}	Address Setup to ALE Low	t – 15		ns
T_{LLAX}	Address Hold after ALE Low	t – 40		ns
T_{LLRL}	ALE Low to RD# Low	t – 30		ns
T_{RLCL}	RD# Low to CLKOUT Low	4	30	ns
T_{RLRH}	RD# Low to RD# High	t – 5		ns
T_{RHLH}	RD# High to ALE Rising	t	t + 25	ns(3)
T_{RLAZ}	RD# Low to Address Float		5	ns
T_{LLWL}	ALE Low to WR# Low	t – 10		ns
T_{CLWL}	CLKOUT Low to WR# Falling Edge	– 5	25	ns
T_{QVWH}	Data Valid to WR# High	t – 23		ns
T_{CHWH}	CLKOUT High to WR# Rising Edge	– 10	15	ns
T_{WLWH}	WR# Low to WR# High	t – 20		ns
T_{WHQX}	Data Hold after WR# High	t – 25		ns

NOTES:
1. Testing performed at 4.0 MHz with PLL enabled. With the PLL bypassed, the device is only tested down to 8 MHz. However, the device is static by design and will typically operate below 1 Hz.
2. Typical specifications, not guaranteed.
3. Assuming back-to-back bus cycles.
4. 8-bit bus only.

Table 7. AC Characteristics (Continued)

Symbol	Parameter	Min	Max	Units
T_{WHLH}	WR# High to ALE High	t – 10	t + 15	ns(3)
T_{WHAX}	AD15:8 Hold after WR# High	t – 30(4)		ns
T_{RHAX}	AD15:8 Hold after RD# High	t – 30(4)		ns
The system must meet these specifications to work with the 87C196LB				
T_{AVDV}	Address Valid to Input Data Valid		3t – 55	ns
T_{RLDV}	RD# Low to Input Data Valid		t – 22	ns
T_{CLDV}	CLKOUT Low to Input Data Valid		t – 50	ns
T_{RHDZ}	RD# High to Input Data Float		t	ns
T_{RXDX}	Data Hold after RD# Inactive	0		ns

NOTES:
1. Testing performed at 4.0 MHz with PLL enabled. With the PLL bypassed, the device is only tested down to 8 MHz. However, the device is static by design and will typically operate below 1 Hz.
2. Typical specifications, not guaranteed.
3. Assuming back-to-back bus cycles.
4. 8-bit bus only.

6.0 THERMAL CHARACTERISTICS

All thermal impedance data is approximate for static air conditions at 1 watt of power dissipation. Values will change depending on operating conditions and the application. The Intel *Packaging Handbook* (order number 240800) describes Intel's thermal impedance test methodology. The *Components Quality and Reliability Handbook* (order number 210997) provides quality and reliability information.

Table 8. Thermal Characteristics

Package Type	θ_{JA}	θ_{JC}
AN87C196LB (52-pin PLCC)	42°C/W	15°C/W

NOTES:
1. θ_{JA} = Thermal resistance between junction and the surrounding environment (ambient). Measurements are taken 1 ft. away from case in static air flow environment.
   θ_{JC} = Thermal resistance between juction and package surface (case).
2. All values of θ_{JA} and θ_{JC} may fluctuate depending on the environment (with or without airflow, and how much airflow) and device power dissipation at temperature of operation. Typical variations are ± 2°C/W.
3. Values listed are at a maximum power dissipation of 0.50 W.

7.0 DESIGN CONSIDERATIONS

To be supplied.

8.0 DEVICE ERRATA

There is no known device errata at this time.

9.0 DATASHEET REVISION HISTORY

This datasheet is valid for devices with an "A" at the end of the topside field process order (FPO) number. Datasheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.