SYNCHRONOUS PWM CONTROLLER WITH DUAL LOW DROPOUT REGULATOR CONTROLLERS

SC1109

PRELIMINARY - October 16, 2000

DESCRIPTION

The SC1109 was designed for the latest high speed motherboards. It combines a synchronous voltage mode controller (switching section) with two low-dropout linear regulator controllers. The voltage mode controller provides the power supply for the system AGTL bus. The 1.8V and 2.5V linear controllers power the Chipset and clock circuitry.

The SC1109 switching section features lossless current sensing and latched driver outputs for enhanced noise immunity. It operates at a fixed frequency of 200kHz, the output voltage is internally fixed at 1.2V

The SC1109 linear sections are low dropout regulators designed to track the 3.3V power supply when it turns on or off.

FEATURES

- 1.8V, 2.5V linear controllers
- LDOs track input voltage within 200mV until regulation
- Integrated drivers
- Power Good Signal
- Soft Start
- Lossless Current Sense

APPLICATIONS

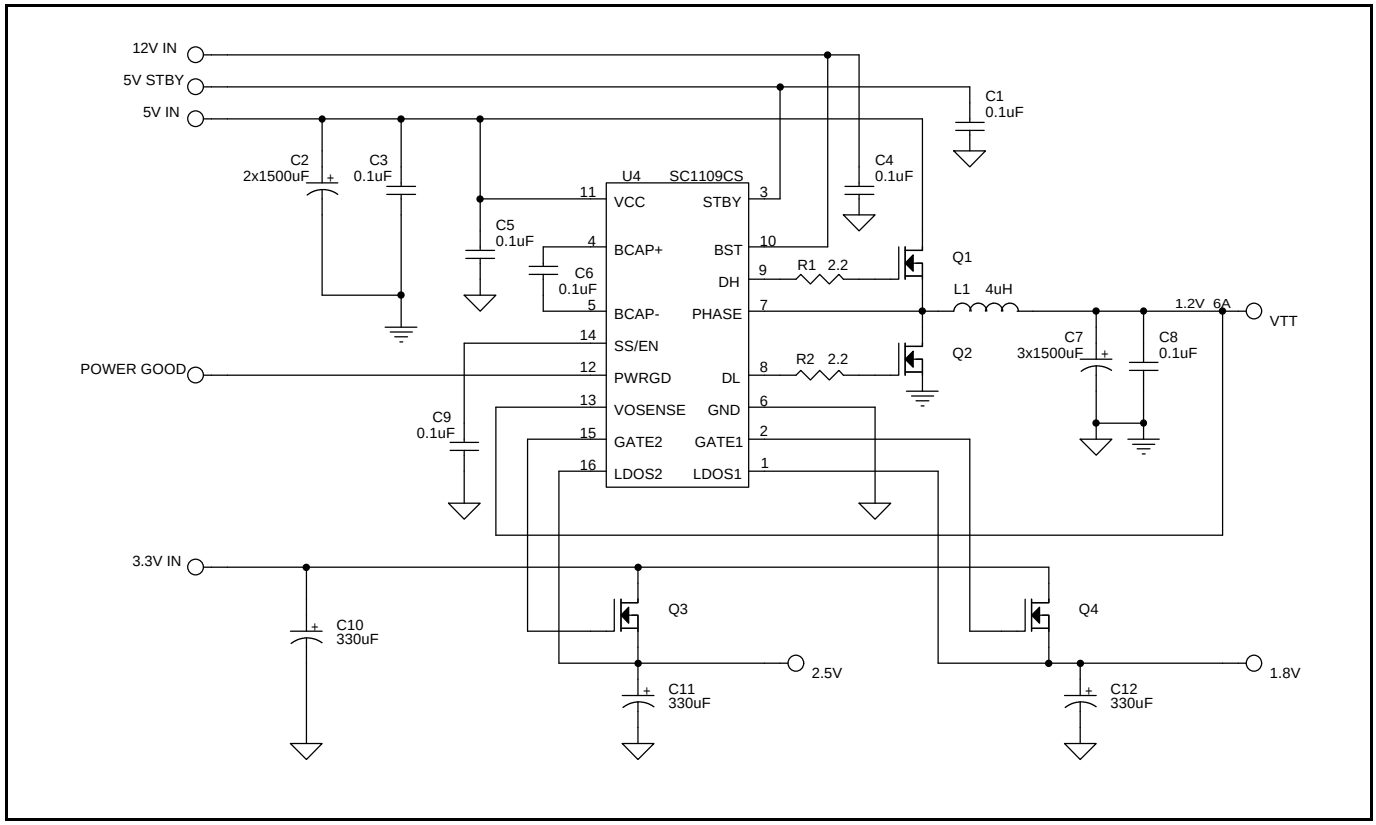
- Pentium® III Motherboards
- Triple power supplies

ORDERING INFORMATION

Part Number(1)	Package	Linear Voltage	Temp. Range (T_J)
SC1109CSTR	SO-16	1.8V/2.5V	0° to 125°C
SC1109EVB	Evaluation Board		

Note:
(1) Only available in tape and reel packaging. A reel contains 1000 devices.

TYPICAL APPLICATION CIRCUIT



TEL:805-498-2111 FAX:805-498-3804 WEB:http://www.semtech.com

PRELIMINARY - October 16, 2000

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Maximum	Units
VCC to GND		-0.3 to +7	V
STBY to GND		-0.3 to +7	V
BST to GND		-0.3 to +15	V
PHASE to GND		-1 to +8	V
LDOSx		-0.3 to 5	V
Operating Temperature Range	T_A	0 to +70	°C
Junction Temperature Range	T_J	0 to +125	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Lead Temperature (Soldering) 10 seconds	T_L	300	°C
Thermal Impedance Junction to Ambient	θ_{JA}	130	°C/W
Thermal Impedance Junction to Case	θ_{JC}	30	°C/W

Note:
Exceeding the Absolute Maximum Ratings may cause irreversible damage to the device.

ELECTRICAL CHARACTERISTICS

Unless specified: VOSENSE = V_O; Vcc=4.75V to 5.25V; STBY=4.75V to 5.25V; BST = 11.4V to 12.6V; T_A = 0 to 70°C

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Supply (V_{CC})						
Supply Voltage	V_{CC}		4.4	5	5.25	V
Supply Quiescent current	I_{CCQ}	V_{CC} = 5V, SS/EN = 0V	6	8	12	mA
Supply Operating current	I_{CC}	V_{CC} = 5V, SS/EN > 1V			20	mA
Switching Section						
Output Voltage(1)	V_{TT}	I_O = 2A	1.188	1.200	1.212	V
Load Regulation(1)	$LOAD_{REG}$	I_O = 0A to 6A		1		%
Line Regulation(1)	$LINE_{REG}$	Vin=4.75V to 5.25V		±0.15		%
Oscillator Frequency	f_{OSC}		175	200	225	kHz
Oscillator Max Duty Cycle	D		90	95		%
Current Limit trip (Vin-V_{PHASE})	$Vtrip_{Ilimit}$		180	200	220	mV
Gain (A_{OL})(3)	$GAIN_{VTT}$	VOSENSE to V_O		35		dB
Under Voltage Lock Out						
Threashold	VCC_{HIGH}			4.2		V
Hysteresis	VCC_{HYST}			200		mV
Power Good						
Power Good Threshold Voltage	PG_{th}		88		112	%
Soft Start / Enable						
SS/EN Source current(2)	$Isource_{SS/EN}$	$V_{SS/EN}$ = 0V to 3.5V		10		µA
SS/EN Sink current(2)	$Isink_{SS/EN}$	$V_{SS/EN}$ = 0V to 3.5V		2		µA
Shutdown Voltage	$V_{SS/EN}$			600		mV

TEL:805-498-2111 FAX:805-498-3804 WEB:http://www.semtech.com

PRELIMINARY - October 16, 2000

ELECTRICAL CHARACTERISTICS (Cont.)

Unless specified: VOSENSE = V_O; Vcc=4.75V to 5.25V; STBY=4.75V to 5.25V; BST = 11.4V to 12.6V; T_A = 0 to 70°C

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Internal Drivers						
Peak DH Source Current	$Isource_{DH}$	BST-DH = 4.5V	500			mA
Peak DH Sink Current	$Isink_{DH}$	DH-GND = 3.1V DH-GND = 1.5V	500 100			mA mA
Peak DL Source Current	$Isource_{DL}$	VCC-DL = 4.5V	500			mA
Peak DL Sink Current	$Isink_{DL}$	DL-GND = 3.1V DL-GND = 1.5V	500 100			mA mA
Dead time	T_{DEAD}		40	100		ns
Linear Sections						
Standby Voltage	V_{STBY}		4.4	5	5.25	V
Standby Quiescent current	I_{STDBYQ}	VSTBY = 5V, SS/EN = 0V			5	mA
Tracking Difference(4)	$Delta_{TRACK}$			200		mV
Output Voltage LDO1	V_{LDO1}	I_O = 0 to 4A, 3.3V Vin = 3.3V	1.782	1.818	1.854	V
Output Voltage LDO2	V_{LDO2}	I_O = 0 to 4A, 3.3V Vin = 3.3V	2.475	2.525	2.575	V
Load Regulation	$LOAD_{REG}$	I_O = 0 to 4A, 3.3V Vin = 3.3V		0.3		%
Line Regulation	$LINE_{REG}$	3.3V Vin = 3.13V to 3.47V, I_o		0.3		%
LDOS(1,2) Output Impedance	Z_{OUT}	$V_{GATE(1,2)}$ = 6.5V		1	1.5	kΩ
LDOS(1,2) Input Impedance	Z_{IN}		10			kΩ
Gain (A_{OL})(3)	$GAIN_{LDO}$	LDOS (1,2) to GATE (1,2)		50		dB
LDO1 Gate Voltage	$Vgate_{LDO1}$	V_{STDBY} = 5V		8		V
LDO2 Gate Voltage	$Vgate_{LDO2}$	V_{STDBY} = 5V		7		V

Notes:

(1) All electrical characteristics are for the application circuit on page 6.
(2) Soft start function is performed after Vcc is above the UVLO and SS/EN is above 600mV. The Soft start capacitor is then charged at a 10uA constant current until SS/EN is charged to above 1V.
(3) Guaranteed by design
(4) Tracking Difference is defined as the delta between 3.3V Vin and the LDO1, LDO2 output voltages during the linear ramp up until regulation is achieved.

TEL:805-498-2111 FAX:805-498-3804 WEB:http://www.semtech.com

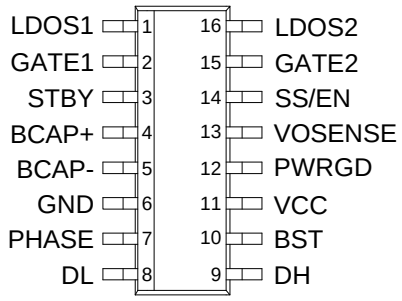
PRELIMINARY - October 16, 2000

PIN DESCRIPTION

Pin	Pin Name	Pin Function
1	LDOS1	Sense Input for LDO1
2	GATE1	Gate Drive Output LDO1 (1.8V)
3	STBY	5V Standby Input, supplies power for Ref, Charge Pump, Oscillator and FET controllers.
4	BCAP+	Positive Connection to Boost Capacitor
5	BCAP-	Negative Connection to Boost Capacitor
6	GND	Ground
7	PHASE	Phase Node
8	DL	Low Side Driver Output
9	DH	High Side Driver Output
10	BST	Boost Input
11	VCC	Power Supply Input
12	PWRGD	Open Collector Power Good Flag for 1.2V Output
13	VOSENSE	Output Sense Input for 1.2V Output
14	SS/EN	Soft Start/ Enable
15	GATE2	Gate Drive Output LDO2 (2.5V)
16	LDOS2	Sense Input for LDO2

PIN CONFIGURATION

Top View

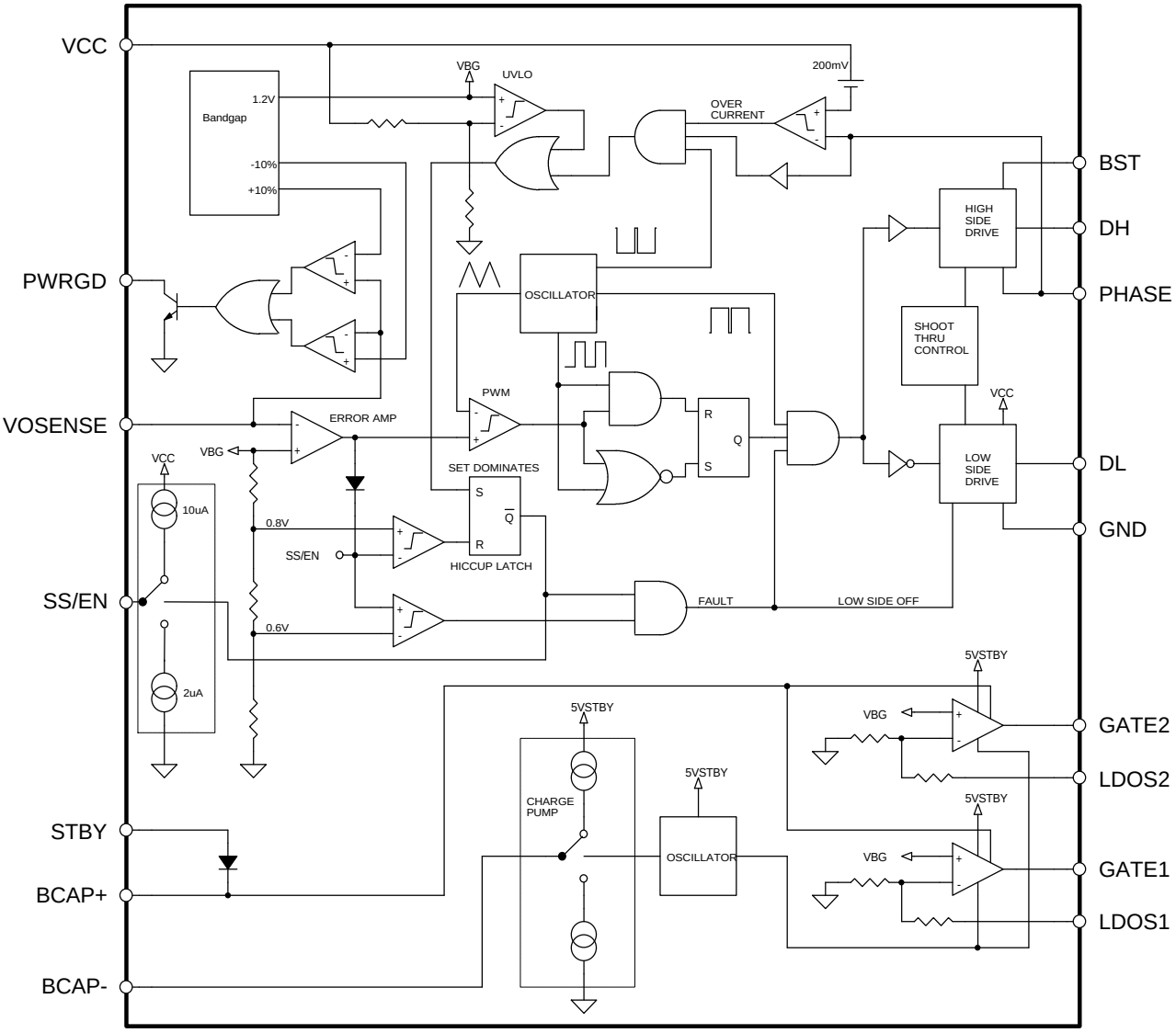


(16 Pin SOIC)

TEL:805-498-2111 FAX:805-498-3804 WEB:http://www.semtech.com

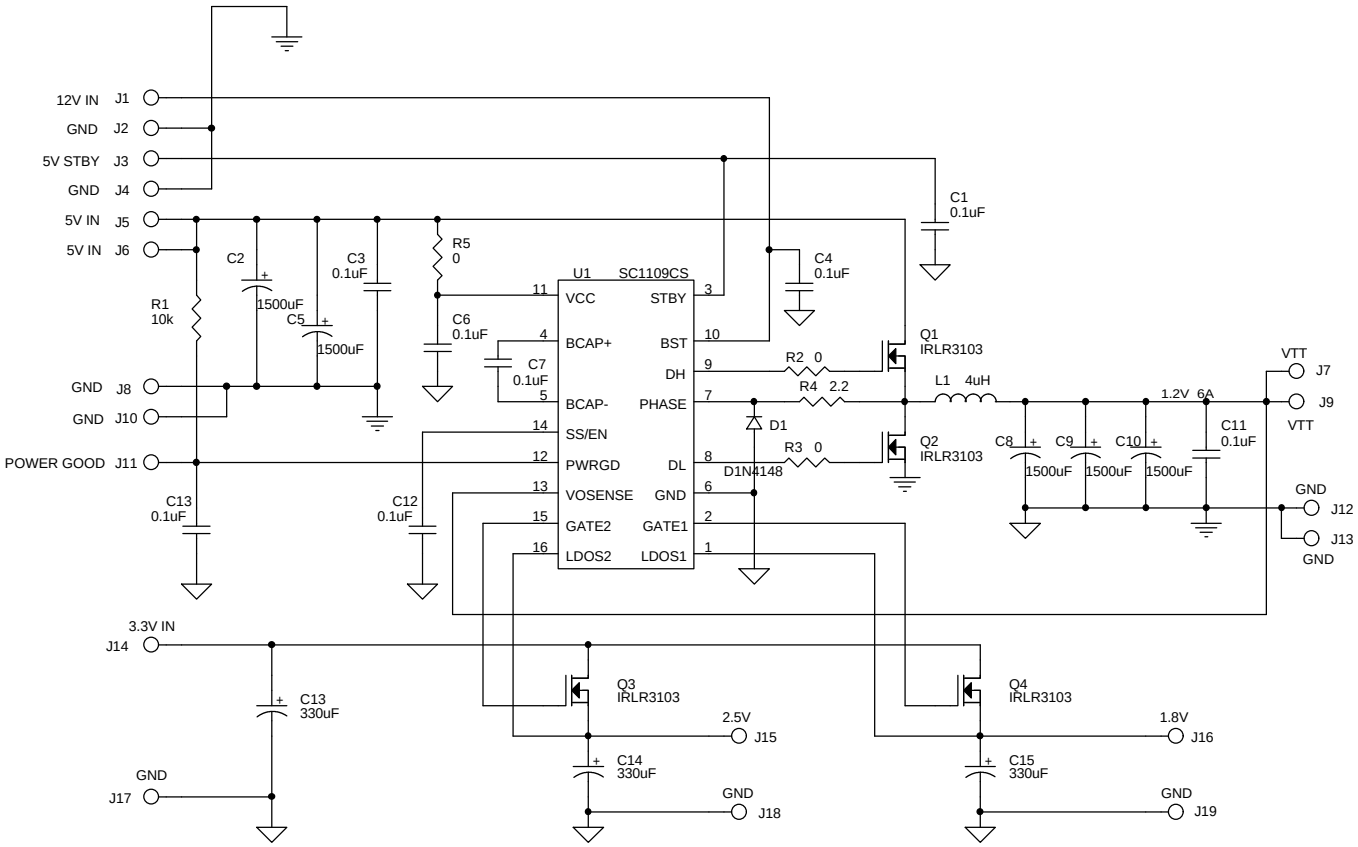
PRELIMINARY - October 16, 2000

BLOCK DIAGRAM



TEL:805-498-2111 FAX:805-498-3804 WEB:http://www.semtech.com

APPLICATION CIRCUIT



TEL:805-498-2111 FAX:805-498-3804 WEB:http://www.semtech.com

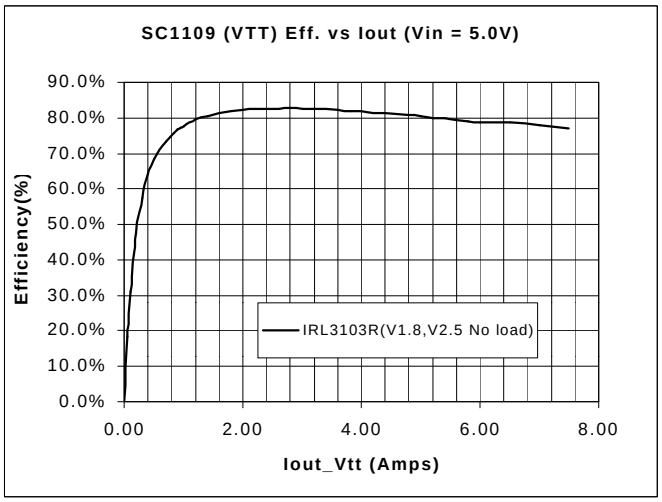
PRELIMINARY - October 16, 2000

MATERIALS LIST

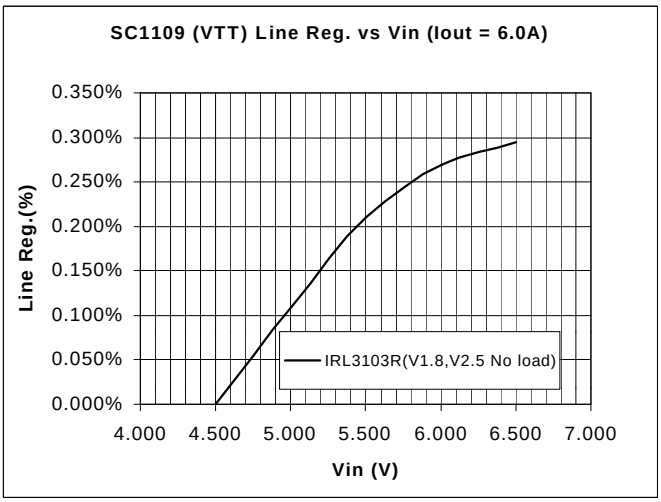
SC1109 Evaluation board Revised: Friday, August 11, 2000 SC1109EVB Revision: 1.1			
Bill Of Materials	**August 8,2000 13:17:55**		**Page1**
Item	**Quantity**	**Reference**	**Part**
1	7	C1,C3,C4,C6,C7,C11,C12,C13	0.1uF
2	5	C2,C5,C8,C9,C10	1500uF
3	3	C13,C14,C15	330uF
4	1	D1	D1N4148
5	1	J1	12V IN
6	9	J2,J4,J8,J10,J12,J13,J17, J18,J19	GND
7	1	J3	5V STBY
8	2	J5,J6	5V IN
9	2	J7,J9	VTT
10	1	J11	POWER GOOD
11	1	J14	3.3V IN
12	1	J15	2.5V
13	1	J16	1.8V
14	1	L1	4uH
15	4	Q1,Q2,Q3,Q4	IRLR3103
16	1	R1	10k
17	2	R2,R3	0
18	1	R4	2.2
19	1	R5	0
20	1	U1	SC1109CS

TEL:805-498-2111 FAX:805-498-3804 WEB:http://www.semtech.com

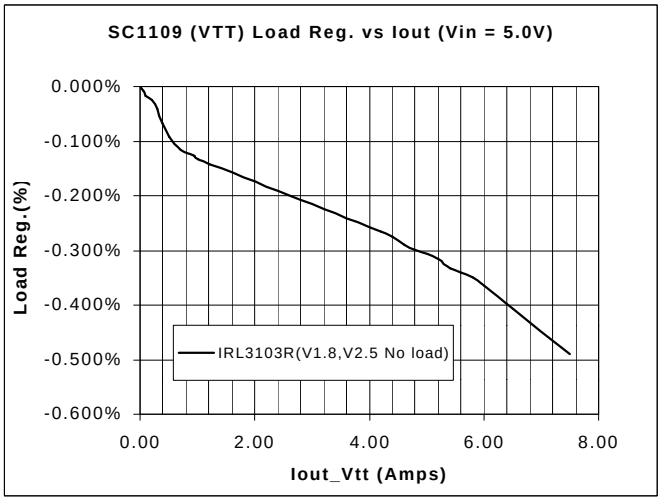
PRELIMINARY - October 16, 2000



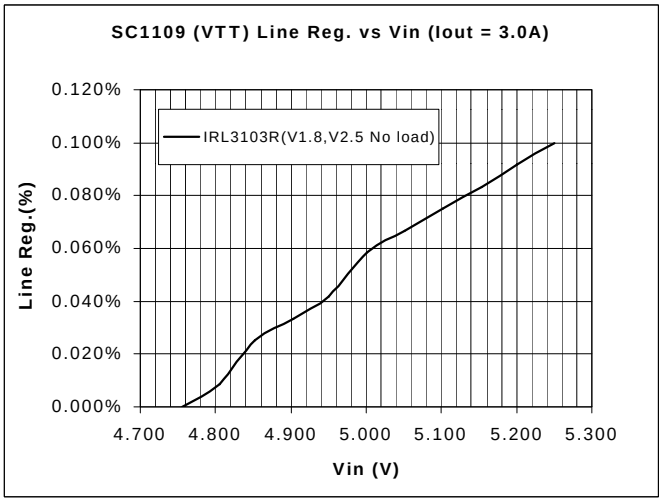
Typical VTT Efficiency at Vin=5V



Typical VTT Line Regulation at Iout = 6 Amps

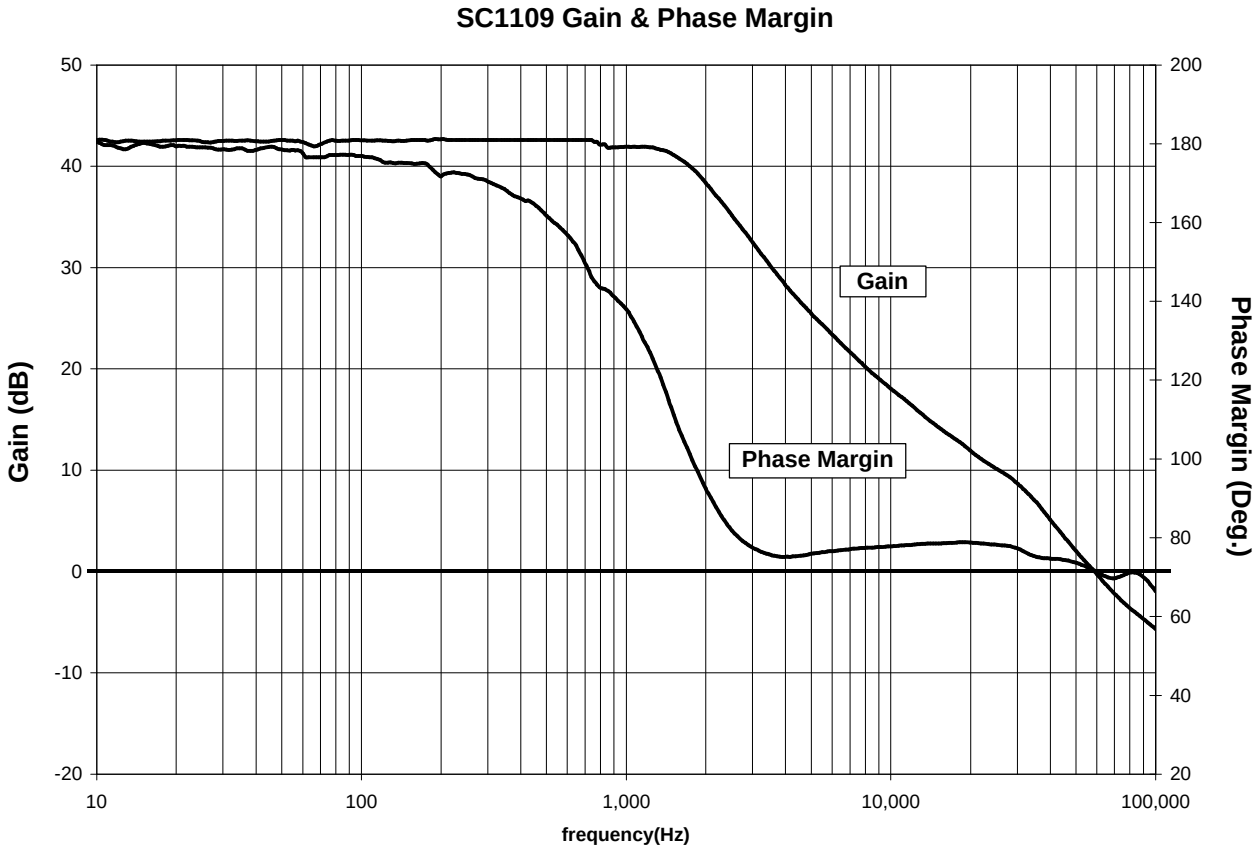


Typical VTT Load Regulation at Vin=5V



Typical VTT Line Regulation at Iout = 3 Amps

TEL:805-498-2111 FAX:805-498-3804 WEB:http://www.semtech.com



Typical VTT Gain/Phase plot at Vin=5V Iout = 3 A

TEL:805-498-2111 FAX:805-498-3804 WEB:http://www.semtech.com

PRELIMINARY - October 16, 2000

THEORY OF OPERATION

The SC1109 has integrated a synchronous buck controller and two Low drop out regulator controllers into a 16 Pin SOIC package. The switching regulator provides a 1.2V (VTT) bus termination voltage for use in AGTL (Assisted Gunning Transceiver Logic), while the dual LDO regulators provide 1.8V, and 2.5V to power up the Chipset and the Clock circuitry used in Pentium® III Motherboards.

SUPPLIES

Two supplies, VSTBY, and VCC are used to power the SC1109. VSTBY supply provides the bias for the Internal Reference, Oscillator, and the LDO FET controllers. The VCC supply provides the bias for the Power Good circuitry, and the high side FET Rdson sensing/over current circuitry, VCC also is used to drive the low side Mosfet gate. An external 12V supply or a classical boot strapping technique can provide the gate drive for the upper Mosfet.

PWM CONTROLLER

SC1109 is a voltage mode buck controller that utilizes an internally compensated high bandwidth error amplifier to sense the VTT output voltage. External compensation components are not needed and a stable closed loop responce is insured due to the internal compensation.

START UP SEQUENCE

Initially during the power up, the SC1109 is in under voltage lock out condition. The latch (SET dominant) in the hiccup section is set , and the SS/EN pin is pulled low by the 2uA soft start current source.

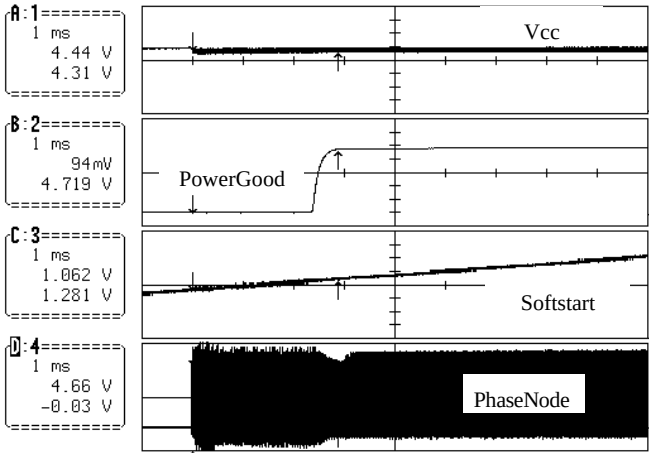
Mean while the high side and low side gate drivers DH, and DL are kept low. Once the VCC exceeds the UVLO threshold of 4.2V, the latch is reset and the external soft start capacitor starts to be charged by a 10uA current source.

The gate drives are still kept off until the soft start capacitors voltage rises above 600mV, when the low side gate is turned on , and the high side gate is kept off.

The gate drive status stays the same until the capacitors voltage reaches 1V, when the error amplifier output starts to cross the oscillator triangular ramp of 1V to 2V.

As the SS/EN pin continues to rise, the error amplifier output also rises at the same rate and the duty cycle increases.

Once the VTT output has reached regulation and is within 1.2V ± 12% , an open collector power good flag is activated, and the error amplifier output will no longer be clamped to the SS/EN voltage and will stay between 1V to 2V and maintain regulation of ± 1%. The SS/EN voltage continues to rise up to 2.5V and will stay at that voltage level during normal operation.



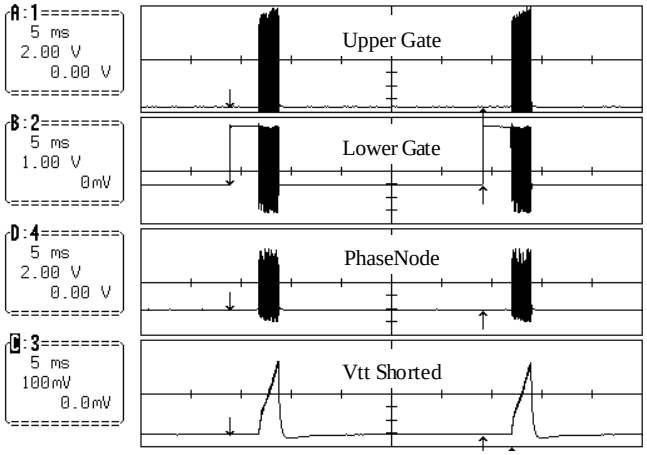
If an over current condition occurs, the SS/EN pin will discharge by a 2uA current source, from 2.5V to 800mV. During this time both DH, and DL will be turned off. Once the SS/EN reaches 800mV, the low side gate will be turned on, and the SS/EN pin will again start to be charged by the 10uA current source, and the same soft start sequence mentioned above will be repeated.

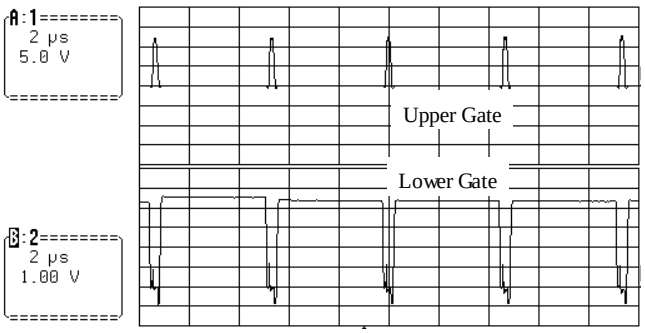
TEL:805-498-2111 FAX:805-498-3804 WEB:http://www.semtech.com

OVER CURRENT

Upper Mosfet's Rdson is used to monitor the drop across the top FET due to an over current condition. This Method of current sensing minimizes any unnecessary losses due to external sense resistance.

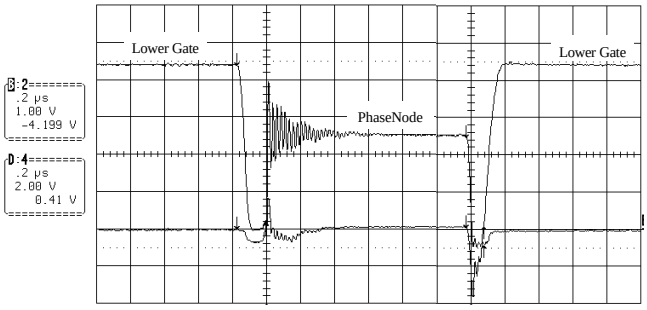
An internal comparator with a 200mV reference monitors the Drop across the upper FET, Once the Vdson of the Mosfet exceeds the 200mV limit, the low side gate is turned on and the upper FET is turned off. Also an internal latch is set and the Soft start capacitor is discharged. Once the lower threshold of the soft start circuit is crossed, the same Softstart sequence mentioned previously is repeated. This sequence is repeated until the over condition is removed.





GATE DRIVERS

The Low side gate driver is supplied from VCC and provide a peak source/sink current of and 500mA. The high side gate drive is also capable of sourcing and sinking peak currents of 500mA. The high side Mosfet gate drive can be provided by an external 12V supply that is connected from BST to GND. The actual gate to source voltage of the upper Mosfet will approximately equal 7V (12V-VCC). If the external 12V supply is not available, a classical boot strap technique can be implemented from the VCC supply. A boot strap capacitor is connected from BST to Phase while VCC is connected through a diode (Schottky or other fast low VF diode) to the BST. This will provide a gate to source voltage approximately to VCC-Vdiode drop.



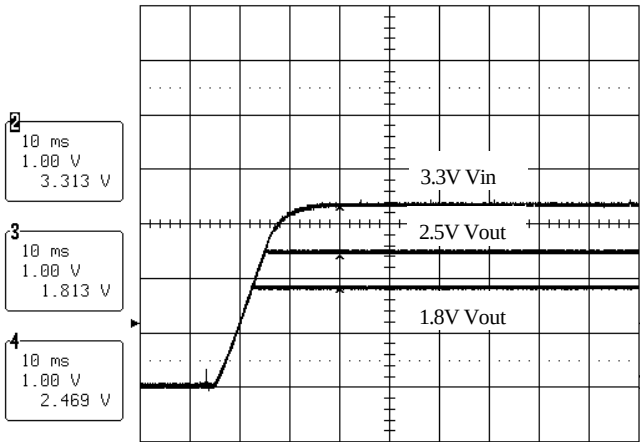
Shoot through control circuitry provides a 100ns dead time to ensure both upper and lower MOSFET will not turn on simultaneously and cause a shoot through condition.

DUAL LDO CONTROLLERS

SC1109 also provides two low drop out linear regulator controllers that can be used to generate a 1.8V (LDO2) and 2.5V (LDO1) outputs. The LDO output voltage is achieved by controlling the voltage drop across an external Mosfet from a 3.3V supply voltage.

The output voltage is sensed at the LDOS pin of the SC1109 and compared to an internal reference. The gate drive to the external Mosfet is then adjusted until regulation is achieved. In order to have sufficient voltage to the gate drives of the external Mosfet, an internal charge pump is utilized to boost the gate drive voltage to about two times the VSTBY.

The internal charge pump charges an external Bucket capacitor to VSTBY and then connects it in series with VSTBY to the LDOs supply at a frequency of about 200kHz. This ensures sufficient gate drive voltage for the LDOs independent of the VCC or the 12V external supply being available due to start up timing sequence from the silver box.



The LDO1, and LDO2 output voltages are forced to track the 3.3V input supply. This feature ensures that during the start up application of the 3.3V, the 1.8V, and 2.5V outputs track the 3.3V within 200mV typical until regulation is achieved. However, the VSTBY should be established at least 500us, to allow the charge pump to reach its maximum voltage, before the linear section will track within 200mV. This tracking will sequence the correct start up timing for the external Chipset and Clock circuitry.

LAYOUT GUIDELINES

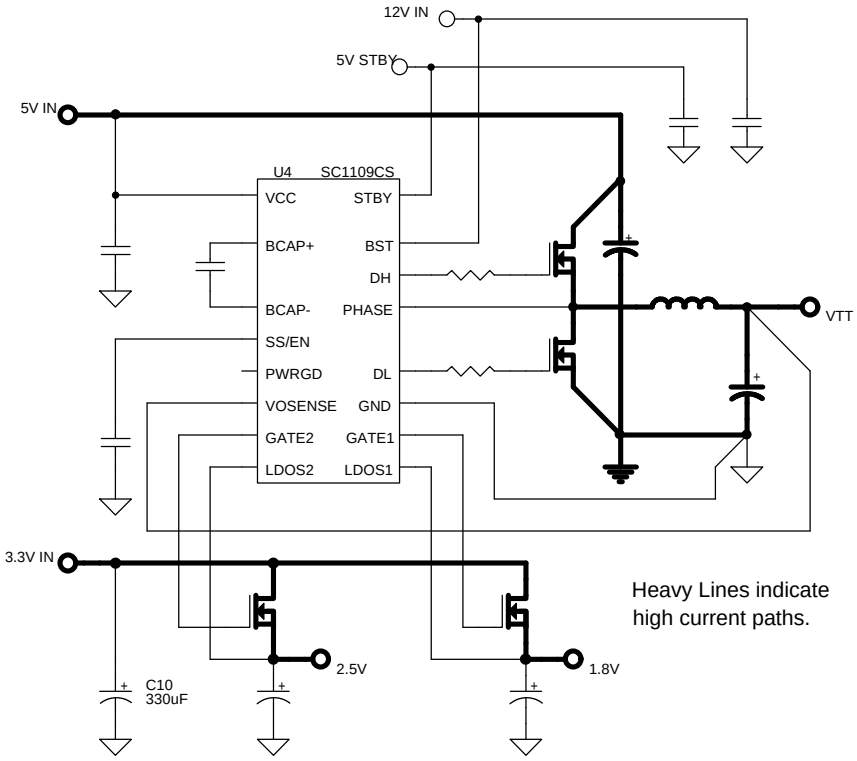
Careful attention to layout requirements are necessary for successful implementation of the SC1109 PWM controller. High currents switching at 200kHz are present in the application and their effect on ground plane voltage differentials must be understood and minimized.

1). The high power parts of the circuit should be laid out first. A ground plane should be used, the number and position of ground plane interruptions should be such as to not unnecessarily compromise ground plane integrity. Isolated or semi-isolated areas of the ground plane may be deliberately introduced to constrain ground currents to particular areas, for example the input capacitor and bottom FET ground.

2). The loop formed by the Input Capacitor(s) (Cin), the Top FET (Q1) and the Bottom FET (Q2) must be kept as small as possible. This loop contains all the high current, fast transition switching. Connections should be as wide and as short as possible to minimize loop inductance. Minimizing this loop area will a) reduce EMI, b) lower ground injection currents, resulting in electrically "cleaner" grounds for the rest of the system and c) minimize source ringing, resulting in more reliable gate switching signals.

3). The connection between the junction of Q1, Q2 and the output inductor should be a wide trace or copper region. It should be as short as practical. Since this connection has fast voltage transitions, keeping this connection short will minimize EMI. Also keep the Phase connection to the IC short, top FET gate charge currents flow in this trace.

4) The Output Capacitor(s) (Cout) should be located as close to the load as possible, fast transient load cur-



Layout diagram for the SC1109

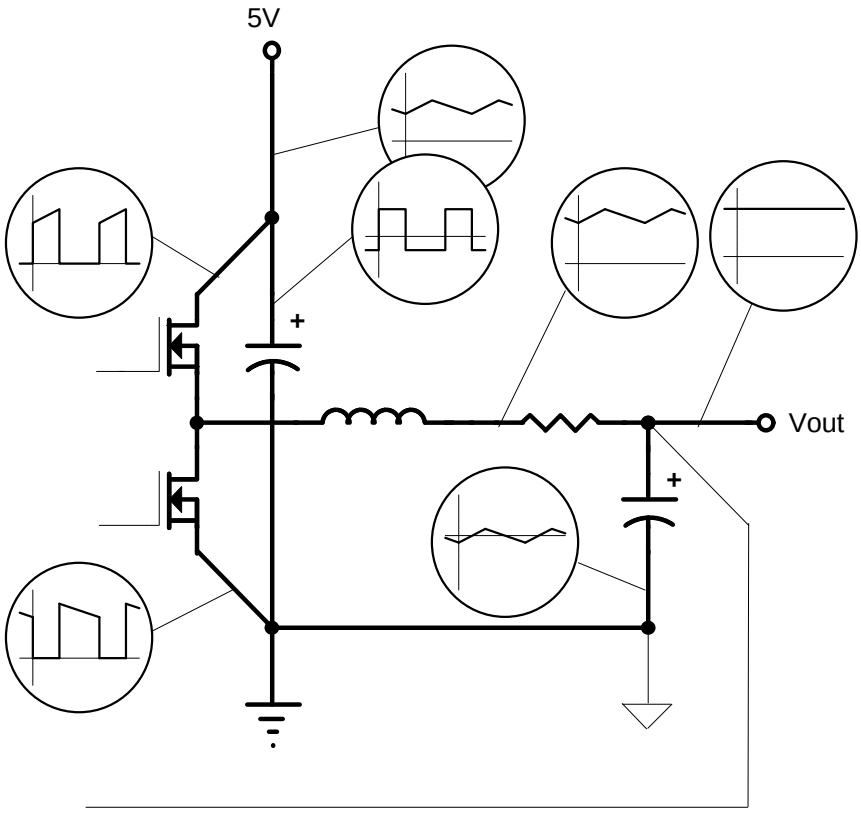
rents are supplied by Cout only, and connections between Cout and the load must be short, wide copper areas to minimize inductance and resistance.

5) The SC1109 is best placed over a quiet ground plane area, avoid pulse currents in the Cin, Q1, Q2 loop flowing in this area. GND should be returned to the ground plane close to the package and close to the ground side of (one of) the output capacitor(s). If this is not possible, the GND pin may be connected to the ground path between the Output Capacitor(s) and the Cin, Q1, Q2 loop. Under no circumstances should GND be returned to a ground inside the Cin, Q1, Q2 loop.

6) BST for the SC1109 should be supplied from the 12V supply, the BST pin should be decoupled directly to GND by a 0.1µF ceramic capacitor, trace lengths should be as short as possible. If a 12V supply is not available, a classical boot strap method could be implemented to achieve the upper Mosfet's gate drive.

7) The Phase connection should be short .

8) Ideally, the grounds for the two LDO sections should be returned to the ground side of (one of) the output capacitor(s).



Currents in various parts of the power section

 TEL:805-498-2111 FAX:805-498-3804 WEB:http://www.semtech.com

PRELIMINARY - October 16, 2000

COMPONENT SELECTION

SWITCHING SECTION

OUTPUT CAPACITORS - Selection begins with the most critical component. Because of fast transient load current requirements in modern microprocessor core supplies, the output capacitors must supply all transient load current requirements until the current in the output inductor ramps up to the new level. Output capacitor ESR is therefore one of the most important criteria. The maximum ESR can be simply calculated from:

$$R_{ESR} \le \frac{V_t}{I_t}$$

Where

V_t = **Maximum transient voltage excursion**

I_t = **Transient current step**

For example, to meet a 100mV transient limit with a 10A load step, the output capacitor ESR must be less than 10mΩ. To meet this kind of ESR level, there are three available capacitor technologies.

Technology	Each Capacitor		Qty. Rqd.	Total	
	C (µF)	ESR (mΩ)		C (µF)	ESR (mΩ)
Low ESR Tantalum	330	60	6	2000	10
OS-CON	330	25	3	990	8.3
Low ESR Aluminum	1500	44	5	7500	8.8

The choice of which to use is simply a cost/performance issue, with Low ESR Aluminum being the cheapest, but taking up the most space.

INDUCTOR - Having decided on a suitable type and value of output capacitor, the maximum allowable value of inductor can be calculated. Too large an inductor will produce a slow current ramp rate and will cause the output capacitor to supply more of the transient load current for longer - leading to an output voltage sag below the ESR excursion calculated above. The maximum inductor value may be calculated from:

$$L \le \frac{R_{ESR}\, C}{I_t}\left(V_{IN} - V_O\right)$$

The calculated maximum inductor value assumes 100% duty cycle, so some allowance must be made. Choosing an inductor value of 50 to 75% of the calculated maximum will guarantee that the inductor current will ramp fast enough to reduce the voltage dropped across the ESR at a faster rate than the capacitor sags, hence ensuring a good recovery from transient with no additional excursions.

We must also be concerned with ripple current in the output inductor and a general rule of thumb has been to allow 10% of maximum output current as ripple current. Note that most of the output voltage ripple is produced by the inductor ripple current flowing in the output capacitor ESR. Ripple current can be calculated from:

$$I_{L_{RIPPLE}} = \frac{V_{IN}}{4 \cdot L \cdot f_{OSC}}$$

Ripple current allowance will define the minimum permitted inductor value.

POWER FETS - The FETs are chosen based on several criteria with probably the most important being power dissipation and power handling capability.

TOP FET - The power dissipation in the top FET is a combination of conduction losses, switching losses and bottom FET body diode recovery losses.

a) Conduction losses are simply calculated as:

$$P_{COND} = I_O^2 \cdot R_{DS(on)} \cdot \mathbf{d}$$

where

$$\mathbf{d = duty\ cycle} \approx \frac{V_O}{V_{IN}}$$

b) Switching losses can be estimated by assuming a switching time, if we assume 100ns then:

$$P_{SW} = I_O \cdot V_{IN} \cdot 10^{-2}$$

or more generally,

$$P_{SW} = \frac{I_O \cdot V_{IN} \cdot (t_r + t_f) \cdot f_{OSC}}{4}$$

c) Body diode recovery losses are more difficult to estimate, but to a first approximation, it is reasonable to assume that the stored charge on the bottom FET body diode will be moved through the top FET as it starts to turn on. The resulting power dissipation in the top FET will be:

$$P_{RR} = Q_{RR} \cdot V_{IN} \cdot f_{OSC}$$

To a first order approximation, it is convenient to only consider conduction losses to determine FET suitability. For a 5V in; 2.8V out at 14.2A requirement, typical FET losses would be:

 TEL:805-498-2111 FAX:805-498-3804 WEB:http://www.semtech.com

Using 1.5X Room temp $R_{DS(ON)}$ to allow for temperature rise.

FET type	$R_{DS(on)}$ (mΩ)	P_D (W)	Package
IRL34025	15	1.69	D^2PAK
IRL2203	10.5	1.19	D^2PAK
Si4410	20	2.26	SO-8

BOTTOM FET - Bottom FET losses are almost entirely due to conduction. The body diode is forced into conduction at the beginning and end of the bottom switch conduction period, so when the FET turns on and off, there is very little voltage across it, resulting in low switching losses. Conduction losses for the FET can be determined by:

$$P_{COND} = I_O^2 \cdot R_{DS(on)} \cdot (1 - \mathbf{d})$$

For the example above:

FET type	$R_{DS(on)}$ (mΩ)	P_D (W)	Package
IRL34025	15	1.33	D^2PAK
IRL2203	10.5	0.93	D^2PAK
Si4410	20	1.77	SO-8

Each of the package types has a characteristic thermal impedance, for the TO-220 package, thermal impedance is mostly determined by the heatsink used. For the surface mount packages on double sided FR4, 2 oz printed circuit board material, thermal impedances of 40°C/W for the D^2PAK and 80°C/W for the SO-8 are readily achievable. The corresponding temperature rise is detailed below:

	Temperature rise (°C)	
FET type	Top FET	Bottom FET
IRL34025	67.6	53.2
IRL2203	47.6	37.2
Si4410	180.8	141.6

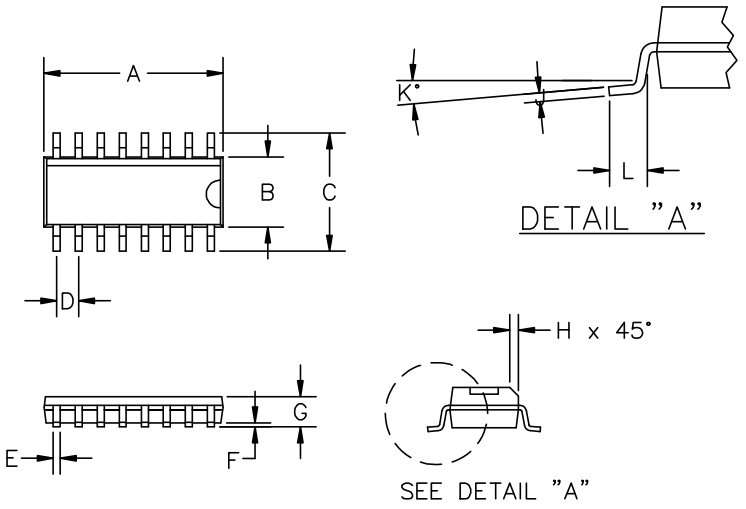
It is apparent that single SO-8 Si4410 are not adequate for this application, but by using parallel pairs in each position, power dissipation will be approximately halved and temperature rise reduced by a factor of 4.

INPUT CAPACITORS - since the RMS ripple current in the input capacitors may be as high as 50% of the output current, suitable capacitors must be chosen accordingly. Also, during fast load transients, there may be restrictions on input di/dt. These restrictions require useable energy storage within the converter circuitry, either as extra output capacitance or, more usually, additional input capacitors. Choosing low ESR input capacitors will help maximize ripple rating for a given size.

 TEL:805-498-2111 FAX:805-498-3804 WEB:http://www.semtech.com

PRELIMINARY - October 16, 2000

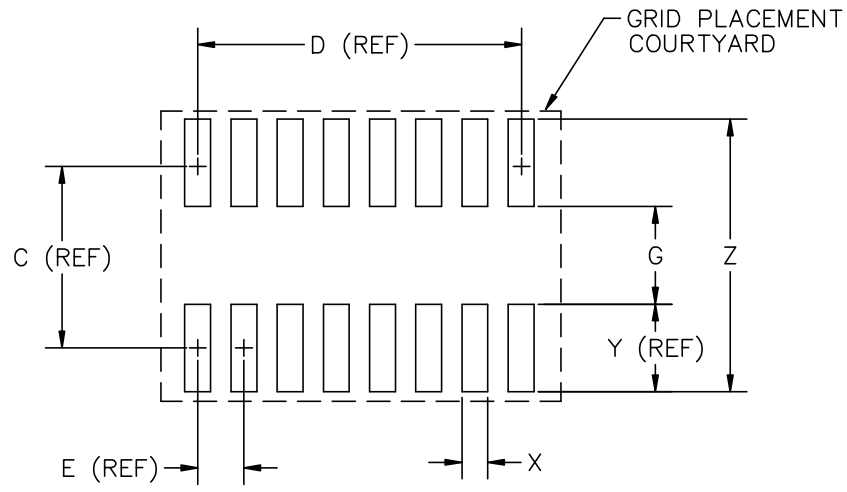
OUTLINE DRAWING SO-16



DIMENSIONS					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.386	.393	9.80	10.0	[2]
B	.150	.158	3.80	4.00	[2]
C	.228	.244	5.80	6.20	–
D	.050 BSC		1.27 BSC		–
E	.013	.020	0.33	0.51	–
F	.004	.010	.10	.25	–
G	.053	.069	1.35	1.75	–
H	.010	.020	.25	.50	–
J	.007	.010	.19	.25	–
K	0°	8°	0°	8°	–
L	.016	.050	.40	1.27	–

[2] DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTUSIONS

LAND PATTERN SO-16



DIMENSIONS					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
C	–	.197	–	5.00	–
D	–	.35	–	8.89	–
E	–	.05	–	1.27	–
G	.102	.110	2.60	2.80	–
X	.02	.03	.60	.80	–
Y	–	.095	–	2.40	–
Z	.28	.29	7.20	7.40	–

[1] GRID PLACEMENT COURTYARD IS 22 X 16 ELEMENTS (11mm X 8mm) IN ACCORDANCE WITH THE INTERNATIONAL GRID DETAILED IN IEC PUBLICATION 97.

ECN 00-817

TEL:805-498-2111 FAX:805-498-3804 WEB:http://www.semtech.com