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TECHNICAL DATA

MC68HC05M9

Technical Summary

MC68HC05M9
microcomputer unit with VFD drive capability

The MC68HC05M9 (HCMOS) 8-bit microcomputer unit (MCU) is a member of the M68HC05 family of devices, and is closely related to the MC68HC05C9 and the MC68HC05M4. Its special features include the addition of three high current, high voltage 8-bit output ports suitable for driving vacuum fluorescent displays.

For more detailed information, contact your local Motorola sales office.

The main hardware and software features of the MC68HC05M9 are as follows.

- Low-power M68HC05 family CPU core – fully static operation
- Power saving WAIT and very low power STOP modes
- Three 8-bit high-voltage ports, with pull-down resistors, for VFD drive
- Three 8-bit ports providing 24 bi-directional I/O lines
- Memory mapped I/O
- Software selectable memory configurations
- 16K bytes of ROM
- 352 bytes of RAM
- Serial Communications Interface (SCI)
- 16-bit timer with Input Capture and Output Compare functions
- 8-bit timer with modulus latch and 7-bit prescaler
- Computer Operating Properly (COP) watchdog timer
- Clock Monitor
- Single 3.0 to 5.5 Volt supply (2 Volt data retention mode)
- On-chip oscillator with crystal/ceramic resonator or RC mask option
- External, Timer and SCI interrupts
- Software programmable external interrupt sensitivity
- Available in 64-pin DIL and 64-pin QFP packages

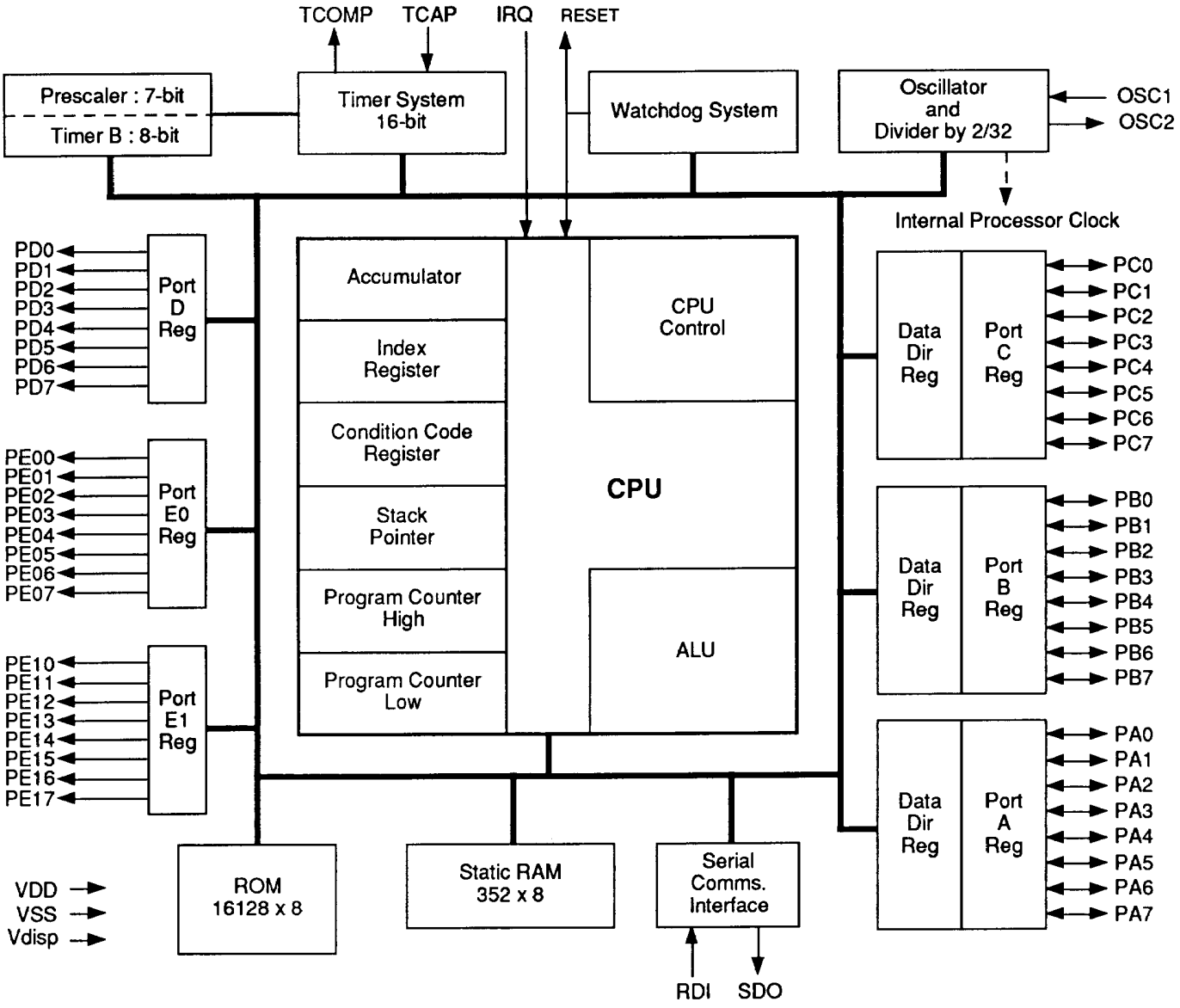


Figure 1. MC68HC05M9 Block Diagram

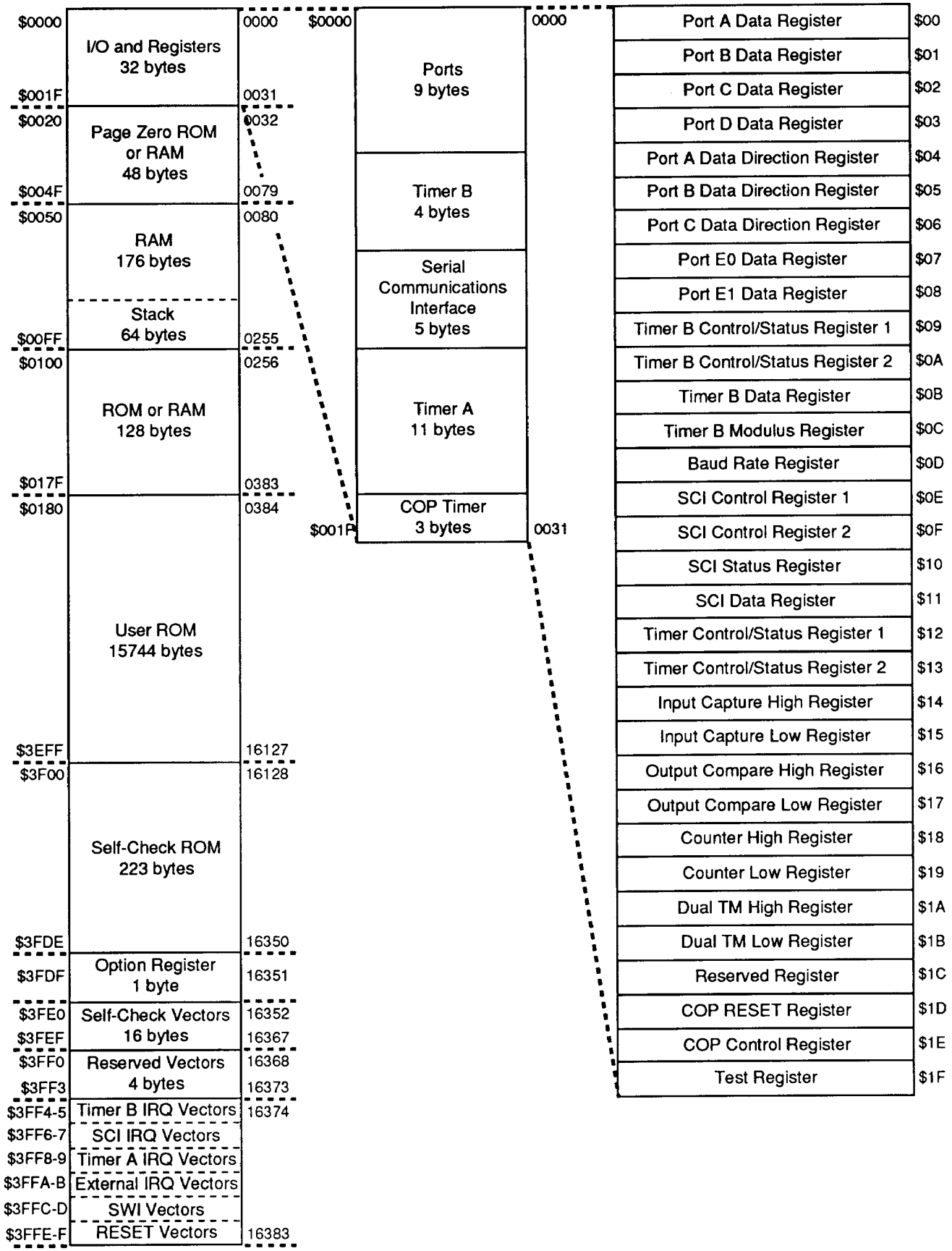


Figure 2. MC68HC05M9 Memory Map

RESETS

The MC68HC05M9 can be reset in four ways: a power-on reset function, an active-low external reset pin, an internal watchdog timer and an internal clock monitor.

RESET pin

The RESET pin is used to provide an orderly software and hardware startup. It also contains an internal Schmitt trigger to improve noise immunity.

Power-on reset (POR)

The Power-on reset occurs when a positive transition is detected on VDD. Power-on reset is strictly for power turn-on and should not be used to detect a drop in the power supply voltage.

Note: There is no internal provision for a power-off reset.

MODES OF OPERATION

The MC68HC05M9 has two modes of operation available to the user: Single chip (normal) mode and Self-check mode.

Single chip mode

The normal operating mode of the device is the single chip mode. Entry to this mode is achieved when the MCU comes out of reset if the IRQ pin is at a logic low level.

Self check mode

The MC68HC05M9 contains, in mask ROM location $3F00 to $3FDE, a program which checks the integrity of the device with a minimum of support hardware.

This program is executed in the self-check mode, entered when the MCU comes out of reset if the IRQ pin is at 9 volts. Under these circumstances, the self-check vector will be fetched and the self-check firmware will start to execute.

INTERRUPTS

The MC68HC05M9 has 5 different interrupt sources, each with its own vector (four hardware and one software).

When the I-bit in the condition code register (CCR) is set, it blocks all interrupts except the software interrupt (SWI). If an interrupt enable bit is set to zero it prevents the interrupt from occurring but does not inhibit the associated status flags from being set. RESET clears all interrupt enable bits.

The general sequence for clearing an interrupt is to read the status register while the flag is set, followed by a read or write of the associated data register.

Software interrupt

The software interrupt is generated by executing an SWI instruction. The SWI is executed regardless of the state of the interrupt mask in the CCR.

Hardware interrupts

A hardware interrupt can be generated from 4 sources; the external IRQ pin, the SCI interface, Timer A and Timer B.

External interrupts are caused by transitions or levels on the IRQ pin.

The SCI can generate an interrupt when various conditions are met thus allowing the serial interface to be interrupt driven.

Timer A can generate an interrupt when one of three conditions is met; overflow, input capture, and output compare. Each of the 3 interrupt sources can be individually enabled.

Timer B can generate an interrupt only when the overflow condition is met.

SERIAL COMMUNICATIONS INTERFACE

A full-duplex asynchronous Serial Communications Interface (SCI) is provided with a standard NRZ format and a variety of baud rates. The SCI transmitter and receiver are functionally independent, but use the same data format and bit rate. The serial data format is standard mark/space (NRZ) with one start bit, eight or nine data bits and one stop bit. The SCI can be interrupt driven.

OPTION REGISTER

The option register contains 3 bits which control the configuration of the memory map and the I-bit which controls the operation of the external interrupt IRQ. The three option bits operate in the following way:

$3FDF	OPTION	RAM0	RAM1	—	—	—	—	IRQEL	—

- IRQEL When set, this bit selects the EDGE and LEVEL interrupt option.

  When clear, the EDGE only option is selected. This bit is not readable and can only be written once after RESET.

  RESET sets this bit.

- RAM1 When set, this bit maps 128 bytes of RAM into the memory map starting at address $100. This makes inaccessible the 128 bytes of ROM that were formerly at these addresses. This bit is readable and writable at all times, allowing the user to switch back and forth between memory types during the course of execution.

  RESET clears this bit.

- RAM0 When set, this bit maps 48 bytes of RAM into page zero starting at address $20. This makes the 48 bytes of page zero ROM inaccessible. This bit is readable and writable at all times, allowing the user to switch back and forth between memory types during the course of execution.

  RESET clears this bit.

COMPUTER OPERATING PROPERLY(COP)

The MC68HC05M9 includes a COP watchdog system to help protect against software failures.

In order to use the COP watchdog timer, the application must be able to execute the special watchdog reset sequence on a regular periodic basis so that the watchdog timer never times out. Although most software disciplines permit the watchdog system concept there is no widely accepted time out period. To keep the MC68HC05M9 compatible with as many different applications as possible, the COP function includes special control bits which allow one of four time out periods to be specified. These control bits also allow the function to be disabled completely.

Since the COP function relies on the system clock (E) to detect a software failure, it follows that a Clock Monitor system is included to guard against clock failure. The COP timer cannot operate if the E-clock fails. To protect against this the Clock Monitor system should be enabled while the COP system is enabled.

Clock Monitor

The clock monitor is enabled/disabled by a software control bit in the COP control register and will generate a reset when the internal clock of the processor is absent for more than a certain period of time.

The time-out period is dependent on the processing parameters but will be between 5 and 100µs. Systems operating near or below 200kHz E-clock rate should not use the Clock Monitor function.

TIMERS

Timer A

The 16-bit programmable timer can be used for measuring the pulse width of an input signal while simultaneously generating an output signal. Pulse widths of the input and output signals can vary from several microseconds to many seconds. The timer is also capable of generating periodic interrupts or indicating the passage of an arbitrary number of process cycles.

Because the timer has a 16-bit architecture, each specific functional segment is represented by two registers. These registers contain the 'High' and 'Low' bytes of this functional segment. Generally, accessing the Low byte of a specific timer function allows full control of that function; accessing the High byte will inhibit that capability until the Low byte is accessed.

Note: The I-bit in the condition code register should be set, while manipulating both the High and Low byte register of a specific timer function, to ensure that an interrupt does not occur. A problem could arise if an interrupt were to occur in the time interval between accessing the Low byte and accessing the High byte.

Timer B

Timer B, the second timer in the MC68HC05M9, is an 8-bit free running down counter with a modulus latch, a 7-bit prescaler and, an overflow output signal with a toggle option. It also has input options for pulse counting and width measurement.

The Timer B prescaler counter is not accessible directly by software, but can be affected by it. The prescaler divides the Timer B source by a selectable power of 2 before presentation to the data register counter.

PORTS

Parallel ports

In the single chip mode, there is a total of three I/O ports and three high voltage ports available.

I/O ports

Ports A, B and C are dedicated 8-bit I/O ports. Their I/O pins are individually programmable (under software control) to be either input or output. The direction of the pins of these ports is determined by the associated data direction register (DDR).

When a data direction register bit is set to one, the corresponding I/O pin becomes an output. A read of the pin, configured as an output, returns the last logic level written to that pin, rather than a logic level derived from the existing voltage on the pin at the time of the read. This is necessary for the proper operation of read/modify/write instructions in the presence of heavy electrical loads on the port's output drivers.

At power-on or external reset all DDRs are set to zero which forces all I/O pins to appear as inputs. The DDRs can be written to and read by the processor.

High Voltage ports

Ports D, E0 and E1 are high voltage, high current output ports suitable for use with vacuum fluorescent displays (VFD). Each output is configured as an open drain PMOS device with an associated, on-chip pull-down resistor. The other side of the resistor is connected to the Vdisp power supply rail, which is the source of the negative high voltage required for the vacuum fluorescent displays.

ELECTRICAL SPECIFICATIONS

Maximum Ratings

Rating	Symbol	Value	Unit
Positive Supply Voltage	V_{DD}	–0.3 to +7.0	V
Negative Supply Voltage	V_{DISP}	–35 to 0	V
Input Voltage (except IRQ pin)	V_{IN}	V_{SS} – 0.3 to V_{DD} + 0.3	V
IRQ Voltage	V_{IN}	V_{SS} – 0.3 to 2xV_{DD} + 0.3	V
Current Drain per pin (except V_{SS} and V_{DD})	I	30	mA
Current Drain for Port D (total)	I	240	mA
Current Drain for Port D (per pin)	I	40	mA
Current Drain for Port E0, E1 (total)	I	80	mA
Current Drain for Port E0, E1 (per pin)	I	13	mA
Operating Temperature range	T_A	0 to +70	°C
Storage Temperature range	T_{STG}	-65 to +150	°C

Note: Usually chip power is greater than the input/output port power but in the MC68HC05M9 this may not be the case. The majority of the current can in fact be sourced by the VF driver ports PD, PE0 and PE1.

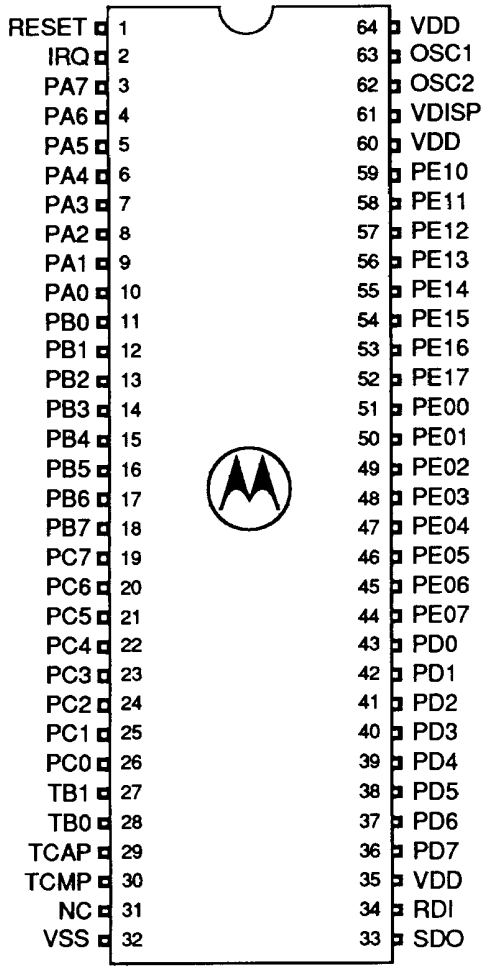
DC Electrical Characteristics

(V_{DD} = 5Vdc±10%, V_{SS} = 0Vdc, T_A = 0^0 to 70^0 C)

Characteristic	Symbol	Min	Typ	Max	Unit
Output High Voltage	V_{OH}				V
$I_{LOAD} \leq$ -10μA		V_{DD} – 0.1	—	—	
$I_{LOAD} \leq$ -0.8mA PA, PB, PC, TBO, TCMP, SDO		V_{DD} – 0.8	—	—	
$I_{LOAD} \leq$ -10mA PE1 & PE2		V_{DD} – 2.0	—	—	
$I_{LOAD} \leq$ -30mA PD		V_{DD} – 2.0	—	—	
Output Low Voltage	V_{OL}				V
$I_{LOAD} \leq$ 10μA		—	—	0.1	
$I_{LOAD} \leq$ 1.6mA PA, PB, PC, TBO, TCMP, SDO		—	—	0.4	
Input High Voltage	V_{IH}				V
PA, PB, PC, RESET, OSC1, RDI, TCAP, TBI		V_{DD} x 0.7	—	V_{DD}	
IRQ		—	—	V_{DD} x 2	
Input Low Voltage	V_{IL}				V
PA, PB, PC, RESET, OSC1, RDI, TCAP, TBI, IRQ		V_{SS}	—	V_{DD} x 0.2	
Supply Currents	I_{DD}				mA
Run		—	15	—	
Wait		—	5	—	
Stop		—	0.25	—	
C_{LOAD} = 50pF, no DC loads, T_{CYC} = 500ns					
Data retention mode (0° - 70° C)	V_{RM}	2.0	—	—	V
Input/Output ports Hi-Z Leakage Current	I_{IN}				μA
PA, PB, PC		—	—	±10	
Input Leakage Current	I_{IN}				μA
PA, PB, PC, IRQ, RESET, OSC1, RDI, TCAP, TBI		—	—	±1	
Capacitance					pF
PA, PB, PC (as input or output)	C_{OUT}	—	—	12	
PE0, PE1, PD, SDO, TCMP, TBO	C_{OUT}	—	—	12	
RESET, OSC1, IRQ, RDI, TCAP, TBI	C_{IN}	—	—	8	
On chip pull-down to V_{DISP} (Nom. 50KΩ) **TBD**	R_{DISP}	25	—	100	KΩ

Note: Typical values are at mid point of voltage range and at 25°C only.

64 pin DIL



64 pin QFP

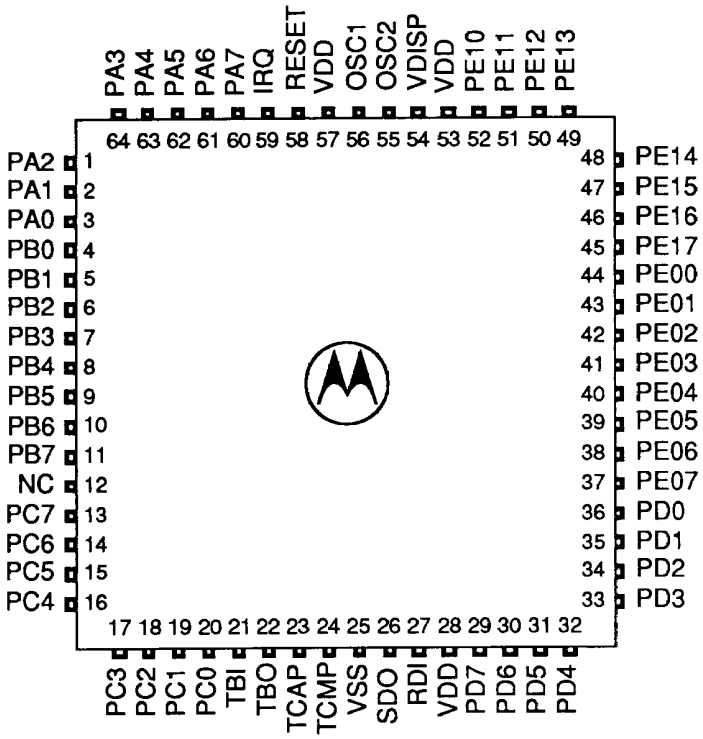


Figure 3. Pinouts

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