

## Description

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The M16C/62M group of single-chip microcomputers are built using the high-performance silicon gate CMOS process using a M16C/60 Series CPU core and are packaged in a 100-pin plastic molded QFP. These single-chip microcomputers operate using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, low voltage (2.2V to 3.6V), they are capable of executing instructions at high speed. They also feature a built-in multiplier and DMAC, making them ideal for controlling office, communications, industrial equipment, and other high-speed processing applications.

The M16C/62M group includes a wide range of products with different internal memory types and sizes and various package types.

### Features

- Memory capacity ..... ROM (See Figure 1.1.4. ROM Expansion)  
RAM 10K to 20K bytes
- Shortest instruction execution time ..... 100ns (f(XIN)=10MHz, VCC=2.7V to 3.6V)  
142.9ns (f(XIN)=7MHz, VCC=2.2V to 3.6V with software one-wait)
- Supply voltage ..... 2.7V to 3.6V (f(XIN)=10MHz, without software wait)  
2.4V to 2.7V (f(XIN)=7MHz, without software wait)  
2.2V to 2.4V (f(XIN)=7MHz with software one-wait)
- Low power consumption ..... 28.5mW (VCC = 3V, f(XIN)=10MHz, without software wait)
- Interrupts ..... 25 internal and 8 external interrupt sources, 4 software  
interrupt sources; 7 levels (including key input interrupt)
- Multifunction 16-bit timer ..... 5 output timers + 6 input timers
- Serial I/O ..... 5 channels  
(3 for UART or clock synchronous, 2 for clock synchronous)
- DMAC ..... 2 channels (trigger: 24 sources)
- A-D converter ..... 10 bits X 8 channels (Expandable up to 10 channels)
- D-A converter ..... 8 bits X 2 channels
- CRC calculation circuit ..... 1 circuit
- Watchdog timer ..... 1 line
- Programmable I/O ..... 87 lines
- Input port ..... 1 line (P85 shared with  $\overline{\text{NMI}}$  pin)
- Memory expansion ..... Available (to a maximum of 1M bytes)
- Chip select output ..... 4 lines
- Clock generating circuit ..... 2 built-in clock generation circuits  
(built-in feedback resistor, and external ceramic or quartz oscillator)

### Applications

Audio, cameras, office equipment, communications equipment, portable equipment

Description

Pin Configuration

Figures 1.1.1 and 1.1.2 show the pin configurations (top view).

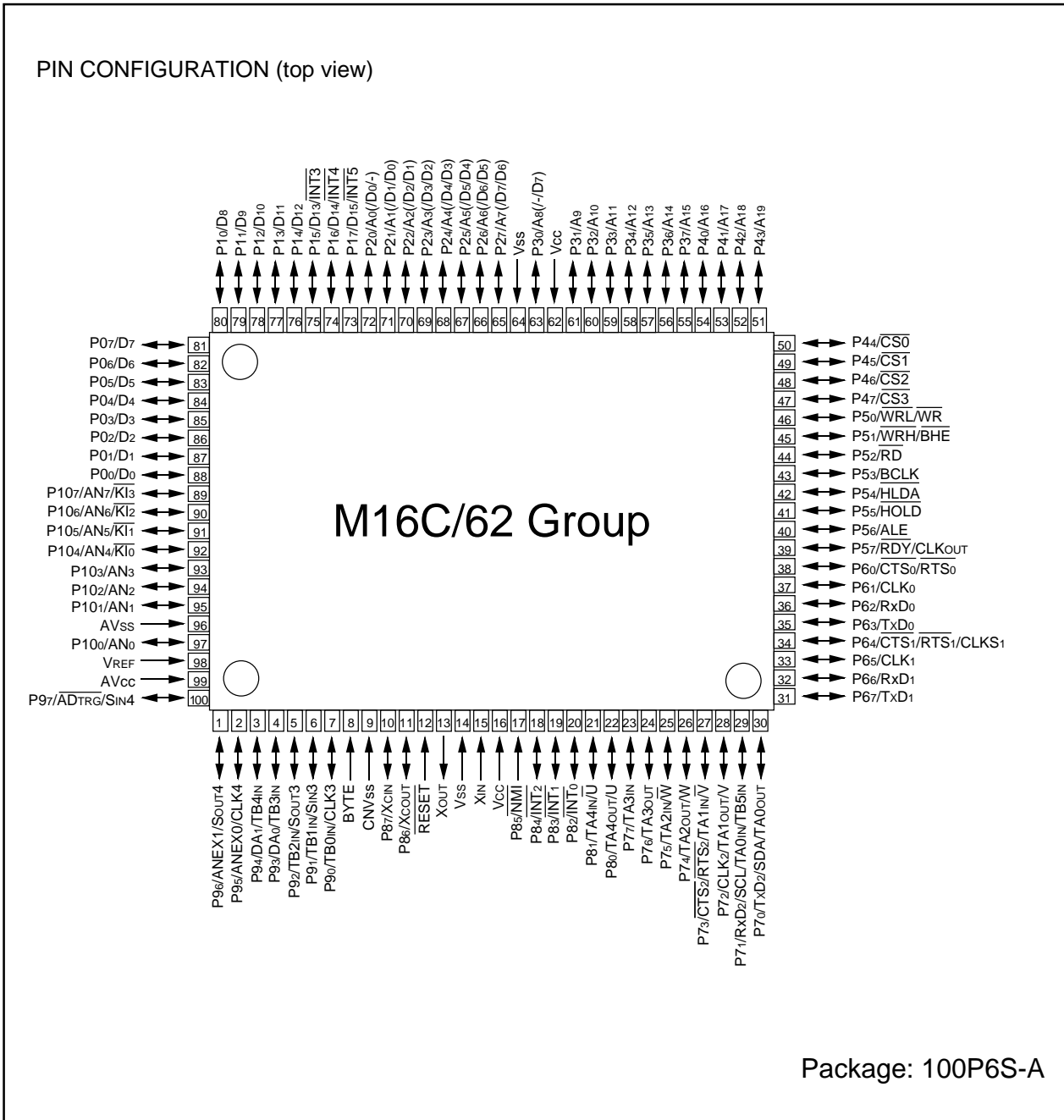


Figure 1.1.1. Pin configuration (top view)

Description

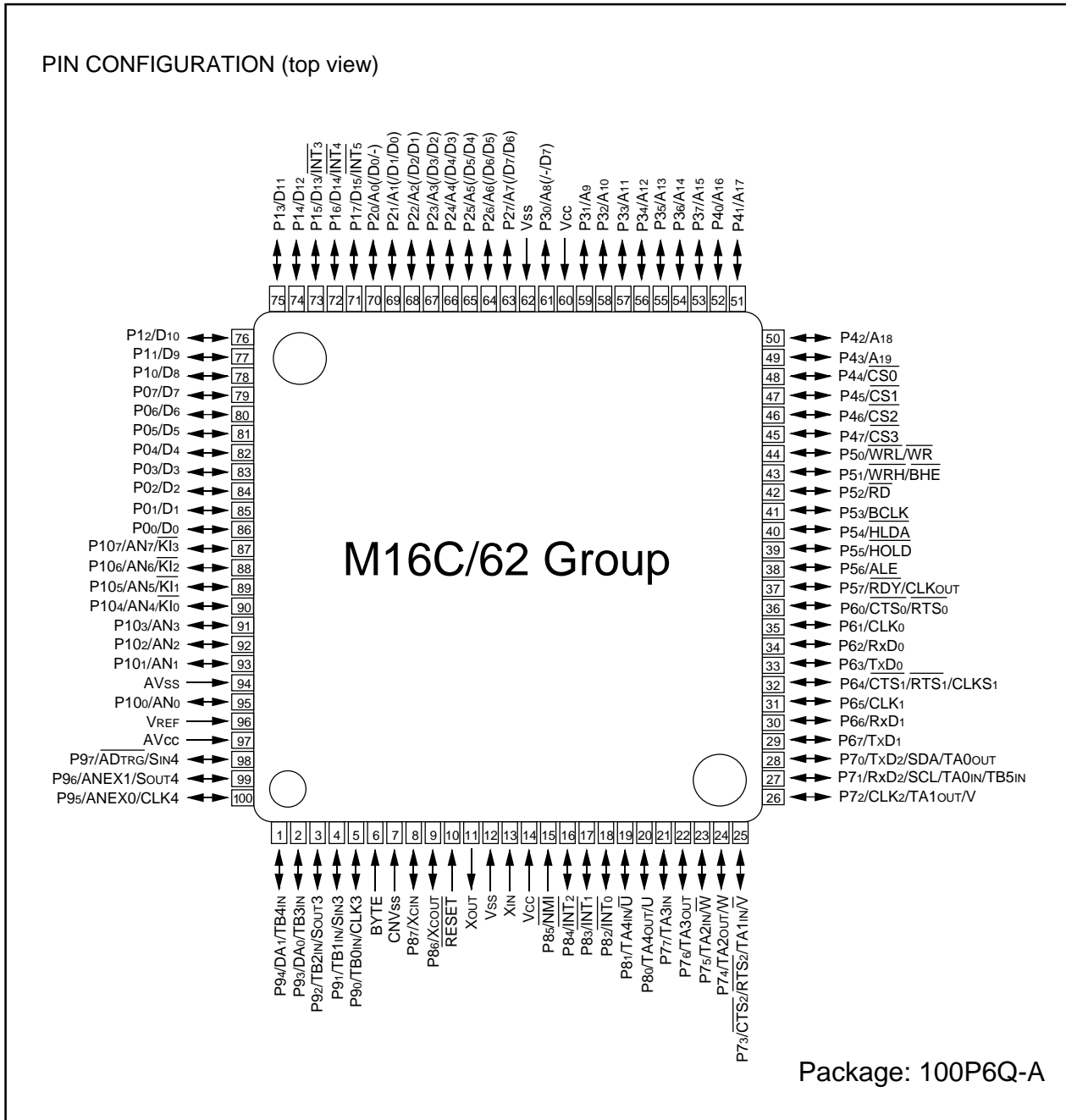


Figure 1.1.2. Pin configuration (top view)

Description

Block Diagram

Figure 1.1.3 is a block diagram of the M16C/62M group.

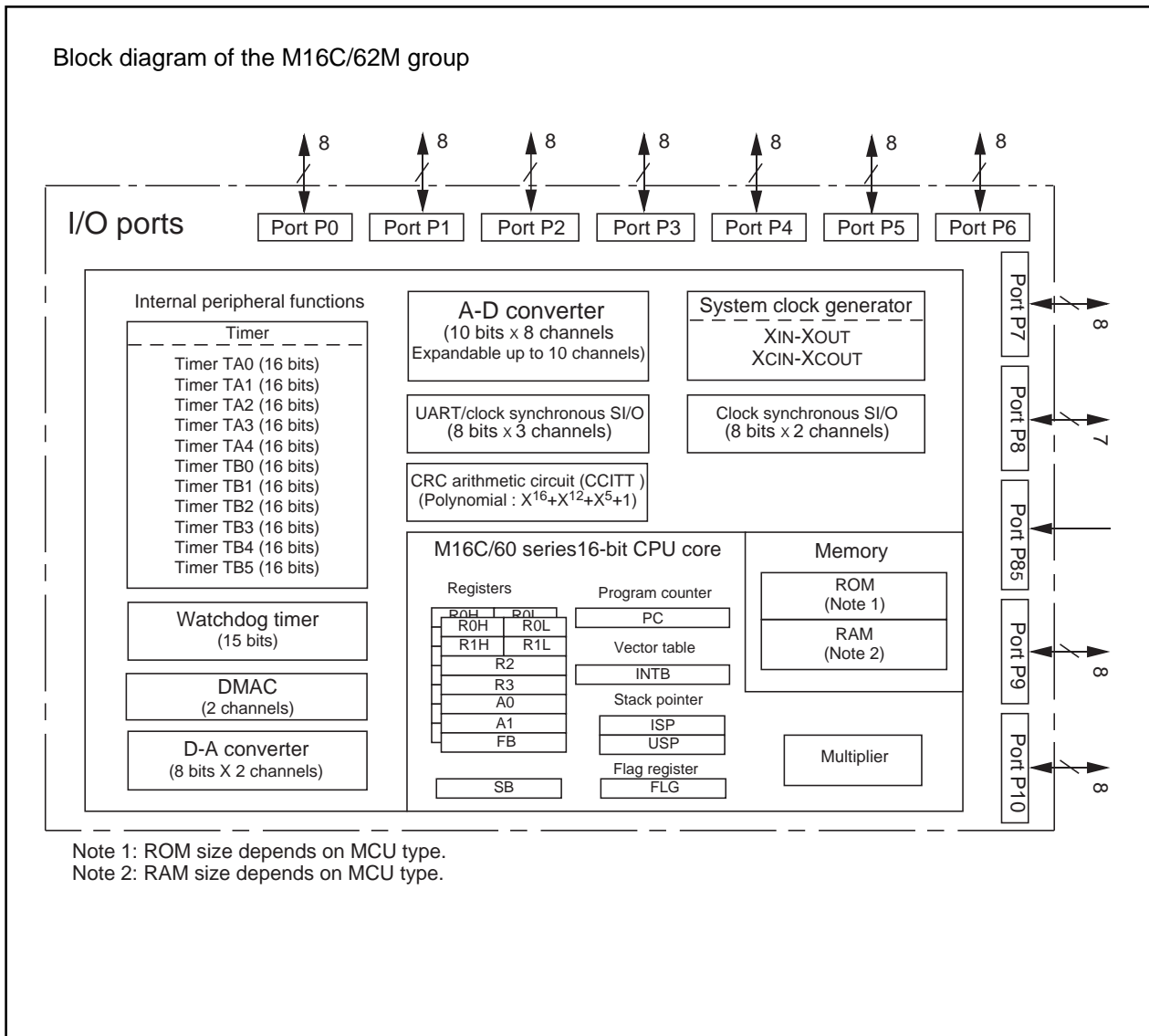


Figure 1.1.3. Block diagram of M16C/62M group

Description

**Performance Outline**

Table 1.1.1 is a performance outline of M16C/62M group.

**Table 1.1.1. Performance outline of M16C/62M group**

Item		Performance
Number of basic instructions		91 instructions
Shortest instruction execution time		100ns( $f(X_{IN})=10\text{MHz}$ , $V_{CC}=2.7\text{V}$ to $3.6\text{V}$ ) 142.9ns ( $f(X_{IN})=7\text{MHz}$ , $V_{CC}=2.2\text{V}$ to $3.6\text{V}$ with software one-wait)
Memory capacity	ROM	(See the figure 1.1.4. ROM Expansion)
	RAM	10K to 20K bytes
I/O port	P0 to P10 (except P85)	8 bits x 10, 7 bits x 1
Input port	P85	1 bit x 1
Multifunction timer	TA0, TA1, TA2, TA3, TA4	16 bits x 5
	TB0, TB1, TB2, TB3, TB4, TB5	16 bits x 6
Serial I/O	UART0, UART1, UART2	(UART or clock synchronous) x 3
	SI/O3, SI/O4	(Clock synchronous) x 2
A-D converter		10 bits x (8 + 2) channels
D-A converter		8 bits x 2
DMAC		2 channels (trigger: 24 sources)
CRC calculation circuit		CRC-CCITT
Watchdog timer		15 bits x 1 (with prescaler)
Interrupt		25 internal and 8 external sources, 4 software sources, 7 levels
Clock generating circuit		2 built-in clock generation circuits (built-in feedback resistor, and external ceramic or quartz oscillator)
Supply voltage		2.7V to 3.6V ( $f(X_{IN})=10\text{MHz}$ , without software wait) 2.4V to 2.7V ( $f(X_{IN})=7\text{MHz}$ , without software wait) 2.2V to 2.4V ( $f(X_{IN})=7\text{MHz}$ with software one-wait)
Power consumption		28.5mW ( $f(X_{IN})=10\text{MHz}$ , $V_{CC}=3\text{V}$ without software wait)
I/O characteristics	I/O withstand voltage	3V
	Output current	1mA
Memory expansion		Available (to a maximum of 1M bytes)
Device configuration		CMOS high performance silicon gate
Package		100-pin plastic mold QFP

Description

Mitsubishi plans to release the following products in the M16C/62M group:

(1) Support for mask ROM version and Flash memory version

(2) ROM capacity

(3) Package

100P6S-A : Plastic molded QFP (mask ROM and flash memory versions)

100P6Q-A : Plastic molded QFP (mask ROM and flash memory versions)

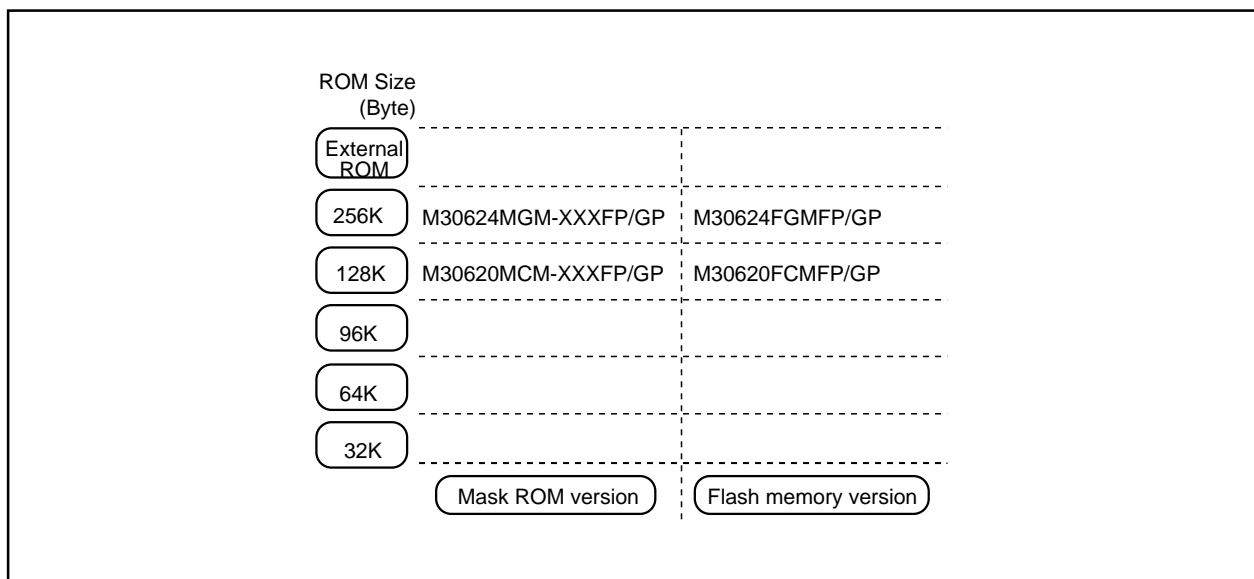


Figure 1.1.4. ROM expansion

The M16C/62M group products currently supported are listed in Table 1.1.2.

Table 1.1.2. M16C/62M group

June, 2000

Type No	ROM capacity	RAM capacity	Package type	Remarks
M30620MCM-XXXFP	128K byte	10K byte	100P6S-A	mask ROM version
M30620MCM-XXXGP			100P6Q-A	
M30624MGM-XXXFP	256K byte	20K byte	100P6S-A	
M30624MGM-XXXGP			100P6Q-A	
M30620FCMFP	128K byte	10K byte	100P6S-A	Flash memory 3V version
M30620FCMGP			100P6Q-A	
M30624FGMFP	256K byte	20K byte	100P6S-A	
M30624FGMGP			100P6Q-A	

Description

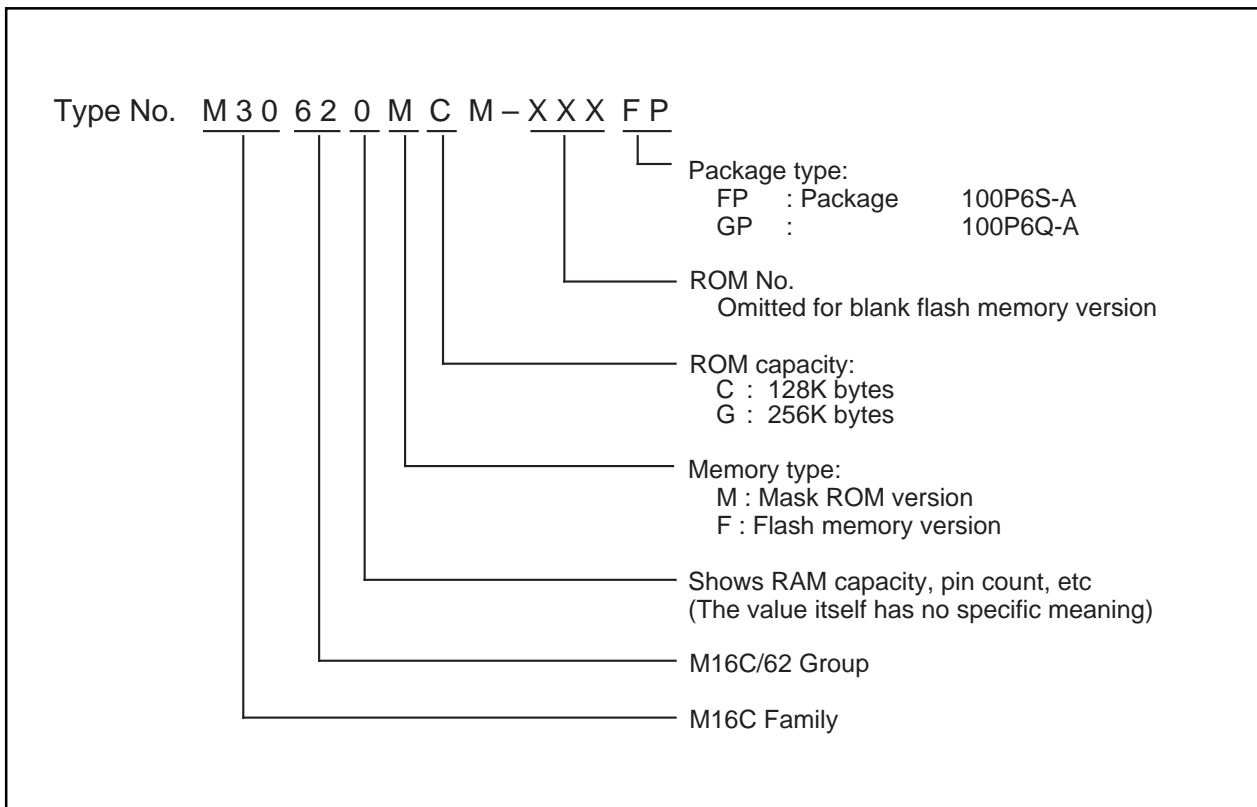


Figure 1.1.5. Type No., memory size, and package

**Table 1.26.1. Absolute maximum ratings**

Symbol	Parameter		Condition	Rated value	Unit
V <sub>cc</sub>	Supply voltage		V <sub>cc</sub> =AV <sub>cc</sub>	- 0.3 to 4.6	V
AV <sub>cc</sub>	Analog supply voltage		V <sub>cc</sub> =AV <sub>cc</sub>	- 0.3 to 4.6	V
V <sub>I</sub>	Input voltage	RESET, CNV <sub>ss</sub> , BYTE, P0 <sub>0</sub> to P0 <sub>7</sub> , P1 <sub>0</sub> to P1 <sub>7</sub> , P2 <sub>0</sub> to P2 <sub>7</sub> , P3 <sub>0</sub> to P3 <sub>7</sub> , P4 <sub>0</sub> to P4 <sub>7</sub> , P5 <sub>0</sub> to P5 <sub>7</sub> , P6 <sub>0</sub> to P6 <sub>7</sub> , P7 <sub>2</sub> to P7 <sub>7</sub> , P8 <sub>0</sub> to P8 <sub>7</sub> , P9 <sub>0</sub> to P9 <sub>7</sub> , P10 <sub>0</sub> to P10 <sub>7</sub> , VREF, X <sub>IN</sub>		- 0.3 to V <sub>cc</sub> + 0.3	V
		P7 <sub>0</sub> , P7 <sub>1</sub>		- 0.3 to 4.6	V
V <sub>O</sub>	Output voltage	P0 <sub>0</sub> to P0 <sub>7</sub> , P1 <sub>0</sub> to P1 <sub>7</sub> , P2 <sub>0</sub> to P2 <sub>7</sub> , P3 <sub>0</sub> to P3 <sub>7</sub> , P4 <sub>0</sub> to P4 <sub>7</sub> , P5 <sub>0</sub> to P5 <sub>7</sub> , P6 <sub>0</sub> to P6 <sub>7</sub> , P7 <sub>2</sub> to P7 <sub>7</sub> , P8 <sub>0</sub> to P8 <sub>4</sub> , P8 <sub>6</sub> , P8 <sub>7</sub> , P9 <sub>0</sub> to P9 <sub>7</sub> , P10 <sub>0</sub> to P10 <sub>7</sub> , X <sub>OUT</sub>		- 0.3 to V <sub>cc</sub> + 0.3	V
		P7 <sub>0</sub> , P7 <sub>1</sub>		- 0.3 to 4.6	V
P <sub>d</sub>	Power dissipation		T <sub>a</sub> =25 °C	300	mW
T <sub>opr</sub>	Operating ambient temperature			- 20 to 85 / -40 to 85 (Note)	°C
T <sub>stg</sub>	Storage temperature			- 65 to 150	°C

Note : Specify a product of -40°C to 85°C to use it.



Electrical characteristics

**Table 1.26.2. Recommended operating conditions (referenced to V<sub>CC</sub> = 2.2V to 3.6V at Ta = -20°C to 85°C / -40°C to 85°C(Note3) unless otherwise specified)**

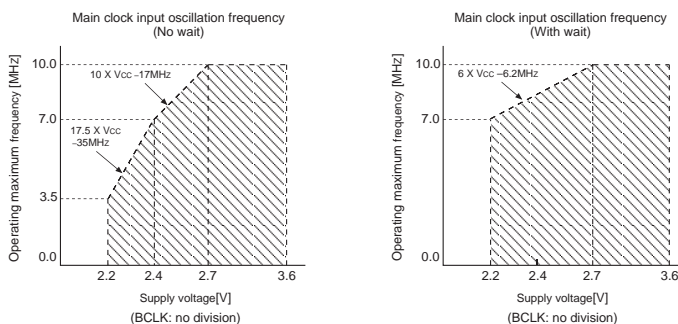
Symbol	Parameter	Standard			Unit	
		Min.	Typ.	Max.		
V <sub>CC</sub>	Supply voltage	2.2	3.0	3.6	V	
AV <sub>CC</sub>	Analog supply voltage		V <sub>CC</sub>		V	
V <sub>SS</sub>	Supply voltage		0		V	
AV <sub>SS</sub>	Analog supply voltage		0		V	
V <sub>IH</sub>	HIGH input voltage P31 to P37, P40 to P47, P50 to P57, P60 to P67, P72 to P77, P80 to P87, P90 to P97, P100 to P107, X <sub>IN</sub> , RESET, CNV <sub>SS</sub> , BYTE P70, P71	P31 to P37, P40 to P47, P50 to P57, P60 to P67, P72 to P77, P80 to P87, P90 to P97, P100 to P107, X <sub>IN</sub> , RESET, CNV <sub>SS</sub> , BYTE	0.8V <sub>CC</sub>	V <sub>CC</sub>	V	
		P70, P71	0.8V <sub>CC</sub>	4.6	V	
		P00 to P07, P10 to P17, P20 to P27, P30 (during single-chip mode)	0.8V <sub>CC</sub>	V <sub>CC</sub>	V	
		P00 to P07, P10 to P17, P20 to P27, P30 (data input function during memory expansion and microprocessor modes)	0.5V <sub>CC</sub>	V <sub>CC</sub>	V	
V <sub>IL</sub>	LOW input voltage P31 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P107, X <sub>IN</sub> , RESET, CNV <sub>SS</sub> , BYTE	P31 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P107, X <sub>IN</sub> , RESET, CNV <sub>SS</sub> , BYTE	0	0.2V <sub>CC</sub>	V	
		P00 to P07, P10 to P17, P20 to P27, P30 (during single-chip mode)	0	0.2V <sub>CC</sub>	V	
		P00 to P07, P10 to P17, P20 to P27, P30 (data input function during memory expansion and microprocessor modes)	0	0.16V <sub>CC</sub>	V	
I <sub>OH</sub> (peak)	HIGH peak output current P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P72 to P77, P80 to P84, P86, P87, P90 to P97, P100 to P107			- 10.0	mA	
I <sub>OH</sub> (avg)	HIGH average output current P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P72 to P77, P80 to P84, P86, P87, P90 to P97, P100 to P107			- 5.0	mA	
I <sub>OL</sub> (peak)	LOW peak output current P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P72 to P77, P80 to P84, P86, P87, P90 to P97, P100 to P107			10.0	mA	
I <sub>OL</sub> (avg)	LOW average output current P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P72 to P77, P80 to P84, P86, P87, P90 to P97, P100 to P107			5.0	mA	
f (X <sub>IN</sub> )	Main clock input oscillation frequency	No wait	V <sub>CC</sub> =2.7V to 3.6V	0	10	MHz
			V <sub>CC</sub> =2.4V to 2.7V	0	10 X V <sub>CC</sub> - 17	MHz
		with wait	V <sub>CC</sub> =2.2V to 2.4V	0	17.5 X V <sub>CC</sub> - 35	MHz
			V <sub>CC</sub> =2.7V to 3.6V	0	10	MHz
			V <sub>CC</sub> =2.2V to 2.7V	0	6 X V <sub>CC</sub> - 6.2	MHz
f (X <sub>CIN</sub> )	Subclock oscillation frequency		32.768	50	kHz	

Note 1: The mean output current is the mean value within 100ms.

Note 2: The total I<sub>OL</sub> (peak) for ports P0, P1, P2, P86, P87, P9, and P10 must be 80mA max. The total I<sub>OH</sub> (peak) for ports P0, P1, P2, P86, P87, P9, and P10 must be 80mA max. The total I<sub>OL</sub> (peak) for ports P3, P4, P5, P6, P7, and P80 to P84 must be 80mA max. The total I<sub>OH</sub> (peak) for ports P3, P4, P5, P6, P72 to P77, and P80 to P84 must be 80mA max.

Note 3: Specify a product of -40°C to 85°C to use it.

Note 4: Relationship between main clock oscillation frequency and supply voltage.



Flash memory version program voltage and read operation voltage characteristics

Flash program voltage	Flash read operation voltage
V <sub>CC</sub> =2.7V to 3.6V	V <sub>CC</sub> =2.4V to 3.6V
V <sub>CC</sub> =2.7V to 3.4V	V <sub>CC</sub> =2.2V to 2.4V

Note 5: Execute case without wait, program / erase of flash memory by V<sub>CC</sub>=2.7V to 3.6V and f(BCLK) ≤ 6.25 MHz. Execute case with wait, program / erase of flash memory by V<sub>CC</sub>=2.7V to 3.6V and f(BCLK) ≤ 10.0 MHz.

**Table 1.26.3. Electrical characteristics (referenced to  $V_{CC} = 2.7V$  to  $3.6V$ ,  $V_{SS} = 0V$  at  $T_a = -20^{\circ}C$  to  $85^{\circ}C$  /  $-40^{\circ}C$  to  $85^{\circ}C$  (Note1),  $f(X_{IN}) = 10MHz$  without wait unless otherwise specified)**

Symbol	Parameter		Measuring condition	Standard			Unit	
				Min	Typ.	Max.		
$V_{OH}$	HIGH output voltage	P0 <sub>0</sub> to P0 <sub>7</sub> , P1 <sub>0</sub> to P1 <sub>7</sub> , P2 <sub>0</sub> to P2 <sub>7</sub> , P3 <sub>0</sub> to P3 <sub>7</sub> , P4 <sub>0</sub> to P4 <sub>7</sub> , P5 <sub>0</sub> to P5 <sub>7</sub> , P6 <sub>0</sub> to P6 <sub>7</sub> , P7 <sub>2</sub> to P7 <sub>7</sub> , P8 <sub>0</sub> to P8 <sub>4</sub> , P8 <sub>6</sub> , P8 <sub>7</sub> , P9 <sub>0</sub> to P9 <sub>7</sub> , P10 <sub>0</sub> to P10 <sub>7</sub>	$I_{OH} = -1mA$	2.5			V	
$V_{OH}$	HIGH output voltage	$X_{OUT}$	HIGHPOWER	$I_{OH} = -0.1mA$	2.5		V	
			LOWPOWER	$I_{OH} = -50\mu A$	2.5			
$V_{OH}$	HIGH output voltage	$X_{COUT}$	HIGHPOWER	With no load applied		3.0	V	
			LOWPOWER	With no load applied		1.6		
$V_{OL}$	LOW output voltage	P0 <sub>0</sub> to P0 <sub>7</sub> , P1 <sub>0</sub> to P1 <sub>7</sub> , P2 <sub>0</sub> to P2 <sub>7</sub> , P3 <sub>0</sub> to P3 <sub>7</sub> , P4 <sub>0</sub> to P4 <sub>7</sub> , P5 <sub>0</sub> to P5 <sub>7</sub> , P6 <sub>0</sub> to P6 <sub>7</sub> , P7 <sub>0</sub> to P7 <sub>7</sub> , P8 <sub>0</sub> to P8 <sub>4</sub> , P8 <sub>6</sub> , P8 <sub>7</sub> , P9 <sub>0</sub> to P9 <sub>7</sub> , P10 <sub>0</sub> to P10 <sub>7</sub>	$I_{OL} = 1mA$			0.5	V	
$V_{OL}$	LOW output voltage	$X_{OUT}$	HIGHPOWER	$I_{OL} = 0.1mA$		0.5	V	
			LOWPOWER	$I_{OL} = 50\mu A$		0.5		
$V_{OL}$	LOW output voltage	$X_{COUT}$	HIGHPOWER	With no load applied		0	V	
			LOWPOWER	With no load applied		0		
$V_{T+}-V_{T-}$	Hysteresis	HOLD, RDY, TA0 <sub>IN</sub> to TA4 <sub>IN</sub> , TB0 <sub>IN</sub> to TB5 <sub>IN</sub> , INT0 to INT5, NMI, ADTRG, CTS0 to CTS2, SCL, SDA, CLK0 to CLK4, TA2 <sub>OUT</sub> to TA4 <sub>OUT</sub> , KI0 to KI3, RxD0 to RxD2, SIN3, SIN4		0.2		0.8	V	
$V_{T+}-V_{T-}$	Hysteresis	RESET		0.2		1.8	V	
$I_{IH}$	HIGH input current	P0 <sub>0</sub> to P0 <sub>7</sub> , P1 <sub>0</sub> to P1 <sub>7</sub> , P2 <sub>0</sub> to P2 <sub>7</sub> , P3 <sub>0</sub> to P3 <sub>7</sub> , P4 <sub>0</sub> to P4 <sub>7</sub> , P5 <sub>0</sub> to P5 <sub>7</sub> , P6 <sub>0</sub> to P6 <sub>7</sub> , P7 <sub>0</sub> to P7 <sub>7</sub> , P8 <sub>0</sub> to P8 <sub>7</sub> , P9 <sub>0</sub> to P9 <sub>7</sub> , P10 <sub>0</sub> to P10 <sub>7</sub> , X <sub>IN</sub> , RESET, CNV <sub>SS</sub> , BYTE	$V_i = 3V$			4.0	$\mu A$	
$I_{IL}$	LOW input current	P0 <sub>0</sub> to P0 <sub>7</sub> , P1 <sub>0</sub> to P1 <sub>7</sub> , P2 <sub>0</sub> to P2 <sub>7</sub> , P3 <sub>0</sub> to P3 <sub>7</sub> , P4 <sub>0</sub> to P4 <sub>7</sub> , P5 <sub>0</sub> to P5 <sub>7</sub> , P6 <sub>0</sub> to P6 <sub>7</sub> , P7 <sub>0</sub> to P7 <sub>7</sub> , P8 <sub>0</sub> to P8 <sub>7</sub> , P9 <sub>0</sub> to P9 <sub>7</sub> , P10 <sub>0</sub> to P10 <sub>7</sub> , X <sub>IN</sub> , RESET, CNV <sub>SS</sub> , BYTE	$V_i = 0V$			-4.0	$\mu A$	
RPULLUP	Pull-up resistance	P0 <sub>0</sub> to P0 <sub>7</sub> , P1 <sub>0</sub> to P1 <sub>7</sub> , P2 <sub>0</sub> to P2 <sub>7</sub> , P3 <sub>0</sub> to P3 <sub>7</sub> , P4 <sub>0</sub> to P4 <sub>7</sub> , P5 <sub>0</sub> to P5 <sub>7</sub> , P6 <sub>0</sub> to P6 <sub>7</sub> , P7 <sub>2</sub> to P7 <sub>7</sub> , P8 <sub>0</sub> to P8 <sub>4</sub> , P8 <sub>6</sub> , P8 <sub>7</sub> , P9 <sub>0</sub> to P9 <sub>7</sub> , P10 <sub>0</sub> to P10 <sub>7</sub>	$V_i = 0V$	20	75	330	k $\Omega$	
RfXIN	Feedback resistance	X <sub>IN</sub>			3.0		M $\Omega$	
RfXCIN	Feedback resistance	X <sub>CIN</sub>			10.0		M $\Omega$	
VRAM	RAM retention voltage		When clock is stopped	2.0			V	
$I_{CC}$	Power supply current	In single-chip mode, the output pins are open and other pins are V <sub>SS</sub>	Mask ROM version	$f(X_{IN}) = 10MHz$ Square wave, no division		9.5	21.25	mA
			Flash memory 3V version	$f(X_{IN}) = 10MHz$ Square wave, no division		12.0	21.25	
			Mask ROM version, flash memory 3V version	$f(X_{CIN}) = 32kHz$ Square wave		45.0		$\mu A$
			Flash memory 3V version program	$f(X_{IN}) = 10MHz$ Square wave, division by 2		14.0		mA
			Flash memory 3V version erase	$f(X_{IN}) = 10MHz$ Square wave, division by 2		17.0		
			Mask ROM version, flash memory 3V version	$f(X_{CIN}) = 32kHz$ When a WAIT instruction is executed. Oscillation capacity High (Note2)		2.8		$\mu A$
				$f(X_{CIN}) = 32kHz$ When a WAIT instruction is executed. Oscillation capacity Low (Note2)		0.9		$\mu A$
	When clock is stopped	$T_a = 25^{\circ}C$			1.0	$\mu A$		
	When clock is stopped	$T_a = 85^{\circ}C$			20.0			

Note 1: Specify a product of  $-40^{\circ}C$  to  $85^{\circ}C$  to use it.

Note 2: With one timer operated using fc32.

## Electrical characteristics

**Table 1.26.4. A-D conversion characteristics (referenced to  $V_{CC} = AV_{CC} = V_{REF} = 2.4V$  to  $3.6V$ ,  $V_{SS} = AV_{SS} = 0V$ , at  $T_a = -20^{\circ}C$  to  $85^{\circ}C$  /  $-40^{\circ}C$  to  $85^{\circ}C$  (Note2),  $f(X_{IN})=10MHz$  unless otherwise specified)**

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max	
–	Resolution		$V_{REF} = V_{CC}$			10	Bits
–	Absolute accuracy	Sample & hold function not available (8 bit)	$V_{REF} = V_{CC} = 3V$ , $f_{AD} = f_{AD}/2$			$\pm 2$	LSB
$R_{LADDER}$	Ladder resistance		$V_{REF} = V_{CC}$	10		40	$k\Omega$
$t_{CONV}$	Conversion time(8bit)			9.8			$\mu s$
$V_{REF}$	Reference voltage			2.4		$V_{CC}$	V
$V_{IA}$	Analog input voltage			0		$V_{REF}$	V

Note 1: Connect  $AV_{CC}$  pin to  $V_{CC}$  pin and apply the same electric potential.

Note 2: Specify a product of  $-40^{\circ}C$  to  $85^{\circ}C$  to use it.

**Table 1.26.5. D-A conversion characteristics (referenced to  $V_{CC} = 2.4V$  to  $3.6V$ ,  $V_{SS} = AV_{SS} = 0V$ ,  $V_{REF} = 3V$ , at  $T_a = -20^{\circ}C$  to  $85^{\circ}C$  /  $-40^{\circ}C$  to  $85^{\circ}C$  (Note2),  $f(X_{IN})=10MHz$  unless otherwise specified)**

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max	
–	Resolution					8	Bits
–	Absolute accuracy					1.0	%
$t_{su}$	Setup time					3	$\mu s$
$R_o$	Output resistance			4	10	20	$k\Omega$
$I_{VREF}$	Reference power supply input current		(Note1)			1.0	mA

Note 1: This applies when using one D-A converter, with the D-A register for the unused D-A converter set to "0016". The A-D converter's ladder resistance is not included.

Also, when DA register contents are not "00", the current  $I_{VREF}$  always flows even though  $V_{ref}$  may have been set to be "unconnected" by the A-D control register.

Note 2: Specify a product of  $-40^{\circ}C$  to  $85^{\circ}C$  to use it.

**Table 1.26.6. Flash memory version electrical characteristics**

(referenced to  $V_{CC} = 2.7V$  to  $3.6V$ , at  $T_a = 0^{\circ}C$  to  $60^{\circ}C$  unless otherwise specified)

Parameter	Standard			Unit
	Min.	Typ.	Max	
Page program time		6	120	ms
Block erase time		50	600	ms
Erase all unlocked blocks time		50 X n (Note)	600 X n (Note)	ms
Lock bit program time		6	120	ms

Note : n denotes the number of block erases.

**Table 1.26.7. Flash memory version program voltage and read operation voltage characteristics ( $T_a = 0^{\circ}C$  to  $60^{\circ}C$ )**

Flash program voltage	Flash read operation voltage
$V_{CC} = 2.7V$ to $3.6V$	$V_{CC} = 2.4V$ to $3.6V$
$V_{CC} = 2.7V$ to $3.4V$	$V_{CC} = 2.2V$ to $2.4V$

## Timing

### Timing requirements

(referenced to  $V_{CC} = 3V$ ,  $V_{SS} = 0V$ , at  $T_a = -20^{\circ}C$  to  $85^{\circ}C$  /  $-40^{\circ}C$  to  $85^{\circ}C$  (\*) unless otherwise specified)

\* : Specify a product of  $-40^{\circ}C$  to  $85^{\circ}C$  to use it.

**Table 1.26.8. External clock input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_c$	External clock input cycle time	100		ns
$t_{w(H)}$	External clock input HIGH pulse width	40		ns
$t_{w(L)}$	External clock input LOW pulse width	40		ns
$t_r$	External clock rise time		18	ns
$t_f$	External clock fall time		18	ns

**Table 1.26.9. Memory expansion and microprocessor modes**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{ac1(RD-DB)}$	Data input access time (no wait)		(Note)	ns
$t_{ac2(RD-DB)}$	Data input access time (with wait)		(Note)	ns
$t_{ac3(RD-DB)}$	Data input access time (when accessing multiplex bus area)		(Note)	ns
$t_{su(DB-RD)}$	Data input setup time	80		ns
$t_{su(RDY-BCLK)}$	RDY input setup time	60		ns
$t_{su(HOLD-BCLK)}$	HOLD input setup time	80		ns
$t_h(RD-DB)$	Data input hold time	0		ns
$t_h(BCLK-RDY)$	RDY input hold time	0		ns
$t_h(BCLK-HOLD)$	HOLD input hold time	0		ns
$t_d(BCLK-HLDA)$	HLDA output delay time		100	ns

Note: Calculated according to the BCLK frequency as follows:

$$t_{ac1(RD-DB)} = \frac{10^9}{f(BCLK) \times 2} - 90 \quad [ns]$$

$$t_{ac2(RD-DB)} = \frac{3 \times 10^9}{f(BCLK) \times 2} - 90 \quad [ns]$$

$$t_{ac3(RD-DB)} = \frac{3 \times 10^9}{f(BCLK) \times 2} - 90 \quad [ns]$$

## Timing

**Timing requirements**(referenced to  $V_{CC} = 3V$ ,  $V_{SS} = 0V$ , at  $T_a = -20^{\circ}C$  to  $85^{\circ}C$  /  $-40^{\circ}C$  to  $85^{\circ}C$  (\*) unless otherwise specified)\* : Specify a product of  $-40^{\circ}C$  to  $85^{\circ}C$  to use it.**Table 1.26.10. Timer A input (counter input in event counter mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIn input cycle time	150		ns
$t_{w(TAH)}$	TAiIn input HIGH pulse width	60		ns
$t_{w(TAL)}$	TAiIn input LOW pulse width	60		ns

**Table 1.26.11. Timer A input (gating input in timer mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIn input cycle time	600		ns
$t_{w(TAH)}$	TAiIn input HIGH pulse width	300		ns
$t_{w(TAL)}$	TAiIn input LOW pulse width	300		ns

**Table 1.26.12. Timer A input (external trigger input in one-shot timer mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIn input cycle time	300		ns
$t_{w(TAH)}$	TAiIn input HIGH pulse width	150		ns
$t_{w(TAL)}$	TAiIn input LOW pulse width	150		ns

**Table 1.26.13. Timer A input (external trigger input in pulse width modulation mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIn input HIGH pulse width	150		ns
$t_{w(TAL)}$	TAiIn input LOW pulse width	150		ns

**Table 1.26.14. Timer A input (up/down input in event counter mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(UP)}$	TAiOUT input cycle time	3000		ns
$t_{w(UPH)}$	TAiOUT input HIGH pulse width	1500		ns
$t_{w(UPL)}$	TAiOUT input LOW pulse width	1500		ns
$t_{su(UP-TiN)}$	TAiOUT input setup time	600		ns
$t_{h(TiN-UP)}$	TAiOUT input hold time	600		ns

## Timing

**Timing requirements**(referenced to  $V_{CC} = 3V$ ,  $V_{SS} = 0V$ , at  $T_a = -20^{\circ}C$  to  $85^{\circ}C$  /  $-40^{\circ}C$  to  $85^{\circ}C$  (\*) unless otherwise specified)\* : Specify a product of  $-40^{\circ}C$  to  $85^{\circ}C$  to use it.**Table 1.26.15. Timer B input (counter input in event counter mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIn input cycle time (counted on one edge)	150		ns
$t_{w(TBH)}$	TBiIn input HIGH pulse width (counted on one edge)	60		ns
$t_{w(TBL)}$	TBiIn input LOW pulse width (counted on one edge)	60		ns
$t_{c(TB)}$	TBiIn input cycle time (counted on both edges)	300		ns
$t_{w(TBH)}$	TBiIn input HIGH pulse width (counted on both edges)	160		ns
$t_{w(TBL)}$	TBiIn input LOW pulse width (counted on both edges)	160		ns

**Table 1.26.16. Timer B input (pulse period measurement mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIn input cycle time	600		ns
$t_{w(TBH)}$	TBiIn input HIGH pulse width	300		ns
$t_{w(TBL)}$	TBiIn input LOW pulse width	300		ns

**Table 1.26.17. Timer B input (pulse width measurement mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIn input cycle time	600		ns
$t_{w(TBH)}$	TBiIn input HIGH pulse width	300		ns
$t_{w(TBL)}$	TBiIn input LOW pulse width	300		ns

**Table 1.26.18. A-D trigger input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(AD)}$	$\overline{ADTRG}$ input cycle time (trigger able minimum)	1500		ns
$t_{w(ADL)}$	$\overline{ADTRG}$ input LOW pulse width	200		ns

**Table 1.26.19. Serial I/O**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300		ns
$t_{w(CKH)}$	CLKi input HIGH pulse width	150		ns
$t_{w(CKL)}$	CLKi input LOW pulse width	150		ns
$t_d(C-Q)$	TxDi output delay time		160	ns
$t_h(C-Q)$	TxDi hold time	0		ns
$t_{su}(D-C)$	RxDi input setup time	50		ns
$t_h(C-D)$	RxDi input hold time	90		ns

**Table 1.26.20. External interrupt  $\overline{INTi}$  inputs**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input HIGH pulse width	380		ns
$t_{w(INL)}$	$\overline{INTi}$ input LOW pulse width	380		ns

Timing

Switching characteristics (referenced to  $V_{CC} = 3V$ ,  $V_{SS} = 0V$  at  $T_a = -20^{\circ}C$  to  $85^{\circ}C$  /  $-40^{\circ}C$  to  $85^{\circ}C$   
(Note 3), CM15 = "1" unless otherwise specified)

Table 1.26.21. Memory expansion and microprocessor modes (with no wait)

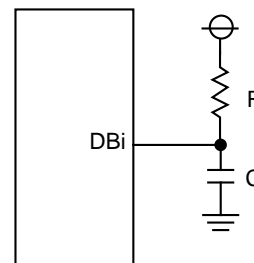
Symbol	Parameter	Measuring condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	Figure 1.26.1		60	ns
$t_{h(BCLK-AD)}$	Address output hold time (BCLK standard)		4		ns
$t_{h(RD-AD)}$	Address output hold time (RD standard)		0		ns
$t_{h(WR-AD)}$	Address output hold time (WR standard)		0		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			60	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (BCLK standard)		4		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			60	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		-4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			60	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			60	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (BCLK standard)			80	ns
$t_{h(BCLK-DB)}$	Data output hold time (BCLK standard)		4		ns
$t_{d(DB-WR)}$	Data output delay time (WR standard)		(Note1)		ns
$t_{h(WR-DB)}$	Data output hold time (WR standard)(Note2)		0		ns

Note 1: Calculated according to the BCLK frequency as follows:

$$t_{d(DB-WR)} = \frac{10^9}{f(BCLK) \times 2} - 80 \quad [ns]$$

Note 2: This is standard value shows the timing when the output is off, and doesn't show hold time of data bus.  
Hold time of data bus is different by capacitor volume and pull-up (pull-down) resistance value.  
Hold time of data bus is expressed in  
 $t = -CR \times \ln(1 - V_{OL} / V_{CC})$   
by a circuit of the right figure.  
For example, when  $V_{OL} = 0.2V_{CC}$ ,  $C = 30pF$ ,  $R = 1k\Omega$ , hold time of output "L" level is

$$t = -30pF \times 1k\Omega \times \ln(1 - 0.2V_{CC} / V_{CC}) = 6.7ns.$$



Note 3: Specify a product of  $-40^{\circ}C$  to  $85^{\circ}C$  to use it.

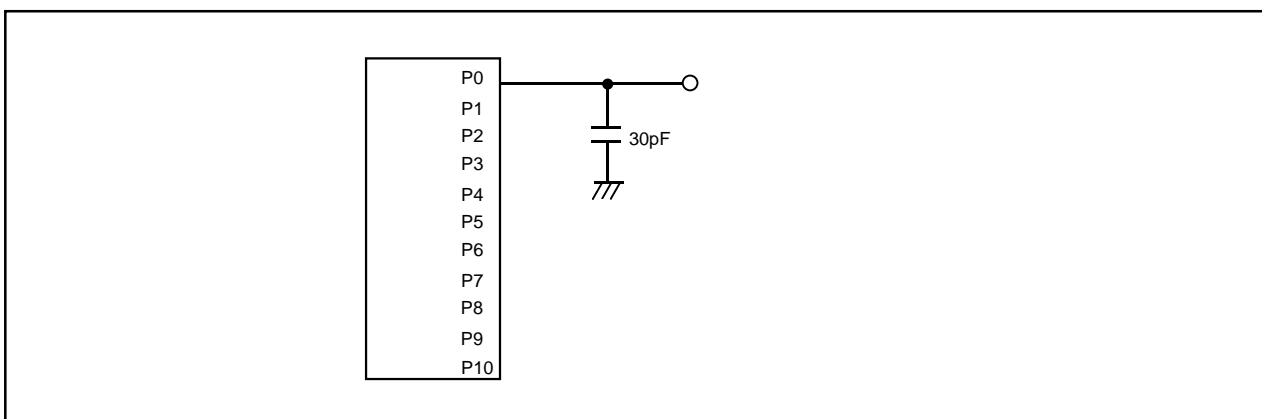


Figure 1.26.1. Port P0 to P10 measurement circuit

Timing

Switching characteristics (referenced to  $V_{cc} = 3V$ ,  $V_{ss} = 0V$  at  $T_a = -20^{\circ}C$  to  $85^{\circ}C$  /  $-40^{\circ}C$  to  $85^{\circ}C$   
(Note 3), CM15 = "1" unless otherwise specified)

Table 1.26.22. Memory expansion and microprocessor modes  
(when accessing external memory area with wait)

Symbol	Parameter	Measuring condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	Figure 1.26.1		60	ns
$t_{h(BCLK-AD)}$	Address output hold time (BCLK standard)		4		ns
$t_{h(RD-AD)}$	Address output hold time (RD standard)		0		ns
$t_{h(WR-AD)}$	Address output hold time (WR standard)		0		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			60	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (BCLK standard)		4		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			60	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		-4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			60	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			60	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (BCLK standard)			80	ns
$t_{h(BCLK-DB)}$	Data output hold time (BCLK standard)		4		ns
$t_{d(DB-WR)}$	Data output delay time (WR standard)		(Note1)		ns
$t_{h(WR-DB)}$	Data output hold time (WR standard)(Note2)		0		ns

Note 1: Calculated according to the BCLK frequency as follows:

$$t_{d(DB - WR)} = \frac{10^9}{f(BCLK)} - 80 \quad [ns]$$

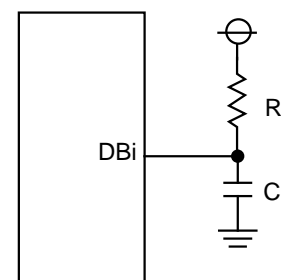
Note 2: This is standard value shows the timing when the output is off, and doesn't show hold time of data bus. Hold time of data bus is different by capacitor volume and pull-up (pull-down) resistance value.

Hold time of data bus is expressed in  
 $t = -CR \times \ln(1 - V_{OL} / V_{CC})$

by a circuit of the right figure.

For example, when  $V_{OL} = 0.2V_{CC}$ ,  $C = 30pF$ ,  $R = 1k\Omega$ , hold time of output "L" level is

$$t = -30pF \times 1k\Omega \times \ln(1 - 0.2V_{CC} / V_{CC}) = 6.7ns.$$



Note 3: Specify a product of  $-40^{\circ}C$  to  $85^{\circ}C$  to use it.



Timing

Switching characteristics (referenced to  $V_{CC} = 3V$ ,  $V_{SS} = 0V$  at  $T_a = -20^{\circ}C$  to  $85^{\circ}C$  /  $-40^{\circ}C$  to  $85^{\circ}C$  (Note 2), CM15 = "1" unless otherwise specified)

**Table 1.26.23. Memory expansion and microprocessor modes**  
(when accessing external memory area with wait, and select multiplexed bus)

Symbol	Parameter	Measuring condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	Figure 1.26.1		60	ns
$t_{h(BCLK-AD)}$	Address output hold time (BCLK standard)		4		ns
$t_{h(RD-AD)}$	Address output hold time (RD standard)		(Note 1)		ns
$t_{h(WR-AD)}$	Address output hold time (WR standard)		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			60	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (BCLK standard)		4		ns
$t_{h(RD-CS)}$	Chip select output hold time (RD standard)		(Note 1)		ns
$t_{h(WR-CS)}$	Chip select output hold time (WR standard)		(Note 1)		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			60	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			60	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (BCLK standard)			80	ns
$t_{h(BCLK-DB)}$	Data output hold time (BCLK standard)		4		ns
$t_{d(DB-WR)}$	Data output delay time (WR standard)		(Note 1)		ns
$t_{h(WR-DB)}$	Data output hold time (WR standard)		(Note 1)		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time (BCLK standard)			60	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time (BCLK standard)		-4		ns
$t_{d(AD-ALE)}$	ALE signal output delay time (Address standard)		(Note 1)		ns
$t_{h(ALE-AD)}$	ALE signal output hold time (Address standard)		40		ns
$t_{d(AD-RD)}$	Post-address RD signal output delay time	0		ns	
$t_{d(AD-WR)}$	Post-address WR signal output delay time	0		ns	
$t_{dZ(RD-AD)}$	Address output floating start time		8	ns	

Note 1: Calculated according to the BCLK frequency as follows:

$$t_{h(RD-AD)} = \frac{10^9}{f(BCLK) \times 2} \quad [ns]$$

$$t_{h(WR-AD)} = \frac{10^9}{f(BCLK) \times 2} \quad [ns]$$

$$t_{h(RD-CS)} = \frac{10^9}{f(BCLK) \times 2} \quad [ns]$$

$$t_{h(WR-CS)} = \frac{10^9}{f(BCLK) \times 2} \quad [ns]$$

$$t_{d(DB-WR)} = \frac{10^9 \times 3}{f(BCLK) \times 2} - 80 \quad [ns]$$

$$t_{h(WR-DB)} = \frac{10^9}{f(BCLK) \times 2} \quad [ns]$$

$$t_{d(AD-ALE)} = \frac{10^9}{f(BCLK) \times 2} - 45 \quad [ns]$$

Note 2: Specify a product of  $-40^{\circ}C$  to  $85^{\circ}C$  to use it.

Timing

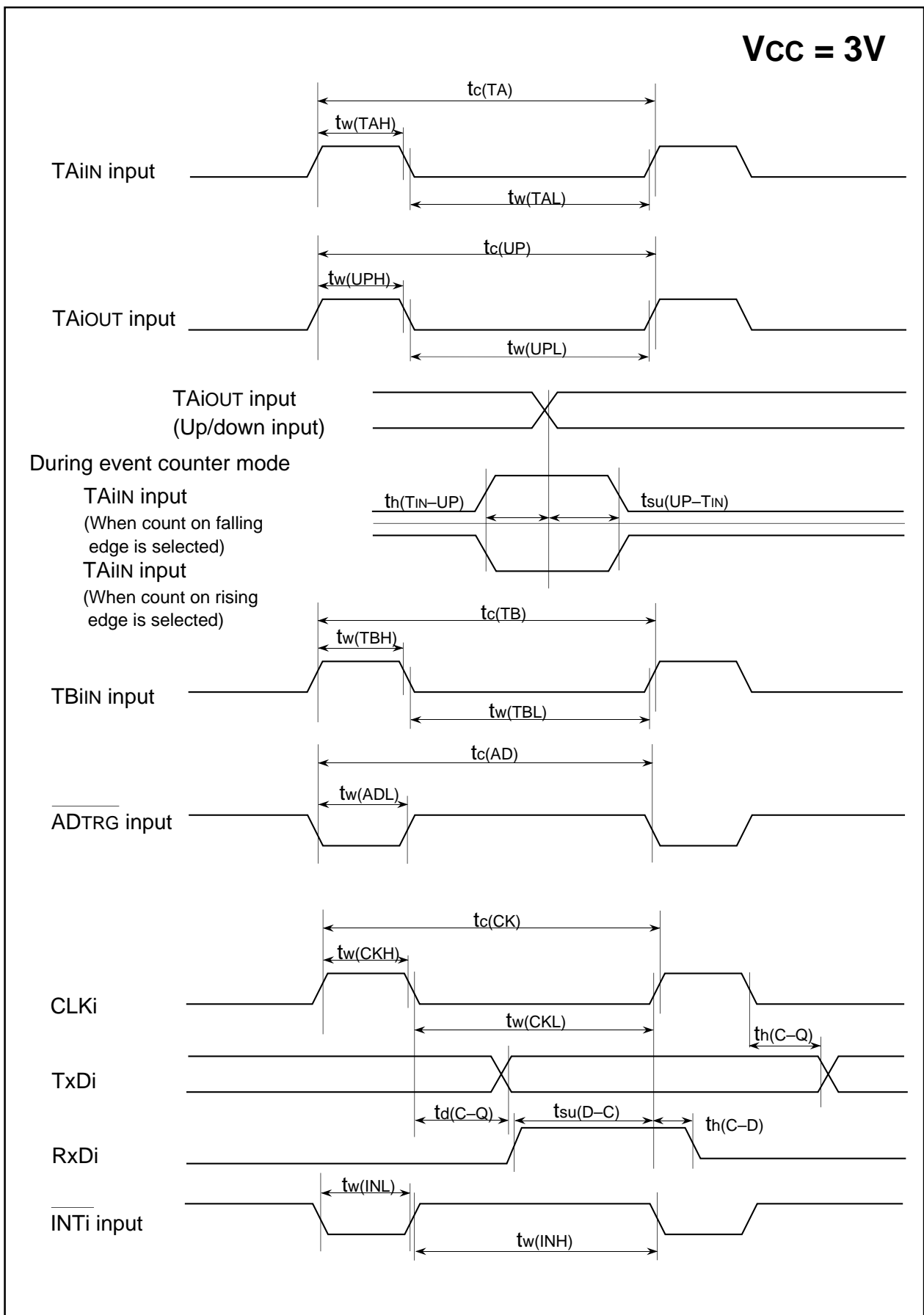


Figure 1.26.2. V<sub>CC</sub>=3V timing diagram (1)

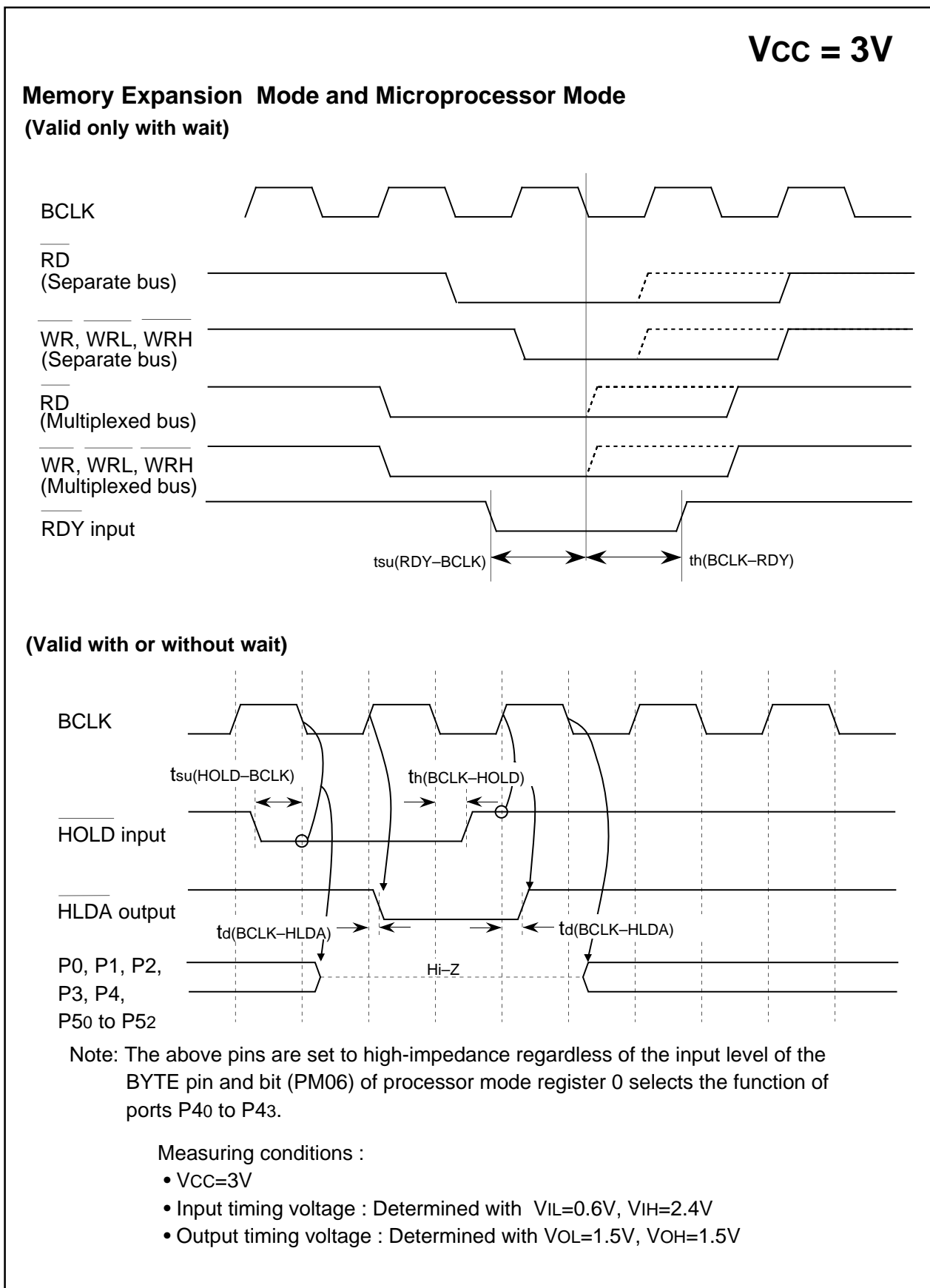


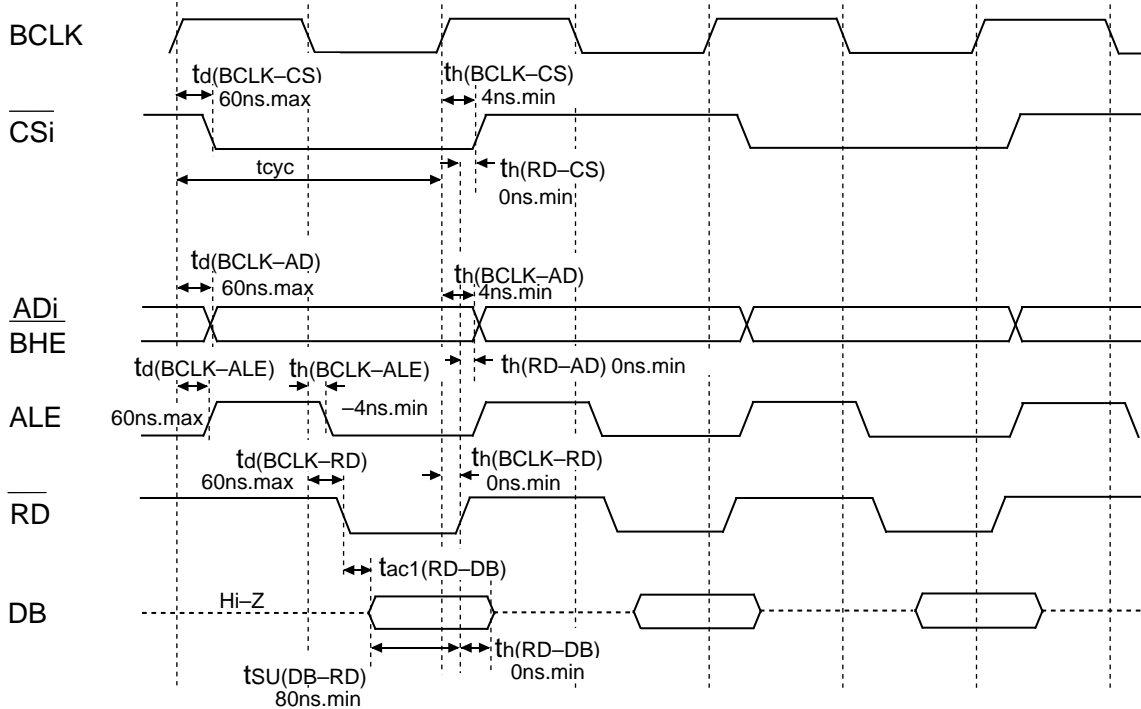
Figure 1.26.3. VCC=3V timing diagram (2)

**VCC = 3V**

**Memory Expansion Mode and Microprocessor Mode**

(With no wait)

**Read timing**



**Write timing**

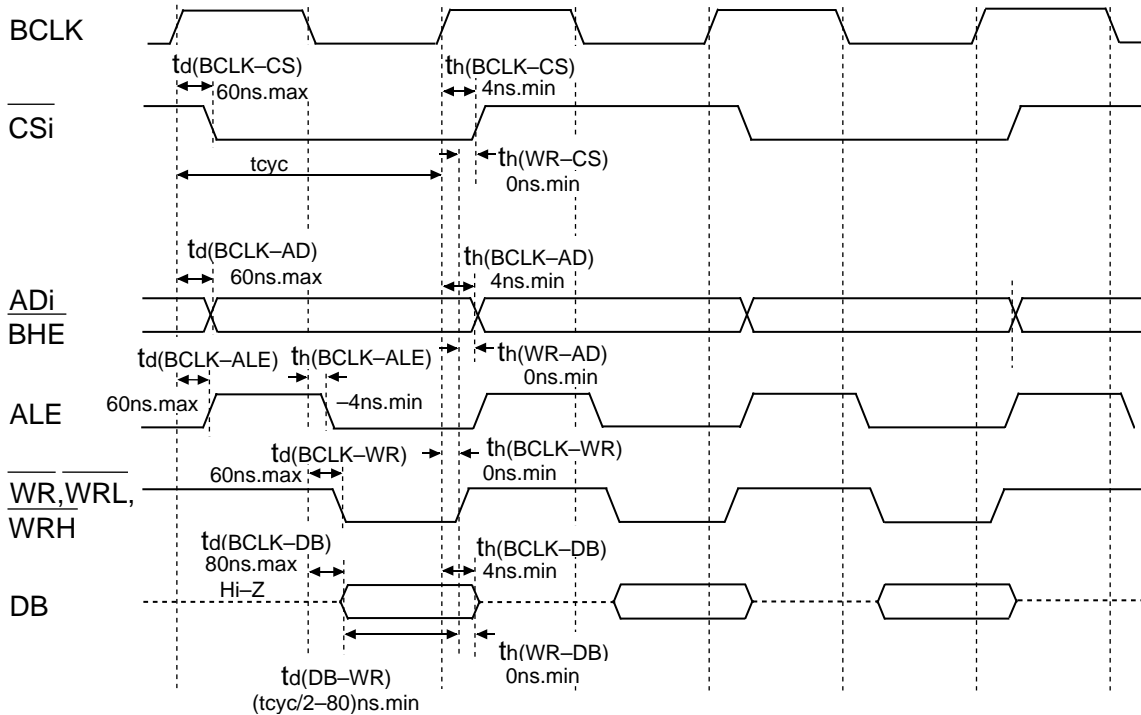


Figure 1.26.4. VCC=3V timing diagram (3)

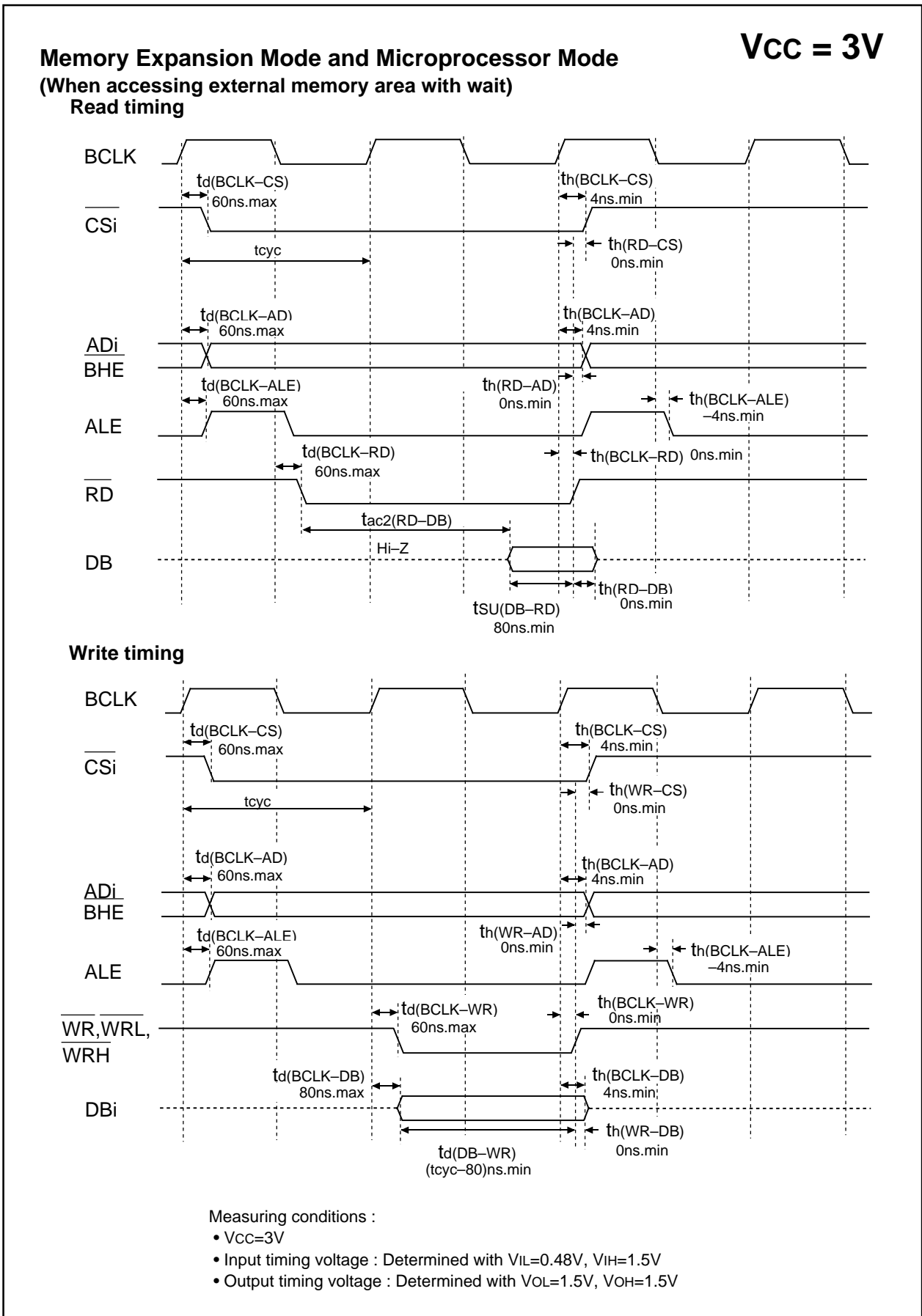


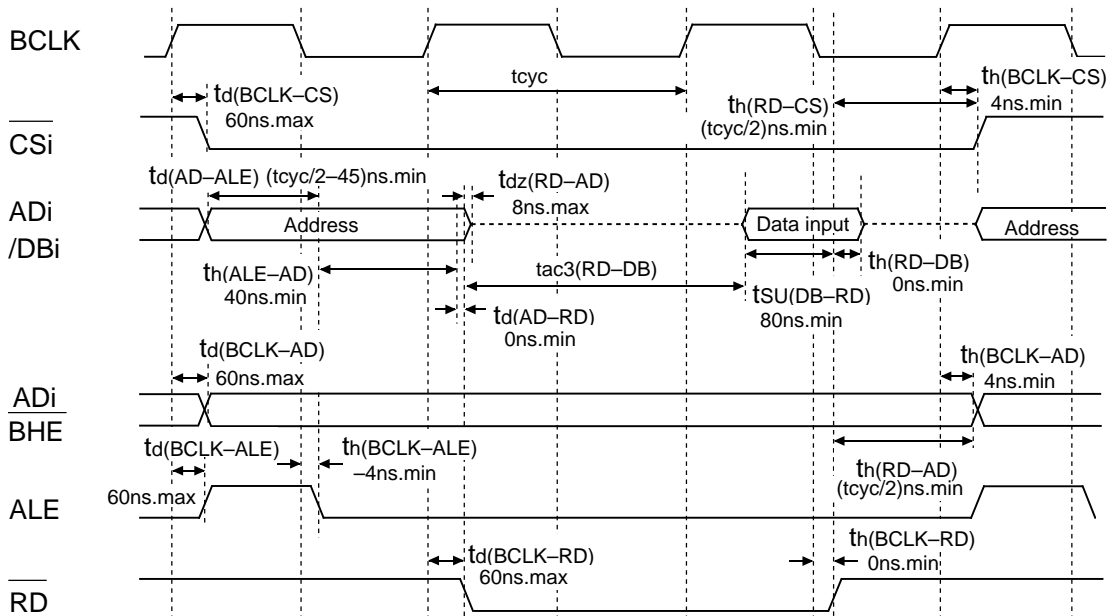
Figure 1.26.5. Vcc=3V timing diagram (4)

**VCC = 3V**

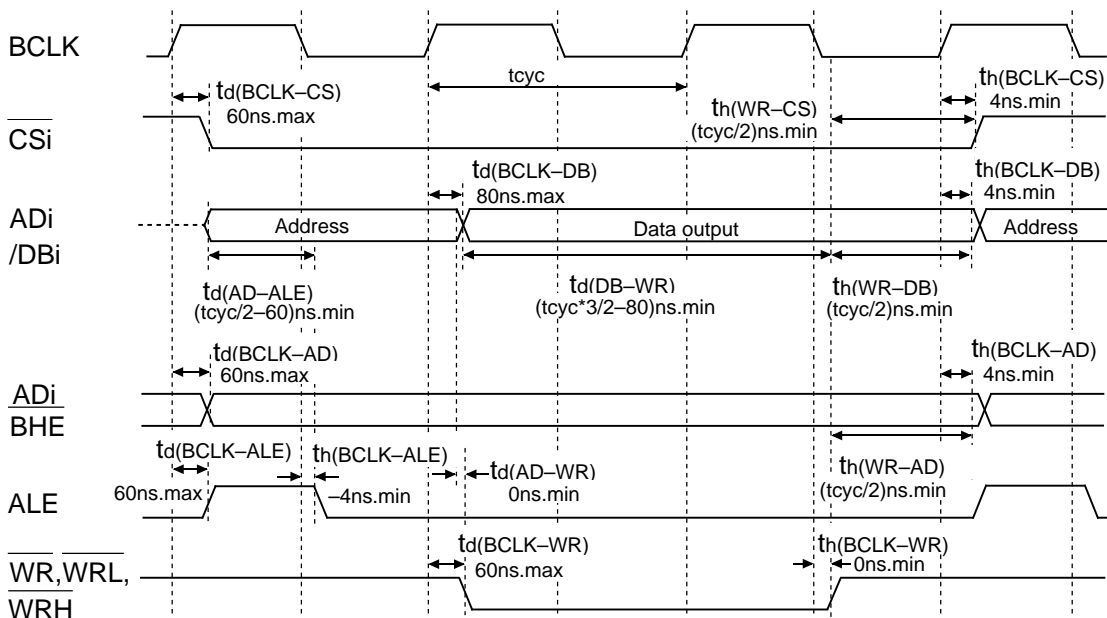
**Memory Expansion Mode and Microprocessor Mode**

(When accessing external memory area with wait, and select multiplexed bus)

**Read timing**



**Write timing**



Measuring conditions :

- VCC=3V
- Input timing voltage : Determined with  $V_{IL}=0.48V, V_{IH}=1.5V$
- Output timing voltage : Determined with  $V_{OL}=1.5V, V_{OH}=1.5V$

Figure 1.26.6. VCC=3V timing diagram (5)

## Usage Precaution

### Timer A (timer mode)

- (1) Reading the timer Ai register while a count is in progress allows reading, with arbitrary timing, the value of the counter. Reading the timer Ai register with the reload timing gets "FFFF<sub>16</sub>". Reading the timer Ai register after setting a value in the timer Ai register with a count halted but before the counter starts counting gets a proper value.

### Timer A (event counter mode)

- (1) Reading the timer Ai register while a count is in progress allows reading, with arbitrary timing, the value of the counter. Reading the timer Ai register with the reload timing gets "FFFF<sub>16</sub>" by underflow or "0000<sub>16</sub>" by overflow. Reading the timer Ai register after setting a value in the timer Ai register with a count halted but before the counter starts counting gets a proper value.
- (2) When stop counting in free run type, set timer again.

### Timer A (one-shot timer mode)

- (1) Setting the count start flag to "0" while a count is in progress causes as follows:
  - The counter stops counting and a content of reload register is reloaded.
  - The TAIOUT pin outputs "L" level.
  - The interrupt request generated and the timer Ai interrupt request bit goes to "1".
- (2) The timer Ai interrupt request bit goes to "1" if the timer's operation mode is set using any of the following procedures:
  - Selecting one-shot timer mode after reset.
  - Changing operation mode from timer mode to one-shot timer mode.
  - Changing operation mode from event counter mode to one-shot timer mode.Therefore, to use timer Ai interrupt (interrupt request bit), set timer Ai interrupt request bit to "0" after the above listed changes have been made.

### Timer A (pulse width modulation mode)

- (1) The timer Ai interrupt request bit becomes "1" if setting operation mode of the timer in compliance with any of the following procedures:
  - Selecting PWM mode after reset.
  - Changing operation mode from timer mode to PWM mode.
  - Changing operation mode from event counter mode to PWM mode.Therefore, to use timer Ai interrupt (interrupt request bit), set timer Ai interrupt request bit to "0" after the above listed changes have been made.
- (2) Setting the count start flag to "0" while PWM pulses are being output causes the counter to stop counting. If the TAIOUT pin is outputting an "H" level in this instance, the output level goes to "L", and the timer Ai interrupt request bit goes to "1". If the TAIOUT pin is outputting an "L" level in this instance, the level does not change, and the timer Ai interrupt request bit does not becomes "1".

### Timer B (timer mode, event counter mode)

- (1) Reading the timer Bi register while a count is in progress allows reading, with arbitrary timing, the value of the counter. Reading the timer Bi register with the reload timing gets "FFFF<sub>16</sub>". Reading the timer Bi register after setting a value in the timer Bi register with a count halted but before the counter starts counting gets a proper value.

### Timer B (pulse period/pulse width measurement mode)

- (1) If changing the measurement mode select bit is set after a count is started, the timer Bi interrupt request bit goes to "1".
- (2) When the first effective edge is input after a count is started, an indeterminate value is transferred to the reload register. At this time, timer Bi interrupt request is not generated.

### A-D Converter

- (1) Write to each bit (except bit 6) of A-D control register 0, to each bit of A-D control register 1, and to bit 0 of A-D control register 2 when A-D conversion is stopped (before a trigger occurs).  
In particular, when the Vref connection bit is changed from "0" to "1", start A-D conversion after an elapse of 1  $\mu$ s or longer.
- (2) When changing A-D operation mode, select analog input pin again.
- (3) Using one-shot mode or single sweep mode  
Read the correspondence A-D register after confirming A-D conversion is finished. (It is known by A-D conversion interrupt request bit.)
- (4) Using repeat mode, repeat sweep mode 0 or repeat sweep mode 1  
Use the undivided main clock as the internal CPU clock.

### Stop Mode and Wait Mode

- (1) When returning from stop mode by hardware reset,  $\overline{\text{RESET}}$  pin must be set to "L" level until main clock oscillation is stabilized.
- (2) When switching to either wait mode or stop mode, instructions occupying four bytes either from the WAIT instruction or from the instruction that sets the every-clock stop bit to "1" within the instruction queue are prefetched and then the program stops. So put at least four NOPs in succession either to the WAIT instruction or to the instruction that sets the every-clock stop bit to "1".

### Interrupts

- (1) Reading address 00000<sub>16</sub>
  - When maskable interrupt is occurred, CPU read the interrupt information (the interrupt number and interrupt request level) in the interrupt sequence.  
The interrupt request bit of the certain interrupt written in address 00000<sub>16</sub> will then be set to "0".  
Reading address 00000<sub>16</sub> by software sets enabled highest priority interrupt source request bit to "0".  
Though the interrupt is generated, the interrupt routine may not be executed.  
Do not read address 00000<sub>16</sub> by software.
- (2) Setting the stack pointer
  - The value of the stack pointer immediately after reset is initialized to 0000<sub>16</sub>. Accepting an interrupt before setting a value in the stack pointer may become a factor of runaway. Be sure to set a value in the stack pointer before accepting an interrupt.  
When using the  $\overline{\text{NMI}}$  interrupt, initialize the stack point at the beginning of a program. Concerning the first instruction immediately after reset, generating any interrupts including the  $\overline{\text{NMI}}$  interrupt is prohibited.
- (3) The  $\overline{\text{NMI}}$  interrupt
  - The  $\overline{\text{NMI}}$  interrupt can not be disabled. Be sure to connect  $\overline{\text{NMI}}$  pin to Vcc via a pull-up resistor if unused.
  - Do not get either into stop mode with the  $\overline{\text{NMI}}$  pin set to "L".



## Usage precaution

### (4) External interrupt

- When the polarity of the  $\overline{\text{INT0}}$  to  $\overline{\text{INT5}}$  pins is changed, the interrupt request bit is sometimes set to "1". After changing the polarity, set the interrupt request bit to "0".

### (5) Rewrite the interrupt control register

- To rewrite the interrupt control register, do so at a point that does not generate the interrupt request for that register. If there is possibility of the interrupt request occur, rewrite the interrupt control register after the interrupt is disabled. The program examples are described as follow:

#### Example 1:

```
INT_SWITCH1:
  FCLR  I           ; Disable interrupts.
  AND.B #00h, 0055h ; Clear TA0IC int. priority level and int. request bit.
  NOP                               ; Four NOP instructions are required when using HOLD function.
  NOP
  FSET  I           ; Enable interrupts.
```

#### Example 2:

```
INT_SWITCH2:
  FCLR  I           ; Disable interrupts.
  AND.B #00h, 0055h ; Clear TA0IC int. priority level and int. request bit.
  MOV.W MEM, R0    ; Dummy read.
  FSET  I           ; Enable interrupts.
```

#### Example 3:

```
INT_SWITCH3:
  PUSHC FLG        ; Push Flag register onto stack
  FCLR  I           ; Disable interrupts.
  AND.B #00h, 0055h ; Clear TA0IC int. priority level and int. request bit.
  POPC  FLG        ; Enable interrupts.
```

The reason why two NOP instructions (four when using the HOLD function) or dummy read are inserted before FSET I in Examples 1 and 2 is to prevent the interrupt enable flag I from being set before the interrupt control register is rewritten due to effects of the instruction queue.

- When a instruction to rewrite the interrupt control register is executed but the interrupt is disabled, the interrupt request bit is not set sometimes even if the interrupt request for that register has been generated. This will depend on the instruction. If this creates problems, use the below instructions to change the register.

Instructions : AND, OR, BCLR, BSET

## Noise

- (1) Insert bypass capacitor between Vcc and Vss pin for noise and latch up countermeasure.
  - Insert bypass capacitor (about 0.1  $\mu\text{F}$ ) and connect short and wide line between Vcc and Vss lines.

### **Notes on the microprocessor mode and transition after shifting from the microprocessor mode to the memory expansion mode**

- Microprocessor mode

In microprocessor mode, the SFR, internal RAM, and external memory space can be accessed.

For that reason, the internal ROM area cannot be accessed.

- Memory expansion mode

In memory expansion mode, external memory can be accessed in addition to the internal memory space (SFR, internal RAM, and internal ROM).

However, after the reset has been released and the operation of shifting from the microprocessor mode has started ("H" applied to the CNVss pin), the internal ROM area cannot be accessed even if the CPU shifts to the memory expansion mode.

GZZ-SH13-95B<02A0>

**MITSUBISHI ELECTRIC-CHIP 16-BIT  
MICROCOMPUTER M30620MCM-XXXFP/GP  
MASK ROM CONFIRMATION FORM**

Mask ROM number	
-----------------	--

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please complete all items marked \* .

* Customer	Company name	TEL (      )	Issuance signature	Submitted by	Supervisor
	Date issued	Date :			

\*1. Check sheet

Mitsubishi processes the mask files generated by the mask file generation utilities out of those held on the floppy disks you give in to us, and forms them into masks. Hence, we assume liability provided that there is any discrepancy between the contents of these mask files and the ROM data to be burned into products we produce. Check thoroughly the contents of the mask files you give in.

Prepare 3.5 inches 2HD (IBM format) floppy disks. And store only one mask file in a floppy disk.

Microcomputer type No. :       M30620MCM-XXXFP       M30620MCM-XXXGP

File code :      

--	--	--	--	--	--	--	--

 (hex)

Mask file name :      

--	--	--	--	--	--	--	--

 .MSK (alpha-numeric 8-digit)

\*2. Mark specification

The mark specification differs according to the type of package. After entering the mark specification on the separate mark specification sheet (for each package), attach that sheet to this masking check sheet for submission to Mitsubishi.

For the M30620MCM-XXXFP, submit the 100P6S mark specification sheet. For the M30620MCM-XXXGP, submit the 100P6Q mark specification sheet.

\*3. Usage Conditions

For our reference when of testing our products, please reply to the following questions about the usage of the products you ordered.

(1) Which kind of XIN-XOUT oscillation circuit is used?

- Ceramic resonator       Quartz-crystal oscillator  
 External clock input       Other (                      )

What frequency do not use?

f(XIN) =  MHz

GZZ-SH13-95B<02A0>

Mask ROM number	
-----------------	--

**MITSUBISHI ELECTRIC-CHIP 16-BIT  
MICROCOMPUTER M30620MCM-XXXFP/GP  
MASK ROM CONFIRMATION FORM**

(2) Which kind of XCIN-XCOUT oscillation circuit is used?

- Ceramic resonator                       Quartz-crystal oscillator  
 External clock input                       Other (                      )

What frequency do not use?

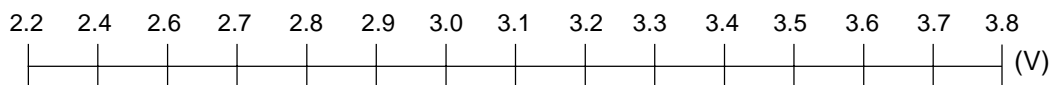
f(XCIN) =  kHz

(3) Which operation mode do you use?

- Single-chip mode                       Memory expansion mode  
 Microprocessor mode

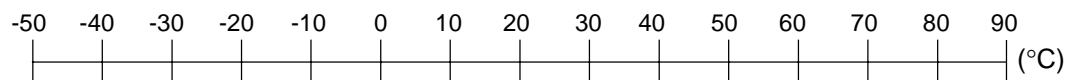
(4) Which operating supply voltage do you use?

(Circle the operating voltage range of use)



(5) Which operating ambient temperature do you use?

(Circle the operating temperature range of use)



(6) Do you use I<sup>2</sup>C (Inter IC) bus function?

- Not use                                       Use

(7) Do you use IE (Inter Equipment) bus function?

- Not use                                       Use

Thank you cooperation.

\*4. Special item (Indicate none if there is not specified item)

GZZ-SH13-48B<98A1>

**MITSUBISHI ELECTRIC-CHIP 16-BIT  
MICROCOMPUTER M30624MGM-XXXFP/GP  
MASK ROM CONFIRMATION FORM**

Mask ROM number	
-----------------	--

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please complete all items marked \* .

* Customer	Company name	TEL (      )	Issuance signature	Submitted by	Supervisor
	Date issued	Date :			

\*1. Check sheet

Mitsubishi processes the mask files generated by the mask file generation utilities out of those held on the floppy disks you give in to us, and forms them into masks. Hence, we assume liability provided that there is any discrepancy between the contents of these mask files and the ROM data to be burned into products we produce. Check thoroughly the contents of the mask files you give in.

Prepare 3.5 inches 2HD (IBM format) floppy disks. And store only one mask file in a floppy disk.

Microcomputer type No. :       M30624MGM-XXXFP       M30624MGM-XXXGP

File code :      

--	--	--	--	--	--	--	--

 (hex)

Mask file name :      

--	--	--	--	--	--	--	--

 .MSK (alpha-numeric 8-digit)

\*2. Mark specification

The mark specification differs according to the type of package. After entering the mark specification on the separate mark specification sheet (for each package), attach that sheet to this masking check sheet for submission to Mitsubishi.

For the M30624MGM-XXXFP, submit the 100P6S mark specification sheet. For the M30624MGM-XXXGP, submit the 100P6Q mark specification sheet.

\*3. Usage Conditions

For our reference when of testing our products, please reply to the following questions about the usage of the products you ordered.

(1) Which kind of X<sub>IN</sub>-X<sub>OUT</sub> oscillation circuit is used?

- Ceramic resonator       Quartz-crystal oscillator  
 External clock input       Other (                      )

What frequency do not use?

f(X<sub>IN</sub>) = 

--

 MHz

GZZ-SH13-48B<98A1>

Mask ROM number	
-----------------	--

**MITSUBISHI ELECTRIC-CHIP 16-BIT  
MICROCOMPUTER M30624MGM-XXXFP/GP  
MASK ROM CONFIRMATION FORM**

(2) Which kind of XCIN-XCOUT oscillation circuit is used?

- Ceramic resonator                       Quartz-crystal oscillator  
 External clock input                       Other (                      )

What frequency do not use?

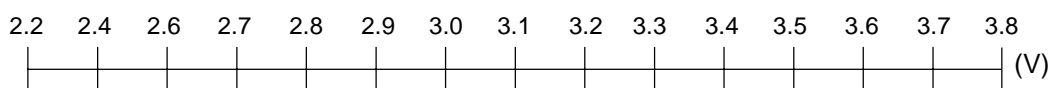
f(XCIN) =  kHz

(3) Which operation mode do you use?

- Single-chip mode                       Memory expansion mode  
 Microprocessor mode

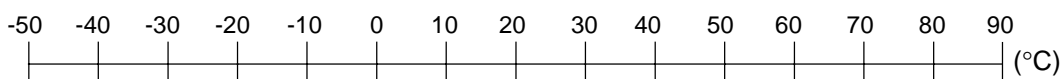
(4) Which operating supply voltage do you use?

(Circle the operating voltage range of use)



(5) Which operating ambient temperature do you use?

(Circle the operating temperature range of use)



(6) Do you use I<sup>2</sup>C (Inter IC) bus function?

- Not use                                       Use

(7) Do you use IE (Inter Equipment) bus function?

- Not use                                       Use

Thank you cooperation.

\*4. Special item (Indicate none if there is not specified item)

Differences between M16C/62M (Low voltage version) and M30624FGLFP/GP

Item	M16C/62M (Low voltage version)	M30624FGLFP/GP
Memory area	1 Mbyte fixed	Memory expansion 1.2 Mbytes mode 4 Mbytes mode
Serial I/O	No CTS/RTS separate function	CTS/RTS separate function
IIC bus mode	Analog or digital delay is selected as SDA delay	Only analog delay is selected as SDA delay
Memory version	Mask ROM version Flash memory version	Flash memory version only
Standard serial I/O mode (Flash memory version)	Clock synchronized Clock asynchronous	Clock synchronized only

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MITSUBISHI SEMICONDUCTORS  
M16C/62M Group (Low voltage version)  
Specifications REV.B

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