Ordering number : EN5056A

CMOS LSI

LC75395E

Single-Chip Electronic Volume Control System

Overview

The LC75395E is an electronic volume control that provides volume, balance, five-band equalization and input switching functions. These functions are controlled from serial input data.

Functions

- Volume control: The volume control provides 25 attenuation positions: from 0 dB to –17.5 dB in 1.25 dB steps, from –17.5 dB to –25 dB in 2.5 dB steps, from –25 dB to –36.25 dB in 3.75 dB steps and with settings for –41.25 dB, –50 dB, –60 dB and –∞.
  A balance function can be implemented by controlling the left and right channels independently.
- Equalizer: The equalizer function supports ±10 dB control in 2 dB steps in each of the five bands. Of the five bands, four provide peaking characteristics, and one provides shelving characteristics.
- Selector: The selector function selects one of four inputs for each of the left and right channels. An arbitrary amplification level can be set for each input signal using external components.
- Serial data input: All controls can be set from serial input data (CCB format)

Features

- On-chip buffer amplifiers to minimize the number of external components
- Silicon-gate CMOS process for minimal switching noise
- On-chip circuit to generate the $V_{DD}/2$ reference voltage

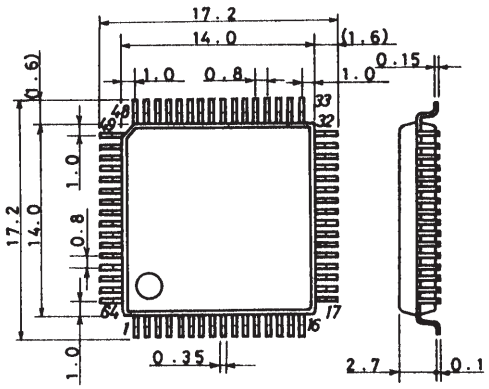
- **CCB is a trademark of SANYO ELECTRIC CO., LTD.**
- **CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.**

Package Dimensions

unit: mm

3159-QFP64E

[LC75395E]



SANYO: QIP64E

Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD}	12	V
Maximum input voltage	V_{IN} max	CL, DI, CE, L1 to L4, R1 to R4, LTIN, RTIN, LVRIN, RVRIN	V_{SS} – 0.3 to V_{DD} + 0.3	V
Allowable power dissipation	Pd max	Ta ≤ 85°C	310	mW
Operating temperature	Topr		–30 to +85	°C
Storage temperature	Tstg		–40 to +125	°C

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Allowable Operating Ranges at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}	V_{DD}	6.0		11.0	V
Input high level voltage	V_{IH}	CL, DI, CE	4.0		V_{DD}	V
Input low level voltage	V_{IL}	CL, DI, CE	V_{SS}		1.0	V
Input voltage amplitude	V_{IN}	CL, DI, CE, L1 to L4, R1 to R4, LTIN, RTIN, LVRIN, RVRIN	V_{SS}		V_{DD}	Vp-p
Input pulse width	$t_{øW}$	CL	1.0			µs
Setup time	t_{SETUP}	CL, DI, CE	1.0			µs
Hold time	t_{HOLD}	CL, DI, CE	1.0			µs
Operating frequency	fopg	CL			500	kHz

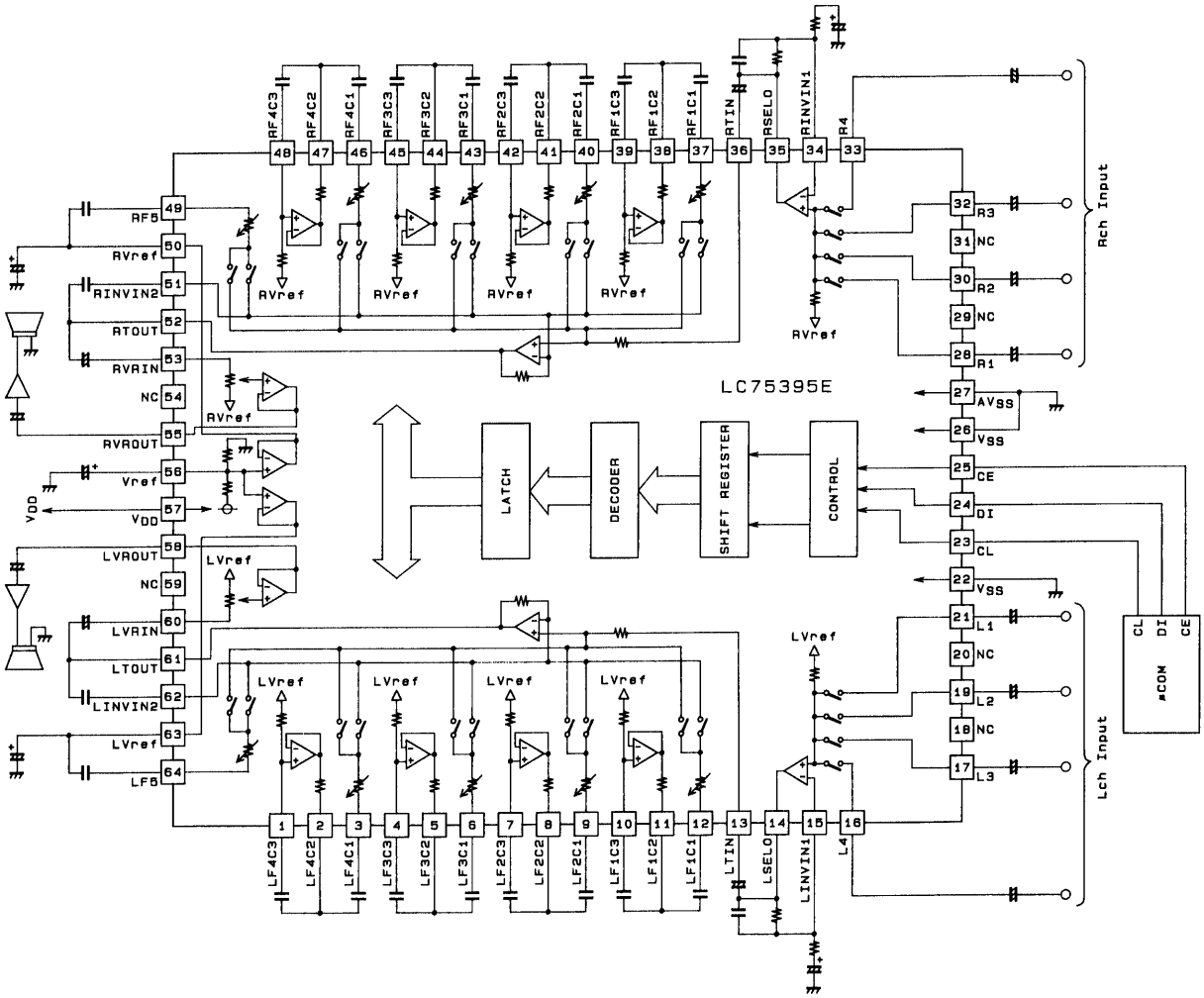
Electrical Characteristics at Ta = 25°C, V_{DD} = 10 V, V_{SS} = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
[Input Block]						
Input resistance	Rin	L1 to L4, R1 to R4		1		MΩ
Clipping level	Vcl	LSELO, RSELO: THD = 1.0%		2.65		Vrms
Output load resistance	R_L	LSELO, RSELO	3			kΩ
[Volume Control Block]						
Input resistance	Rin	LVRIN, RVRIN	21	35	49	kΩ
[Equalizer Control Block]						
Control range	Geq	Max, boost/cut	±8	±10	±12	dB
Step resolution	Estep		1	2	3	dB
Internal feedback resistance	Rfeed		17	28	39	kΩ
[Overall Characteristics]						
Total harmonic distortion	THD (1)	V_{IN} = 1 Vrms, f = 1 kHz, with all controls flat overall		0.0033		%
	THD (2)	V_{IN} = 1 Vrms, f = 20 kHz, with all controls flat overall		0.012		%
Crosstalk	CT	V_{IN} = 1 Vrms, f = 1 kHz, with all controls flat overall Rg = 1 kΩ		86		dB
Output at maximum attenuation	V_O min	V_{IN} = 1 Vrms, f = 1 kHz, with the main volume control at –∞		–84		dB
Output noise voltage	V_N (1)	With all controls flat overall (IHF-A), Rg = 1 kΩ		3.9		µV
	V_N (2)	With all controls flat overall (DIN-AUDIO), Rg = 1 kΩ		5.4		µV
Current drain	I_{DD}	$V_{DD} - V_{SS}$ = 11 V		25	33	mA
Input high level current	I_{IH}	CL, DI, CE: V_{IN} = 11 V			10	µA
Input low level current	I_{IL}	CL, DI, CE: V_{IN} = 0 V	–10			µA

Input Amplifier Characteristics at Ta = 25°C, $V_{DD} - V_{SS}$ = 10 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Input offset voltage	V_{IO}		–10		+10	mV
Input offset current	I_{IO}	$V_{SS} \le V_{IN} \le V_{DD}$		±10		nA
Open-loop voltage gain	A_O			80		dB
0 dB bandwidth	f_T			2.5		MHz
Allowable load resistance	R_L		3			kΩ

Equivalent Circuit Block Diagram and Sample Application Circuit



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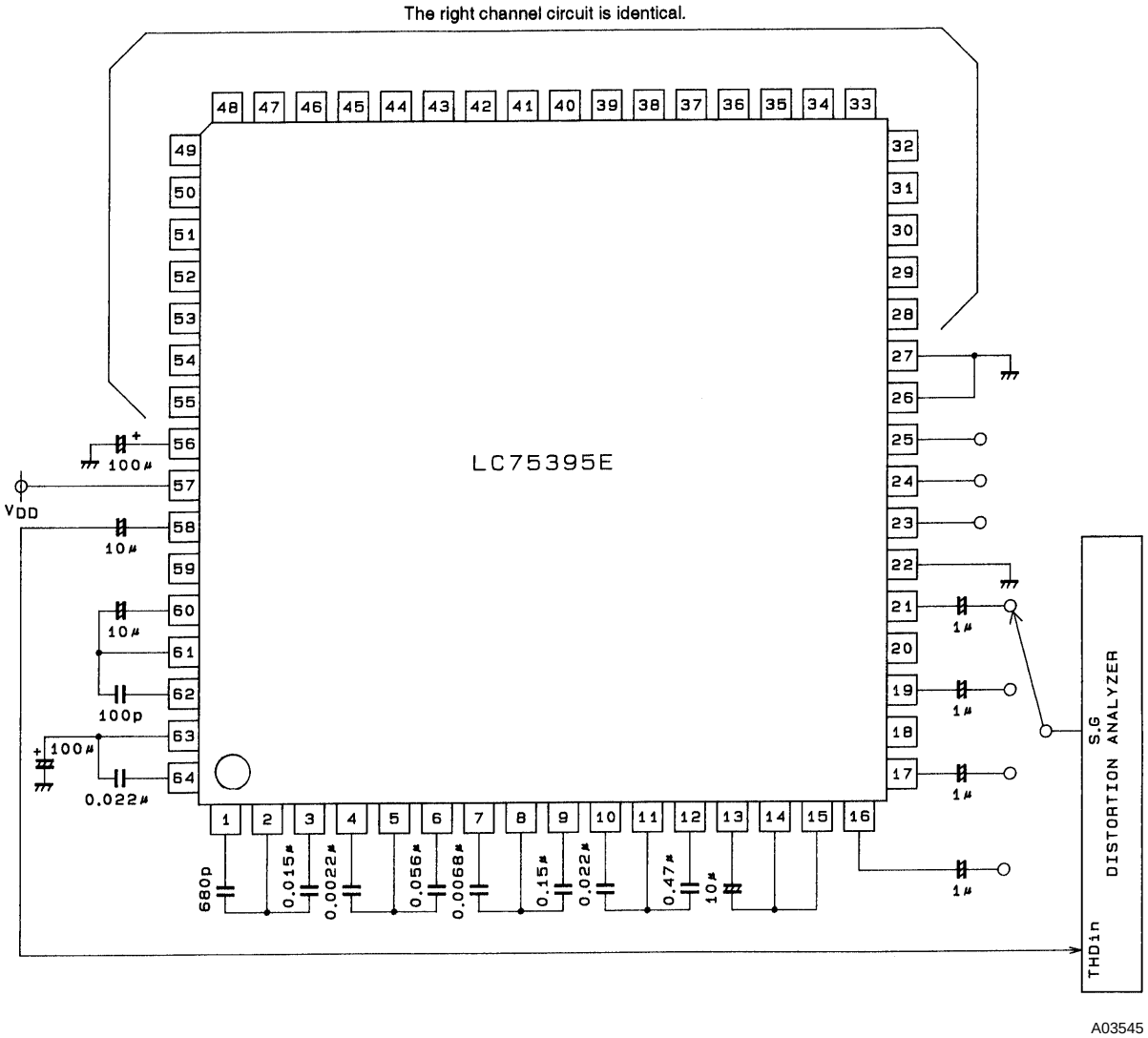
Note: If at all possible, use bipolar capacitors for all capacitors that do not have a polarity specified.

Test Circuits

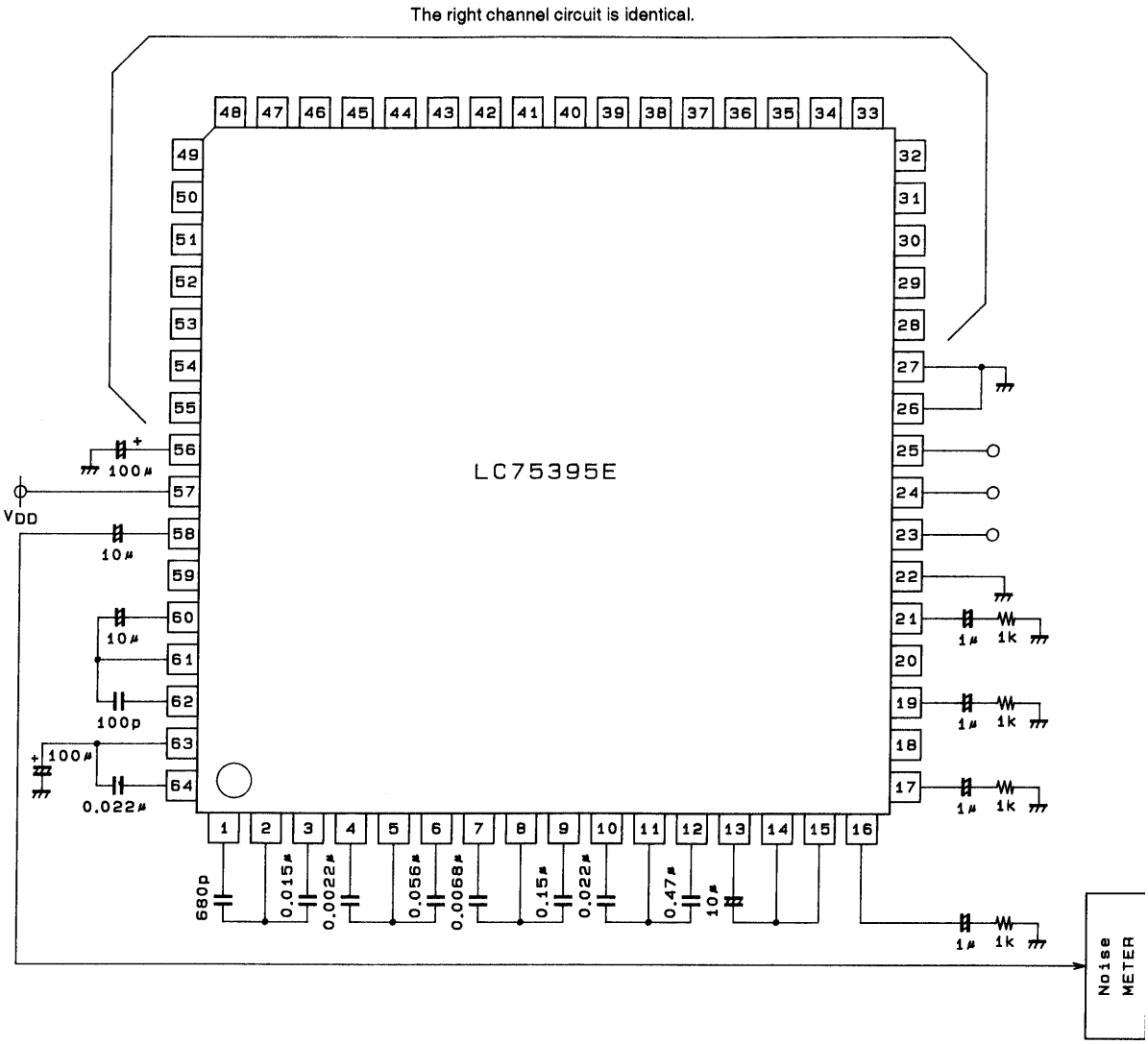
1. Total Harmonic Distortion



Unit (capacitance: F)

Test Circuits

2. Output Noise Voltage



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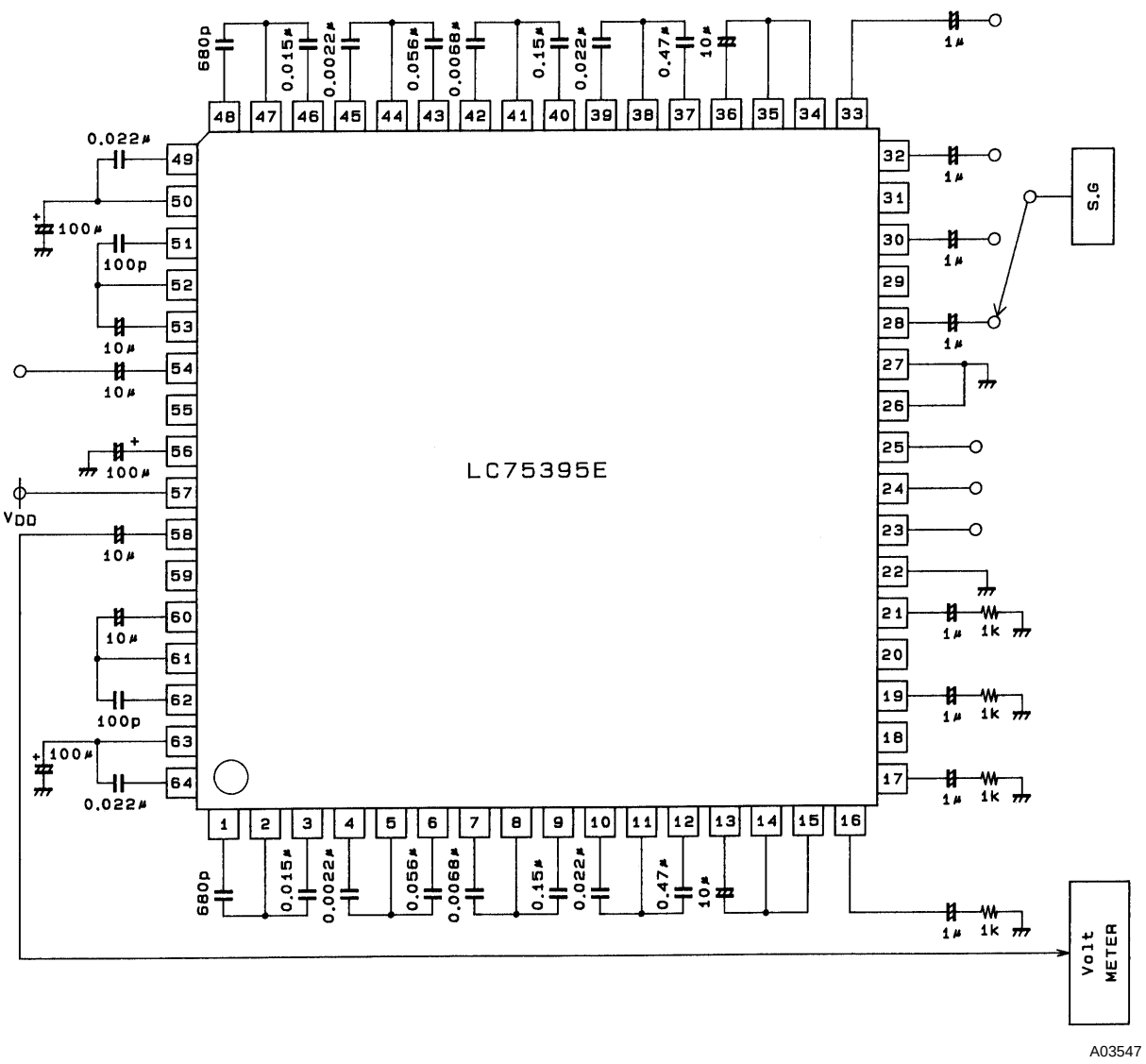
Unit (resistance: Ω, capacitance: F)

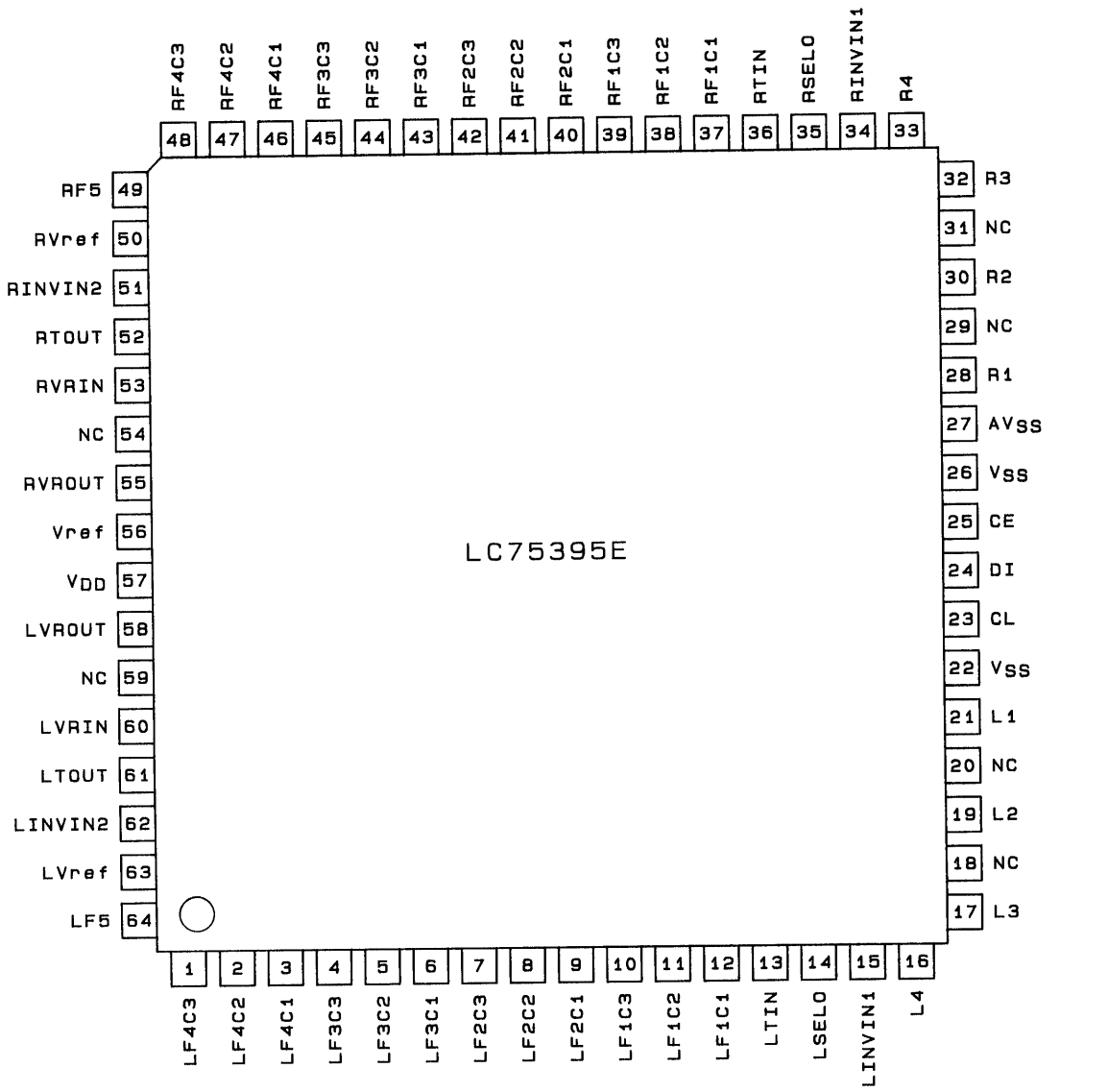
Test Circuits

3. Crosstalk



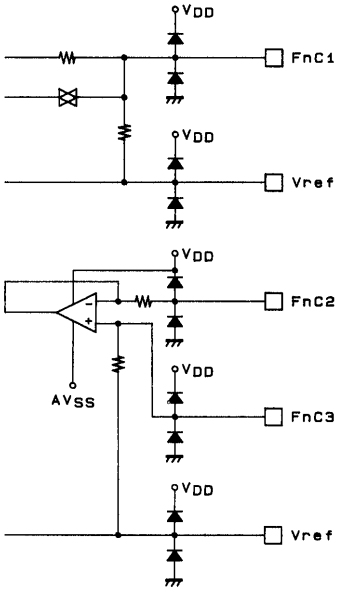
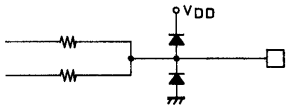
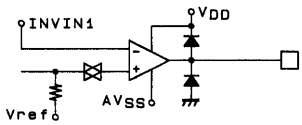
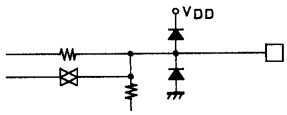
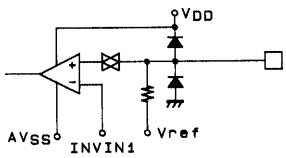
Unit (resistance: Ω, capacitance: F)

Pin Assignment



Top view

Pin Functions

Pin No.	Symbol	Function	Note
12 11 10	LF1C1 LF1C2 LF1C3	The left channel F1 band control block. These are external capacitor connections.	 A03549
37 38 39	RF1C1 RF1C2 RF1C3	The right channel F1 band control block. These are external capacitor connections.	
9 8 7	LF2C1 LF2C2 LF2C3	The left channel F2 band control block. These are external capacitor connections.	
40 41 42	RF2C1 RF2C2 RF2C3	The right channel F2 band control block. These are external capacitor connections.	
6 5 4	LF3C1 LF3C2 LF3C3	The left channel F3 band control block. These are external capacitor connections.	
43 44 45	RF3C1 RF3C2 RF3C3	The right channel F3 band control block. These are external capacitor connections.	
3 2 1	LF4C1 LF4C2 LF4C3	The left channel F4 band control block. These are external capacitor connections.	
46 47 48	RF4C1 RF4C2 RF4C3	The right channel F4 band control block. These are external capacitor connections.	
13 36	LTIN RTIN	Tone control inputs These must be driven by low-impedance circuits.	 A03550
14 35	LSELO RSELO	Input selector outputs	 A03551
64 49	LF5 RF5	F5 band control block. These are external capacitor connections.	 A03552
21 19 17 16 28 30 32 33	L1 L2 L3 L4 R1 R2 R3 R4	Signal inputs	 A03553
57	V_{DD}	Power supply	
22, 26	V_{SS}	Internal logic system ground	
27	AV_{SS}	Internal operational amplifier ground	

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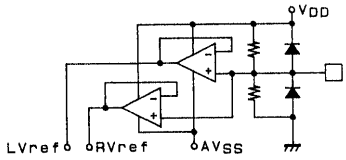
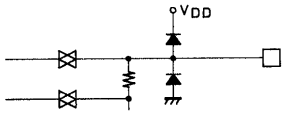
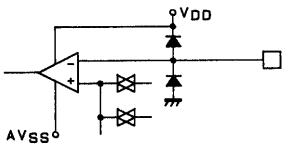
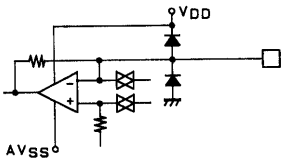
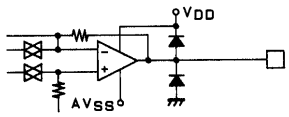
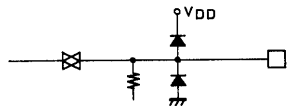
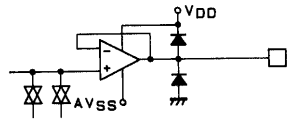
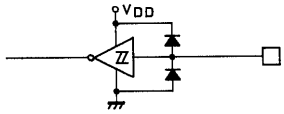
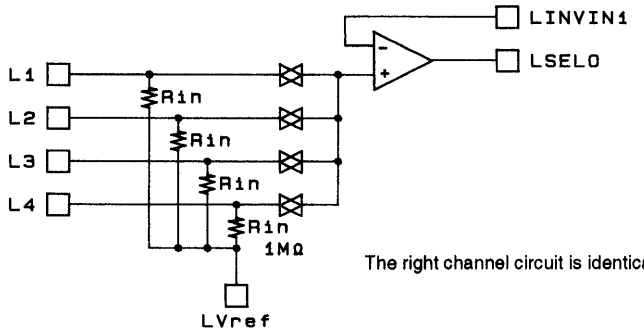
Pin No.	Symbol	Function	Note
56	Vref	V_{DD}/2 voltage generation block. A capacitor must be inserted between Vref and V_{SS} to suppress power supply ripple.	 A04449
63 50	LVref RVref	Common pins for the volume control, tone control and input switching blocks. Since capacitors inserted between LVref (or RVref) and V_{SS} become the residual resistance when the volume control is set at maximum attenuation, the values of these capacitors must be chosen carefully. A voltage higher than V_{DD} must never be applied.	 A03555
15 34	LINVIN1 RINVIN1	Inverting inputs for the operational amplifiers that set the input gain.	 A03556
62 51	LINVIN2 RINVIN2	Inverting inputs for the graphic equalizer operational amplifiers. Unnecessary frequency bands can be excluded and oscillation prevented by inserting arbitrary capacitors between the INVIN2 and TOUT pins.	 A03557
61 52	LTOUT RTOUT	Tone control outputs	 A03558
60 53	LVRIN RVRIN	Volume control inputs These must be driven by low-impedance circuits.	 A03559
58 55	LVROUT RVROUT	Volume control outputs	 A03560
25	CE	Chip enable Data is read into the internal latches and the analog switches operate when this pin goes from high to low. Data transfer is enabled when this pin is high.	 A03561
24 23	DI CL	Serial data and clock connections for chip control	
18 20 29 31 54 59	NC NC NC NC NC NC	Unused pins	

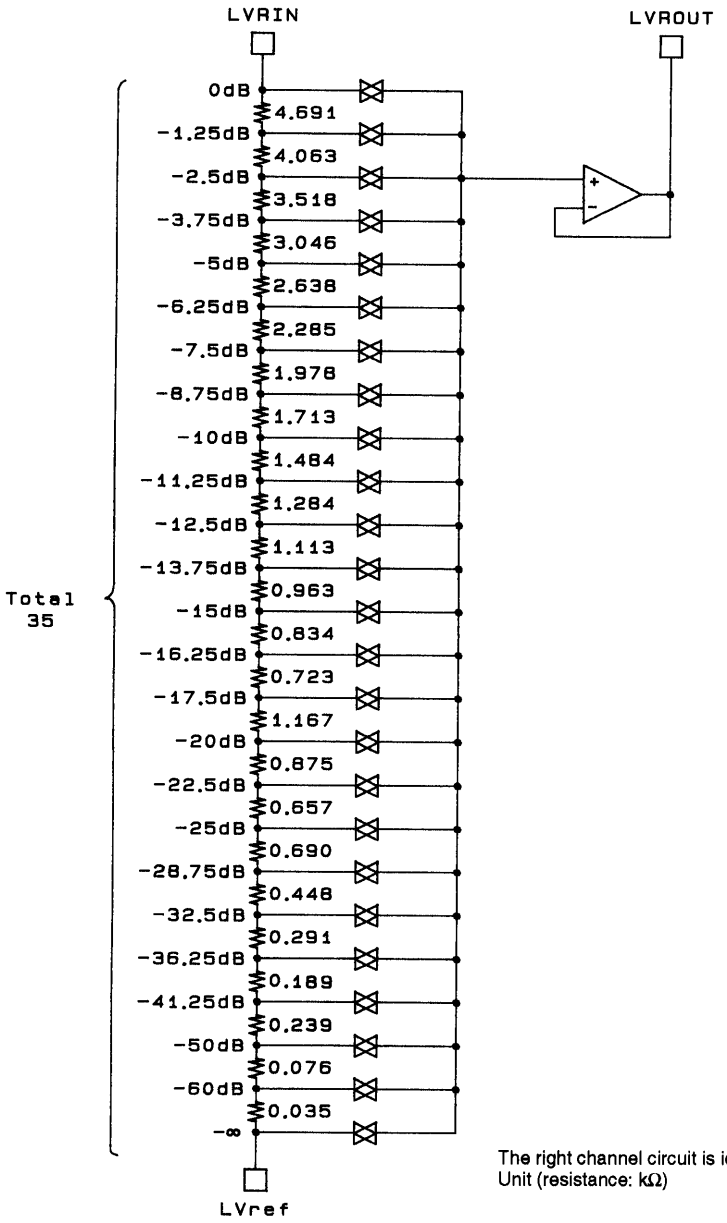
Input Block Internal Equivalent Circuit Diagram



The right channel circuit is identical.

A03562

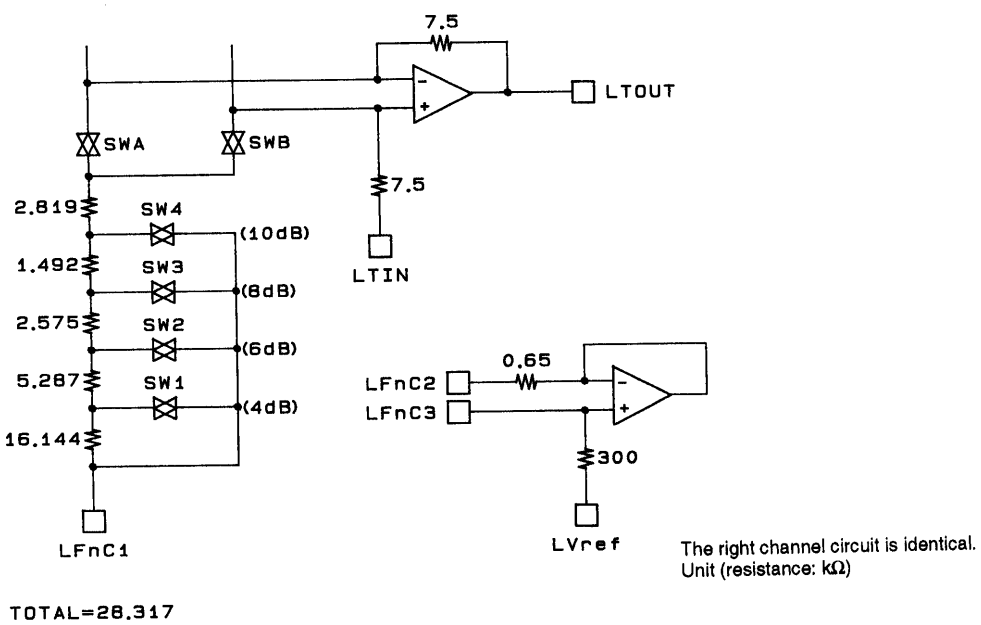
Volume Control Block Internal Equivalent Circuit Diagram



The right channel circuit is identical.
Unit (resistance: kΩ)

A03563

Equalizer Control Block Internal Equivalent Circuit (bands F1 to F4)

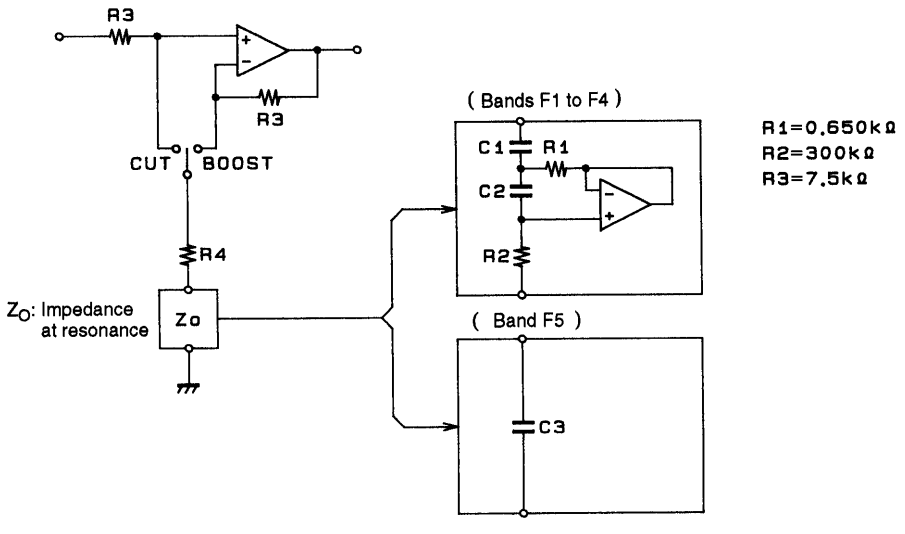


A03564

External Capacitor Calculations

The LC75395E supports four bands with peaking characteristics and one band with shelving characteristics.

1. Peaking Characteristics (bands F1 to F4)
   The external capacitor functions as the structural element of a simulated inductor. The equivalent circuit and the calculations required to achieve the desired center frequency are shown below.
   - Equivalent circuit for the simulated inductor



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- Sample Calculation
  Specifications 1) Center frequency F_O = 107 Hz
  2) Q at maximum boost: $Q_{+10\ dB}$ = 0.8

  ① Derive the sharpness (Q_O) of the simulated inductor itself.
  $Q_O = (R1 + R4)/R1 \times Q_{+10\ dB}$
  $\neq 4.270$
  ② Derive C1.
  $C1 = 1/2\pi F_O R1 Q_O \neq 0.536$ (μF)
  ③ Derive C2.
  $C2 = Q_O/2\pi F_O R2 \neq 0.021$ (μF)

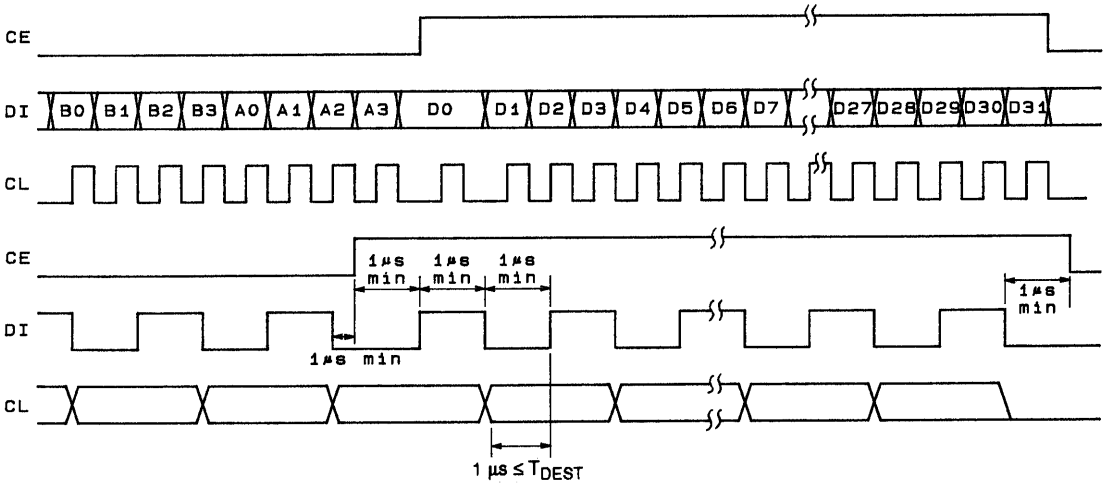
- Sample values for C1 and C2

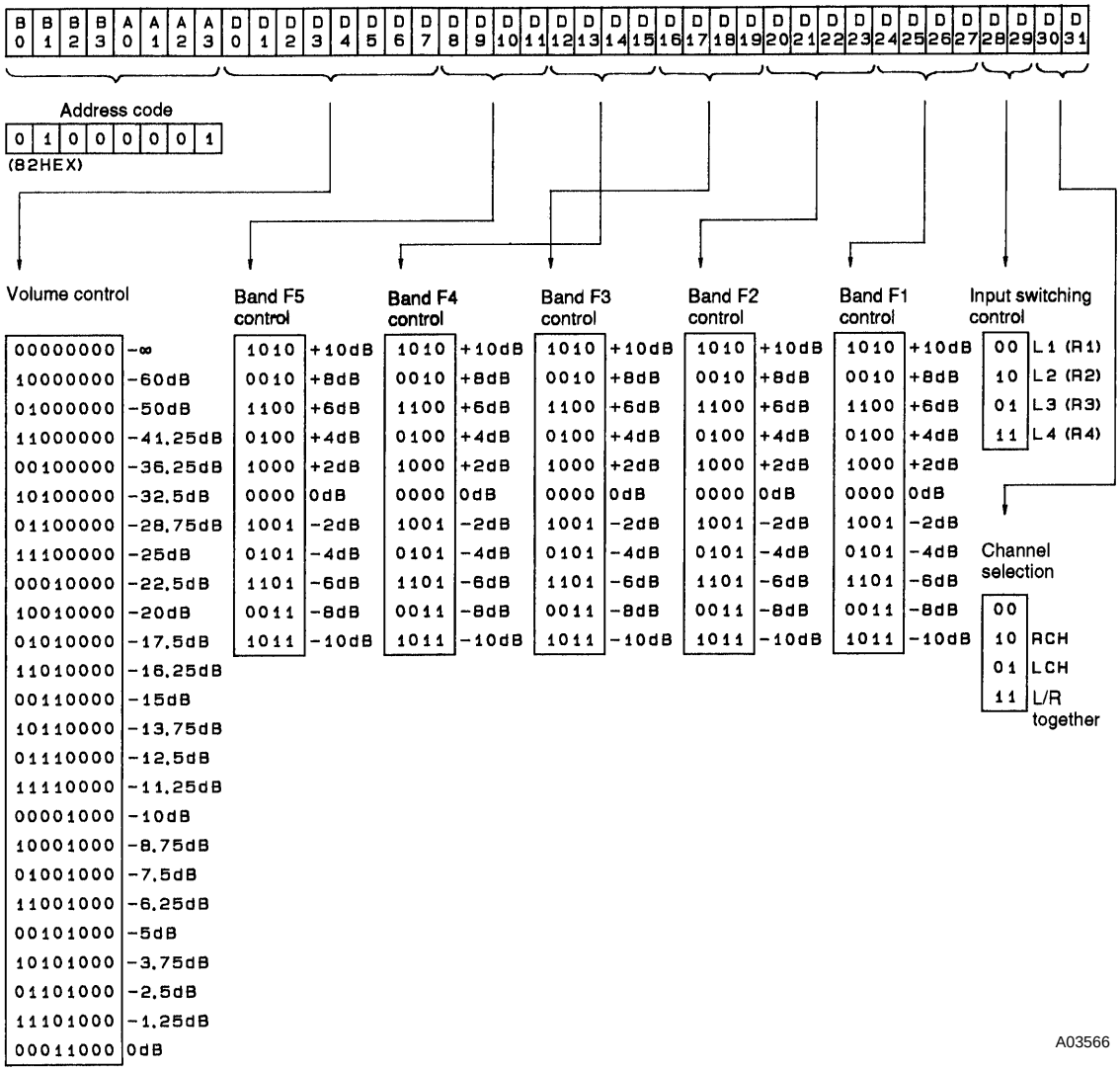
Center frequency F_O (Hz)	C1 (F)	C2 (F)
107	0.536 μ	0.021 μ
340	0.169 μ	6663 p
1070	0.054 μ	2117 p
3400	0.017 μ	666 p

2. Shelving Characteristics (band F5)
   To achieve ±10 dB (in 2 dB steps) at the target frequency, use an external capacitor C3 which has an impedance of 650 Ω.

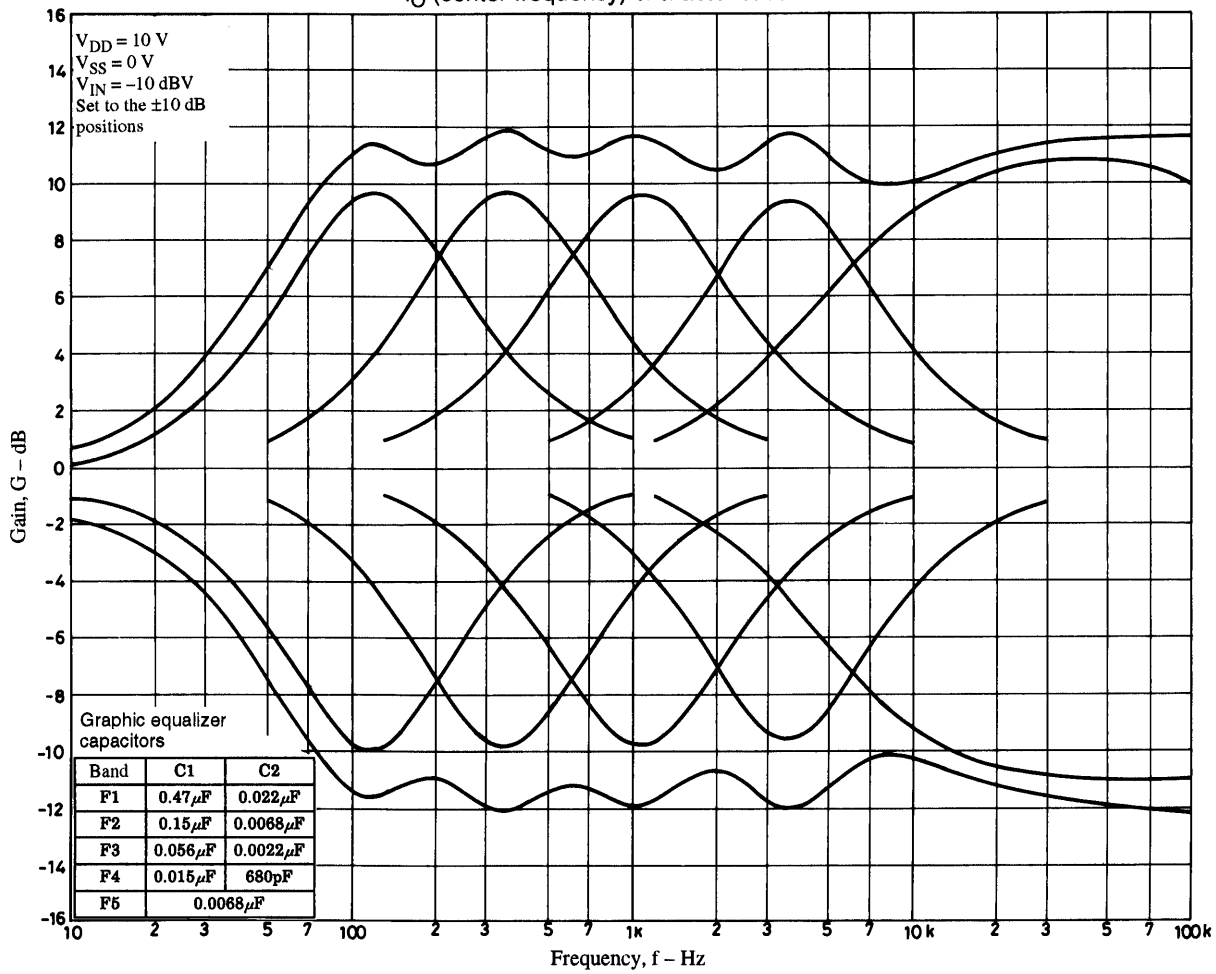
Control System Timing and Data Format

The LC75395E is controlled by inputting stipulated data to the CE, CL, and DI pins. The data consists of a total of 40 bits, of which 8 bits are address and 32 bits are data.

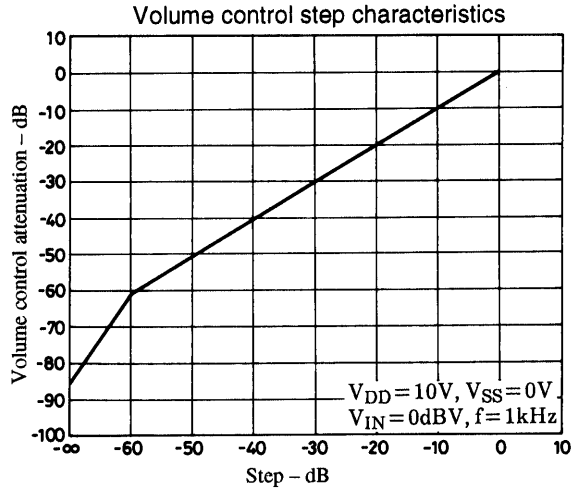




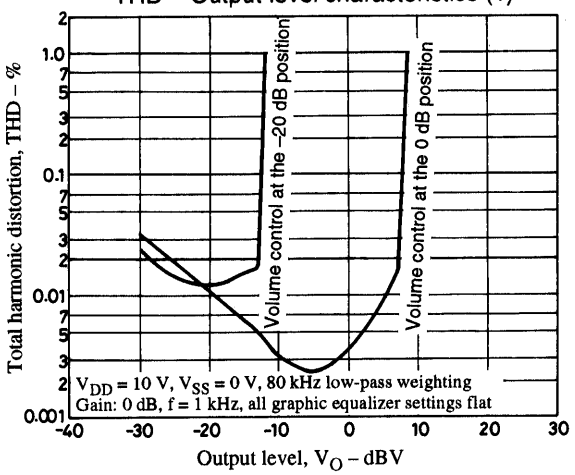
f_O (center frequency) characteristics

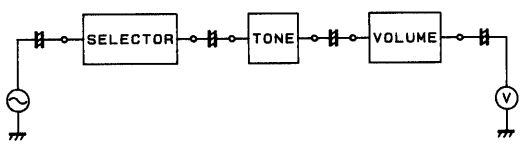


Volume control step characteristics



THD – Output level characteristics (1)





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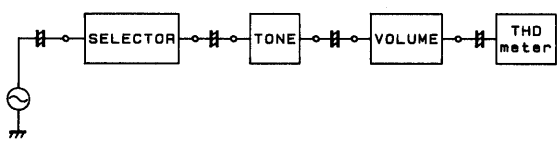
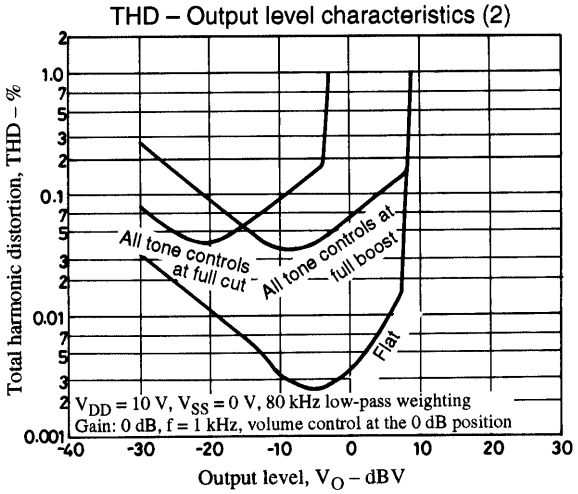
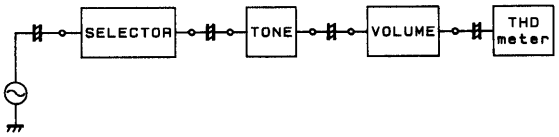


A03731

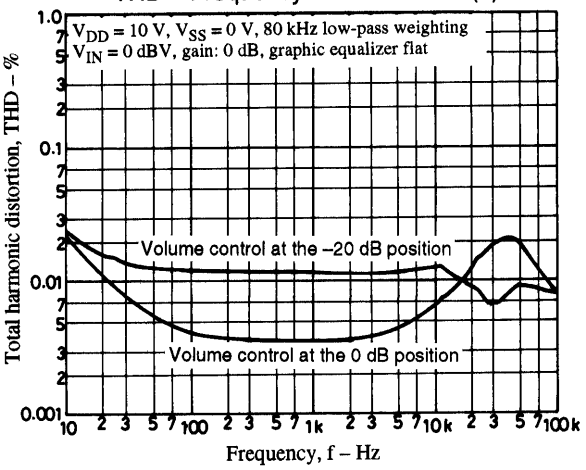
THD – Output level characteristics (2)

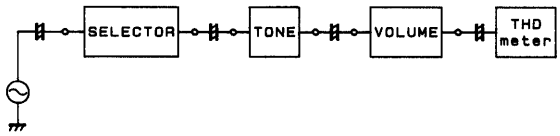




A03732

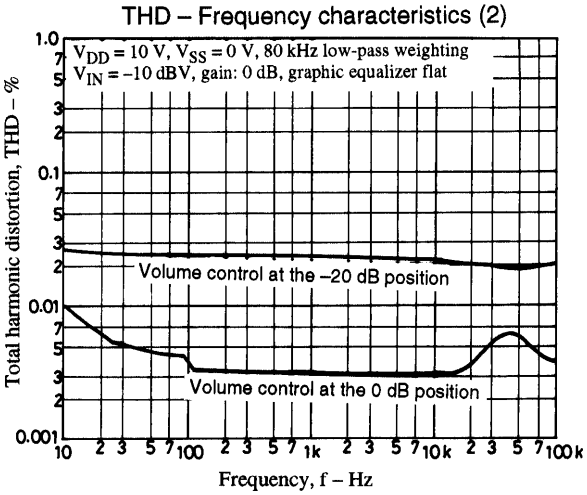
THD – Frequency characteristics (1)

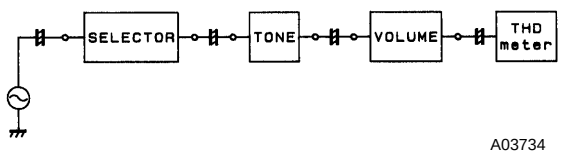




A03733

THD – Frequency characteristics (2)





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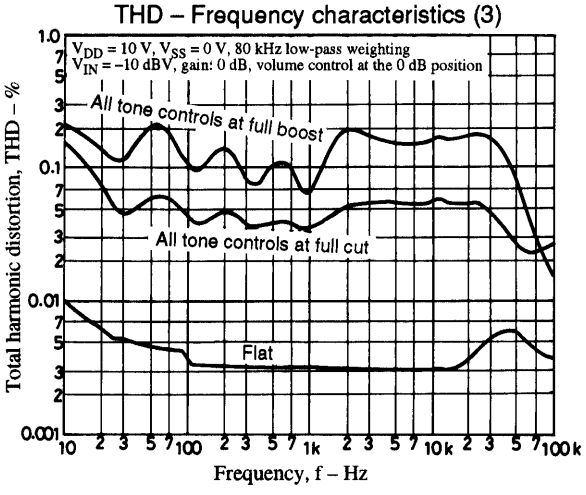
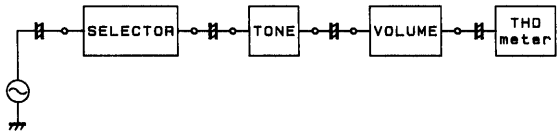
THD – Frequency characteristics (3)





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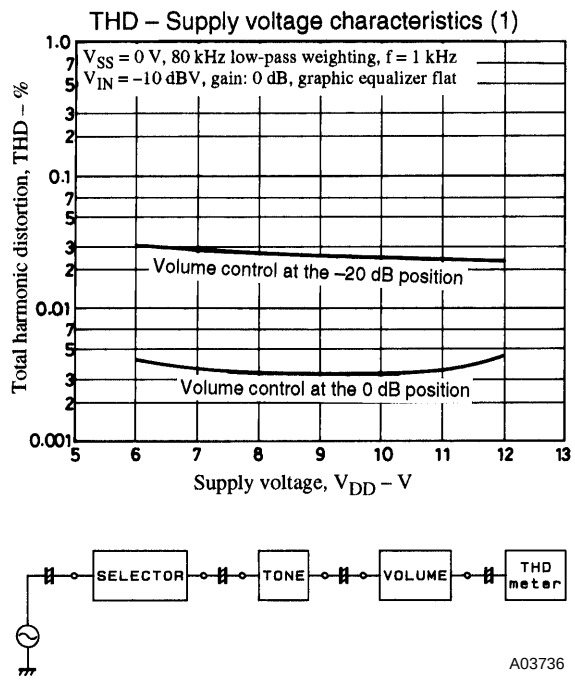

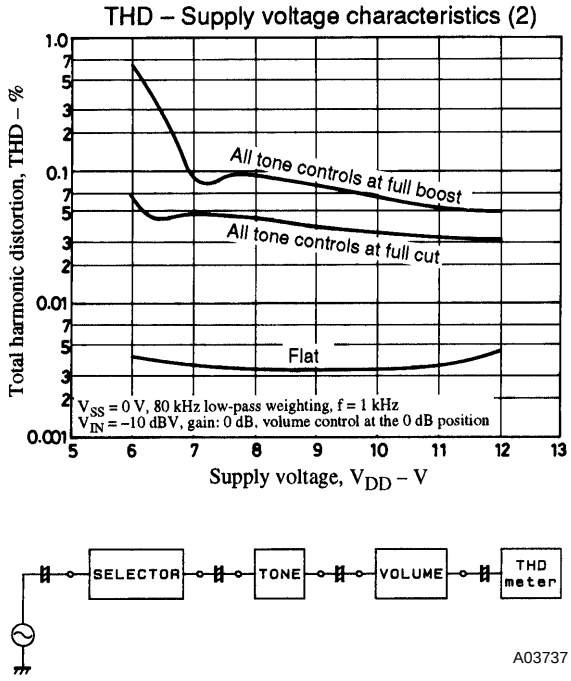

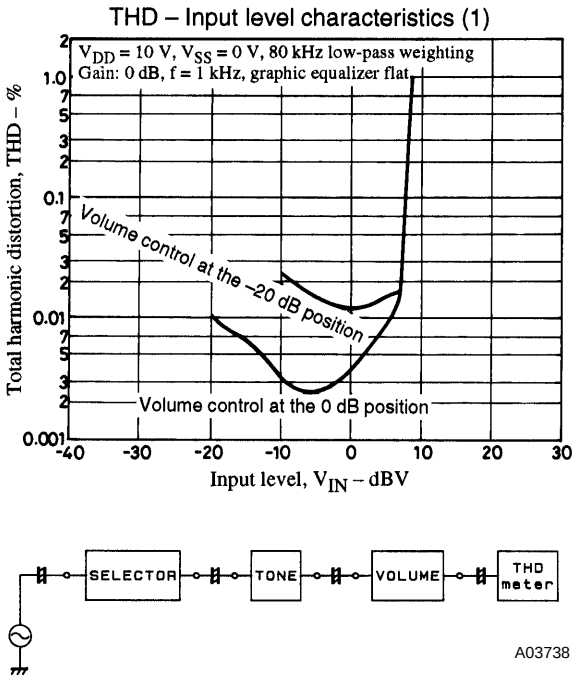

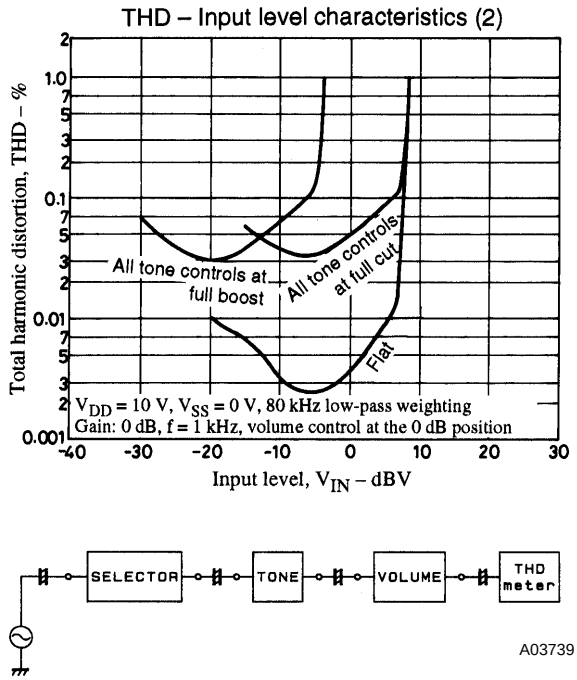

Usage Notes

1. The states of the internal analog switches are undefined when power is first applied. Muting should be applied externally until control data has been transferred and stored.
2. The signal lines for the CL, DI and CE pins should either be covered by the pattern ground or be formed from shielded cable to prevent the high-frequency digital signals transmitted over these lines from entering the analog system.