Ordering number : EN5466

CMOS LSI

LC75394NE

Single-Chip Electronic Volume Control System

Overview

The LC75394NE is an electronic volume control system providing control over volume, balance, 5-band equalizer, and input switching based on serial inputs.

Functions

- Volume control:
  The chip provides 25 levels of volume attenuation: in 2-dB steps between 0 dB and –20 dB, 3-dB steps between –20 dB and –32 dB, 4-dB steps between –32 dB and –52 dB, 4.5-dB steps between –52 dB and –70 dB, and –∞. Independent control over left and right channels provides balance control.
- Equalizer:
  The chip provides control in 2-dB steps over the range between +10 dB and –10 dB. Four of the five bands have peaking equalization; the remaining one, shelving equalization.
- Selector:
  The left and right channels each offer a choice of four inputs. An external constant determines the amplification for the input signal.

Features

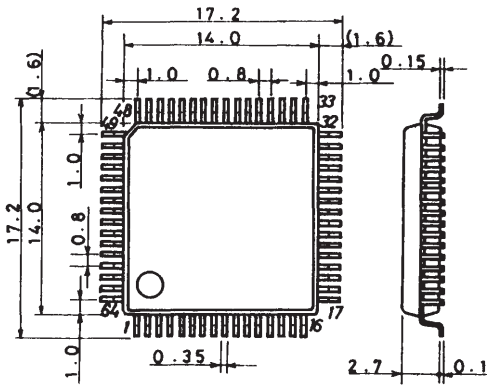
- Built-in buffer amplifiers reduce the number of external parts necessary.
- Silicon gate CMOS reduces switching noise.
- Serial data input
  —Supports CCB* format communication with the system controller.
- A built-in reference voltage circuit divides the supply voltage (V_{DD}) in half.

Package Dimensions

unit: mm

3159-QFP64E

[LC75394NE]



SANYO: QFP64E

*

- **CCB is a trademark of SANYO ELECTRIC CO., LTD.**
- **CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.**

Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD}	12	V
Maximum input voltage	V_{IN} max	CL, DI, CE, L1 to L4, R1 to R4, LTIN, RTIN, LVRIN, RVRIN	V_{SS} – 0.3 to V_{DD} + 0.3	V
Allowable power dissipation	Pd max	Ta ≤ 85°C	310	mW
Operating temperature	Topr		–30 to +85	°C
Storage temperature	Tstg		–40 to +125	°C

Allowable Operating Ranges at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}	V_{DD}	6.0		11.0	V
Input high level voltage	V_{IH}	CL, DI, CE	4.0		V_{DD}	V
Input low level voltage	V_{IL}	CL, DI, CE	V_{SS}		1.0	V
Input voltage amplitude	V_{IN}	CL, DI, CE, L1 to L4, R1 to R4, LTIN, RTIN, LVRIN, RVRIN	V_{SS}		V_{DD}	Vp-p
Input pulse width	$t_{øW}$	CL	1.0			µs
Setup time	t_{SETUP}	CL, DI, CE	1.0			µs
Hold time	t_{HOLD}	CL, DI, CE	1.0			µs
Operating frequency	fopg	CL			500	kHz

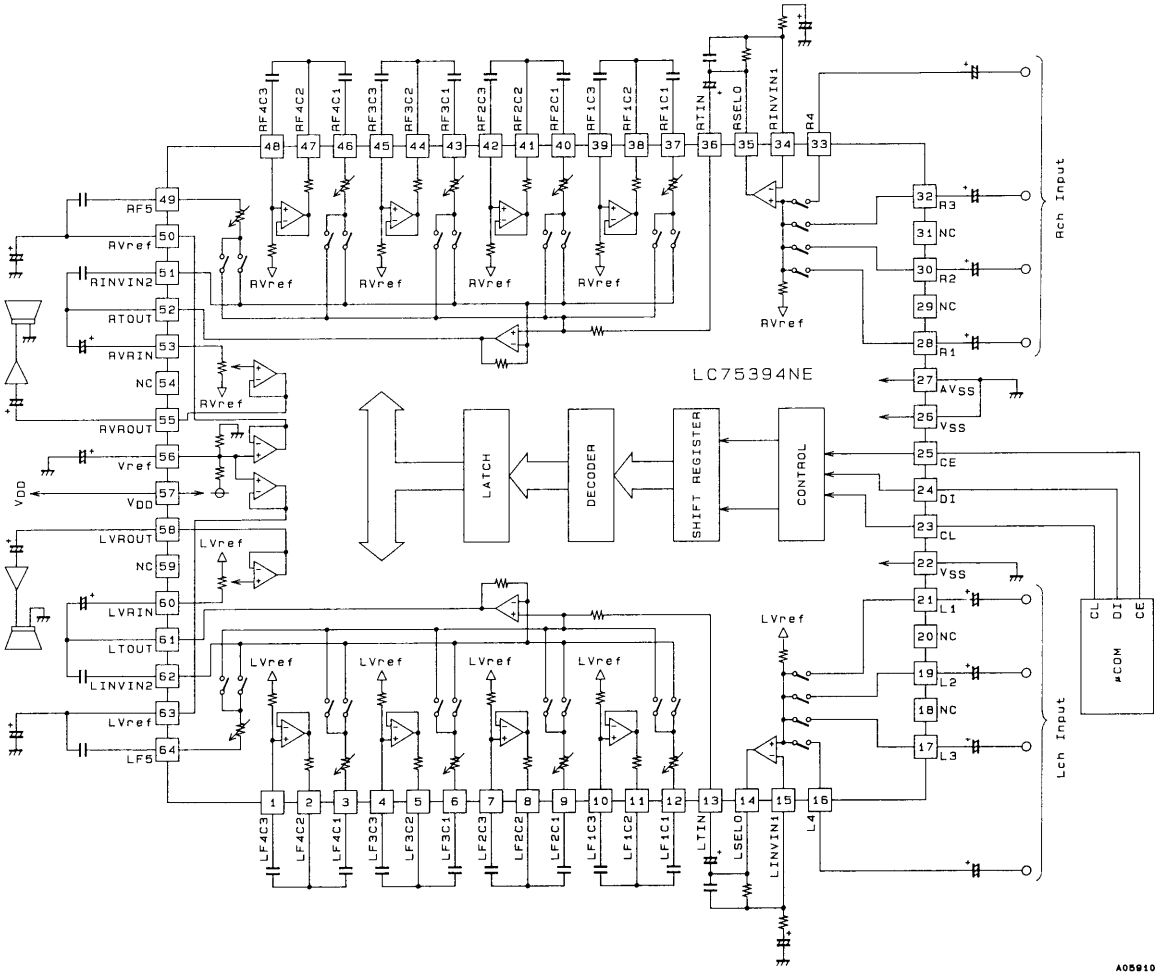
Electrical Characteristics at Ta = 25°C, V_{DD} = 10 V, V_{SS} = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
[Input block]						
Input resistance	Rin	L1 to L4, R1 to R4		1		MΩ
Clipping level	Vcl	LSELO, RSELO: THD = 1.0%		2.65		Vrms
Output load resistance	R_L	LSELO, RSELO	3			kΩ
[Volume control block]						
Input resistance	Rin	LVRIN, RVRIN	60	100	140	kΩ
[Equalizer control block]						
Control range	Geq	Max, boost/cut	±8	±10	±12	dB
Step resolution	Estep		1	2	3	dB
Internal feedback resistance	Rfeed		17	28	39	kΩ
[Overall characteristics]						
Total harmonic distortion	THD (1)	V_{IN} = 1 Vrms, f = 1 kHz, with all controls flat overall		0.0033		%
	THD (2)	V_{IN} = 1 Vrms, f = 20 kHz, with all controls flat overall		0.012		%
Crosstalk	CT	V_{IN} = 1 Vrms, f = 1 kHz, with all controls flat overall, Rg = 1 kΩ		86		dB
Output at maximum attenuation	V_O min	V_{IN} = 1 Vrms, f = 1 kHz, main volume –∞		–90		dB
Output noise voltage	V_N (1)	With all controls flat overall (IHF-A), Rg = 1 kΩ		3.9		µV
	V_N (2)	With all controls flat overall (DIN-AUDIO), Rg = 1 kΩ		5.4		µV
Current drain	I_{DD}	V_{DD} – V_{SS} = 11 V		25	33	mA
Input high level current	I_{IH}	CL, DI, CE, V_{IN} = 11 V			10	µA
Input low level current	I_{IL}	CL, DI, CE, V_{IN} = 0 V	–10			µA

Input Amplifier Characteristics at Ta = 25°C, V_{DD} – V_{SS} = 10 V

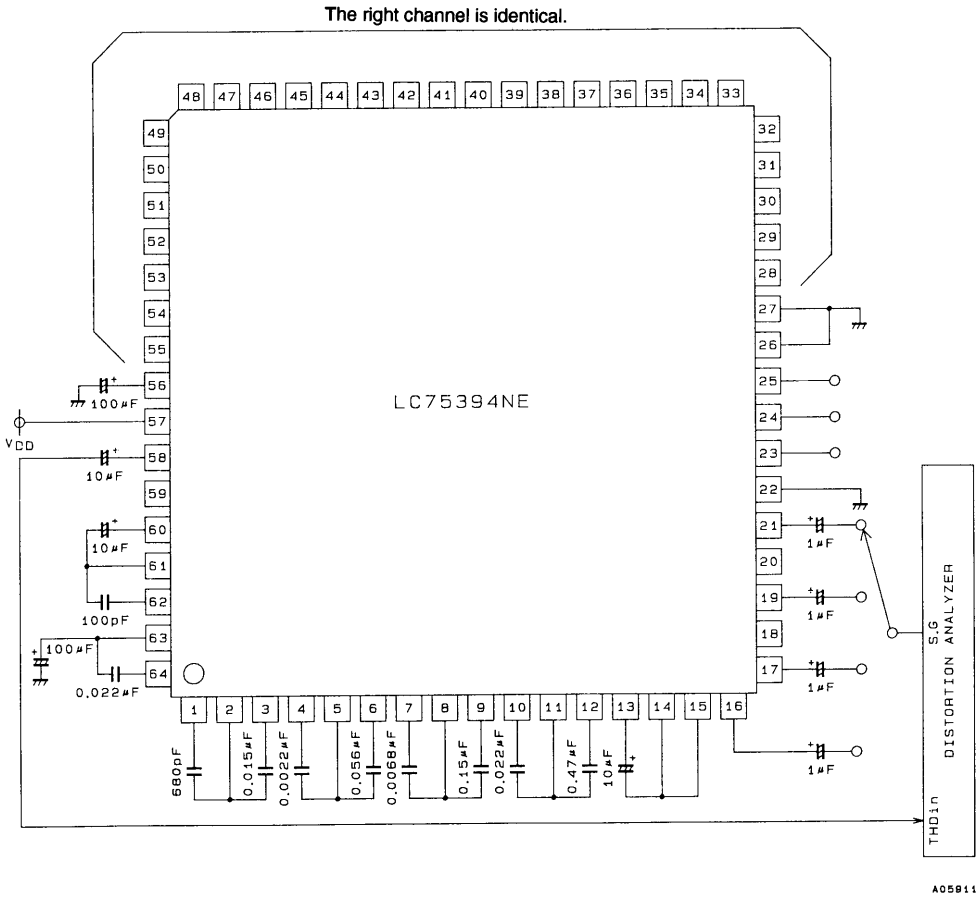
Parameter	Symbol	Conditions	min	typ	max	Unit
Input offset voltage	V_{IO}		–10		+10	mV
Input offset current	I_{IO}	$V_{SS} \le V_{IN} \le V_{DD}$		±10		nA
Open-loop voltage gain	A_O			80		dB
Width of 0 dB band	f_T			2.5		MHz
Allowable load resistance	R_L		3			kΩ

Equivalent Block Diagram and Sample Application Circuit

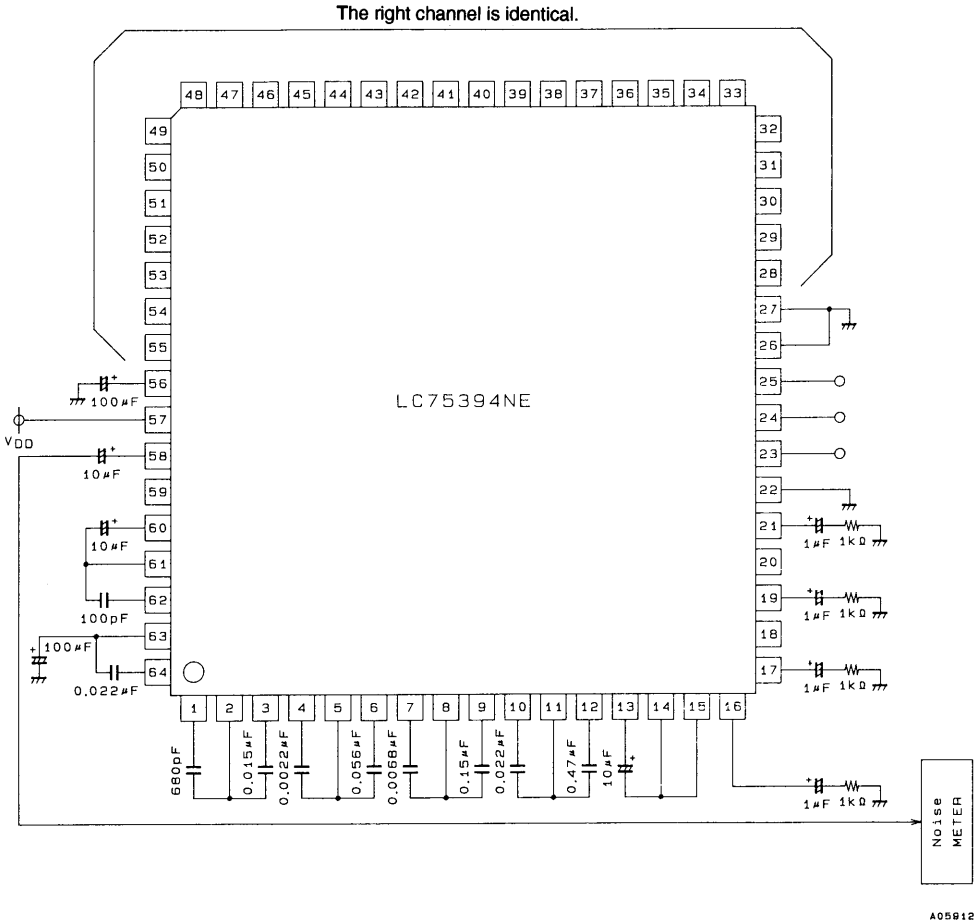


Test Circuits

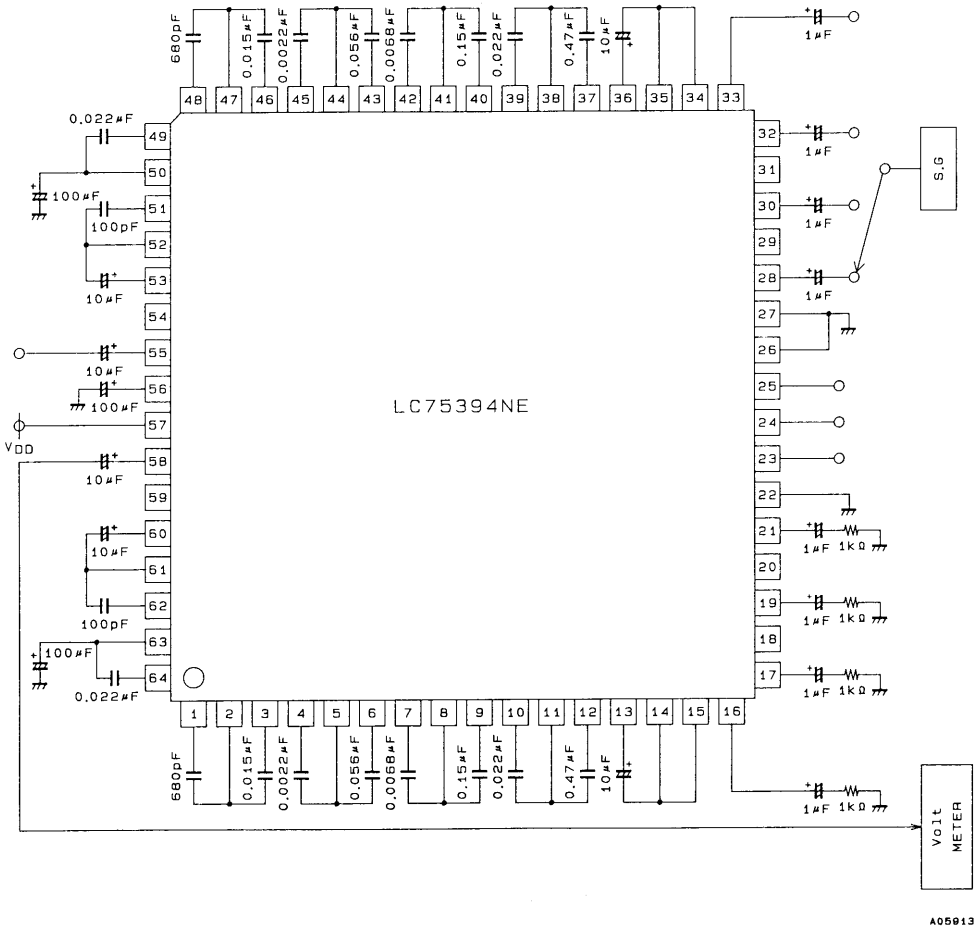
1. Total Harmonic Distortion



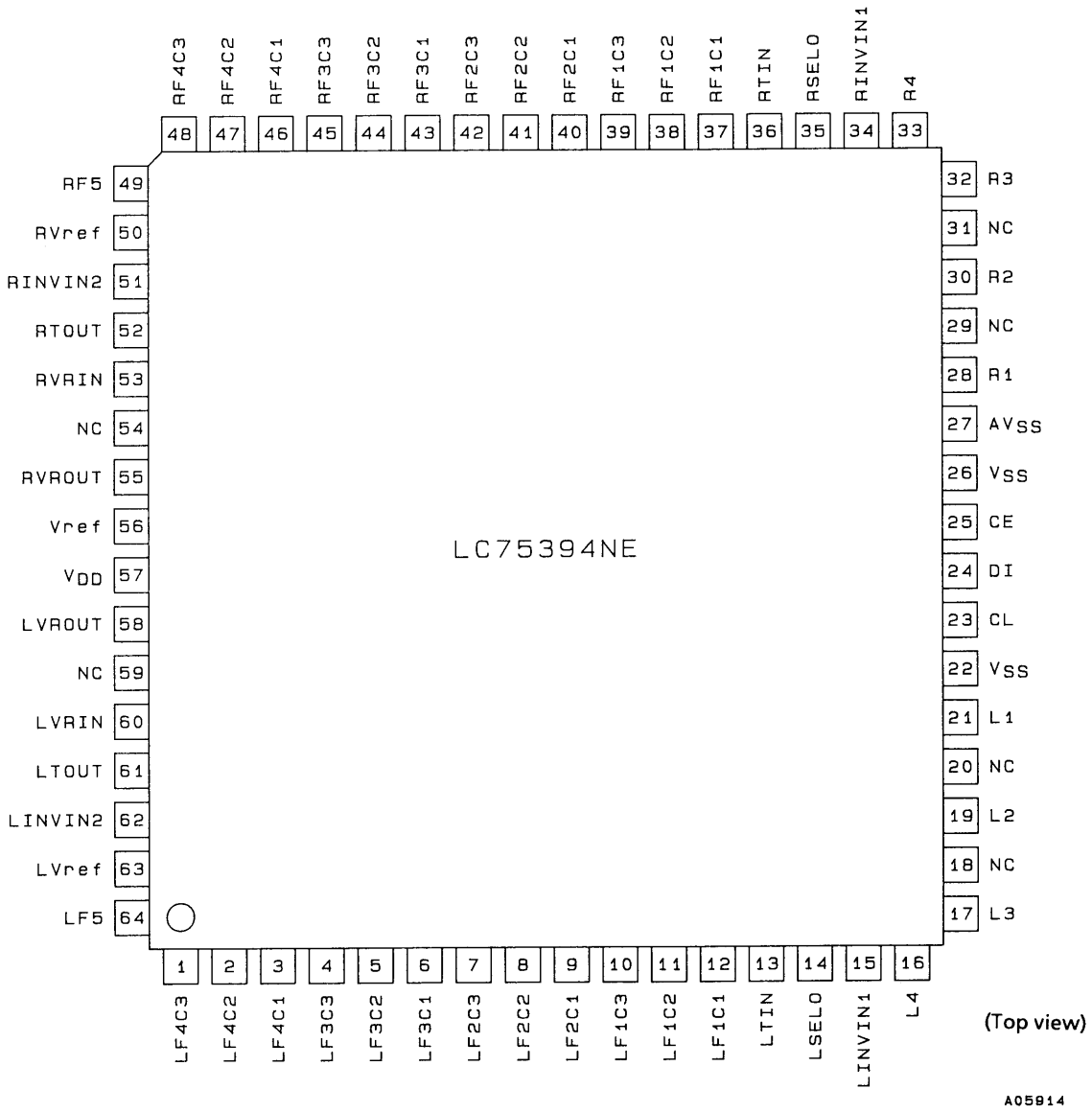
2. Output Noise Voltage



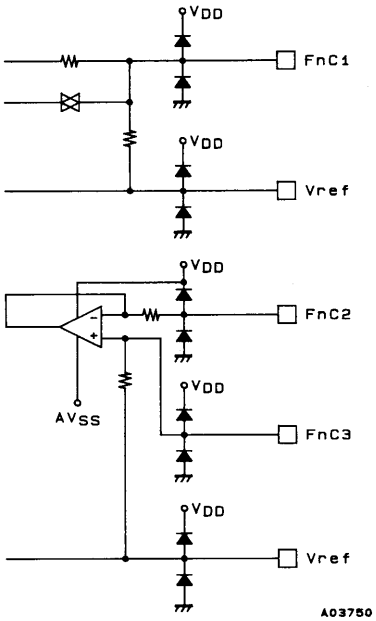
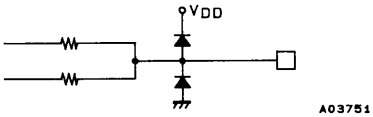
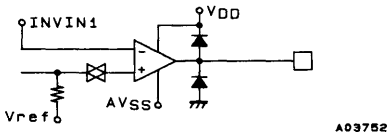
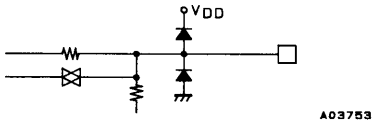
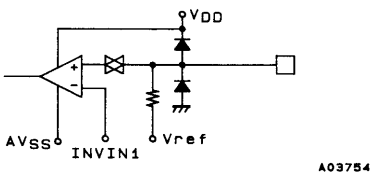
3. Crosstalk


LC75394NE
680pF
0.015μF
0.0022μF
0.056μF
0.0068μF
0.15μF
0.022μF
0.47μF
10μF
1μF
0.022μF
100μF
100pF
10μF
VDD
1kΩ
S.G
Volt METER
A05913

Pin Assignment

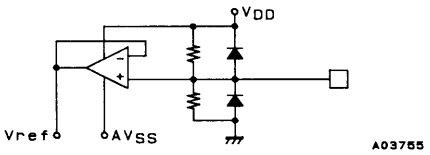
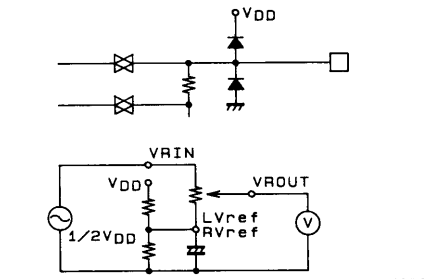
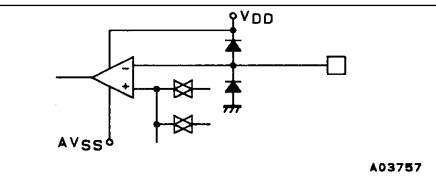
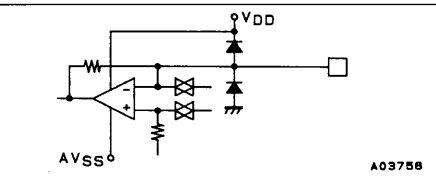
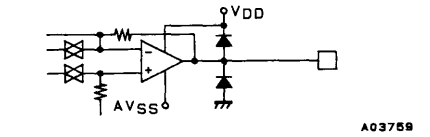
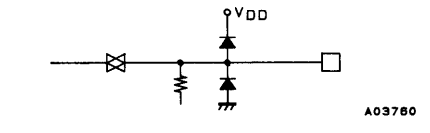
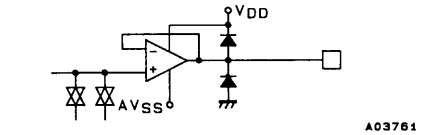
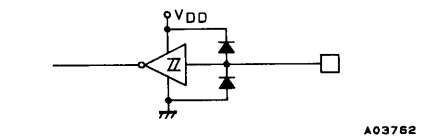


Pin Functions

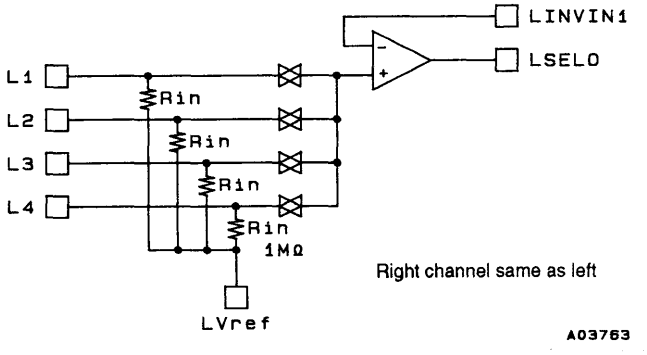
Pin No.	Symbol	Function	Note
12 11 10	LF1C1 LF1C2 LF1C3	F1 band control block for left channel. Connect to external capacitors.	
37 38 39	RF1C1 RF1C2 RF1C3	F1 band control block for right channel. Connect to external capacitors.	
9 8 7	LF2C1 LF2C2 LF2C3	F2 band control block for left channel. Connect to external capacitors.	
40 41 42	RF2C1 RF2C2 RF2C3	F2 band control block for right channel. Connect to external capacitors.	
6 5 4	LF3C1 LF3C2 LF3C3	F3 band control block for left channel. Connect to external capacitors.	
43 44 45	RF3C1 RF3C2 RF3C3	F3 band control block for right channel. Connect to external capacitors.	
3 2 1	LF4C1 LF4C2 LF4C3	F4 band control block for left channel. Connect to external capacitors.	
46 47 48	RF4C1 RF4C2 RF4C3	F4 band control block for right channel. Connect to external capacitors.	
13 36	LTIN RTIN	Tone control inputs. Must be driven with low-impedance circuits.	
14 35	LSELO RSELO	Input selector outputs	
64 49	LF5 RF5	F5 band control block. Connect to external capacitors.	
21 19 17 16 28 30 32 33	L1 L2 L3 L4 R1 R2 R3 R4	Signal inputs	
57	V_{DD}	Power supply connection	
22, 26	V_{SS}	Grounds for internal logic	
27	AV_{SS}	Ground for internal operational amplifier	

Continued on next page.

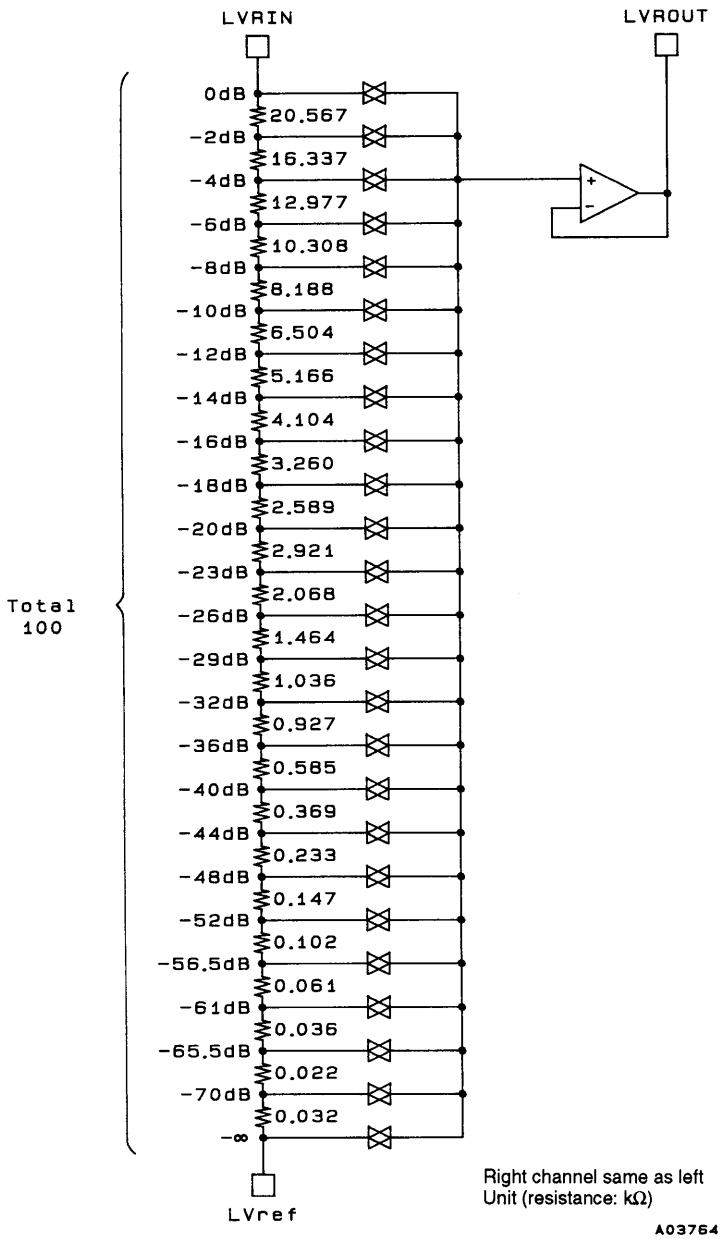
Continued from preceding page.

Pin No.	Symbol	Function	Note
56	Vref	$V_{DD}/2$ voltage generator block. Connect capacitors between Vref and V_{SS} to minimize the effects of power supply ripple.	
63 50	LVref RVref	Pins common to volume control, tone control, and input selection blocks. Select the capacitors between these pins and V_{SS} carefully as they contribute residual resistance when the volume is turned down. The voltage must never exceed V_{DD}.	
15 34	LINVIN1 RINVIN1	Operational amplifier inverted input for specifying input gain.	
62 51	LINVIN2 RINVIN2	Operational amplifier inverted input for specifying graphic equalization. Connecting a capacitor across INVIN2 and TOUT permits the removal of unwanted bands and reduces the risk of oscillation.	
61 52	LTOUT RTOUT	Tone control output	
60 53	LVRIN RVRIN	Volume control input. Must be driven with low-impedance circuits.	
58 55	LVROUT RVROUT	Volume control output	
25	CE	Chip enable pin. The chip uses falling edge timing to write data to the internal latch and shift analog switches. The high level enables data transfer.	
24 23	DI CL	Serial data and clock input used for control	
18 20 29 31 54 59	NC NC NC NC NC NC	Leave unconnected	

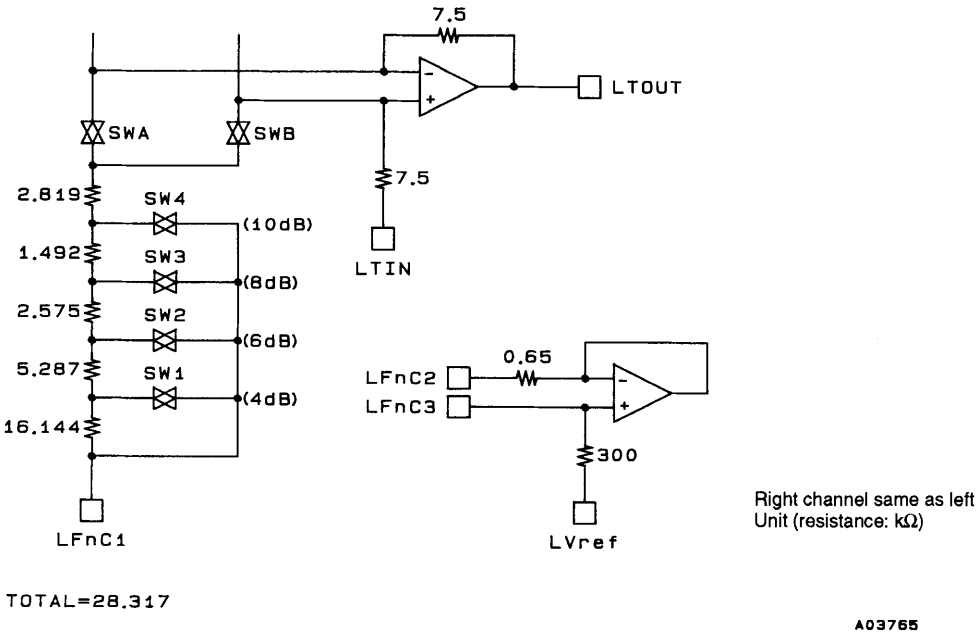
Input Block Internal Equivalent Circuit Diagram



Volume Control Block Internal Equivalent Diagram



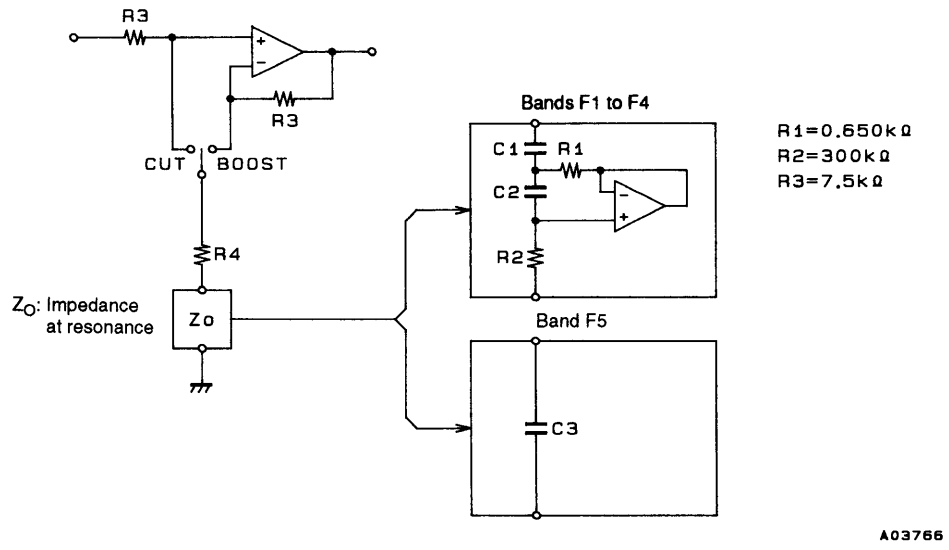
Equalizer Control Block Internal Equivalent Circuit (Bands F1 to F4)



Calculating the Size of External Capacitors

The LC75394NE supports four bands with peaking characteristics and one band with shelving characteristics

1. Peaking Characteristics (bands F1 to F4)
   The external capacitor functions as the structural element of a simulated inductor. The equivalent circuit and the calculations required to achieve the desired center frequency are shown below.
   - Equivalent circuit for the simulated inductor



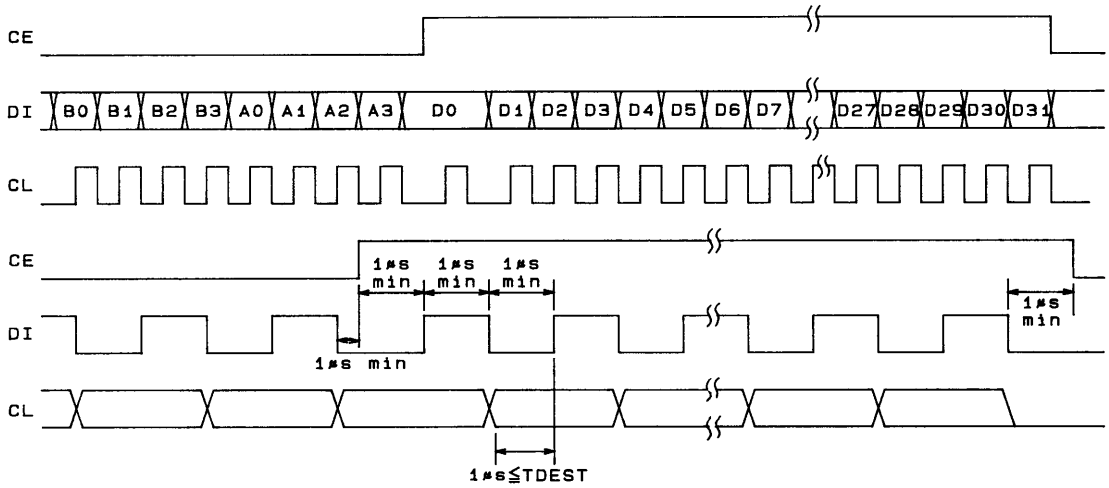
- Calculation example
  Specifications: Central frequency, F_O = 107 Hz
  Q factor at maximum boost, $Q_{+10\ dB}$ = 0.8
  — Calculate Q_O, the sharpness of the simulated inductance itself.
  $Q_O = (R1 + R4)/R1 \times Q_{+10dB}$ Note: R4 is from the separately issued internal block diagram.
  $\neq 4.270$
  — Calculate C1
  $C1 = 1/2\pi F_O R1 Q_O \neq 0.536$ (μF)
  — Calculate C2
  $C2 = Q_O/2\pi F_O R2 \neq 0.021$ (μF)
- Sample results

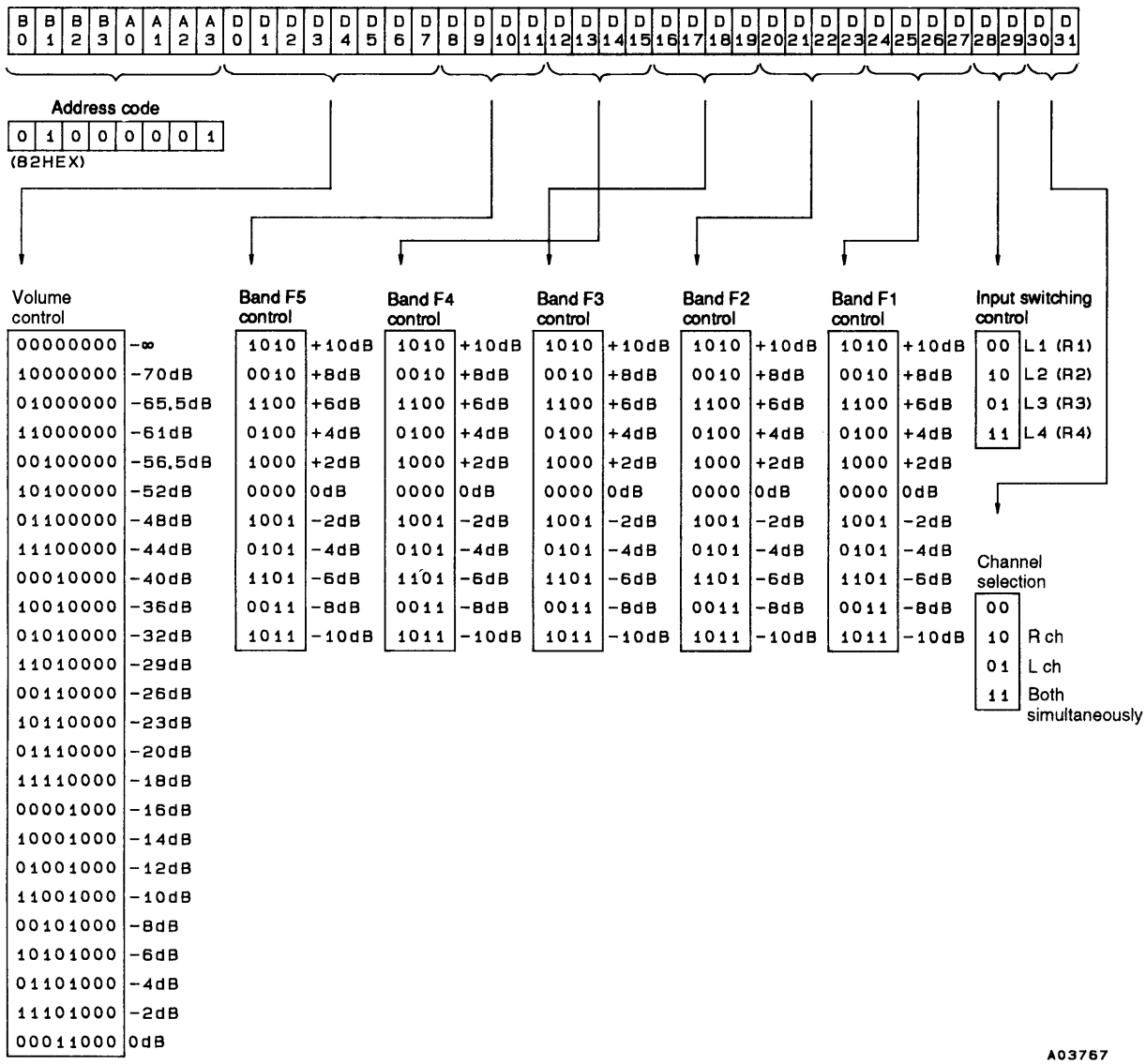
Central frequency F_O (Hz)	C1 (F)	C2 (F)
107	0.536 μ	0.021 μ
340	0.169 μ	6663 P
1070	0.054 μ	2117 P
3400	0.017 μ	666 P

- Shelving characteristics (Band F5)
  Achieving the desired control of 2-dB steps over the range between +10 dB to –10 dB requires choosing a capacitor, C3, with an impedance of 650 Ω.

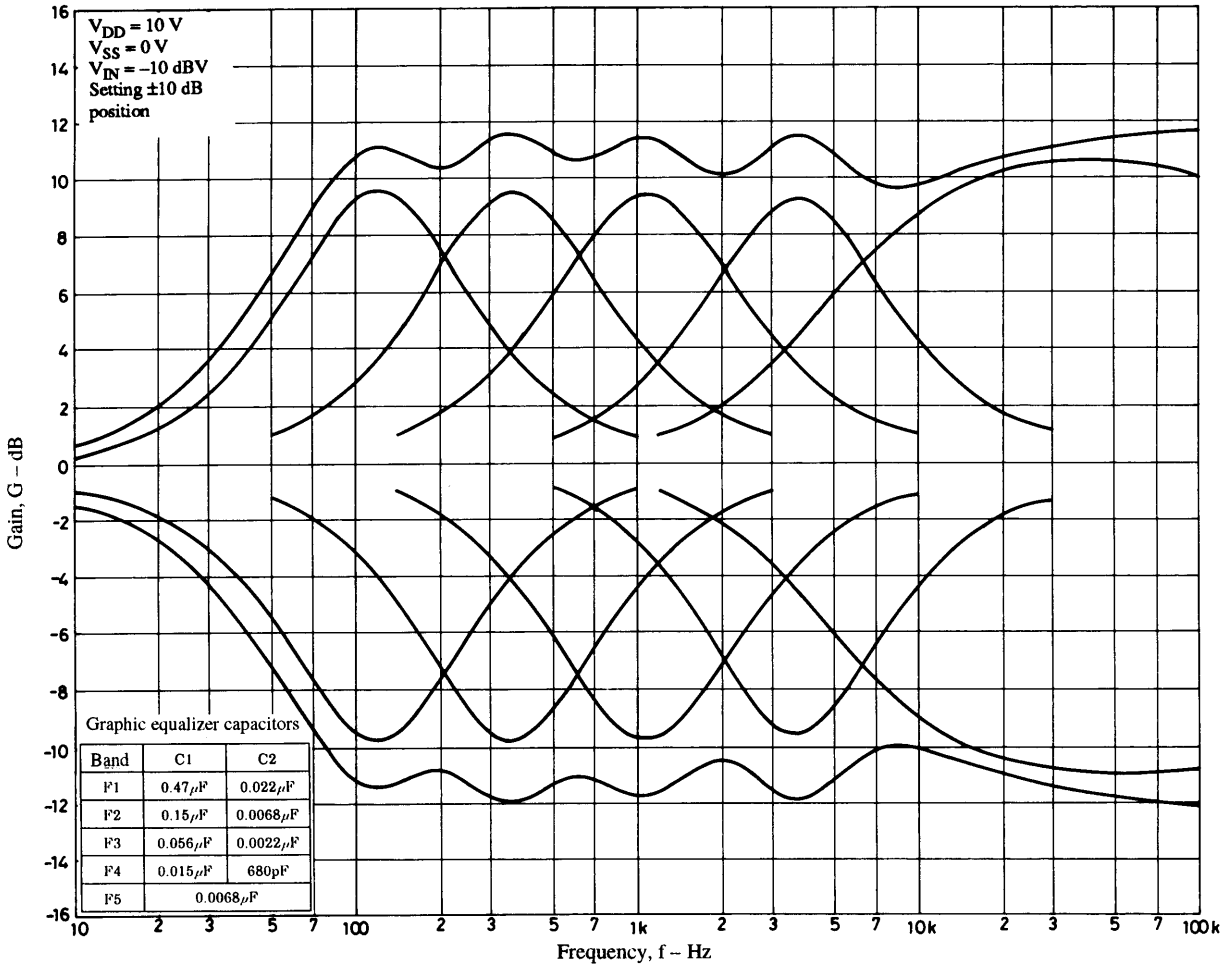
Control System Timing and Data Formats

The LC75394NE receives its control sequences via a serial interface comprised of pins CE, CL, and DI. Each sequence consists of 40 bits: an 8-bit address followed by 32 bits of data.





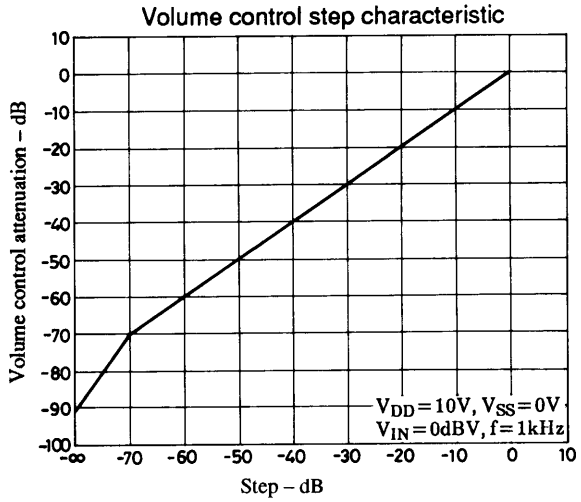
f_O (central frequency) characteristic



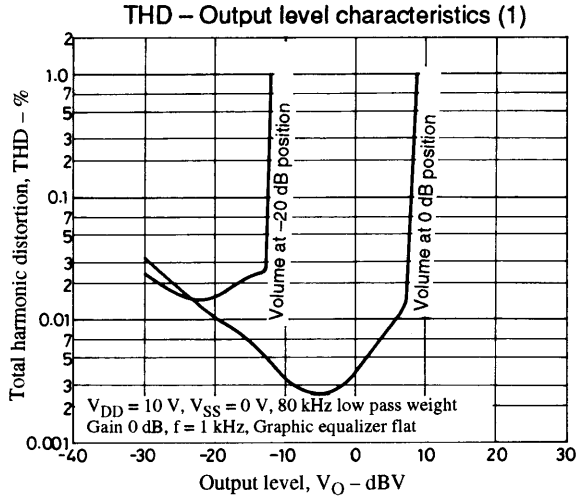
Graphic equalizer capacitors

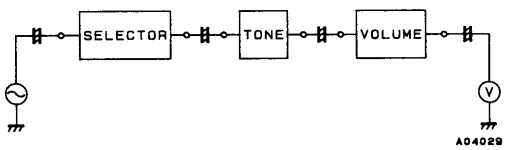
Band	C1	C2
F1	0.47μF	0.022μF
F2	0.15μF	0.0068μF
F3	0.056μF	0.0022μF
F4	0.015μF	680pF
F5	0.0068μF	

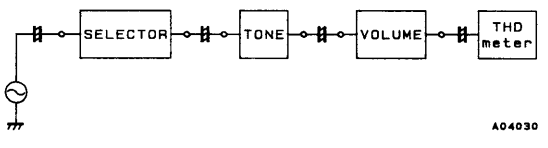
Volume control step characteristic



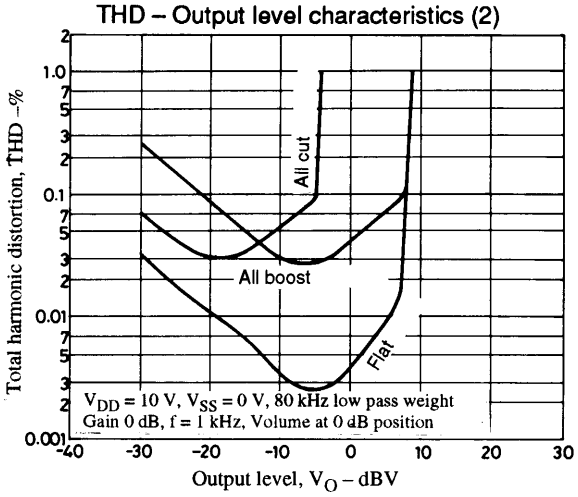
THD – Output level characteristics (1)

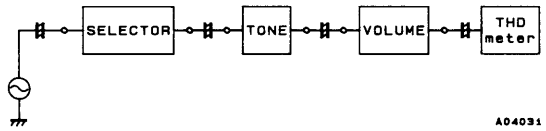




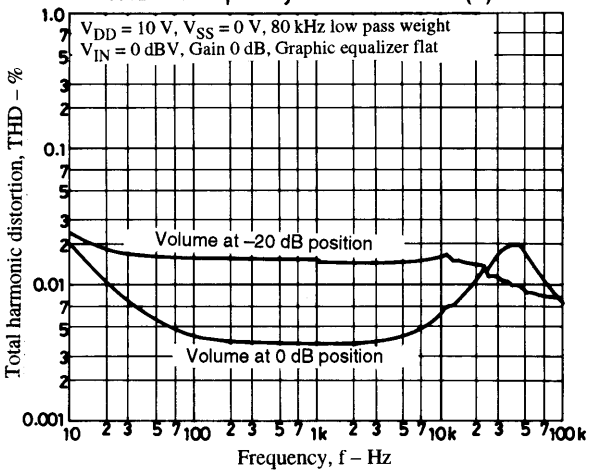


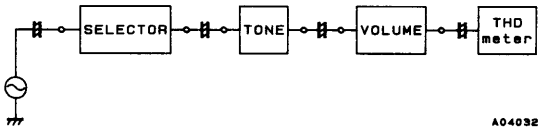
THD – Output level characteristics (2)



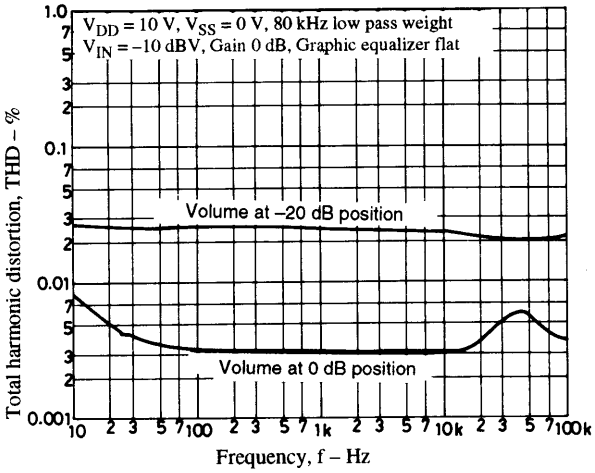


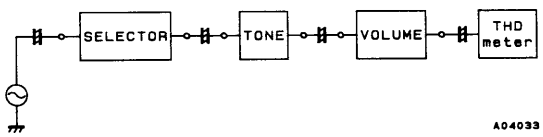
THD – Frequency characteristics (1)



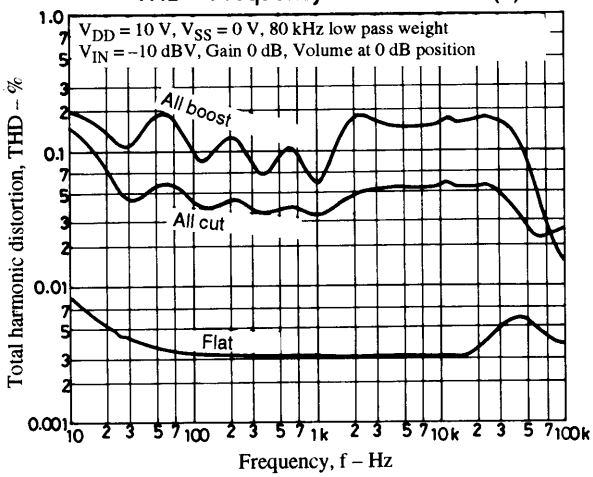


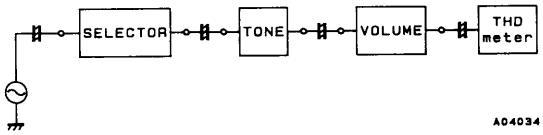
THD – Frequency characteristics (2)



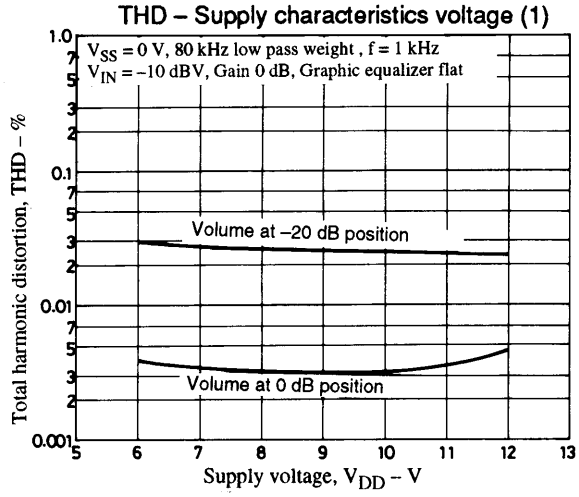


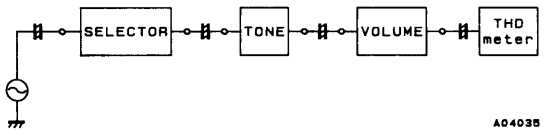
THD – Frequency characteristics (3)



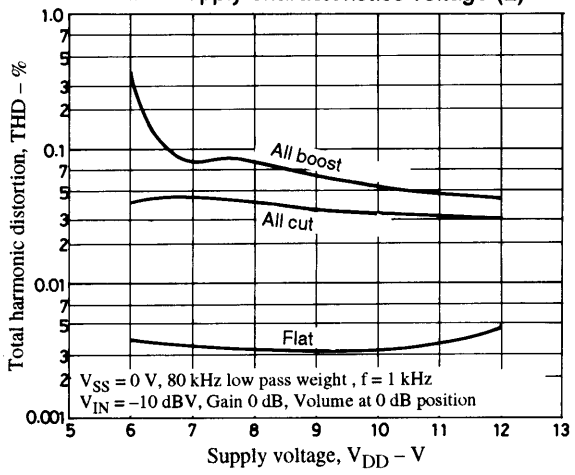


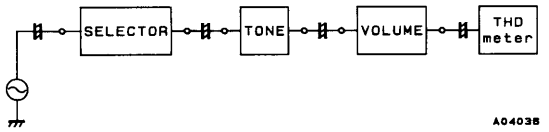
THD – Supply characteristics voltage (1)



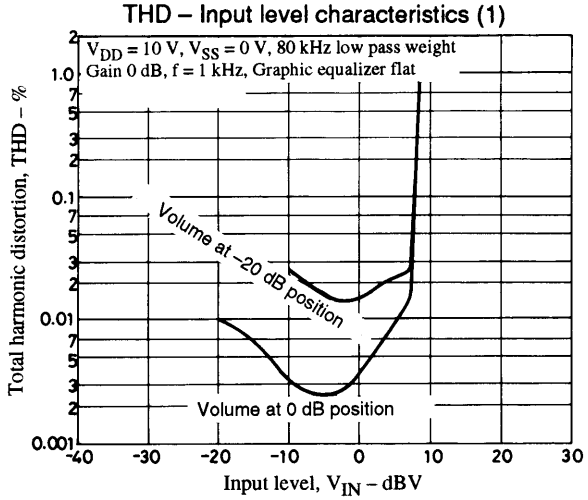


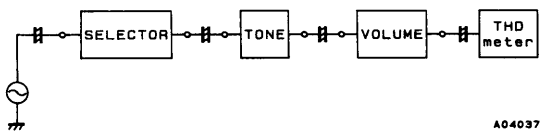
THD – Supply characteristics voltage (2)



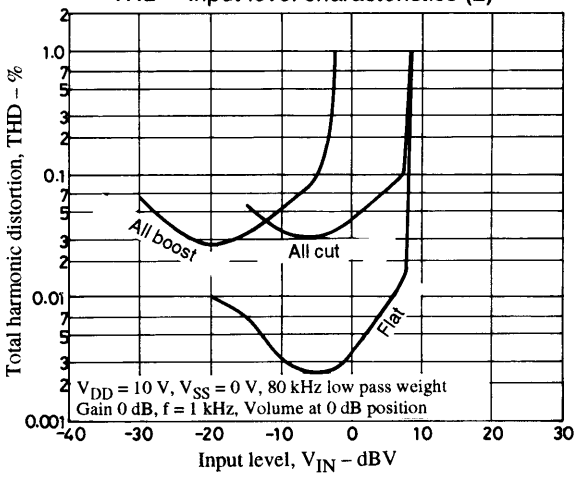


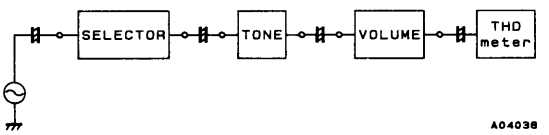
THD – Input level characteristics (1)





THD – Input level characteristics (2)





Usage Notes

1. When the power is first applied, the internal analog switches are in indeterminate states. The chip therefore requires muting or other external measures until it has received the proper data.
2. Provide grounding patterns or shielding for the lines to the CL, DI, and CE pins so as to prevent their high-frequency data signals from interfering with the operation of nearby analog circuits.