

SANYO

No. ※4819

LC36256ALL, AMLL-70W/85W/10W/12W**256 K (32768 words × 8 bits) SRAM**

Preliminary

Overview

The LC36256ALL, AMLL-70W/85W/10W/12W are fully asynchronous silicon gate CMOS static RAMs with an 32,768 words × 8 bits.

This series has \overline{CE} chip enable pin for device select/nonselect control and an \overline{OE} output enable pin for output control, and features high speed, low power dissipation, and wide temperature range.

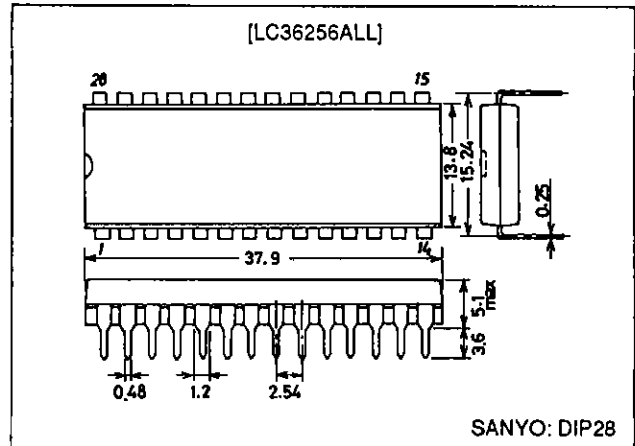
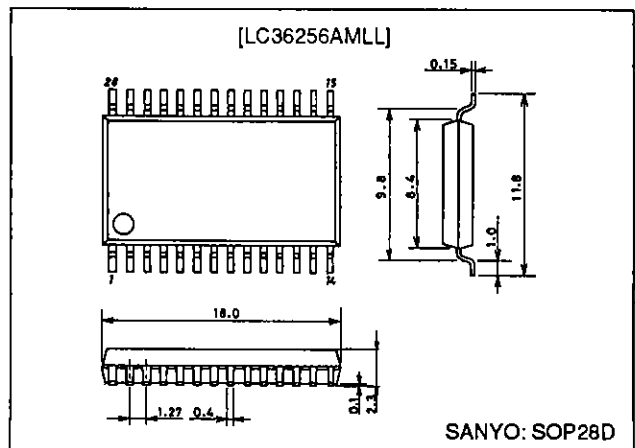
Current dissipation is notably reduced during standby and data retention. For these reasons, this series is most suited for use in systems requiring high speed, low power dissipation, and long-term battery backup. Simple memory capacity expansion is also supported.

Features

- Access time
 - 70 ns (max.) : LC36256ALL-70W,
LC36256AMLL-70W
 - 85 ns (max.) : LC36256ALL-85W,
LC36256AMLL-85W
 - 100 ns (max.) : LC36256ALL-10W,
LC36256AMLL-10W
 - 120 ns (max.) : LC36256ALL-12W,
LC36256AMLL-12W
- Low current dissipation
 - During standby
 - 0.5 μ A (max.) / Ta = 25°C
 - 1 μ A (max.) / Ta = -10 to +40°C
 - 5 μ A (max.) / Ta = -10 to +70°C
 - During data retention
 - 0.3 μ A (max.) / Ta = 25°C
 - 0.6 μ A (max.) / Ta = -10 to +40°C
 - 3 μ A (max.) / Ta = -10 to +70°C
 - During operation (DC)
 - 10 mA (max.)
- Single 5 V power supply: 5 V \pm 10%
- Data retention power supply voltage: 2.0 to 5.5 V
- No clock required (Fully static memory)
- All input/output levels are TTL compatible
- Common input/output pins, with three output states
- Packages
 - DIP 28-pin plastic package (600 mil) : LC36256ALL
 - SOP 28D-pin plastic package (450 mil) : LC36256AMLL

Package Dimensions

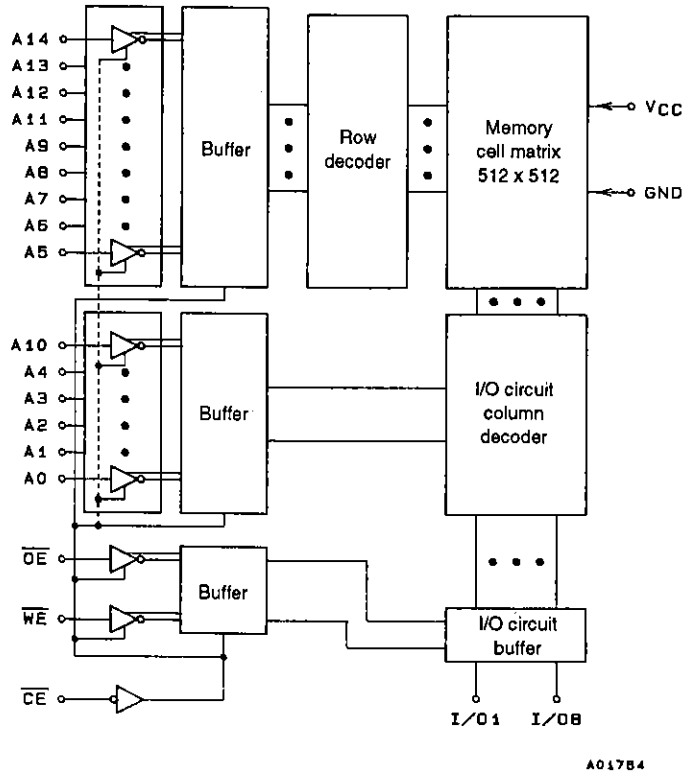
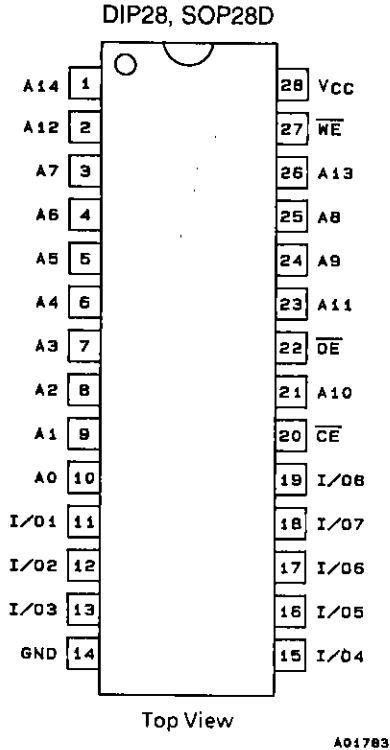
unit: mm

3012A-DIP28**3187-SOP28D****SANYO Electric Co., Ltd. Semiconductor Business Headquarters**

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

Pin Assignment

Block Diagram



Pin Functions

A ₀ to A ₁₄	Address input
\overline{WE}	Read/write control input
\overline{OE}	Output enable input
\overline{CE}	Chip enable input
I/O ₁ to I/O ₈	Data input/output
V _{CC} , GND	Power supply pins

Functions Logic

Mode	\overline{CE}	\overline{OE}	\overline{WE}	I/O	Supply current
Read cycle	L	L	H	Data output	I _{CCA}
Write cycle	L	X	L	Data input	I _{CCA}
Output disable	L	H	H	High impedance	I _{CCA}
Nonselect	H	X	X	High impedance	I _{CCS}

X: H or L

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{CC} max		7.0	V
Input pin voltage	V _{IN}		-0.5* to V _{CC} + 0.5	V
I/O pin voltage	V _{I/O}		-0.5* to V _{CC} + 0.5	V
Allowable power dissipation	Pd max	LC36256ALL	1.0	W
		LC36256AMLL	0.7	W
Operating temperature range	T _{opr}		-10 to +70	°C
Storage temperature range	T _{stg}		-55 to +150	°C

* -3.0 V when pulse width is less than 50 ns

DC Recommended Operating Ranges at Ta = -10 to +70°C

Parameter	Symbol	min	typ	max	Unit
Power supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high level voltage	V _{IH}	2.2		V _{CC} + 0.3	V
Input low level voltage	V _{IL}	-0.3*		+0.8	V

* -3.0 V when pulse width is less than 50 ns

DC Electrical Characteristics at Ta = -10 to +70°C, V_{CC} = 5 V ± 10%

Parameter	Symbol	Conditions	min	typ*	max	Unit	
Input leakage current	I _{LI}	V _{IN} = 0 to V _{CC}	-0.5		+0.5	μA	
I/O leakage current	I _{LO}	V _{CE} = V _{IH} or V _{OE} = V _{IH} , V _{I/O} = 0 to V _{CC}	-0.5		+0.5	μA	
Output high level voltage	V _{OH}	I _{OH} = -1.0 mA	2.4			V	
Output low level voltage	V _{OL}	I _{OL} = 2.1 mA			0.4	V	
Operating supply current (DC)	I _{CCA1}	V _{CE} ≤ 0.2 V, V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} - 0.2 V I _{I/O} = 0 mA		1	5	mA	
	I _{CCA2}	V _{CE} = V _{IL} , I _{I/O} = 0 mA		3	10	mA	
Average operating supply current	I _{CCA3}	min cycle Duty = 100% I _{I/O} = 0 mA	Access time	70 ns	30	50	mA
				85 ns	25	50	
				100 ns	23	50	
				120 ns	20	50	
Standby supply current	I _{CCS1}	V _{CE} ≥ V _{CC} - 0.2 V	-10 to +70°C		5	μA	
			-10 to +40°C		1		
			25°C	0.2	0.5		
	I _{CCS2}	V _{CE} = V _{IH}		0.4	2	mA	

* Reference values at V_{CC} = 5 V, Ta = 25°C

LC36256ALL, AMLL-70W/85W/10W/12W

Input/Output Capacitance at $T_a = 25^\circ\text{C}$, $f = 1\text{ MHz}$

Parameter	Symbol	Conditions	min	typ	max	Unit
Input/output capacitance	$C_{I/O}$	$V_{I/O} = 0\text{ V}$			8	pF
Input capacitance	C_{IN}	$V_{IN} = 0\text{ V}$			6	pF

These parameters were obtained through sampling, and not full-lot measurement.

AC Electrical Characteristics at $T_a = -10$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$

AC testing conditions

Input pulse voltage level	: 0.8 V, 2.2 V
Input rise and fall time	: 5 ns
Input - output timing level	: 1.5 V
Output load	: 1 TTL gate + $C_L = 100\text{ pF}$ (85 ns/100 ns/120 ns) 1 TTL gate + $C_L = 30\text{ pF}$ (70 ns) (including scope and jig capacitance)

Read Cycle

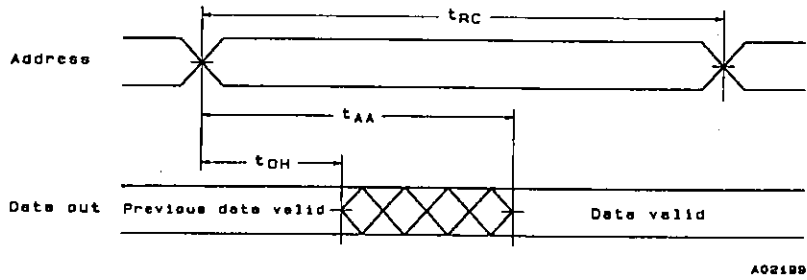
Parameter	Symbol	LC36256ALL-70W LC36256AMLL-70W		LC36256ALL-85W LC36256AMLL-85W		LC36256ALL-10W LC36256AMLL-10W		LC36256ALL-12W LC36256AMLL-12W		Unit
		min	max	min	max	min	max	min	max	
Read cycle time	t_{RC}	70		85		100		120		ns
Address access time	t_{AA}		70		85		100		120	ns
$\overline{\text{CE}}$ access time	t_{CA}		70		85		100		120	ns
$\overline{\text{OE}}$ access time	t_{OA}		35		45		50		60	ns
Output hold time	t_{OH}	20		20		20		20		ns
$\overline{\text{CE}}$ output enable time	t_{COE}	10		10		10		10		ns
$\overline{\text{OE}}$ output enable time	t_{OOE}	5		5		5		5		ns
$\overline{\text{CE}}$ output disable time	t_{COD}	0	30	0	30	0	30	0	30	ns
$\overline{\text{OE}}$ output disable time	t_{OOD}	0	30	0	30	0	30	0	30	ns

Write Cycle

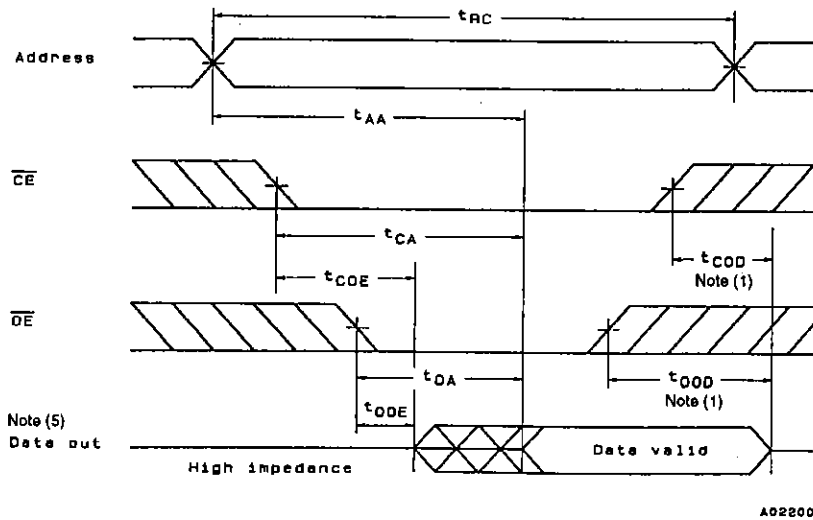
Parameter	Symbol	LC36256ALL-70W LC36256AMLL-70W		LC36256ALL-85W LC36256AMLL-85W		LC36256ALL-10W LC36256AMLL-10W		LC36256ALL-12W LC36256AMLL-12W		Unit
		min	max	min	max	min	max	min	max	
Write cycle time	t_{WC}	70		85		100		120		ns
Address valid to end of write	t_{AW}	65		75		80		100		ns
Address setup time	t_{AS}	0		0		0		0		ns
Write pulse width	t_{WP}	50		50		60		70		ns
$\overline{\text{CE}}$ setup time	t_{CW}	65		75		80		100		ns
Write recovery time ($\overline{\text{WE}}$)	t_{WR}	0		0		0		0		ns
Write recovery time ($\overline{\text{CE}}$)	t_{WR1}	0		0		0		0		ns
Data setup time	t_{DS}	30		30		35		40		ns
Data hold time	t_{DH}	0		0		0		0		ns
$\overline{\text{WE}}$ output enable time	t_{WOE}	10		10		10		10		ns
$\overline{\text{WE}}$ output disable time	t_{WOD}	0	25	0	25	0	25	0	25	ns

Timing Chart

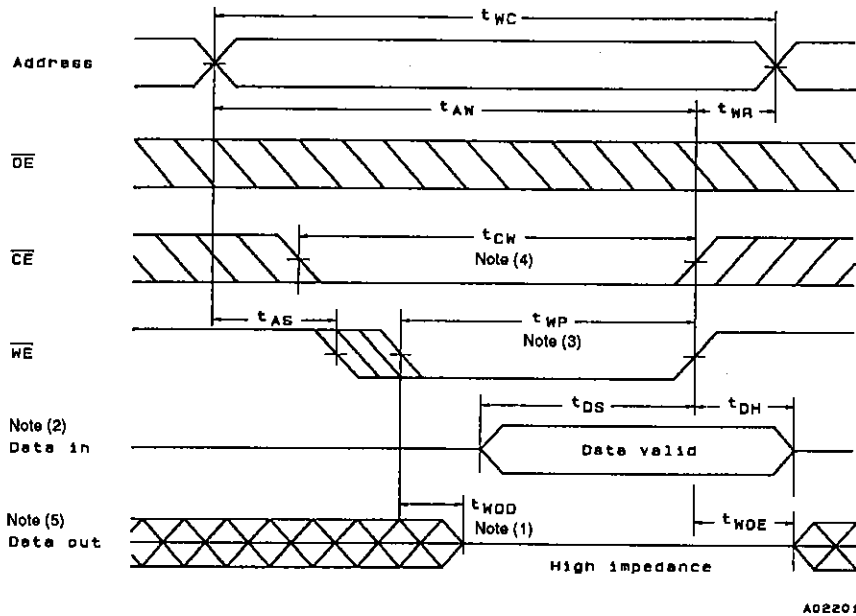
- Read Cycle (1): $\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$



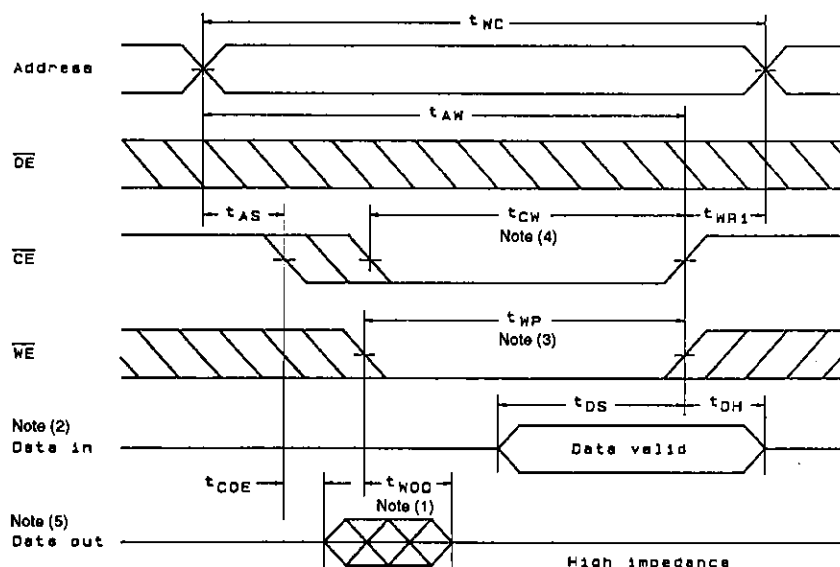
- Read Cycle (2): $\overline{WE} = V_{IH}$



- Write Cycle (1): \overline{WE} Control Note (6)



• Write Cycle (2): \overline{CE} Control Note (6)



A02202

- Notes: (1) t_{COD} , t_{OOD} , and t_{WOD} are defined as the time at which the outputs becomes the high impedance state and are not referred to output voltage levels.
- (2) An external antiphase signal must not be applied when D_{OUT} is in the output state.
- (3) t_{WP} is the time interval that \overline{CE} and \overline{WE} are low-level and is defined as the interval from the falling of \overline{WE} to the rising of \overline{CE} or \overline{WE} whichever is earlier.
- (4) t_{CW} is the time interval that \overline{CE} and \overline{WE} are low-level and is defined as the time from the falling of \overline{CE} to the rising of \overline{CE} or \overline{WE} , whichever is earlier.
- (5) D_{OUT} goes to the high-impedance state when either \overline{OE} is high-level, \overline{CE} is high-level, or \overline{WE} is low-level.
- (6) When \overline{OE} is high-level during the write cycle, D_{OUT} goes to the high-impedance state.

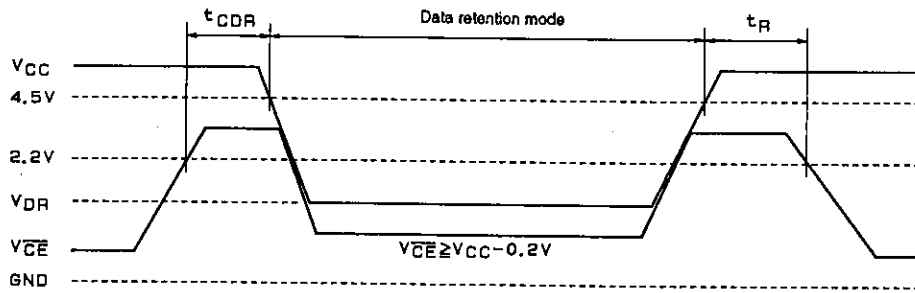
Data Retention Characteristics at $T_a = -10$ to $+70^\circ\text{C}$

Parameter	Symbol	Conditions	min	typ*1	max	Unit
Data retention supply voltage	V_{DR}	$V_{\overline{CE}} \geq V_{CC} - 0.2\text{ V}$	2.0		5.5	V
Data retention supply current	I_{CCDR1}	$V_{CC} = 3.0\text{ V}, V_{\overline{CE}} \geq 2.8\text{ V}$	-10 to $+70^\circ\text{C}$		3	μA
			-10 to $+40^\circ\text{C}$		0.6	
			25 $^\circ\text{C}$	0.1	0.9	
	I_{CCDR2}	$V_{CC} = 2.0$ to $5.5\text{ V}, V_{\overline{CE}} \geq V_{CC} - 0.2\text{ V}$		0.2	5	μA
\overline{CE} setup time	t_{CDR}		0			ns
\overline{CE} hold time	t_H		t_{RC} *2			ns

* 1. Reference values at $V_{CC} = 5\text{ V}, T_a = 25^\circ\text{C}$

* 2. t_{RC} = Read Cycle time

Data Retention Waveform



A01788

- No products described or contained herein are intended for use in surgical implants, life-support systems, aerospace equipment, nuclear power control systems, vehicles, disaster/crime-prevention equipment and the like, the failure of which may directly or indirectly cause injury, death or property loss.
- Anyone purchasing any products described or contained herein for an above-mentioned use shall:
 - ① Accept full responsibility and indemnify and defend SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors and all their officers and employees, jointly and severally, against any and all claims and litigation and all damages, cost and expenses associated with such use;
 - ② Not impose any responsibility for any fault or negligence which may be cited in any such claim or litigation on SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors or any of their officers and employees jointly or severally.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.