DATA SHEET

NEC

Compound Field Effect Power Transistor

μPA1572B

N-CHANNEL POWER MOS FET ARRAY
SWITCHING
INDUSTRIAL USE

DESCRIPTION

The μPA1572B is N-channel Power MOS FET Array that built in 4 circuits designed for solenoid, motor and lamp driver.

FEATURES

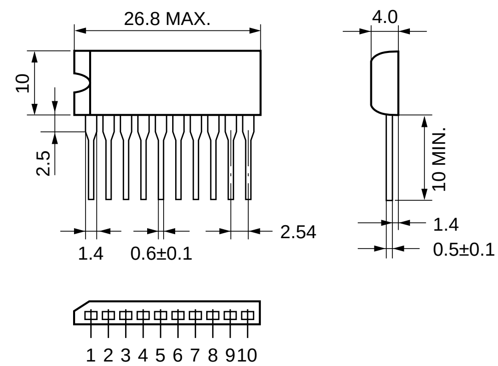
- Full Mold Package with 4 Circuits
- 4 V driving is possible
- Low On-state Resistance
  $R_{DS(on)}$ = 0.6 Ω MAX. (V_{GS} = 10 V, I_D = 1 A)
  $R_{DS(on)}$ = 0.8 Ω MAX. (V_{GS} = 4 V, I_D = 1 A)
- Low Input Capacitance Ciss = 110 pF TYP.

ORDERING INFORMATION

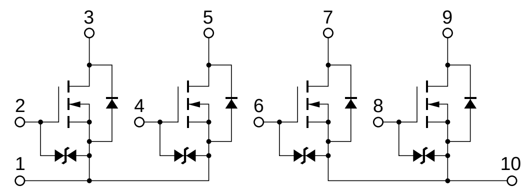
Type Number	Package
μPA1572BH	10Pin SIP

PACKAGE DIMENSIONS

in millimeters



CONNECTION DIAGRAM



ELECTRODE CONNECTION
2, 4, 6, 8 : Gate
3, 5, 7, 9 : Drain
1, 10 : Source

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Drain to Source Voltage (V_{GS} = 0)	V_{DSS}	60	V
Gate to Source Voltage (V_{DS} = 0)	$V_{GSS\ (AC)}$	±20	V
Drain Current (DC)	$I_{D\ (DS)}$	±2.0	A/unit
Drain Current (pulse)	$I_{D\ (pulse)}$ *1	±6.0	A/unit
Total Power Dissipation	P_{T1} *2	20	W
Total Power Dissipation	P_{T2} *3	3.0	W
Channel Temperature	T_{CH}	150	°C
Storage Tempreature	T_{stg}	–55 to +150	°C
Single Avalanche Current	I_{AS} *4	5.0	A
Single Avalanche Energy	E_{AS} *4	0.1	mJ

*1 PW ≤ 10 μs, Duty Cycle ≤ 1 %
*2 4 Circuits T_C = 25 °C
*3 4 Circuits T_A = 25 °C
*4 Starting T_{CH} = 25 °C, V_{DD} = 30 V, V_{GS} = 20 V → 0, R_G = 25 Ω, L = 100 μH

Build-in Gate Diodes are for protection from static electricity in handing.
In case high voltage over V_{GSS} is applied, please append gate protection circuits.

The information in this document is subject to change without notice.

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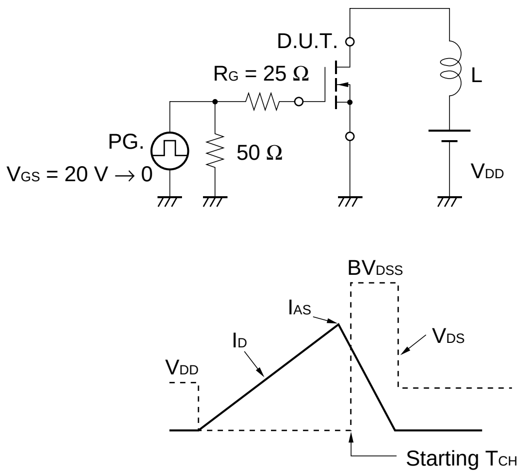
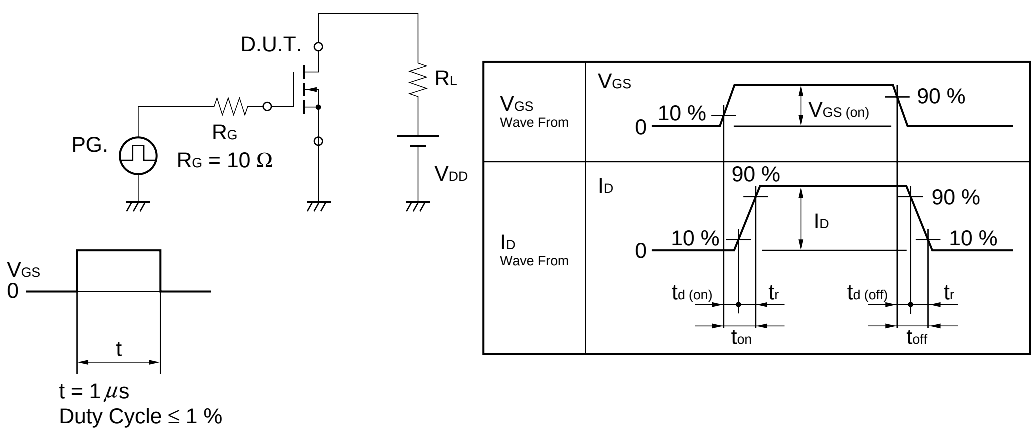
ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Drain Leakage Current	I_{DSS}			10	μA	V_{DS} = 60 V, V_{GS} = 0
Gate Leakage Current	I_{GSS}			±10	μA	V_{GS} = ±20 V, V_{DS} = 0
Gate Cutoff Voltage	$V_{GS\ (off)}$	1.0		2.0	V	V_{DS} = 10 V, I_D = 1.0 mA
Forward Transfer Admittance	$\lvert Y_{fs} \rvert$	0.5			S	V_{DS} = 10 V, I_D = 1.0 A
Drain to Source ON-Resistance	$R_{DS\ (on)1}$		0.3	0.6	Ω	V_{GS} = 10 V, I_D = 1.0 A
Drain to Sourse ON-Resistance	$R_{DS\ (on)2}$		0.4	0.8	Ω	V_{GS} = 4.0 V, I_D = 1.0 A
Input Capacitance	C_{iss}		110		pF	V_{DS} = 10 V, V_{GS} = 0, f = 1.0 MHz
Output Capacitance	C_{oss}		70		pF	
Reverse Transfer Capacitance	C_{rss}		25		pF	
Turn-on Delay Time	$t_{d\ (on)}$		30		ns	I_D = 1.0 A, $V_{GS\ (on)}$ = 10 V, V_{DD} = 30 V, R_L = 30 Ω
Rise Time	t_r		200		ns	
Turn-off Delay Time	$t_{d\ (off)}$		100		ns	
Fall Time	t_f		160		ns	
Total Gate Charge	Q_G		5.4		nC	V_{GS} = 10 V, I_D = 2.0 A, V_{DD} = 48 V
Gate to Source Charge	Q_{GS}		0.7		nC	
Gate to Drain Charge	Q_{GD}		2.0		nC	
Body Diode Forward Voltage	$V_{F\ (S-D)}$		1.0		V	I_F = 2.0 A, V_{GS} = 0
Reverse Recovery Time	t_{rr}		130		ns	I_F = 2.0 A, V_{GS} = 0, di/dt = 50 A/μs
Reverse Recovery Charge	Q_{rr}		110		nC	

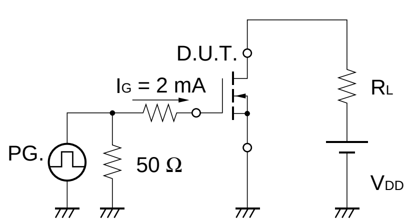
Test Circuit 1 Avalanche Capability



Test Circuit 2 Switching Time

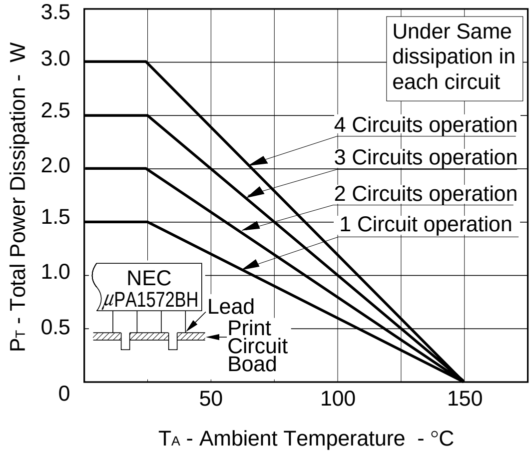


Test Circuit 3 Gate Charge

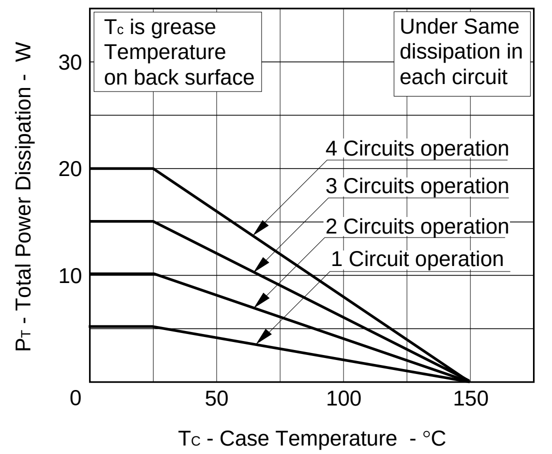


CHARACTERISTICS (T_A = 25 °C)

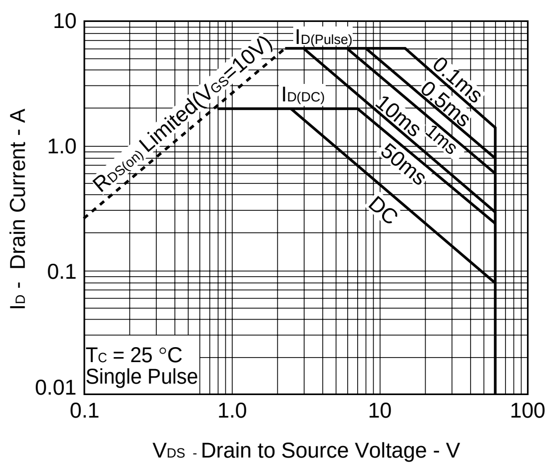
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



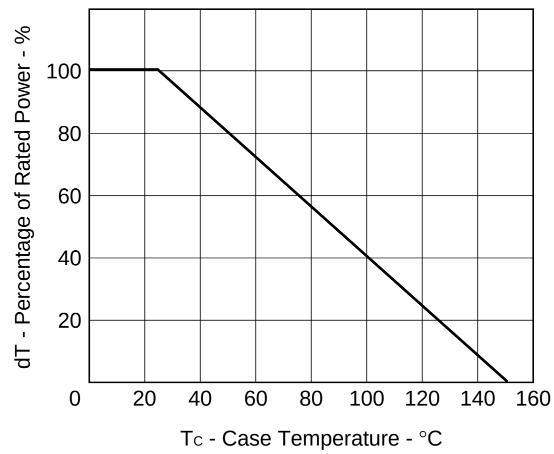
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



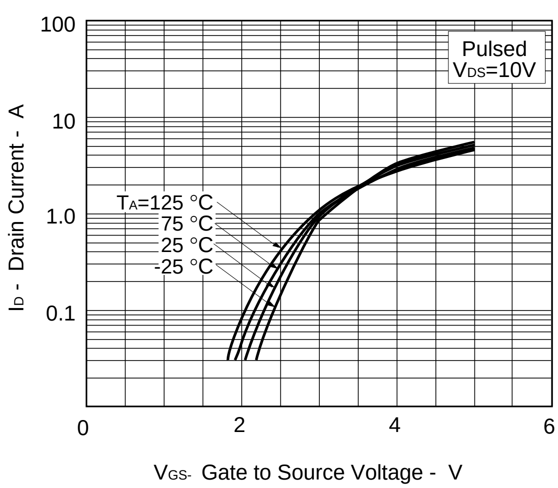
FORWARD BIAS SAFE OPERATING AREA



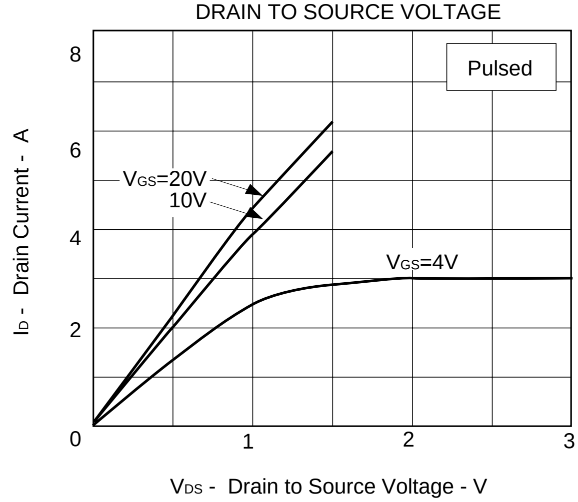
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



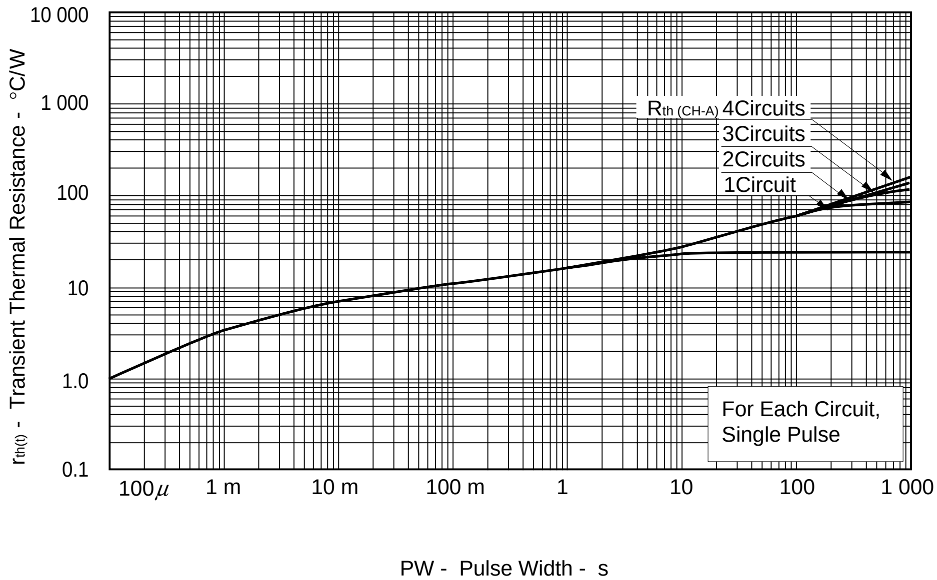
FORWARD TRANSFER CHARACTERISTICS



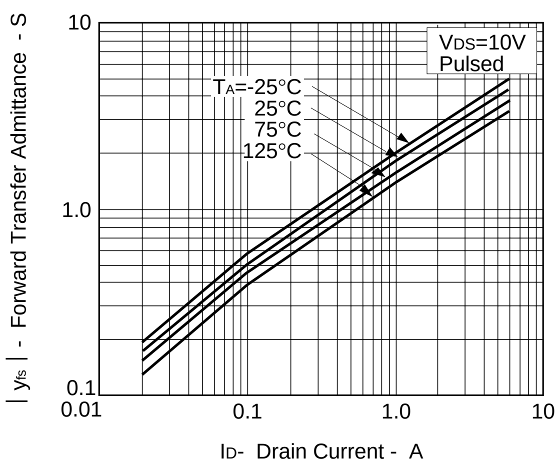
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



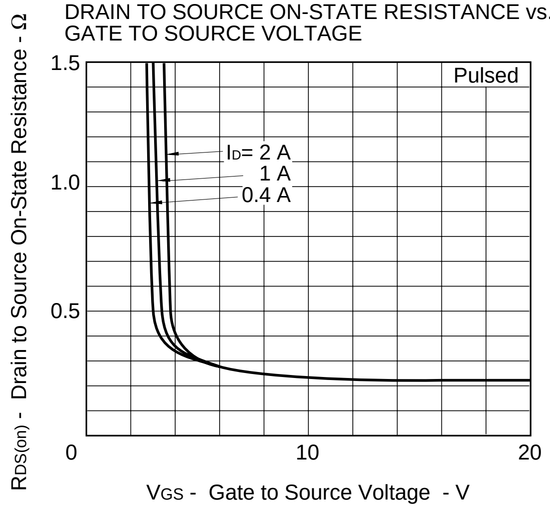
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



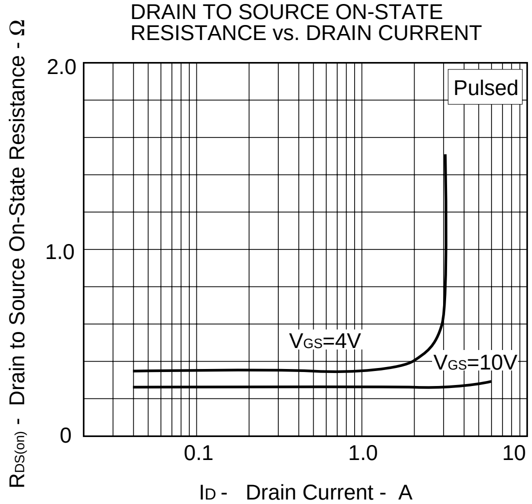
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



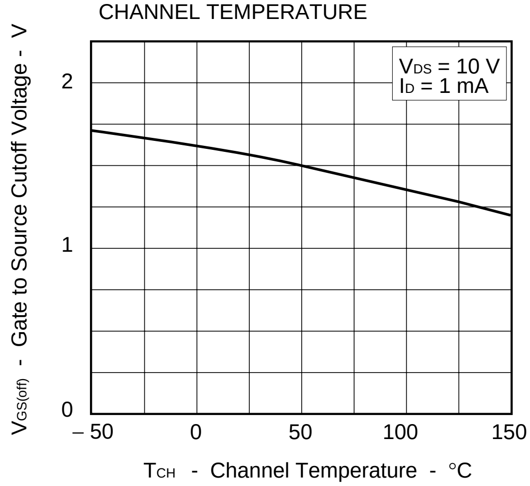
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



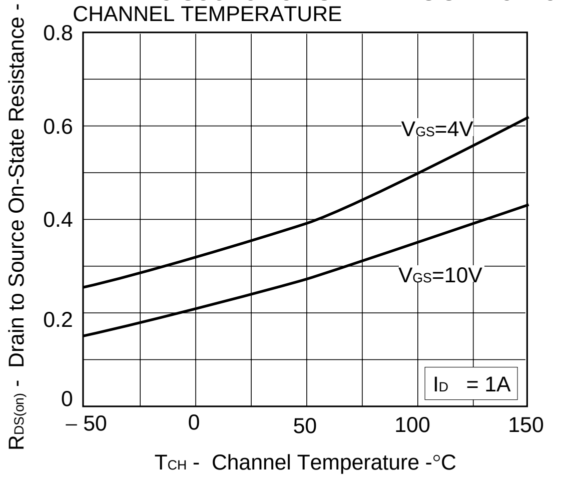
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



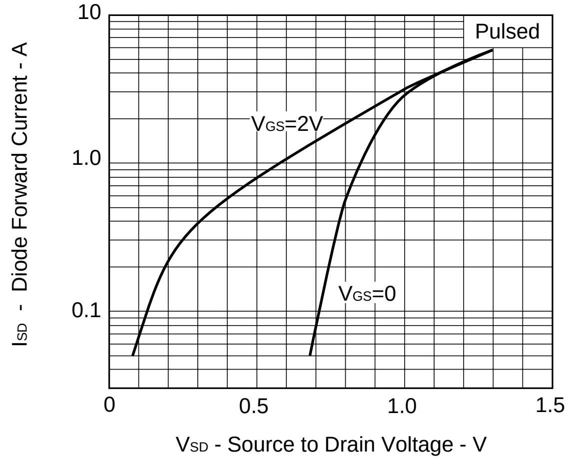
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



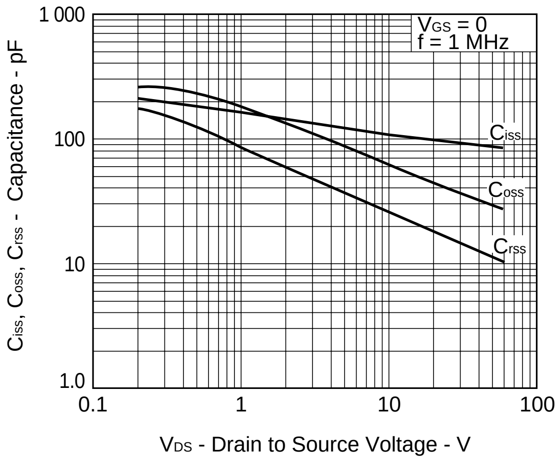
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



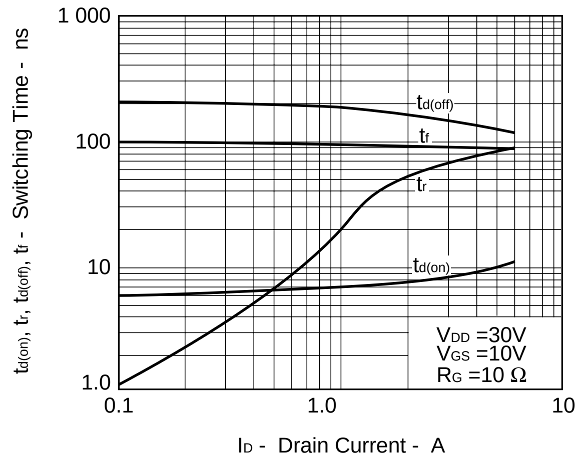
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



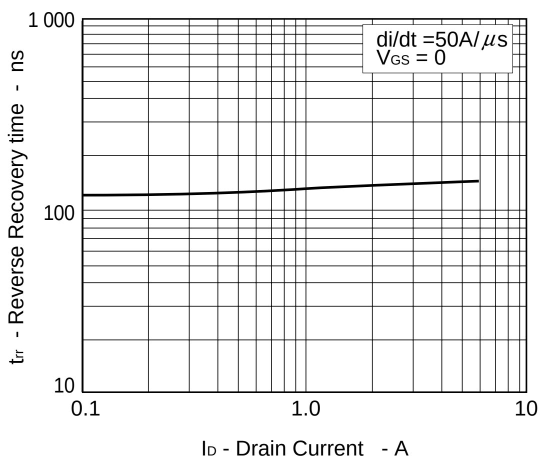
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



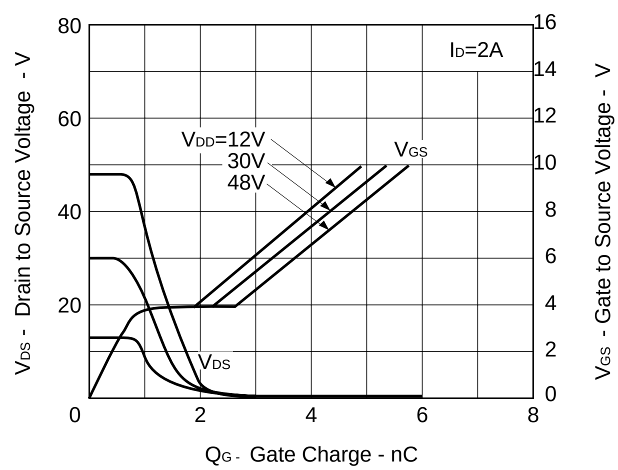
SWITCHING CHARACTERISTICS

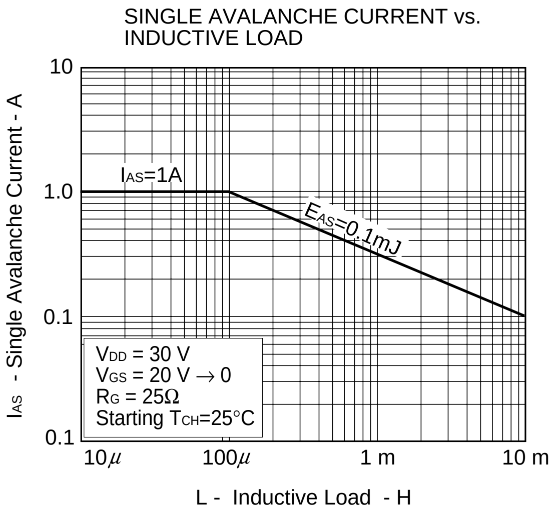


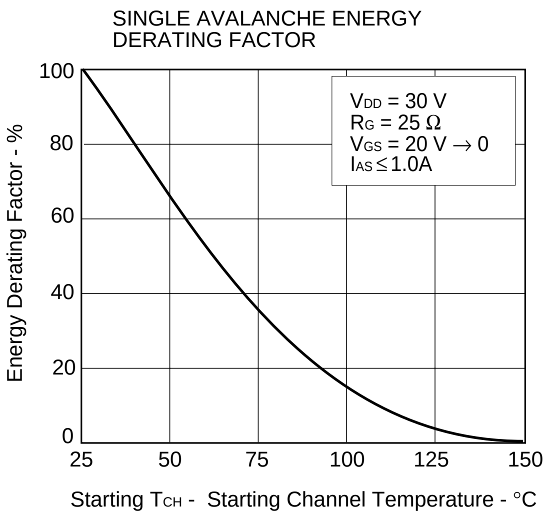
REVERSE RECOVERY TIME vs. DRAIN CURRENT



DYNAMIC INPUT/OUTPUT CHARACTERISTICS







REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system	TEI-1202
Quality grade on NEC semiconductor devices	IEI-1209
Semiconductor device mounting technology manual	C10535E
Semiconductor device package manual	C10943X
Guide to quality assurance for semiconductor devices	MEI-1202
Semiconductor selection guide	X10679E
Power MOS FET features and application switching power supply	TEA-1034
Application circuits using Power MOS FET	TEA-1035
Safe operating area of Power MOS FET	TEA-1037