HD74ALVCH162270

12-bit to 24-bit Registered Bus Exchanger with 3-state Outputs

HITACHI

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Description

The HD74ALVCH162270 is used in applications where data must be transferred from a narrow high speed bus to a wide lower frequency bus. The device provides synchronous data exchange between the two ports. Data is stored in the internal registers on the low to high transition of the clock (CLK) input when the appropriate $\overline{\text{CLKEN}}$ inputs are low. The select ($\overline{\text{SEL}}$) line selects 1B or 2B data for the A outputs. For data transfer in the A to B direction, a two stage pipeline is provided in the A to 1B path, with a single storage register in the A to 2B path. Proper control of the $\overline{\text{CLKENA}}$ inputs allows two sequential 12-bit words to be presented synchronously as a 24-bit word on the B port. Data flow is controlled by the active low output enables ($\overline{\text{OEA}}$, $\overline{\text{OEB}}$). The control terminals are registered to synchronize the bus direction changes with CLK. Active bus hold circuitry is provided to hold unused or floating data inputs at a valid logic level. All outputs, which are designed to sink up to 12 mA, include 26 Ω resistors to reduce overshoot and undershoot.

Features

- V_{CC} = 2.3 V to 3.6 V
- Typical V_{OL} ground bounce < 0.8 V (@V_{CC} = 3.3 V, Ta = 25°C)
- Typical V_{OH} undershoot > 2.0 V (@V_{CC} = 3.3 V, Ta = 25°C)
- High output current ±12 mA (@V_{CC} = 3.0 V)
- Bus hold on data inputs eliminates the need for external pullup / pulldown resistors
- All outputs have equivalent 26 Ω series resistors, so no external resistors are required.

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Function Table

Inputs			Outputs	
CLK	**$\overline{OEA}$**	**$\overline{OEB}$**	**A**	**1B, 2B**
↑	H	H	Z	Z
↑	H	L	Z	Active
↑	L	H	Active	Z
↑	L	L	Active	Active

Output enable

Inputs				Outputs	
$\overline{CLKENA1}$	**$\overline{CLKENA2}$**	**CLK**	**A**	**1B**	**2B**
X	H	↑	L	$1B_0$ *1, 2	$2B_0$ *1
X	H	↑	H	$1B_0$ *1, 2	$2B_0$ *1
L	L	↑	L	L *2	L
L	L	↑	H	H *2	H
H	L	↑	L	$1B_0$ *1	L
H	L	↑	H	$1B_0$ *1	H
H	H	X	X	$1B_0$ *1	$2B_0$ *1

A-to-B storage ($\overline{OEB}$ = L)

Note: This functional table describes the case of transferring the same data for A to 1B path. For the case of transferring different data, see logic diagrams.

Inputs						Output A
$\overline{\text{CLKEN1B}}$	$\overline{\text{CLKEN2B}}$	CLK	$\overline{\text{SEL}}$	1B	2B	
H	X	X	H	X	X	A_0 *1
X	H	X	L	X	X	A_0 *1
L	X	↑	H	L	X	L
L	X	↑	H	H	X	H
X	L	↑	L	X	L	L
X	L	↑	L	X	H	H

B-to-A storage ($\overline{\text{OEA}}$ = L)

H : High level

L : Low level

X : Immaterial

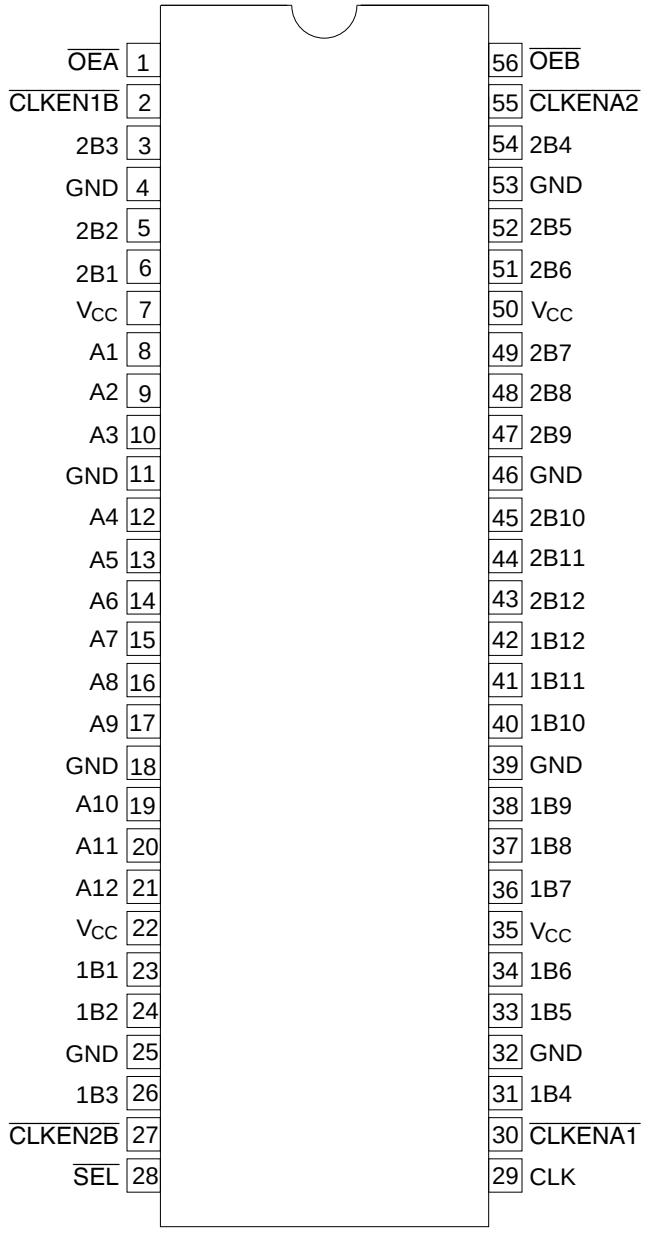
Z : High impedance

↑ : Low to high transition

Notes: 1. Output level before the indicated steady state input conditions were established.

2. Two CLK edges are needed to propagate data.

Pin Arrangement



(Top view)

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	–0.5 to 4.6	V	
Input voltage [*1, 2]	V_I	–0.5 to 4.6	V	Except I/O ports
		–0.5 to V_{CC} +0.5		I/O ports
Output voltage [*1, 2]	V_O	–0.5 to V_{CC} +0.5	V	
Input clamp current	I_{IK}	–50	mA	$V_I < 0$
Output clamp current	I_{OK}	±50	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	I_O	±50	mA	V_O = 0 to V_{CC}
V_{CC}, GND current / pin	I_{CC} or I_{GND}	±100	mA	
Maximum power dissipation at Ta = 55°C (in still air) [*3]	P_T	1	W	TSSOP
Storage temperature	Tstg	–65 to 150	°C	

Notes: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

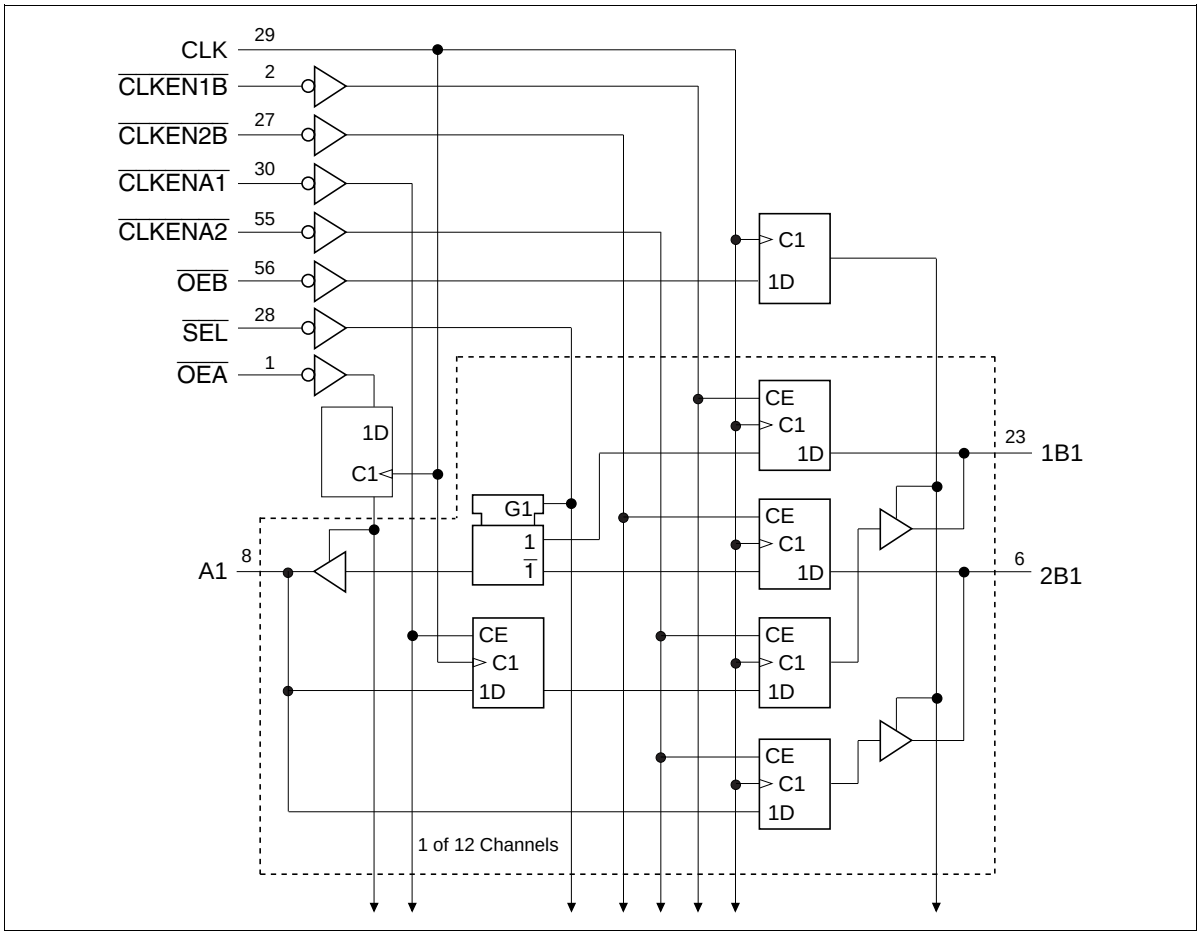
1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

Recommended Operating Conditions

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage	V_{CC}	2.3	3.6	V	
Input voltage	V_I	0	V_{CC}	V	
Output voltage	V_O	0	V_{CC}	V	
High level output current	I_{OH}	—	–6	mA	V_{CC} = 2.3 V
		—	–8		V_{CC} = 2.7 V
		—	–12		V_{CC} = 3.0 V
Low level output current	I_{OL}	—	6	mA	V_{CC} = 2.3 V
		—	8		V_{CC} = 2.7 V
		—	12		V_{CC} = 3.0 V
Input transition rise or fall rate	$\Delta t / \Delta v$	0	10	ns / V	
Operating temperature	Ta	–40	85	°C	

Note: Unused control inputs must be held high or low to prevent them from floating.

Logic Diagram



Electrical Characteristics (Ta = –40 to 85°C)

Item	Symbol	V_{CC} (V)	Min	Max	Unit	Test Conditions
Input voltage	V_{IH}	2.3 to 2.7	1.7	—	V	
		2.7 to 3.6	2.0	—		
	V_{IL}	2.3 to 2.7	—	0.7		
		2.7 to 3.6	—	0.8		
Output voltage	V_{OH}	2.3 to 3.6	V_{CC}–0.2	—	V	I_{OH} = –100 µA
		2.3	1.9	—		I_{OH} = –4 mA, V_{IH} = 1.7 V
		2.3	1.7	—		I_{OH} = –6 mA, V_{IH} = 1.7 V
		3.0	2.4	—		I_{OH} = –6 mA, V_{IH} = 2.0 V
		2.7	2.0	—		I_{OH} = –8 mA, V_{IH} = 2.0 V
		3.0	2.0	—		I_{OH} = –12 mA, V_{IH} = 2.0 V
	V_{OL}	2.3 to 3.6	—	0.2		I_{OL} = 100 µA
		2.3	—	0.4		I_{OL} = 4 mA, V_{IL} = 0.7 V
		2.3	—	0.55		I_{OL} = 6 mA, V_{IL} = 0.7 V
		3.0	—	0.55		I_{OL} = 6 mA, V_{IL} = 0.8 V
		2.7	—	0.6		I_{OL} = 8 mA, V_{IL} = 0.8 V
		3.0	—	0.8		I_{OL} = 12 mA, V_{IL} = 0.8 V
Input current	I_{IN}	3.6	—	±5	µA	V_{IN} = V_{CC} or GND
	$I_{IN\ (hold)}$	2.3	45	—		V_{IN} = 0.7 V
		2.3	–45	—		V_{IN} = 1.7 V
		3.0	75	—		V_{IN} = 0.8 V
		3.0	–75	—		V_{IN} = 2.0 V
		3.6	—	±500		V_{IN} = 0 to 3.6 V [*1]
Off state output current	I_{OZ}	3.6	—	±10	µA	V_{OUT} = V_{CC} or GND
Quiescent supply current	I_{CC}	3.6	—	40	µA	V_{IN} = V_{CC} or GND
	ΔI_{CC}	3.0 to 3.6	—	750	µA	V_{IN} = one input at (V_{CC}–0.6) V, other inputs at V_{CC} or GND

Note: 1. This is the bus hold maximum dynamic current required to switch the input from one state to another.

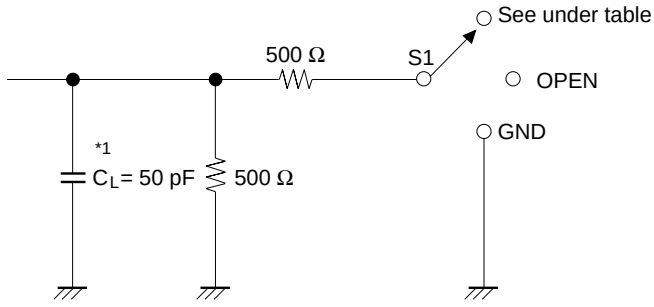
Switching Characteristics (Ta = –40 to 85°C)

Item	Symbol	V_{cc} (V)	Min	Typ	Max	Unit	FROM (Input)	TO (Output)
Maximum clock frequency	f_{max}	2.5±0.2	135	—	—	MHz		
		2.7	135	—	—			
		3.3±0.3	135	—	—			
Propagation delay time	t_{PLH}	2.5±0.2	2.5	—	6.9	ns	CLK	B
	t_{PHL}	2.7	—	—	6.4			
		3.3±0.3	1.7	—	5.6			
		2.5±0.2	2.2	—	6.4		CLK	A
		2.7	—	—	6.0			
		3.3±0.3	1.6	—	5.2			
		2.5±0.2	2.4	—	7.2		$\overline{SEL}$	A
		2.7	—	—	7.0			
		3.3±0.3	1.6	—	6.0			
Output enable time	t_{ZH}	2.5±0.2	2.1	—	7.9	ns	CLK	A or B
	t_{ZL}	2.7	—	—	7.4			
		3.3±0.3	1.6	—	6.5			
Output disable time	t_{HZ}	2.5±0.2	3.0	—	7.8	ns	CLK	A or B
	t_{LZ}	2.7	—	—	7.1			
		3.3±0.3	1.7	—	6.2			
Input capacitance	C_{IN}	3.3	—	3.5	—	pF	Control inputs	
Output capacitance	$C_{IN/O}$	3.3	—	9.0	—	pF	A or B ports	

Switching Characteristics (Ta = –40 to 85°C) (cont)

Item	Symbol	V_{cc} (V)	Min	Typ	Max	Unit	FROM (Input)
Setup time	t_{su}	2.5±0.2	4.1	—	—	ns	A data before CLK↑
		2.7	3.8	—	—		
		3.3±0.3	3.1	—	—		
		2.5±0.2	0.9	—	—		B data before CLK↑
		2.7	1.2	—	—		
		3.3±0.3	0.9	—	—		
		2.5±0.2	3.5	—	—		$\overline{\text{CLKENA1}}$ or
		2.7	3.2	—	—		$\overline{\text{CLKENA2}}$ before CLK↑
		3.3±0.3	2.7	—	—		
		2.5±0.2	3.4	—	—		$\overline{\text{CLKEN1B}}$ or
		2.7	3.0	—	—		$\overline{\text{CLKEN2B}}$ before CLK↑
		3.3±0.3	2.6	—	—		
		2.5±0.2	4.4	—	—		$\overline{\text{OE}}$ before CLK↑
		2.7	3.9	—	—		
		3.3±0.3	3.2	—	—		
Hold time	t_h	2.5±0.2	0	—	—	ns	A data after CLK↑
		2.7	0	—	—		
		3.3±0.3	0.2	—	—		
		2.5±0.2	1.4	—	—		B data after CLK↑
		2.7	1.0	—	—		
		3.3±0.3	1.7	—	—		
		2.5±0.2	0	—	—		$\overline{\text{CLKENA1}}$ or
		2.7	0.1	—	—		$\overline{\text{CLKENA2}}$ after CLK↑
		3.3±0.3	0.3	—	—		
		2.5±0.2	0	—	—		$\overline{\text{CLKEN1B}}$ or
		2.7	0	—	—		$\overline{\text{CLKEN2B}}$ after CLK↑
		3.3±0.3	0.6	—	—		
		2.5±0.2	0	—	—		$\overline{\text{OE}}$ after CLK↑
		2.7	0	—	—		
		3.3±0.3	0.1	—	—		
Pulse width	t_w	2.5±0.2	3.3	—	—	ns	CLK “H” or “L”
		2.7	3.3	—	—		
		3.3±0.3	3.3	—	—		

• **Test Circuit**

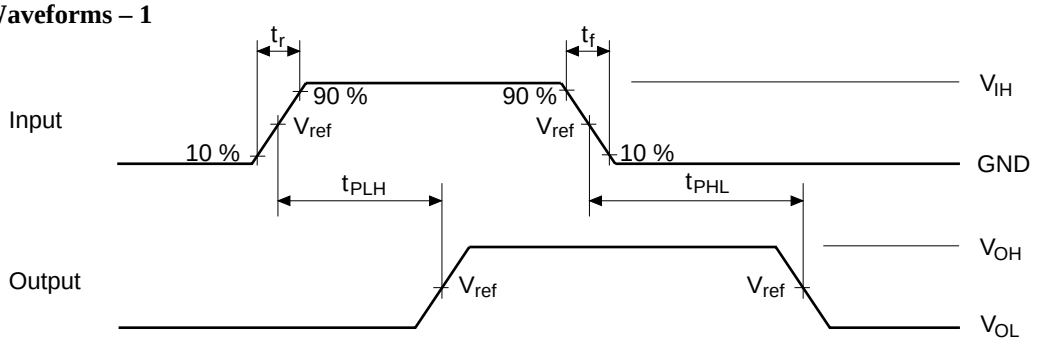


Load Circuit for Outputs

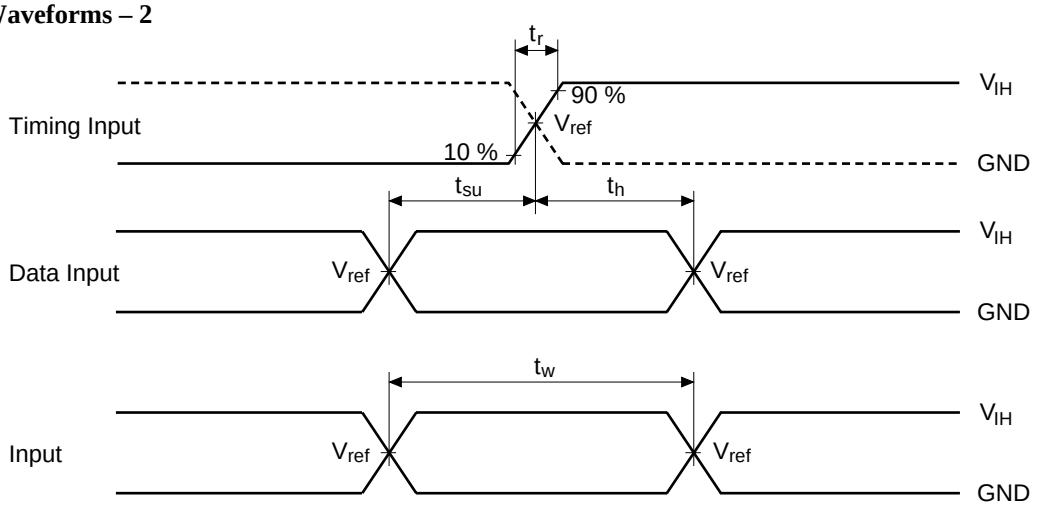
Symbol	Vcc=2.5±0.2V	Vcc=2.7V, 3.3±0.3V
t_{PLH} / t_{PHL}	OPEN	OPEN
t_{su} / t_h / t_w		
t_{ZH} / t_{HZ}	GND	GND
t_{ZL} / t_{LZ}	4.6 V	6.0 V

Note: 1. C_L includes probe and jig capacitance.

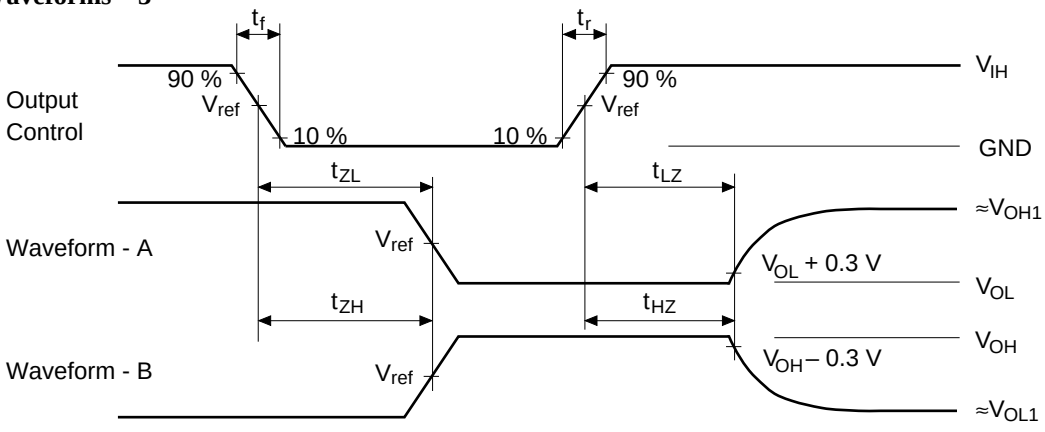
• **Waveforms – 1**



• **Waveforms – 2**



• **Waveforms – 3**

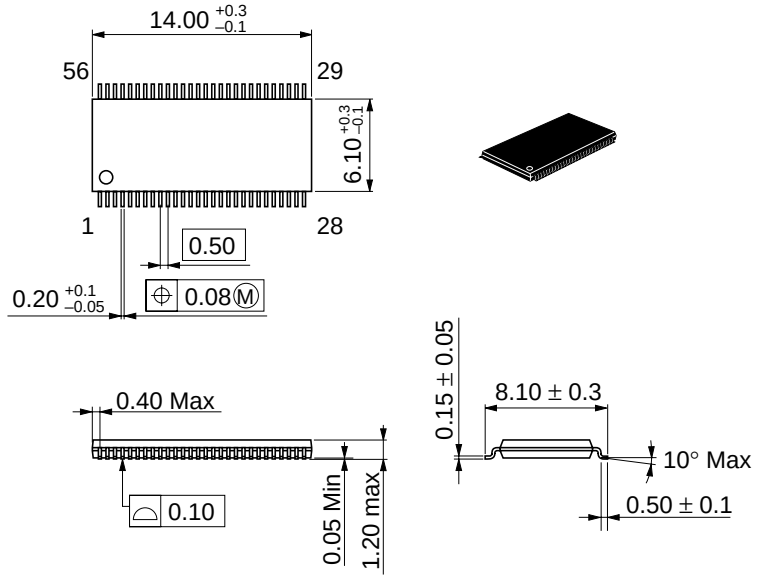


TEST	Vcc=2.5±0.2V	Vcc=2.7V, 3.3±0.3V
V_{IH}	2.3 V	2.7 V
V_{ref}	1.2 V	1.5 V
V_{OH1}	2.3 V	3.0 V
V_{OL1}	GND	GND

Notes: 1. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Zo = 50 Ω, tr ≤ 2.5 ns, tf ≤ 2.5 ns.
2. Waveform – A is for an output with internal conditions such that the output is low except when disabled by the output control.
3. Waveform – B is for an output with internal conditions such that the output is high except when disabled by the output control.
4. The output are measured one at a time with one transition per measurement.

Package Dimensions

Unit : mm



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