HD74ALVC16334

16-bit Universal Bus Driver with 3-state Outputs

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Description

This HD74ALVC16334 is a 16-bit universal bus driver is designed for 2.3 V to 3.6 V V_{CC} operation.

Data flow from A to Y is controlled by the output enable ($\overline{OE}$) input. The device operates in the transparent mode when the latch enable ($\overline{LE}$) input is low. When $\overline{LE}$ is high, the A data is latched if the clock (CLK) input is held at a high or low logic level. If $\overline{LE}$ is high, the A data is stored in the latch/flip flop on the low to high transition of CLK. When $\overline{OE}$ is high, the outputs are in the high impedance state.

To ensure the high impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current sinking capability of the driver.

Features

- V_{CC} = 2.3 V to 3.6 V

- Typical V_{OL} ground bounce < 0.8 V (@V_{CC} = 3.3 V, Ta = 25°C)

- Typical V_{OH} undershoot > 2.0 V (@V_{CC} = 3.3 V, Ta = 25°C)

- High output current ±24 mA (@V_{CC} = 3.0 V)

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Function Table

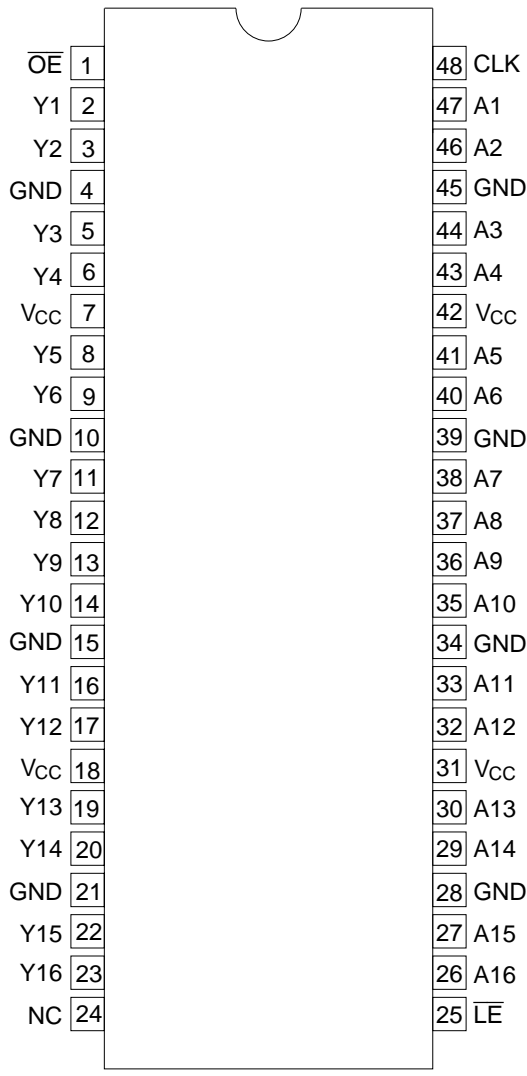| Inputs				Output Y
$\overline{OE}$	$\overline{LE}$	CLK	A	
H	X	X	X	Z
L	L	X	L	L
L	L	X	H	H
L	H	↑	L	L
L	H	↑	H	H
L	H	L or H	X	Y_0 [1]

H : High level

L : Low level

X : Immaterial

Z : High impedance

↑ : Low to high transition

Note: 1. Output level before the indicated steady state input conditions were established.

Pin Arrangement

Left	Pin		Pin	Right
$\overline{OE}$	1		48	CLK
Y1	2		47	A1
Y2	3		46	A2
GND	4		45	GND
Y3	5		44	A3
Y4	6		43	A4
V_{CC}	7		42	V_{CC}
Y5	8		41	A5
Y6	9		40	A6
GND	10		39	GND
Y7	11		38	A7
Y8	12		37	A8
Y9	13		36	A9
Y10	14		35	A10
GND	15		34	GND
Y11	16		33	A11
Y12	17		32	A12
V_{CC}	18		31	V_{CC}
Y13	19		30	A13
Y14	20		29	A14
GND	21		28	GND
Y15	22		27	A15
Y16	23		26	A16
NC	24		25	$\overline{LE}$

(Top view)

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	−0.5 to 4.6	V	
Input voltage [1]	V_I	−0.5 to 4.6	V	
Output voltage [1, 2]	V_O	−0.5 to V_{CC} +0.5	V	
Input clamp current	I_{IK}	−50	mA	$V_I < 0$
Output clamp current	I_{OK}	±50	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	I_O	±50	mA	$V_O = 0$ to V_{CC}
V_{CC}, GND current / pin	I_{CC} or I_{GND}	±100	mA	
Maximum power dissipation at Ta = 55°C (in still air) [3]	P_T	0.85	W	TSSOP
Storage temperature	T_{stg}	−65 to 150	°C	

Notes: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

Recommended Operating Conditions

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage	V_{CC}	2.3	3.6	V	
Input voltage	V_I	0	V_{CC}	V	
Output voltage	V_O	0	V_{CC}	V	
High level output current	I_{OH}	—	−12	mA	$V_{CC} = 2.3$ V
		—	−12		$V_{CC} = 2.7$ V
		—	−24		$V_{CC} = 3.0$ V
Low level output current	I_{OL}	—	12	mA	$V_{CC} = 2.3$ V
		—	12		$V_{CC} = 2.7$ V
		—	24		$V_{CC} = 3.0$ V
Input transition rise or fall rate	$\Delta t / \Delta v$	0	10	ns / V	
Operating temperature	T_a	−40	85	°C	

Note: Unused control inputs must be held high or low to prevent them from floating.

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Logic Diagram

To fifteen other channels
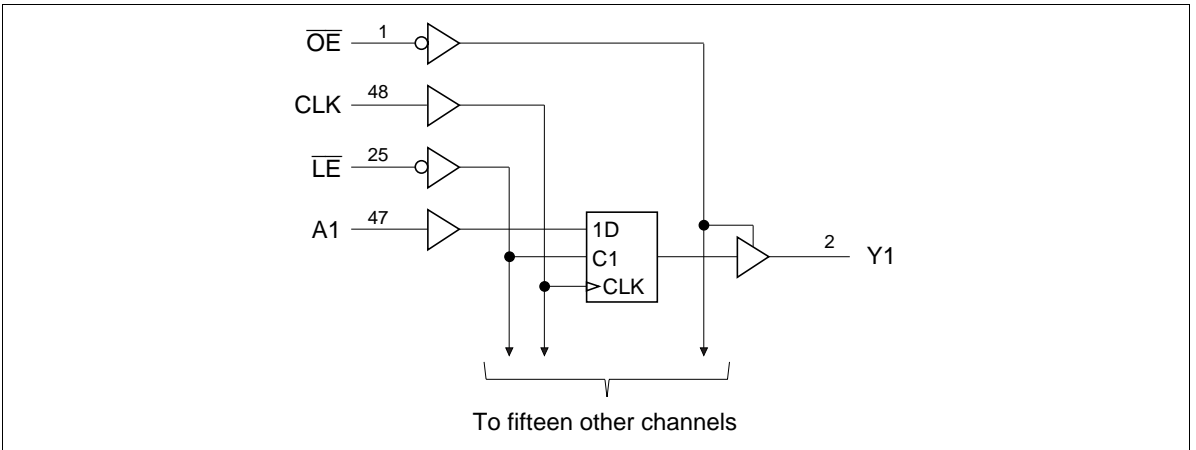
Electrical Characteristics (Ta = –40 to 85°C)

Item	Symbol	V_{cc} (V)	Min	Max	Unit	Test Conditions
Input voltage	V_{IH}	2.3 to 2.7	1.7	—	V	
		2.7 to 3.6	2.0	—		
	V_{IL}	2.3 to 2.7	—	0.7		
		2.7 to 3.6	—	0.8		
Output voltage	V_{OH}	2.3 to 3.6	V_{CC}–0.2	—	V	I_{OH} = −100 µA
		2.3	2.0	—		I_{OH} = −6 mA, V_{IH} = 1.7 V
		2.3	1.7	—		I_{OH} = −12 mA, V_{IH} = 1.7 V
		2.7	2.2	—		I_{OH} = −12 mA, V_{IH} = 2.0 V
		3.0	2.4	—		I_{OH} = −12 mA, V_{IH} = 2.0 V
		3.0	2.0	—		I_{OH} = −24 mA, V_{IH} = 2.0 V
	V_{OL}	2.3 to 3.6	—	0.2		I_{OL} = 100 µA
		2.3	—	0.4		I_{OL} = 6 mA, V_{IL} = 0.7 V
		2.3	—	0.7		I_{OL} = 12 mA, V_{IL} = 0.7 V
		2.7	—	0.4		I_{OL} = 12 mA, V_{IL} = 0.8 V
		3.0	—	0.55		I_{OL} = 24 mA, V_{IL} = 0.8 V
Input current	I_{IN}	3.6	—	±5	µA	V_{IN} = V_{CC} or GND
Off state output current	I_{OZ}	3.6	—	±10	µA	V_{OUT} = V_{CC} or GND
Quiescent supply current	I_{CC}	3.6	—	40	µA	V_{IN} = V_{CC} or GND
	ΔI_{CC}	3.0 to 3.6	—	750	µA	V_{IN} = one input at (V_{CC}–0.6) V, other inputs at V_{CC} or GND

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Switching Characteristics (Ta = –40 to 85°C)

Item	Symbol	V_{cc} (V)	Min	Typ	Max	Unit	FROM (Input)	TO (Output)
Maximum clock frequency	f_{max}	2.5±0.2	150	—	—	MHz		
		2.7	150	—	—			
		3.3±0.3	150	—	—			
Propagation delay time	t_{PLH}	2.5±0.2	1.0	—	3.7	ns	A	Y
	t_{PHL}	2.7	—	—	3.6			
		3.3±0.3	1.1	—	3.3			
		2.5±0.2	1.0	—	4.8		$\overline{LE}$	Y
		2.7	—	—	4.4			
		3.3±0.3	1.3	—	4.4			
		2.5±0.2	1.0	—	4.4		CLK	Y
		2.7	—	—	4.1			
		3.3±0.3	1.0	—	4.1			
Output enable time	t_{ZH}	2.5±0.2	1.0	—	5.4	ns	$\overline{OE}$	Y
	t_{ZL}	2.7	—	—	4.6			
		3.3±0.3	1.1	—	4.6			
Output disable time	t_{HZ}	2.5±0.2	1.0	—	4.1	ns	$\overline{OE}$	Y
	t_{LZ}	2.7	—	—	4.4			
		3.3±0.3	1.7	—	4.4			
Input capacitance	C_{IN}	3.3	—	5.5	—	pF	Control inputs	
		3.3	—	6.0	—		Data inputs	
Output capacitance	C_O	3.3	—	8.0	—	pF	Outputs	

Switching Characteristics (Ta = –40 to 85°C) (cont)

Item	Symbol	V_{cc} (V)	Min	Typ	Max	Unit	FROM (Input)
Setup time	t_{su}	2.5±0.2	1.4	—	—	ns	Data before CLK↑
		2.7	1.7	—	—		
		3.3±0.3	1.5	—	—		
		2.5±0.2	1.2	—	—		Data before $\overline{LE}$↑
		2.7	1.6	—	—		CLK "H"
		3.3±0.3	1.3	—	—		
		2.5±0.2	1.4	—	—		Data before $\overline{LE}$↑
		2.7	1.5	—	—		CLK "L"
		3.3±0.3	1.2	—	—		
Hold time	t_h	2.5±0.2	0.9	—	—	ns	Data after CLK↑
		2.7	0.8	—	—		
		3.3±0.3	0.9	—	—		
		2.5±0.2	1.2	—	—		Data after $\overline{LE}$↑
		2.7	1.1	—	—		CLK "H" or "L"
		3.3±0.3	1.1	—	—		
Pulse width	t_w	2.5±0.2	3.3	—	—	ns	$\overline{LE}$ "L"
		2.7	3.3	—	—		
		3.3±0.3	3.3	—	—		
		2.5±0.2	3.3	—	—		CLK "H" or "L"
		2.7	3.3	—	—		
		3.3±0.3	3.3	—	—		

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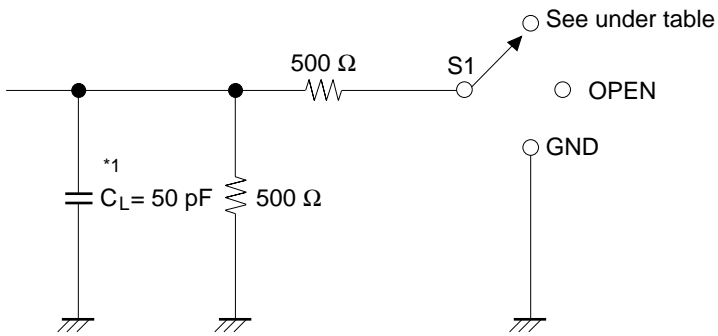
Test Circuit

Load Circuit for Outputs

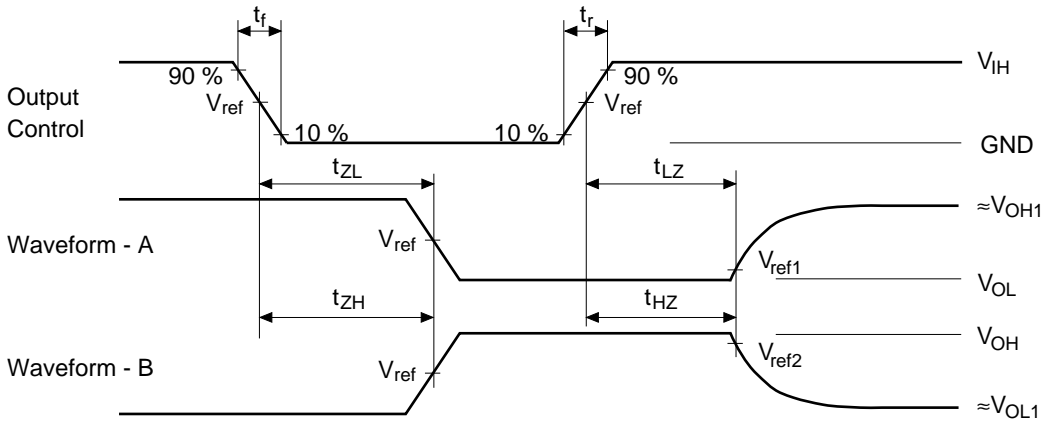| Symbol	Vcc=2.5±0.2V	Vcc=2.7V, 3.3±0.3V
t_{PLH}/t_{PHL} $t_{su}/t_h/t_w$	OPEN	OPEN
t_{ZH}/t_{HZ}	GND	GND
t_{ZL}/t_{LZ}	$2 \times V_{CC}$	6.0 V

Note: 1. C_L includes probe and jig capacitance.

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Waveforms – 1

Waveforms – 2

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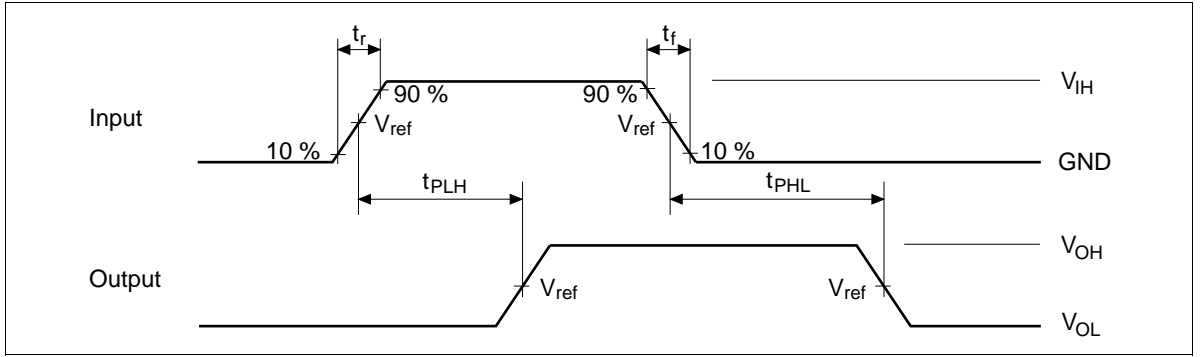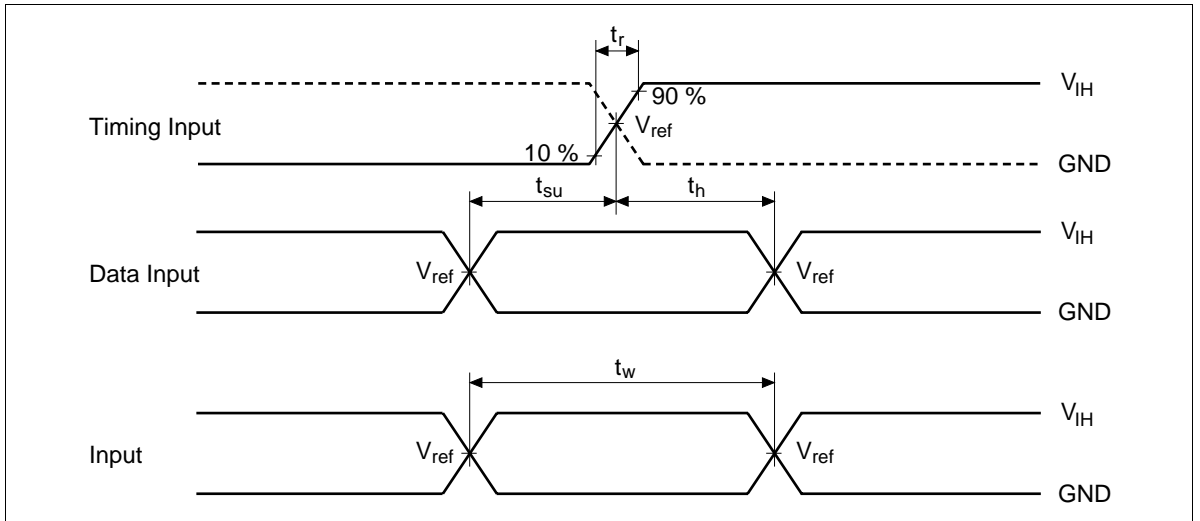
Waveforms – 3

TEST	Vcc=2.5±0.2V	Vcc=2.7V, 3.3±0.3V
V_{IH}	V_{CC}	2.7 V
V_{ref}	1/2 V_{CC}	1.5 V
V_{ref1}	V_{OL} +0.15 V	V_{OL} +0.3 V
V_{ref2}	V_{OH}−0.15 V	V_{OH}−0.3 V
V_{OH1}	V_{CC}	3.0 V
V_{OL1}	GND	GND

Notes: 1.   All input pulses are supplied by generators having the following characteristics :
PRR ≤ 10 MHz, Zo = 50 Ω, t_r ≤ 2.0 ns, t_f ≤ 2.0 ns. (V_{CC} = 2.5±0.2 V)
PRR ≤ 10 MHz, Zo = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns. (V_{CC} = 2.7 V, 3.3±0.3 V)

2.   Waveform – A is for an output with internal conditions such that the output is low except when disabled by the output control.

3.   Waveform – B is for an output with internal conditions such that the output is high except when disabled by the output control.

4.   The output are measured one at a time with one transition per measurement.

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Package Dimensions

Unit : mm
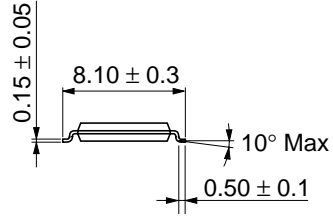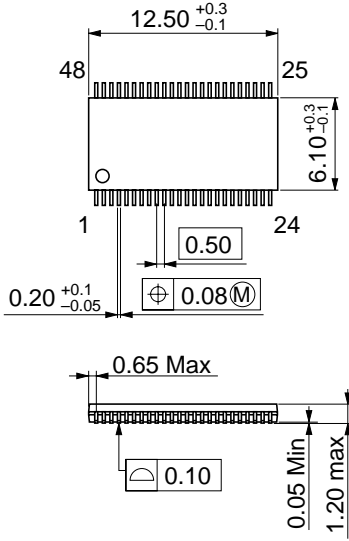
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