

HD14174B

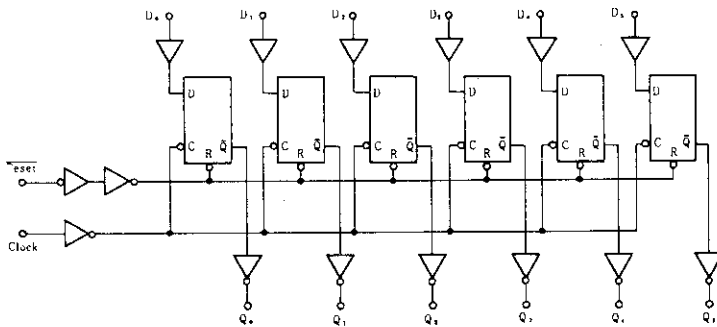
Hex D-type Flip Flop

The HD14174B is hex type D flip-flop. Data on the D inputs which meets the setup time requirements is transferred to the Q outputs on the positive edge of the clock pulse. All six flip-flops share common clock and reset inputs. The reset is active low, and independent of the clock.

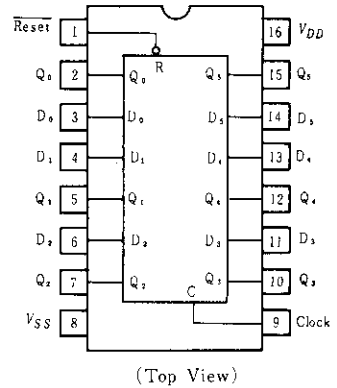
FEATURES

- Supply Voltage Range = 3 to 18V
- Noise Immunity = 45% of V_{DD} typ.
- Output Compatible with One Low-power Schottky TTL Load
- Functional Equivalent to TTL 74174

BLOCK DIAGRAM



PIN ARRANGEMENT

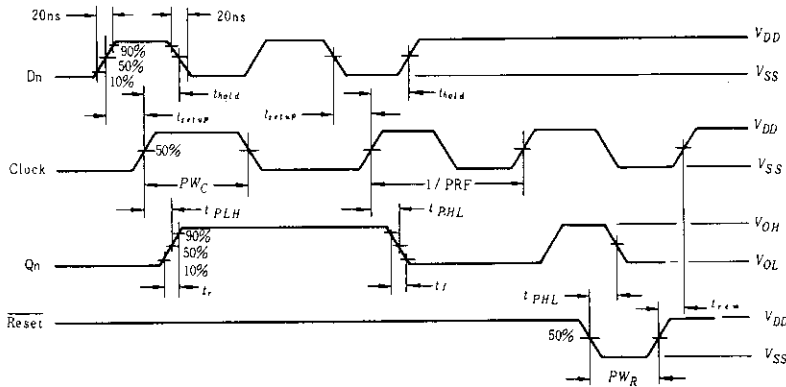


TRUTH TABLE

Inputs			Output
Clock	Data	Reset	Q
	0	1	0
	1	1	1
	X	1	Q
X	X	0	0

X = Don't Care

DYNAMIC SIGNAL WAVEFORMS



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions	-40°C		25°C			85°C		Unit	
			min	max	min	typ	max	min	max		
Output Voltage	V_{OL}	5.0	$V_{in} = V_{DD}$ or 0	—	0.05	—	0	0.05	—	0.05	V
		10		—	0.05	—	0	0.05	—	0.05	
		15		—	0.05	—	0	0.05	—	0.05	
	V_{OH}	5.0	$V_{in} = 0$ or V_{DD}	4.95	—	4.95	5.0	—	4.95	—	V
		10		9.95	—	9.95	10	—	9.95	—	
		15		14.95	—	14.95	15	—	14.95	—	
Input Voltage	V_{IL}	5.0	$V_{out} = 4.5$ or 0.5 V	—	1.5	—	2.25	1.5	—	1.5	V
		10	$V_{out} = 9.0$ or 1.0 V	—	3.0	—	4.50	3.0	—	3.0	
		15	$V_{out} = 13.5$ or 1.5 V	—	4.0	—	6.75	4.0	—	4.0	
	V_{IH}	5.0	$V_{out} = 0.5$ or 4.5 V	3.5	—	3.5	2.75	—	3.5	—	V
		10	$V_{out} = 1.0$ or 9.0 V	7.0	—	7.0	5.50	—	7.0	—	
		15	$V_{out} = 1.5$ or 13.5 V	11.0	—	11.0	8.25	—	11.0	—	
Output Drive Current	I_{OH}	5.0	$V_{OH} = 2.5$ V	-2.5	—	-2.1	-4.2	—	-1.7	—	mA
		5.0	$V_{OH} = 4.6$ V	-0.52	—	-0.44	-0.88	—	-0.36	—	
		10	$V_{OH} = 9.5$ V	-1.3	—	-1.1	-2.25	—	-0.9	—	
	15	$V_{OH} = 13.5$ V	-3.6	—	-3.0	-8.8	—	-2.4	—		
	I_{OL}	5.0	$V_{OL} = 0.4$ V	0.52	—	0.44	0.88	—	0.36	—	mA
		10	$V_{OL} = 0.5$ V	1.3	—	1.1	2.25	—	0.9	—	
15		$V_{OL} = 1.5$ V	3.6	—	3.0	8.8	—	2.4	—		
Input Current	I_{in}	15		—	± 0.3	—	± 0.00001	± 0.3	—	± 1.0	μ A
Input Capacitance	C_{in}		$V_{in} = 0$	—	—	—	5.0	7.5	—	—	pF
Quiescent Current	I_{DD}	5.0	Zero Signal, per Package	—	20	—	0.005	20	—	150	μ A
		10		—	40	—	0.010	40	—	300	
		15		—	80	—	0.015	80	—	600	
Total Supply Current*	I_T	5.0	Dynamic $+I_{DD}$, per Gate, $C_L = 50$ pF $f = 1$ kHz	—	—	—	1.1	—	—	—	μ A
		10		—	—	—	2.3	—	—	—	
		15		—	—	—	3.7	—	—	—	

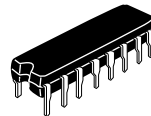
* To calculate total supply current at frequency other than 1kHz.

ⓐ $V_{DD} = 5.0$ V $I_T = (1.1 \mu\text{A}/\text{kHz})f - I_{in}$ ⓑ $V_{DD} = 10$ V $I_T = (2.3 \mu\text{A}/\text{kHz})f - I_{in}$ ⓒ $V_{DD} = 15$ V. $I_T = (3.7 \mu\text{A}/\text{kHz})f + I_{in}$

SWITCHING CHARACTERISTICS ($C_L=50\text{pF}$, $T_a=25^\circ\text{C}$)

Characteristic		Symbol	$V_{DD}(\text{V})$	min	typ	max	Unit
Output Rise and Fall Time		t_r, t_f	5.0	—	100	200	ns
			10	—	50	100	
			15	—	40	80	
Propagation Delay Time	Clock	t_{PLH} t_{PHL}	5.0	—	210	420	ns
			10	—	85	170	
			15	—	65	130	
	Reset	t_{PHL}	5.0	—	250	500	ns
			10	—	100	200	
			15	—	75	150	
Clock Pulse Width		PW_C	5.0	150	75	—	ns
			10	90	45	—	
			15	70	35	—	
Reset Pulse Width		PW_R	5.0	200	100	—	ns
			10	100	50	—	
			15	80	40	—	
Clock Frequency		PRF	5.0	—	7.0	2.0	MHz
			10	—	12.0	5.0	
			15	—	15.5	6.5	
Clock Pulse Rise and Fall Time		t_r, t_f	5.0	—	—	15	μs
			10	—	—	15	
			15	—	—	15	
Setup Time		t_{setup}	5.0	40	20	—	ns
			10	20	10	—	
			15	15	0	—	
Hold Time		t_{hold}	5.0	80	40	—	ns
			10	40	20	—	
			15	30	15	—	
Reset Removal Time		t_{rem}	5.0	250	125	—	ns
			10	100	50	—	
			15	80	40	—	

* The reset signal must be high prior to a positive-going transition of the clock.

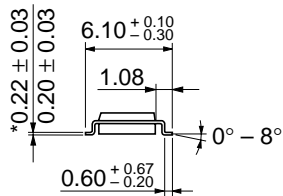
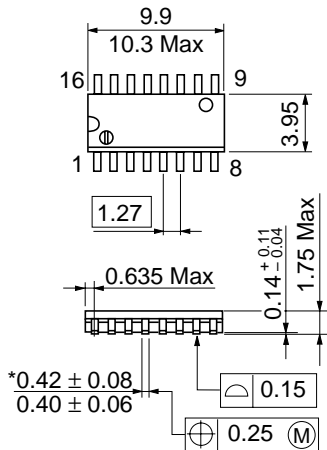


Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

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