ITRI
ERSO

ES52110

8-bit D/A Converter

Features

- On-Chip Latches for Both DACs.
- +5V to +12V Operation .
- DACs Matched to 1%.
- Four Quadrant Multiplication.
- TTL/CMOS Compatibel from 5V to 12V.
- Full Temperature Operation.
- 8-bit Endpoint Linearity(+1/2 LSB)
- Microprocessor Compatible.

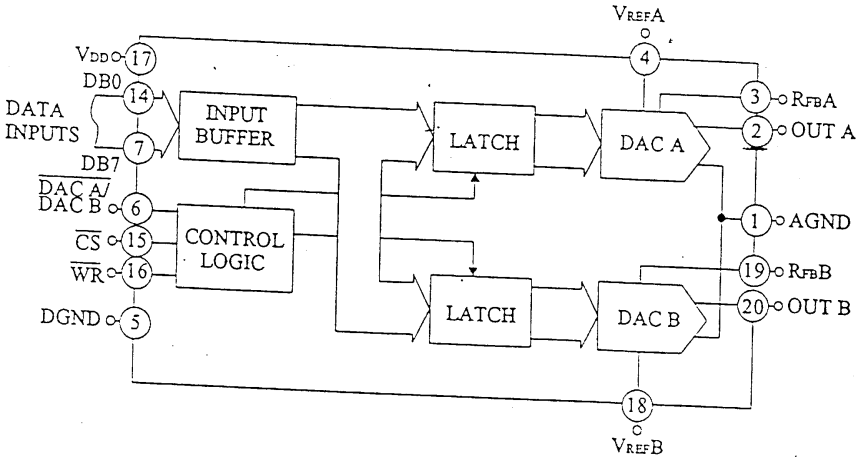
DESCRIPTION

ES52110 contains two & two 8-bit multiplying D/A converter in a single chip.This monolithic construction offers excellent DAC-to DAC matching and trzcking. The ES 52110 consists of two R-2R resistor-ladder networks, two tracking span resistors, two data latches, one input buffer, and control logic circuit, Both DACs offer excellent four quadrant multiplication characteristics with a separated reference input and feedback resistor for each DAC.

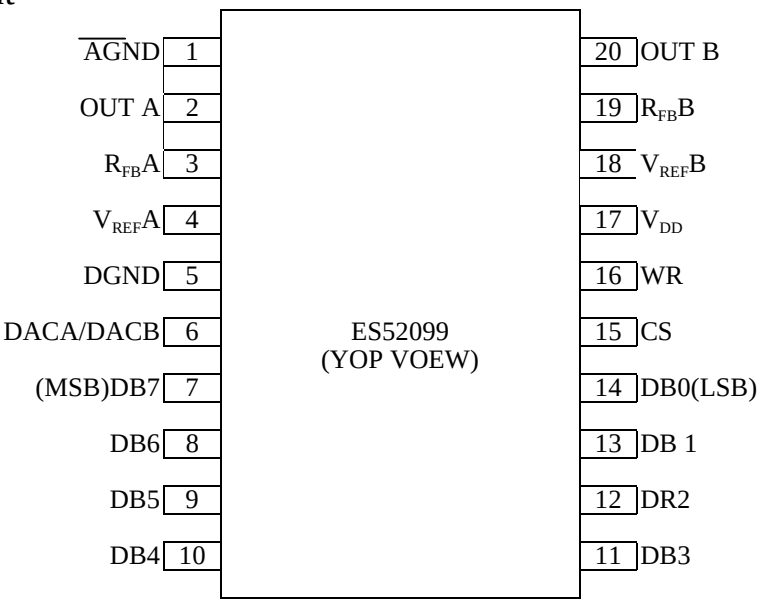
Applications

- Disk Drives
- Digital Gain/Attenuation Control
- Digitally-Controlled Filter Parameters

Block Diagram



PIN Assignment



Pin Description

Pin NUMBER.	NAME	TYPE	DESCRIPTION
1	AGND		The currcnt from the digital input are switched between the DAC OUTPUT and AGND thus maintaining fixed currcnt in cach ladder leg. Independent of switch statc.
2	OUT A	O	Analog data is restored from D/A conveter which the digital data is transferred ino ether of the two DAC.
20	OUT B	O	
3 19	R_{FB} A R_{FB} A		Internal feedback resistor
4 18	V_{REF} A R_{REF} B		The refercnce voltage for the R-2R ladder structure DAC.
5	DGND		
6	$\overline{\text{DAC}}$ A/D ACB	I	Both DAC latchcs sharc a common s-bit input port. The control input DAC A/D ACB selects which DAC can accept data from the input port.
7-14	DB7-DB0	I	Data bus is TTL./CMOS com -patible. Data is transferred into the either of two latches of DAC. DB0 is the least significant bit
15	CS	I	Input $\overline{\text{CS}}$ and $\overline{\text{WR}}$ control the operating mode of the selectod DAC. When $\overline{\text{CS}}$ and $\overline{\text{WR}}$ are both ow. The sclected DAC is in the Write mode. The input dath latches of the sclectod DAC are transparcnt and its analog output responds to activity on DB0-DB7
17	VDD		Power

FUNCTION DESCRIPTION :

Function Mode

The selected DAC latch retains the data which is present on DB0-DB7 just prior to $\overline{CS}$ or $\overline{WR}$ assuming a high state.Both analog outputs remain at the values corresponding to the data in their respective latches.

MODE SELECT TABLE

$\overline{DAC}$ A/D ACB	$\overline{CS}$	$\overline{WR}$	DACA	DACB
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

L=Low State H=High State X=Don't Care

Circuit Description

＊D/A Converter

The ES 52110 contains two identical 8-bit multiplying D/A converters, DAC A and DAC B. Each DAC consists of a highly stable R-2R ladder and eight N-channel current steering switches. Asimplified D/A circuit for DAC A is shown in Figure 1. An inverted R-2R ladder structure is used, that is, binary weighted currents are switched between the DAC ouptut and AGND thus maintaining fixed currents in each ladder leg independent of switch state. There is normally closed switch in series with the internal feedback resistor (R_{FB}). This switch improves linearity performance over temperature and power supply rejection; however , when the circuit is not powered up, the switch assumes and open state.

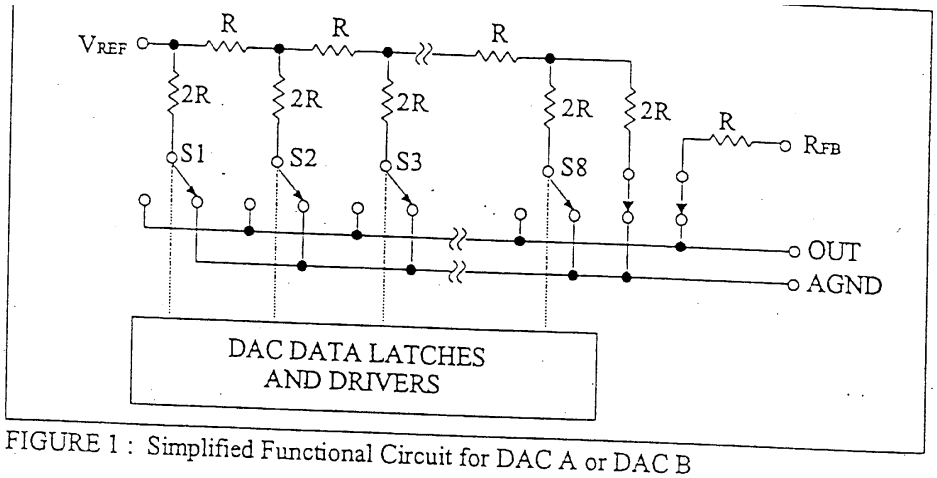


FIGURE 1 : Simplified Functional Circuit for DAC A or DAC B

＊Equivalent Circuit

Figure 2 shows an approximate equivalent circuit for one of the ES 52110's D/A converters, in this case DAC A. A simpilar equivalent circuit can be drawn for DAC B. Note that AGND is common for both DAC A and DAC B. The current source I_{LKG} is composed of surface and junction leakages , as with most semiconductor devices, apporximately doubles every 10℃ . The resistor Ro as shown in Figure 2, is the equivalent output resistance of the device which varies with 11kΩ. C_{OUT} is the capacitance due to the N-channel switches and varies from about 50Pf to 120pF , depending upon the digital input. $g(V_{REF}A,N)$ is the Thevenin equivalent voltage generator, due to the reference input voltage $V_{REF}A$ and transfer function of the R-2R ladder.

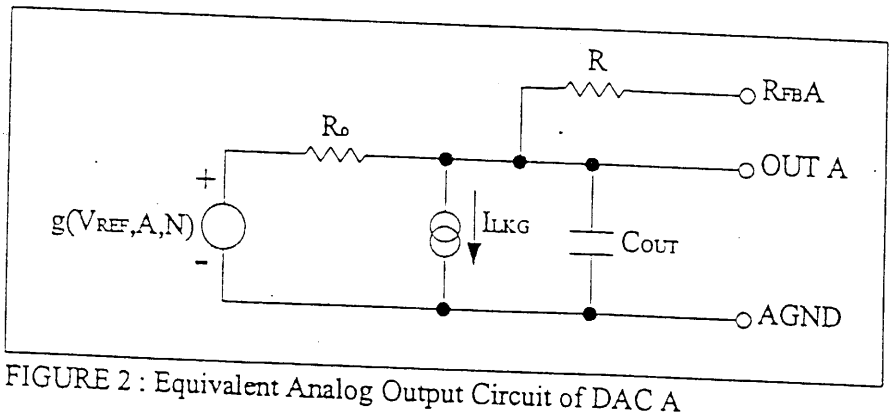


FIGURE 2 : Equivalent Analog Output Circuit of DAC A

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Type	Max	Unit
V_{DD} to AGND	O	—	+15	V
V_{DD} to AGND	O	—	+15	V
AGND to DGND	O	—	V_{DD}+0.3	V
Digital Input Vdtage to DGND	-0.3	—	V_{DD}+0.3	V
V_{PIN2}, V_{PIN20} to AGND	-0.3	—	V_{DD}	V
V_{REF}, V_{REF}B to AGND	-25	—	+20	V
V_{RFB}A, V_{RFB}B to AGND	-25	—	+20	V
Operating Temperature Range	-55	—	+125	℃
Junction Temperature	—	—	+150	℃
Storage Temperature	-65	—	+150	℃
Lead Temperature	—	—	+300	℃

Notes:

1.Do not aplly voltage higher than V_{DD} or less than GND potential on any terminal except V_{REF}.

2.The digital control inputs are Zener-Protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive form at all times until ready for use.

3.Do not insert this device into powered sockets; remove power before insertion or removal.

4.Use proper antistatic handing proced ures.

5.Stressed above those listed under"Abslute Maximum Ratings"may cause permanent damage to the device.

Application Information

The most common application of this DAC is voltage output operation. Unipolar output operation provides a 0 to 10 volt output swing when connected, as shown in Figure 4. The maximum output voltage polarity is the inverse of the input reference voltage, since the op amp inverts the input currents. The transfer equation for unipolar operation is V_{OUT}=-V_{IN} D/256, where Dis the decimal value of the data bit inputs DB0 THRU DB7 and V_{IN} is the reference input voltage. The transfer equation highlights another popular applicaton of CMOS DAC's , The output voltage is the product of the reference voltage and the digital input code. The reference input voltage can be any value in the range of $\pm V_{CC}$ volts for both DC or AC signals. The circuit in Figure 4 performs tow-quadrant multiplication. Table 1 provides example analog outputs for the given digital input codes.

For biploar output operation connect the ES 52110 as shown in Figure 5. This circuit configuration provides an offset current, derived from the reference to enable the output op amp to swing in both polarities. The digital input coding becomes offset binary . Table 2 provides some example analog outputs for various digital nputs (D). The transfer equation for bipolar operation is V_{OUT} = V_{IN}×(D/128-1),where Dis the decimal value of the data bit inputs DB0 thru DB7. This circuit provides full four-quadrant multiplication able to accept both polarities on all input as well as the circuit output.

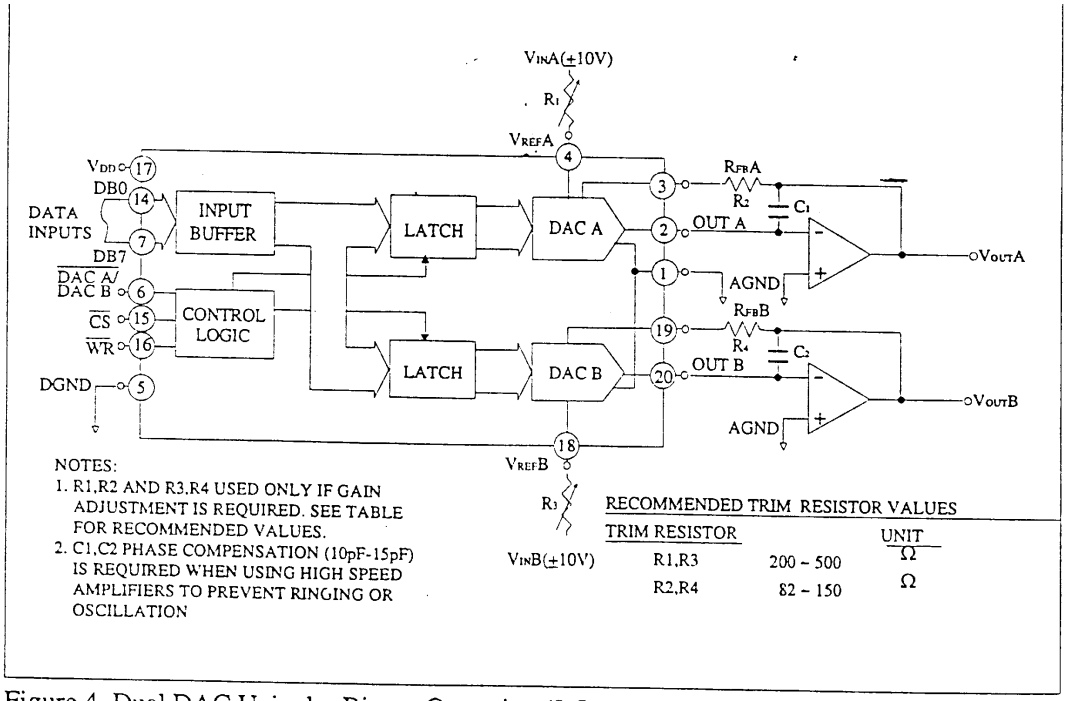


Figure 4. Dual DAC Unipolar Binary Operation (2 Quadrant Multiplication). See Table 1.

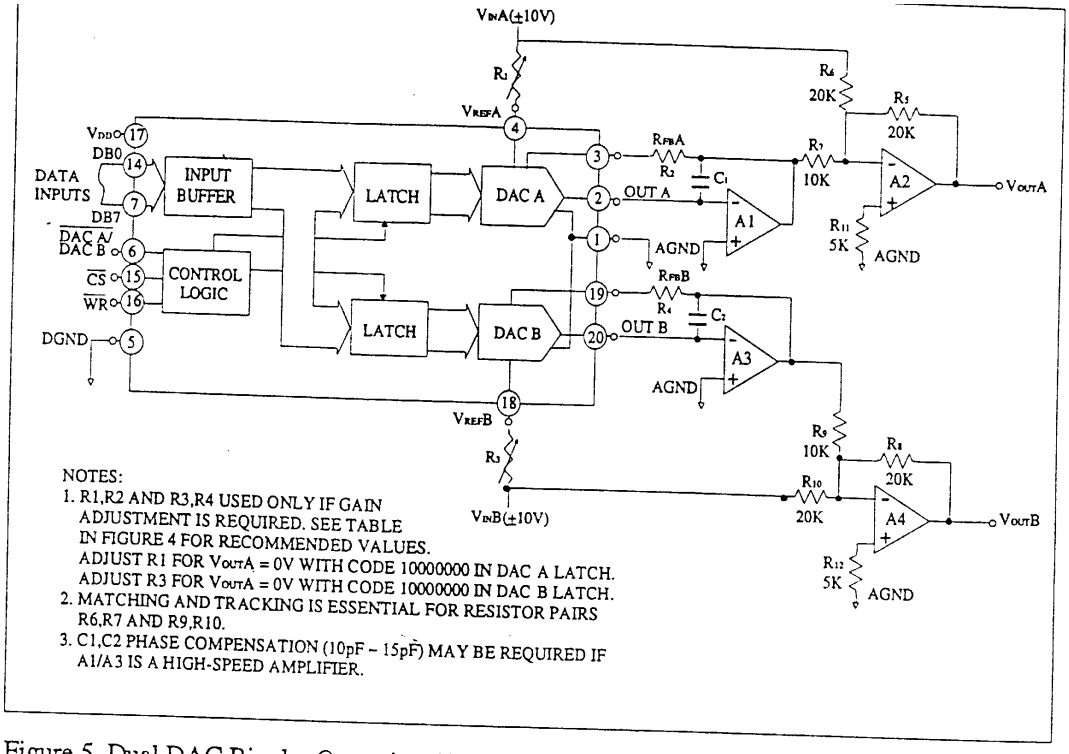


Figure 5. Dual DAC Bipolar Operation (4 Quadrant Multiplication). See Table 2.

DACLATCH CONTENTS MSB LSB	ANALOG OUTPUT (DAC A or DACB)
11111111	-VIN(255/256)
1000001	-VIN(129/256)
10000000	-VIN(128/256) = -VIN /2
01111111	-VIN(127/256)
00000001	-VIN(1/ 256)
00000000	-VIN(0/ 256) = 0

Table 1. Unipolar Binary Code Table.
NOTE: 1 LSB = (2 E-8)(V_{IN}) = (1/256)(V_{IN})

DACLATCH CONTENTS MSB LSB	ANALOG OUTPUT (DAC A or DACB)
111111111	+VIN(127/128)
10000001	+VIN(1 /128)
10000000	0
01111111	+VIN(1 /128)
00000001	+VIN(127 /128)
00000000	+VIN(128 /128)

Table 1. Unipolar Binary Code Table.
NOTE: 1 LSB = (2 E-7)(V_{IN}) = (1/128)(V_{IN})

ELECTRICAL CHARACTERISTICS

＊Operating Conditions:

V_{DD} = +5V±5%;$V_{REF}A$ = $V_{REF}B$ = +10V;I_{OUT} A = $I_{OUT}B$ = 0V; TA = Full Temp. Range specified under Absolute Maximum Rating, unless otherwise noted.

Static Accuracy

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Resolution	N		8	—	—	Bits
Relative Accuracy (Note 2)	INL		—	—	± 1/2	LSB
Differential Nonlineraity (Note 3)	INL		—	—	± 1/2	LSB
Full-Scale Gain Error (Note 4)	G_{FSE}	TA = +25℃ TA = Full Temp. Range	—	—	± 1/2	LSB
Input Resistance ($V_{REF}A$, $V_{REF}B$) (Note 6)	R_{IN}		8	—	15	kΩ
Input Resistance Match ($V_{REF}A/V_{REF}B$)	$\Delta R_{IN}/R_{IN}$		—	± 0.1	±1	%

Digital Inputs
(Note 9)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Digital Input High (Note 8)	V_{INH}		2.4	—	—	V
Digital Input Low (Note 8)	V_{INL}		—	—	0.8	V
Input Current (Note 7)	V_{IN}	TA = +25℃ TA = Full Temp. Range	— —	±0.01 —	±1 ±10	μA
Input Capacitance (Note 10)	C_{IN}	DB0-DB7 WR, CS, DAV, A/DACB	— —	— —	10 15	pF

Switching Characteristics
(Note 10,11)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Chip Select to Write Set-Up To,e	t_{CS}		100	—	—	ns
Chip Select to Write Hold time	t_{CH}		10	—	—	ns
Chip Select to Write Hold time	t_{AS}		100	—	—	ns
Data Select to Write Set-Up time	t_{DS}		100	—	—	ns
Data Select to Write Hold time	t_{DH}		10	—	—	ns
Write Pulse Width	T_{WR}		90	—	—	ns

Power Supply

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Current	I_{DD}	All Digital Input = V_{DE} or V_{NL}	—	—	1	mA
		All Digital Input = 0V or V_{DD} TA = +25℃ TA = Full Temp. Range	— —	— —	0.5 1.0	mA

AC Performance Characteristic

Parameter	Symbol	Conditions	Min	Typ	Max	Units
DC Supply Rejection Ratio (Δgain/ΔV_{DD}) (Note 13)	PSRR	T_A = +25℃ T_A = Full Temp. Range	— —	— —	0.02 0.04	%/%
Current Settling Time (Notes 10, 15, 16, 20)	ts	T_A = Full Temp. Range	— —	— —	350	ns
Digital Charge Injection (Note 17)	Q	T_A = +25℃	—	100	—	nVs
Ouptput Capactiance	C_{OUT}A C_{OUT}A	DAC Latches Loaded With 0000 0000	— —	— —	25 25	pF
	C_{OUT}A C_{OUT}A	DAC Latches Loaded With 0000 0000	— —	— —	60 60	pF
AC Feedthrough	FT_A	V_{REF}A to IaxA : T_A = +25℃ T_A = Full Temp. Range	— —	— —	-70 -65	dB
	FT_A	V_{REF}A to IaxA : T_A = +25℃ T_A = Full Temp. Range	— —	— —	-70 -65	dB
Channel-to-Channel Isolation (Note 19)	CCI_{BA}	V_{REF}A to I_{OUT}B : V_{REF}A = +20VP-P Sinewave @ f = 10kHz V_{REF}B = 0V;TA = 25℃	—	-80	—	dB
	CCI_{BA}	V_{REF}A to I_{OUT}B : V_{REF}A = +20VP-P Sinewave @ f = 10kHz V_{REF}B = 0V;TA = 25℃	—	-80	—	dB
Digital Crosstalk	Q	For Code Transition from 0000 0000 to 1111 1111 T_A = +25℃	—	30	—	nVs
Harmonic Distortion	THD	V_{DD} = 6V @f = 1kHz T_A = +25℃	—	-85	—	dB

＊Operating Conditions :

V_{DD} = +12V±5% ;$V_{REF}A = V_{REF}B$ = +10V;$I_{OUT}A$ = IOUTB = 0V;T_A = Full Temp. Range specified under Absolute Maximum Rating, unless otherwise noted.

Static Accuracy

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Resolution	N		8	—	—	Bits
Relative Accuracy (Note 2)	INL		—	—	± 1/2	LSB
Differential Nonlineraity (Note 3)	DNL		—	—	± 1	LSB
Full-Scale Gain Error (Note 4)	G_{FSE}	TA = +25℃ T_A = Full Temp. Range	—	±0.5 ±0.1	±2 ±3	LSB
Gain Tmperaturceoefficient (△gain/△tempertme) (Note 4)	TCG_{FSE}		—	—	±0.0035	%℃
Output Leakage Curent $I_{AT}A$(Pin 2)I_{OUT}(Pin 2) (Note 4)	I_{LKG}	TA = +25℃ T_A = Full Temp.Range	— —	±0.5 —	±5 ±200	nA
Input Resistance ($V_{REF}A$, $V_{REF}B$) (Note 6)	R_{IN}		8	—	15	kΩ
Input Resistance Match ($V_{REF}A$, $V_{REF}B$)	$\triangle R_{IN}/R_{IN}$		—	±0.1	±1	%

Digital Inputs
(Note 9)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Digital Input High (Note 8)	V_{INH}		3.4	—	—	V
Digital Input Low (Note 8)	V_{INL}		—	—	1.5	V
Input Current (Note 7)	I_{IN}	TA = +25℃ T_A = Full Temp.Range	— —	±0.01 —	±1 ±10	μA
Input Capacitance (Note 10)	C_{IN}	DB0-DB7 WR,CS,DAV A/DACB	— —	— —	10 15	pF

Switchin g C harac teris tucs
(Note 10, 11)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Chip Select to Write Set-Up Time	T_{CS}		60		—	ns
Chip Select to Write Hold Time	T_{CH}		10	—	—	ns
DAC Select to Write Set-Up Time	T_{AS}		60	—	—	ns
DAC Select to Write Hold Time	T_{AH}		10	—	—	ns
Data Select to Write Set-Up Time	T_{DS}		70	—	—	ns
Data Select to Write Hold Time	T_{DH}		10	—	—	ns
Write Pulse Width	T_{WR}		60	—	—	ns

Power Supply

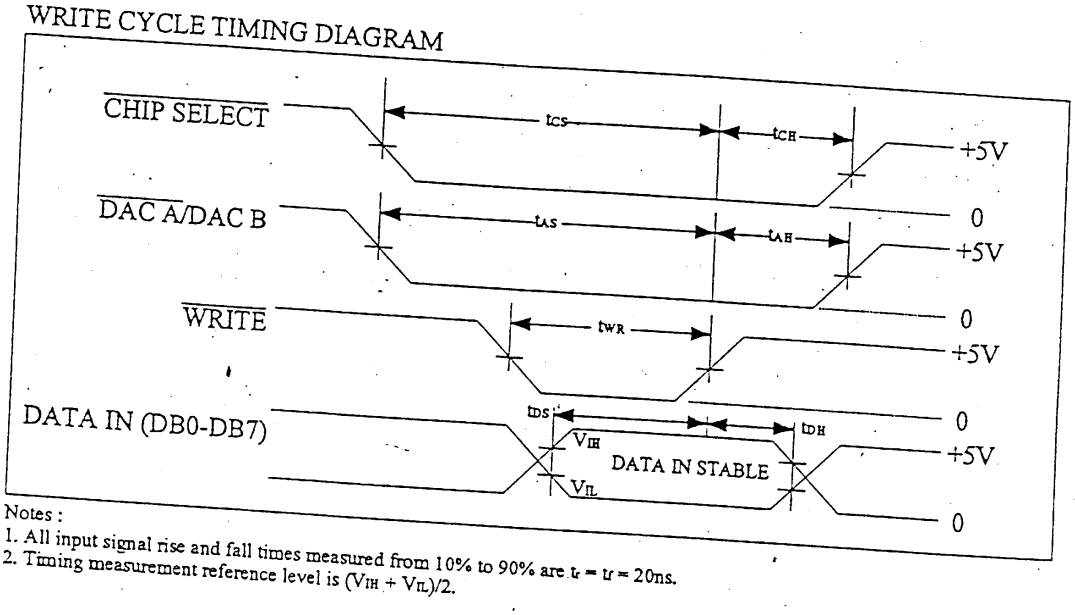
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Current	I_{DD}	All Digital Input = V_{INH} or V_{INL}				
		TA = +25℃	—	—	6	
		TA = Full Temp. Range	—	—	6.5	mA
		All Digital Input = 0V or V_{DD}				
		TA = +25℃	—	—	0.5	
		TA = Full Temp. Range	—	—	1.0	mA

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DC Supply Rejection Ratio (Δ gain / ΔV_{DD}) (Note 13)	PSRR	TA = +25℃ T_A = Full Temp. Range	— —	— —	0.01 0.02	%/%
Current Settling Time (Note 10,15,16,20)	ts	T_A = Full Temp. Range	—	—	250	ns
Digital Charge Injection (Note 17)	Q	T_A = +25℃	—	160	—	nVs
Ouptput Capactiance	C_{OUT}A C_{OUT}A	DAC Latches Loaded With 0000 0000	— —	— —	25 25	pF
	C_{OUT}A C_{OUT}A	DAC Latches Loaded With 0000 0000	— —	— —	60 60	pF
AC Feedthrough	FT_A	V_{REF}A to IaxA : T_A = +25℃ T_A = Full Temp. Range	 — —	 — —	 -70 -65	 dB
	FT_B	V_{REF}A to IaxA : T_A = +25℃ T_A = Full Temp. Range	 — —	 — —	 -70 -65	 dB
Channel-to-Channel Isolation (Note 19)	CCI_{BA}	V_{REF}A to I_{OUT}B : V_{REF}A = +20VP-P Sinewave @ f = 10kHz V_{REF}B = 0V;TA = 25℃	—	-80	—	dB
	CCI_{AB}	V_{REF}A to I_{OUT}B : V_{REF}A = +20VP-P Sinewave @ f = 10kHz V_{REF}B = 0V;TA = 25℃	—	-80	—	dB
Digital Crosstalk	Q	For Code Transition from 0000 0000 to 1111 1111 T_A = +25℃	—	50	—	nVs
Harmonic Distortion	THD	V_{DD} = 6V @f = 1kHz T_A = +25℃	—	-85	—	dB

Notes:
1.Specifications apply to both DAC A and DAC B.
2.This is an endpoint linearity specification.
3.All grades guaranteed to be monotonic over the full operating the full operating temp. range.
4.Measured using internal R_{FB}A and R_{FB}B. Both DAC latches loaded with 1111 1111.
5.DAC loaded with 0000 0000.
6.Input resistance TC = 300 ppm/℃.
7.V_{IN} = 0V or V_{DD}.
8.For all data bits DB0-DB7, WR, CS, DAC A/DACB.
9.Logic inputs are MOS gates. Typical input current(+25℃)is less than lnA.
10.Guaranteed and not tested.
11.See timing diagram.
12.These characteristics are for design guidance only and not subject to test.
13.ΔVDD = ±5%.
14.From digital input to 90% of final analog-output current.
15.V_{REF}A = V_{REF}B = +10V;L_{OUT}A, I_{OUT}B load = 100Ω, C_{EXT} = 13Pf.
16.WR, CS = 0V, DB0-DB7 = 0V to V_{DD} or V_{DD} to 0V.

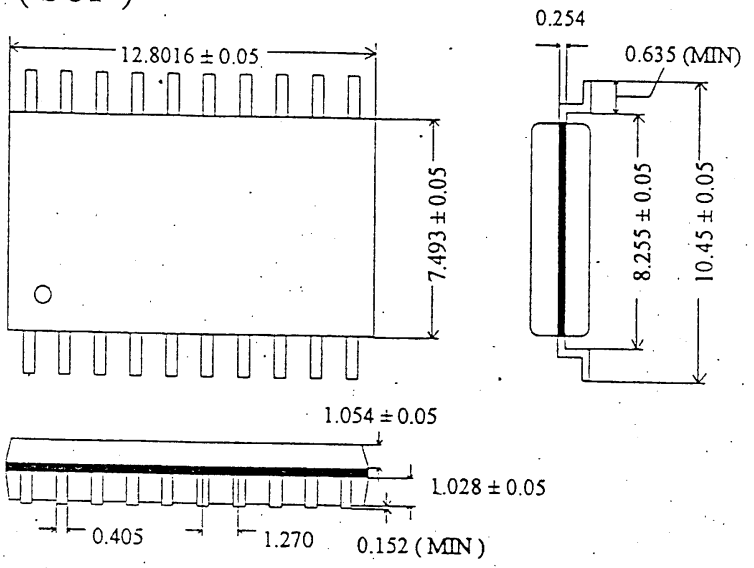
17.For code transition 0000 0000 to 1111 1111.
18.$V_{REF}A$, $V_{REF}B$ = $20V_{P-P}$ sinewave @ f = 10kHz.
19.Both DAC latches loaded with 1111 1111.
20.Extrapolated:ts(1/2LSB) = TPD + 6.2 τ , where τ = the measured first time constant of the fimal RC decay.

WRITE CYCLE TIMING DIAGRAM

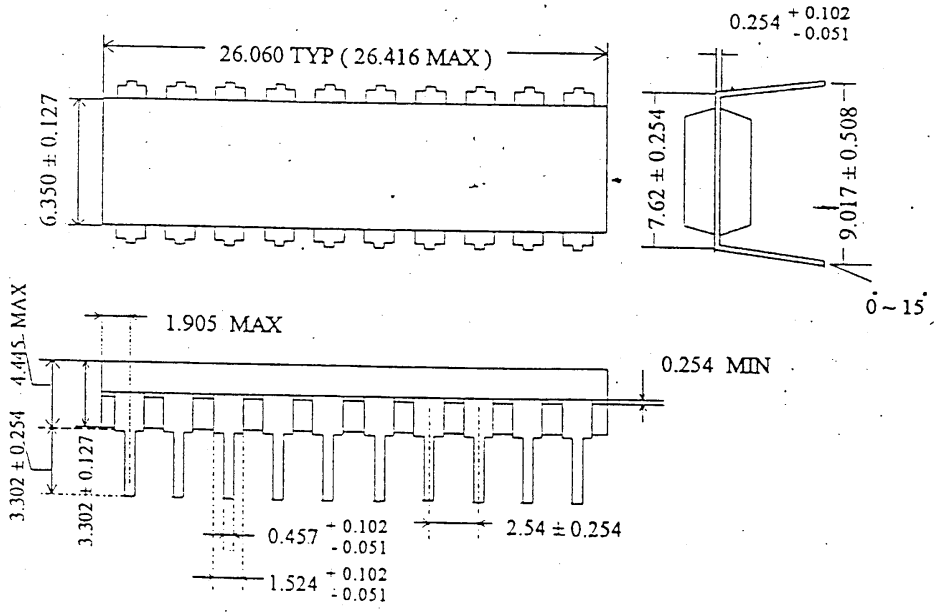


Notes:
1.All input signal rise and fall times measured from 10% to 90% are tr = tf = 20ns.
2.Timing measurement reference level is(V_{IH} + V_{IL})/2.

ES52110S (SOP)



ES52110E (DIP)



unit : mm