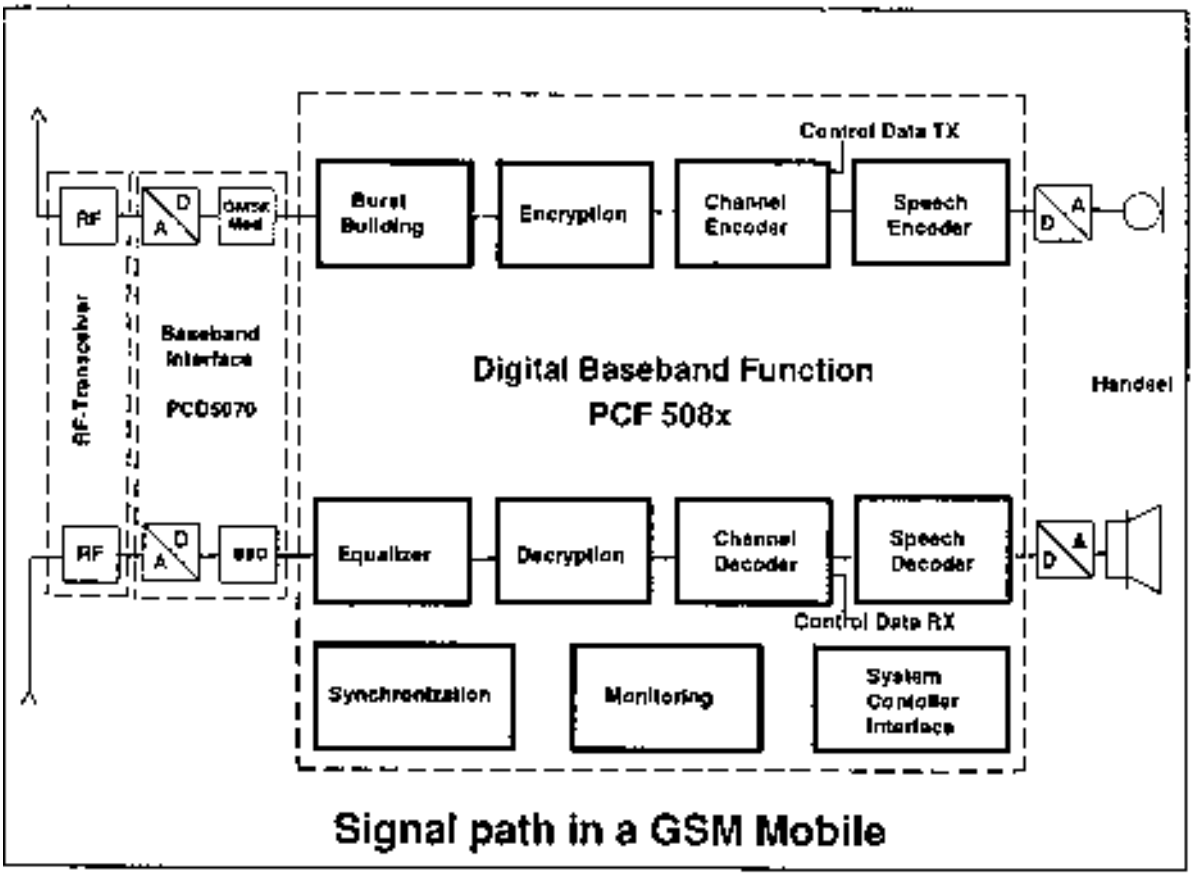
GSM baseband processors for digital mobile cellular radio

PCF5081/PCF5082

GSM Baseband Signal processors

The PCF5081 and the PCF5082 are integral parts of the complete chip-set provided by Philips for the pan-European digital mobile cellular telephone system. The PCF5081 and PCF5082 are key elements for GSM, each performing all the baseband signal processing tasks. Because of their high-level of architectural modularity, these processors can easily be adapted to market requirements in respect to both hardware and software.

The PCF5081 (with ROM) is intended for use in GSM handsets, the PCF5082 (ROM-less) for implementation in the base station. These processors are also considered as the first devices of an entire product line introduced as PCF508x. This family provides powerful computational capabilities which supports the highly sophisticated baseband signal processing required by GSM.



Signal path in a GSM Mobile

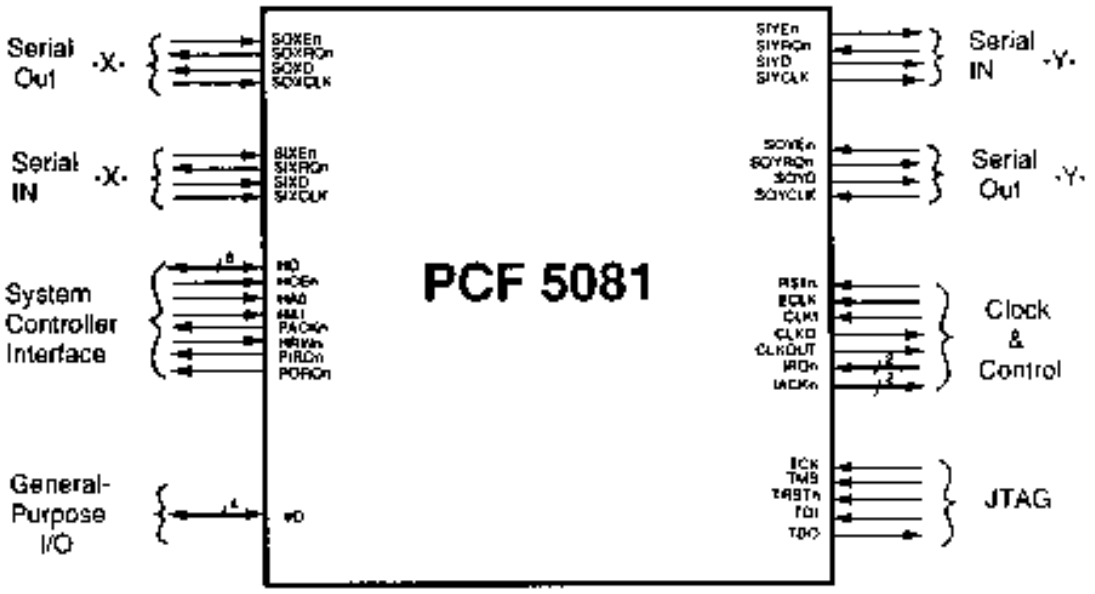
The different tasks performed in the baseband signal path of the GSM-system are carried out by means of software partitioned program modules in the signal processor. This implementation is supported by Application Specific Hardware (ASH) to speed up execution and overall performance.

This partitioning between software and hardware for the different processing tasks has been implemented as a trade-off between dedicated hardware and software to provide fast execution with an optimal level of flexibility.

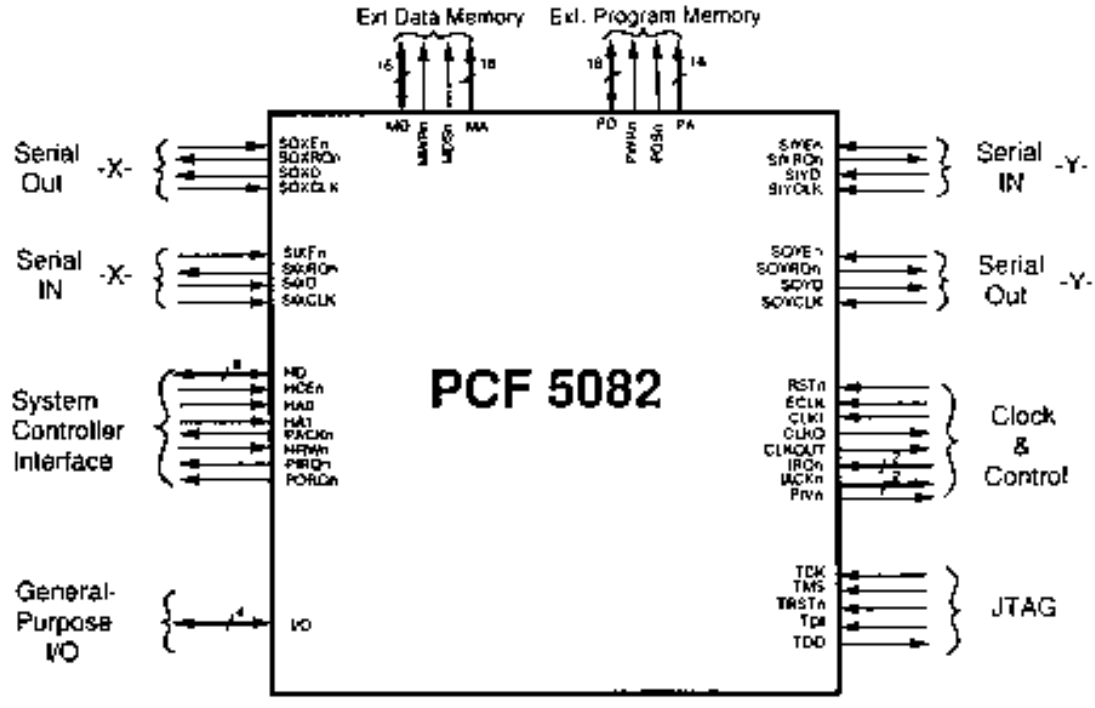
Main Features:

- 16-Bit fixed point double precision architecture
- 40MHz master clock
  20MHz internal clock (50ns instr.cycle)
- Fully pre-programmed modules for GSM baseband tasks.*
- Dedicated processor optimized for:
  - Equalization function
  - Channel Coder/Decoder
  - Encryption/Decryption
- Power-down mode with wake-up facility
- Several levels of interrupts
- Event counter
- Asynchronous serial I/O -X-
- Sophisticated serial I/O -Y- supporting both asynchronous and synchronous communication (i.e. GCI, PCM highway etc.)
- 8-Bit parallel system controller interface supporting both request and acknowledge driven communication.
- Boundary scan facility
- Build-in self test (BIST)
- Self-Aligned-Contacts CMOS (SACMOS) technology with very high design density
- External memory interfaces for both data and program memory **
- Boot-strap facility* *

* on PCF5081 only
** on PCF5082 only



Signal I/O of the PCF 5081



Signal I/O of the PCF 5082

Signal Description

Mnemonic	Type	Function
CLKI	I	Crystal or clock input. Input clock at twice the frequency of internal cycle.
CLKO	O	Crystal output
CLKOUT	O	Synchronization clock. Output clock at half of the frequency of CLKI.
ECLK	I	Event clock to count external events. The frequency of this input signal is limited to 1/4 of the CLKI if the duty cycle is 50%.
HA[1:0]	I	Host address bus. The address signals are used to select the source or destination of the data on the data bus HD. These signals must be stable before the enable signal HCEn is asserted
PACKn	O	Output signal to acknowledge data on the data bus HD if the acknowledge mode is enabled Active low.
HCEn	I	Global chip enable signal for the host interface. Active low.
HD[7:0]	B	Bidirectional host data bus, 8 bit wide The high or low byte of the 16 bit I/O buffer registers are read or written via this port depending on the signals at the address bus HA[1:0]
PIRQn	O**	Data input request signal. Active low. The signal requests data for input if the request mod is enabled. It is driven low if the input buffer register is empty.
PORQn	O**	Data output request signal. Active low. The signal requests for data to be read by the external device if the request mode is enabled It is driven low if the output buffer register is full.
HWRn	I	Write signal Active low The signal controls the direction of the data transfer on the data bus HD [7:0]. When low, data are written by external device.
IACKn [2:1]	O*	External interrupt request acknowledge signals. Active low The signals are set low if the related request is serviced. It is set high if the related flag is cleared.
IRQn[2 1]	I	External interrupt request signals. Active low and edge triggered. If low, the related interrupt is requested. It will be acknowledged if the related interrupt is enabled.
IO[4:1]	B***	General I/O pins. They have open drain outputs and a pull-up resistor. The states of these pins are reflected by four bits in a control register. The pulse width of an input signal has to be at least two internal processor cycles until a change will be recognized in the control register.
RSTn	I	Reset signal, low active. A high-to-low transition causes entry into reset state. A low-to-high transition causes execution to begin at program memory location 0 or booting.
SIXCLK	O*	Serial input clock port X. Asynchronous.
SIXD	I	Serial input data port X. Data are shifted into the input shift register X.
SIXEn	I	Serial input enable port X. Active low.
SIXRQn	O*	Serial input data request, port X. Handshake signal. Active low
SOXCLK	I	Serial output clock port X. Asynchronous
SOXD	O*	Serial output data port X. Data are shifted out of the ouput shift register X.
SOXEn	I	Serial output enable port X. Active low.
SOXRQn	O*	Serial output data request, port X Handshake signal, active low.
SIYCLK	I	Serial input clock port Y. Asynchronous clock.
SIYD	I	Serial input data port Y. Data are shifted into the input shift register Y.
SIYEn	I	Serial input enable port Y. Active low. Frame sync signal in synchr. mode. Active high.
SIYRQn	O*	Serial input data request, port Y. Handshake signal active low Not used in synchr. mode.
SOYCLK	I	Serial output clock port Y Asynchronous
SOYD	O***	Serial output data port Y. Data are shifted out of the output shift register Y
SOYEn	I	Serial output enable port Y. Active low. Serial output data read back for collision detection in synchr mode
SOYRQn	O*	Serial output data request, port Y. Handshake signal, active low Not used in synchr. mode.
TCK	I	JTAG signal. Test clock. Free running clock active rising edge
TDI	I	JTAG signal. Test data input. Shifted in with the rising edge of TCK
TDO	O	JTAG signal. Test data output. Shifted out with the falling edge of TCK.
TMS	I	JTAG signal, Test mode select
TRSTn	I	JTAG signal. Test interface reset. Active low. When setting low, the TAP controller will be reset independently from the processor.

Signal Description

Mnemonic	Type	Function
MA[15:0] 1)	O*	Data address bus for addressing up to 64k x16 bits.
MD[15:0] 1)	B	Bidirectional 16 bit data bus connection to external data memory
MDSn 1)	O*	Data strobe signal for external data memory. Active low.
MWRn 1)	O*	Write signal for external data memory. Active low. When low, data is written. When high, data is read.
1)	O*	Address bus for external program memory address up to 64k x 16 locations.

Mnemonic	Type	Function
PD[15:0] 1)	B	Data bus for external program memory. 16 bit wide
PDSn 1)	O*	Data strobe signal for external program memory. Active low.
PWRn 1)	O*	Write signal for external program memory. Active low. When low, data is written. When high, data is read.
PIVn 1)	O*	Output signal to support emulation. Active low.

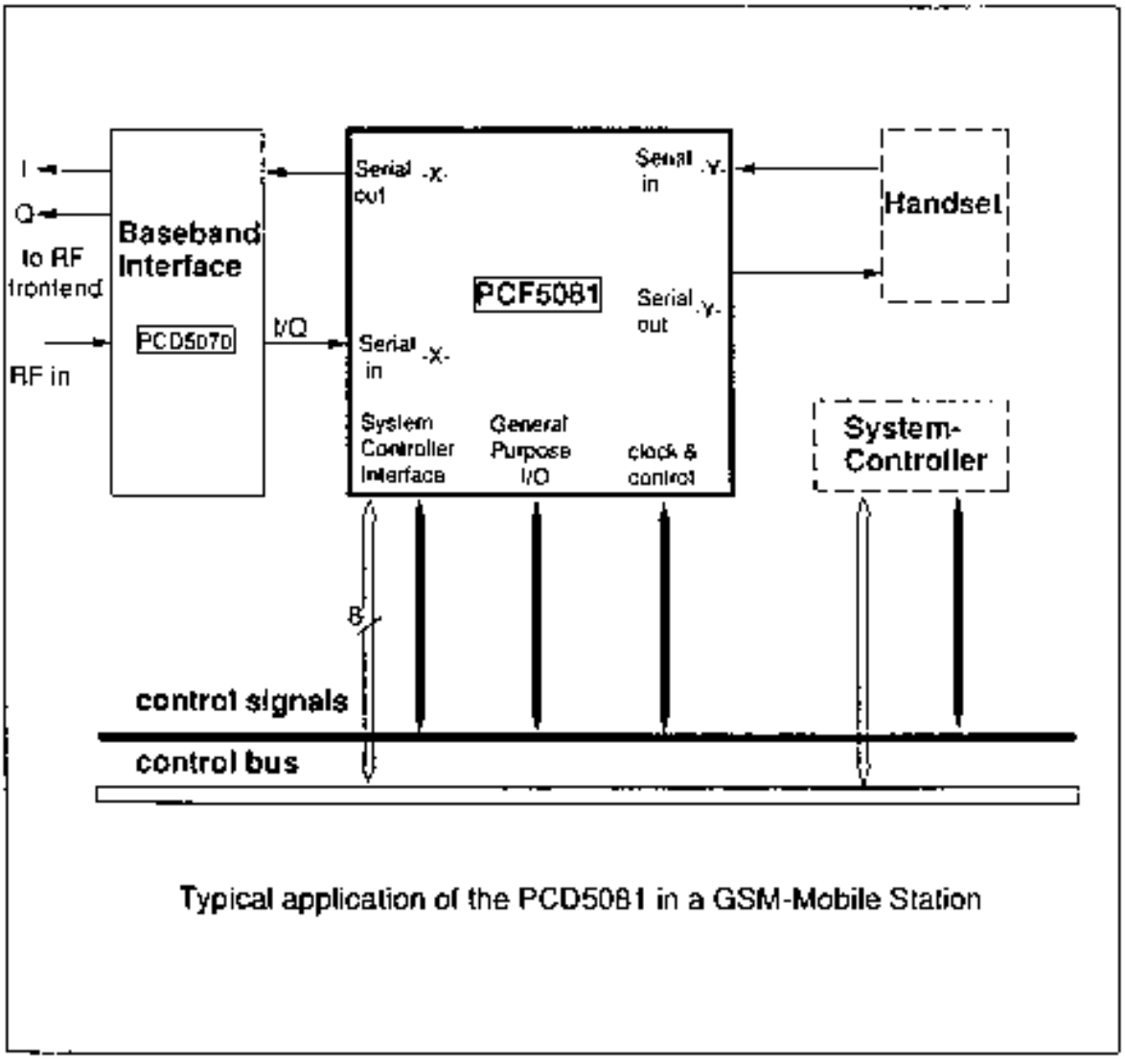
*: 3-state during O: Output signal I : Input signal	**: Open drain output. ***: Open drain output and 3-state during reset. B : Bidirectional signal. 1) : PCF5082 only.

Application of the PCF5081

This PCF5081 is designed to be used in the GSM mobile station. All the necessary baseband signal processing algorithms specified by the GSM-recommendations pertaining to the mobile station can be performed by means of this single chip.

The PCF5081 has on-chip memory (ROM) containing program modules for the different tasks implemented in firmware. A suitable amount of data-RAM/ROM is provided on-chip.

To allow flexible use of the different pre-programmed modules, the sequence of the baseband tasks is defined by the system controller by means of a circular tasks buffer. As soon as no task is left, the baseband processor enters a power-down mode to minimize current consumption.



Typical application of the PCD5081 in a GSM-Mobile Station

The main tasks to be performed by the baseband processor are the following:

- Equalization
- Channel encoder/decoder
- Speech encoder/decoder
- Encryption/Decryption
- Initial synchronization and monitoring of adjacent base station.

The architecture of the PCF5081 baseband processor was not designed for a single task within the baseband signal processing (eg. speech encoder/decoder), but rather to optimally accomplish all the necessary processing tasks. Special attention was placed on the equalization function where viterbi algorithm (MLSE receiver) and soft decision output code (4 bit coding) contribute to an optimal receiver algorithm in contribution with the channel decoder.

To be able to face up to the most severe conditions (hilly environment) a 6T algorithm is in preparation. Moreover, the equalization coefficients are continually updated during a burst to allow use of the mobile radio in vehicules travelling at very high speed.

The channel coder/decoder is capable of handling the speech Traffic Channel (TCH), the Fast and the Slow Associated Control Channel (FACCH and SACCH), the Random Access Channel (RACH) the Broadcast Control Channel (BCCH), the Paging Channel (PCH), the Access Grand Channel (AGCH), the synchronization Channel (SCH) and data transfer at all rates according to GSM Rec. 5.03.

The channel decoder is performed by viterbi algorithm based on soft decision equalizer output and by use of large path memory (up to 32 bits) for the MLSE algorithm.

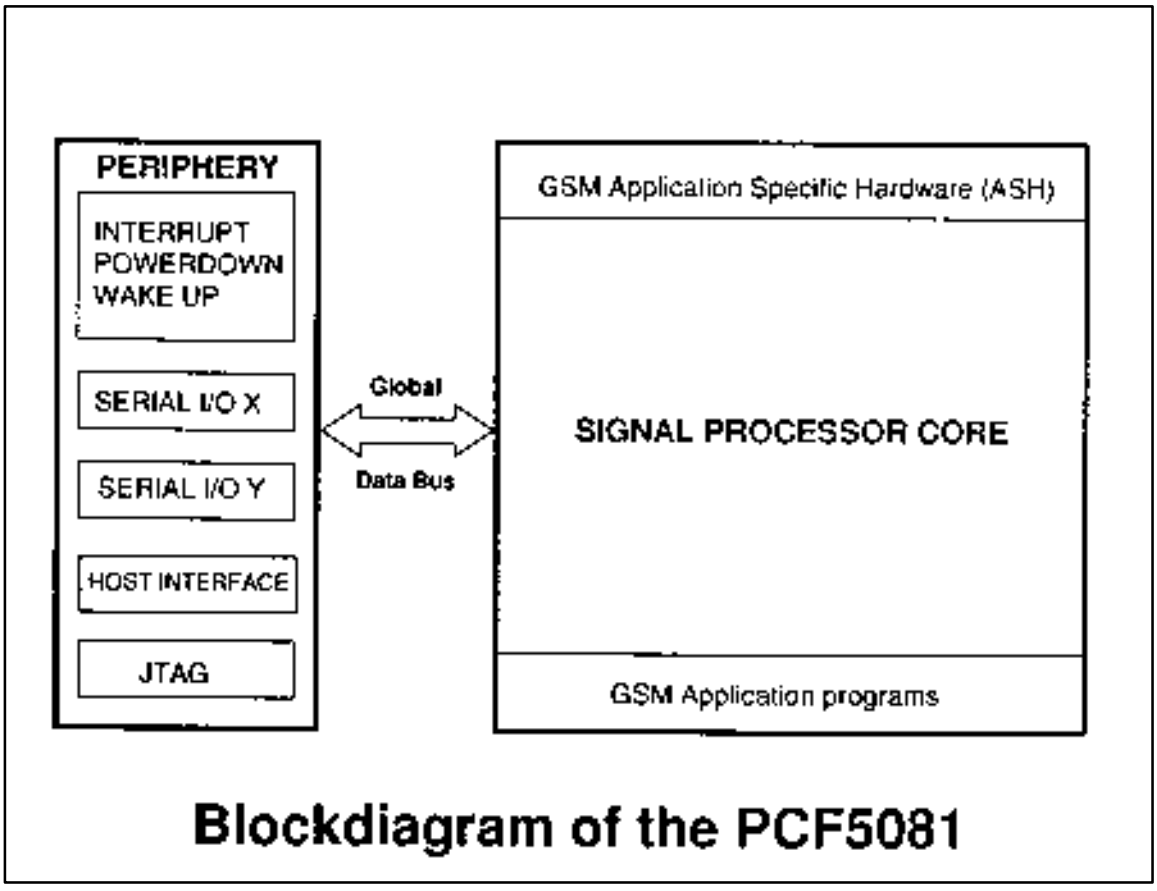
The speech encoder/decoder function includes voice activity detection, discontinous transmission as well as comfort noise insertion and generation.

The user-dataflow takes place via the serial interfaces X and Y. The X-interface looks in the direction of the frontend to the baseband interface (e.g. the Philips PCD5071) and the Y-interface is connected to the handset of the mobile.

The control-dataflow is transmitted via the system controller interface, the general purpose I/O pins, and other I/O available as part of the processor's periphery. The control data and signals are normally provided by the system controller of the mobile.

The architecture of the PCF5081 can be split into two major sections. The processor core consists of all the arithmetic units necessary to carry out the calculations as well as access memories containing data and program information. The application specific hardware is also part of the core. The periphery consists of all the necessary interfaces as well as the interrupt and powerdown/wake-up facilities.

Internal data between these two sections is exchanged via a global data bus.



Blockdiagram of the PCF5081

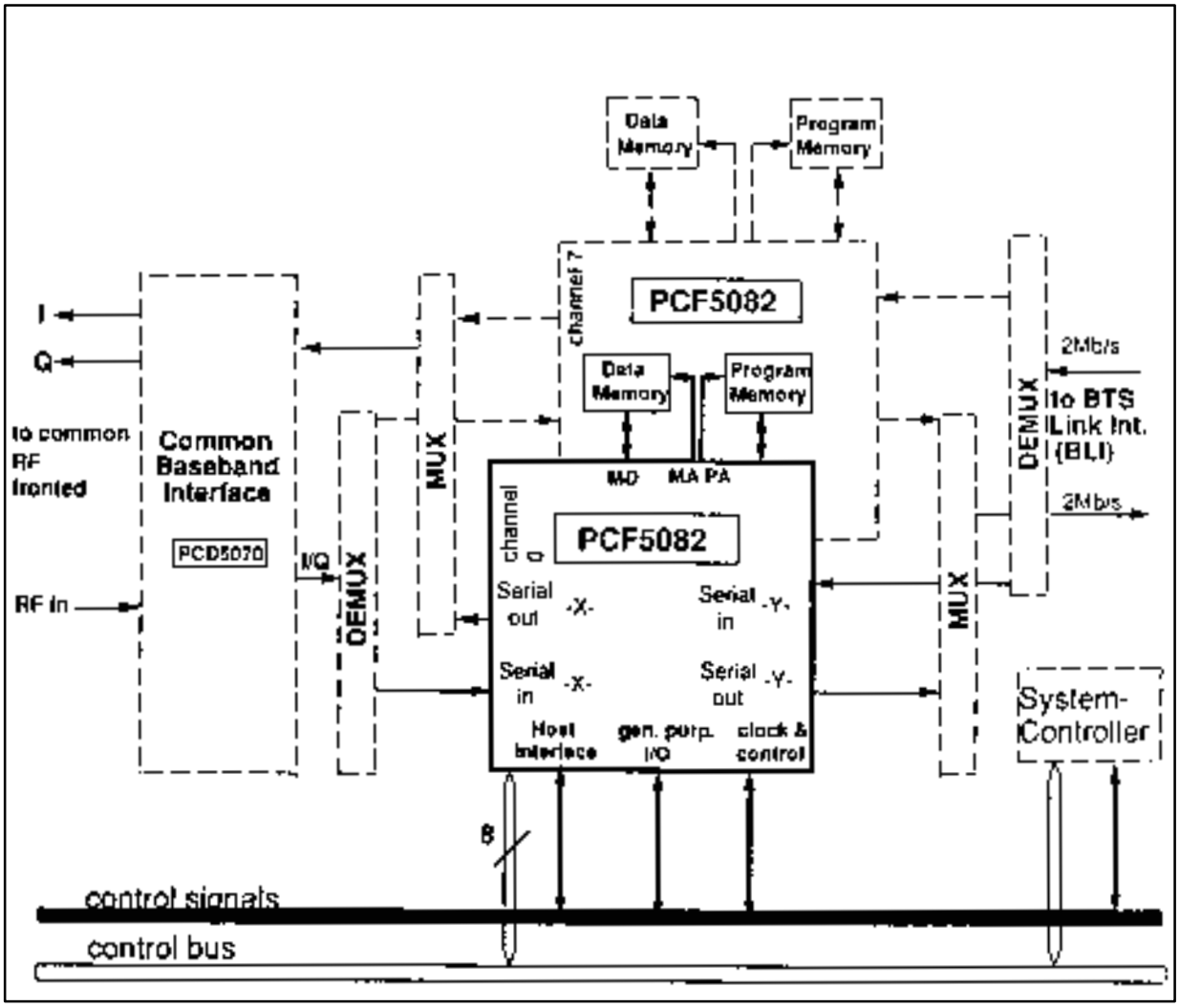
Application of the PCF5082

This version is targetted for use in GSM base station systems (BSS) as well as for real-time emulation purposes during software development and debugging.

ROM

As the baseband processing within a base station requires a certain degree of flexibility, the PCF5082 can externally address memory dedicated for the application program and user data.

The PCF5082 contains 1k x 16 bits or program-ROM used for Built-In Self Tests (BIST), boot-strap and emulation routines. External program memory (ROM/RAM) up to 63k x 16 bits can be connected to run application programs.



Possible application of the PCF5082 in a GSM-Base Taranceiver Station (BTS)

RAM

To keep the overall system costs low, 2k x 16 bits of on-chip data RAM is provided. This range can be extended by external devices (RAM/ROM) up to the maximum value of 64kx16 bits of data memory.

OTHERS

In the switching centre (MSC) the data streams of each of the eight channels are merged to a PCM-highway data-stream (2Mb/2) via a multiplexer (MUX) and vice versa via the BTS link interface (BLI). The serial interfaces Y of each of the processors are used for this data flow. In the frontend of the radio terminal (RT), each channel can be connected to a common baseband interface PCD5070 via a multiplexer (MUX) and a demultiplexer (DEMUX), respectively. The serial interfaces X of each of the processors are used for this data flow.
External memories containing user-data and application programs are connected. As in the PCF5081, the same interfaces are used for control-data and control-signal flow.

The architecture of both the PCF5081 and the PCF5082 can be split into two sections: processor core and the periphery. The PCF5082 processor core contains on-chip boot-strap facility, no user-program-memory and its periphery has additional memory interfaces to connect external memories for both user-data and application programs.

These are the main differences between both the PCF5081 and the PCF5082.

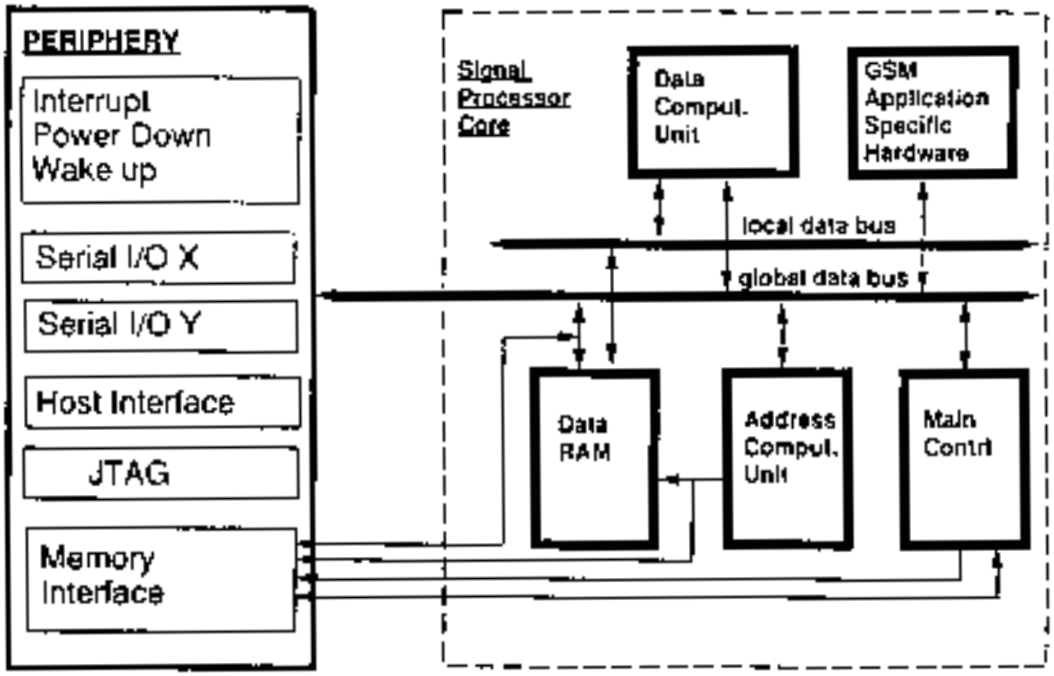
The boot-strap facility is an additional functionality of the PCF5082 allowing for convenient downloading of application programs to the external program memory (RAM) under the control of a host. Several sources for such a download can be selected by the user.

Due to the fact that application programs are stored or downloaded into external program memory, a large degree of flexibility is offered to the base station system designer.

Similar to the PCF5081, the PCF5082 contains application specific hardware to speed up the execution of the baseband signal processing algorithms.

There are several partitionings possible with respect to the different tasks which have to be performed. For instance, the baseband processing can be done by separating receiver and transmitter functions and using one PCF5082 for multiple time-slots (channels) within a TDMA-frame. Alternatively, the receiver and transmitter functions can be kept together and one PCF5082 used for processing both directions simultaneously.

In a typical application the PCF5082 is used for the baseband signal processing in a radio-terminal (RT) of a GSM Base Transceiver Station (BTS). Since the RT must serve all eight time-slots (channels) within a TDMA-frame, eight separate baseband signal-paths have to be used in parallel.



Block diagram of the PCF5082

I/O-Port Descriptions

Parallel Host Interface

The parallel port provides an 8-bit bidirectional link to a host or other external device. It is designed as a passive port, i.e. the external device has to be active in order to access the registers of the port. The communication takes place via 16-bit wide I/O registers with the aid of several control signals. The upper and lower bytes of these registers can be accessed independently.

Two flags are generated (input register full, output register empty) supporting efficient I/O-handling. Whether it is the high byte or the low byte which generates the flag setting is programmable.

By providing several control signals to the external controlling device, this parallel interface is very flexible and supports request-driven as well as acknowledge-driven communications. The selection is done by the external device by means of a status register. This register is exclusively dedicated to the external device and can be read or written.

Serial Interface X

This is a bidirectional 16-bit serial I/O which allows for simultaneous data communication in both directions.

During write operations, data is shifted serially into an input shift register. After termination of the shift operation the contents of the shift register is loaded in parallel into an input buffer register. This allows for a continous data stream transmission. A flag is generated indicating the input buffer register is full. The input port has a fully asynchronous handshake capability.

During read operation data is serially shifted out of an output shift register. After termination of the shift operation the output shift register is reloaded by an output buffer register. During a write operation it allows for a continous data stream transmission and autonomous operation. A flag is generated indicating the output buffer register is empty. The output port has a fully asynchronous handshake capability.

Serial Interface Y

The second serial interface Y covers the same functionality as the serial interface X. In addition, the serial interface Y meets several synchronous transfer protocols such as PCM-Highway or General Communication Interface (GCI). Control registers are provided to select up to 16 data words in a frame from the synchronous data stream. A collision detection unit supports collision detection on the output data stream. It is possible to select

the bits in a data word which are considered for collison detection. If a collision occurs, an error flag will be set which can be used for interrupt processing allowing for efficient error recovery.

General Purpose I/O pins

Four bidirectional general purpose I/O pins are provided as an additional interface to external devices. The state of these pins is reflected in 4 bits of a control register. A write operation to this register causes the appropriate values to appear as output signals on the related pins. With a read operation the incoming signals can then be recognized.

JTAG Interface

The processors provide a standardized test access port which is fully compatible with the IEEE 1149.1 standard. Each time the command NMI is provided to the JTAG interface, a non-maskable interrupt is generated and fed to the interrupt unit of the processor-core. A jump to a non-maskable interrupt service routine will follow as a reaction. The interface provides two I/O registers to the external controlling host. These register are also fully accessable by the processor core which allows for data exchange between an external device and an application program, or service routine.

Several commands to support testing of the device are provided by the JTAG interface, including Boundary- Scan.

Peripheral Functions

Power-down mode

This mode is entered by executing a specific instruction in the application program. It switches the processors into a dormant state where only a fraction of the power dissipation is needed as compared with normal operation mode. The internal clock is stopped and only some synchronization and clock registers are operating.

Wake-up mode

The power-down mode is terminated if an I/O flag occurs and the related wake-up mode is enabled by the application program.

Interrupts

There are 13 different interrupt sources provided by the processors:

1 non-maskable interrupt initiated by a JTAG port instruction.

2 external interrupts initiated by external devices.

6 internal interrupts initiated by the processor's I/O devices.

1 internal interrupt initiated by the collision detection unit of the serial interface Y.

2 internal interrupts initiated by certain conditions in the arithmetic unit.

1 internal interrupt initiated by the event-counter.

Event Counter

A 16-bit event counter is provided as an additional peripheral function. The counter can be loaded by the application program and will be decremented every rising edge of the external signal ECLK, indicating an event to the counter.

ECLK is synchronized to the internal processor clock and is limited to half the frequency of this clock. Each time the counter detects a zero value, a flag is generated which can be used as an interrupt source. The counter will then automatically be reloaded with the start value which is stored in a buffer register